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A New FPN Cancellation Circuit for Time-Domain CMOS Image Sensors

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Additional information is available at the end of the chapter

<http://dx.doi.org/10.5772/60756>

Abstract

A fixed-pattern noise correction technique for time-domain CMOS imagers with high dynamic range is presented in this chapter. Analytical derivations are presented showing how the circuit variations affect the time measured. The error in the time measured can be reduced by using lower reference voltages achieving values smaller than 4%. The fixed-pattern noise correction technique proposed is based on a new readout method for time-domain imagers employing two reference voltages for the discharge time measurement. This new technique is non-sensitive to circuit parameter variations that contribute to fixed-pattern noise such as hold voltages of transistors. A simple electronic circuit is proposed to implement the technique. Circuit and simulation results are presented to demonstrate the feasibility of the proposed technique.

Keywords: CMOS image sensors, Active Pixel Sensor, fixed-pattern noise, photo-diode

1. Introduction

CMOS image sensors have been an important source of research and industrial development in the area of image sensors due to the present high level of integration and low power consumption compared to charge-coupled devices (CCDs). The technology advances of CMOS

image sensor results in image sensors with high dynamic range ($\geq 100\text{dB}$). Higher dynamic range become other important advantage of CMOS image sensors over CCDs. However, most of CMOS imager architecture with high dynamic range neglect the fixed-pattern noise (FPN) and do not present any kind of cancelling circuit or impact on such architectures. Therefore, although conventional linear CMOS sensors incorporate FPN cancellation techniques as correlated-double sampling (CDS), in general, it is still missing in the literature of FPN cancellation techniques for high dynamic range CMOS imagers.

Several techniques were proposed to achieve high dynamic range using CMOS image sensors [1-6]. In [2], by integrating a comparator and a dynamic flip-flop in each pixel, a multi-sampling technique was proposed. In [3], a self-reset technique using one comparator per pixel was described. In general, these techniques are effective as they achieved a dynamic range $>100\text{dB}$, but, none of them show the impact of FPN or present FPN cancellation techniques.

Recently, high dynamic range CMOS imagers using analog-to-digital converters have been proposed and they can incorporate CDS techniques for FPN cancellation although they do not present any FPN impact analysis [7-12]. However, these approaches achieve dynamic ranges of only 70–80dB, which is too low for some applications that typically demand dynamic range higher than 100dB.

In this chapter we present a FPN impact analysis and a technique of FPN cancellation for time-domain CMOS imagers with high dynamic range.

2. Principle of operation of time-domain CMOS imagers

Figure 1a shows the typical time-domain CMOS pixel. It comprises a photodiode, a reset transistor and a comparator. The pixel operation has two stages. The first stage is the reset period. During the reset period the reset transistor operating as switch is closed and the photodiode voltage (V_{pd}) is charged to an initial voltage V_{reset} close to V_{dd} . At the beginning of the second stage, the integration period, the reset transistor is turned off and the photodiode at high impedance starts to discharge. The discharge speed during discharge is according to the photocurrent intensity (see Figure 1b). The discharge time is smaller for higher photocurrent values.

The time-domain CMOS sensor operation consists of measuring the discharge time of the photodiode during the integration period by comparison of photodiode voltage with a reference voltage (see Figure 1b). This comparison is made by using a comparator as seen in Figure 1a. The discharge time is defined as the instant in which the photodiode voltage drops below (or to) the reference voltage and the output comparator goes high. According to [2], the discharge time as function of the photocurrent for a reference voltage V_{ref} is given by:

$$t_d = \frac{C_{pd}}{(I_{dark} + I_{ph})} (V_{reset} - V_{ref}) \quad (1)$$

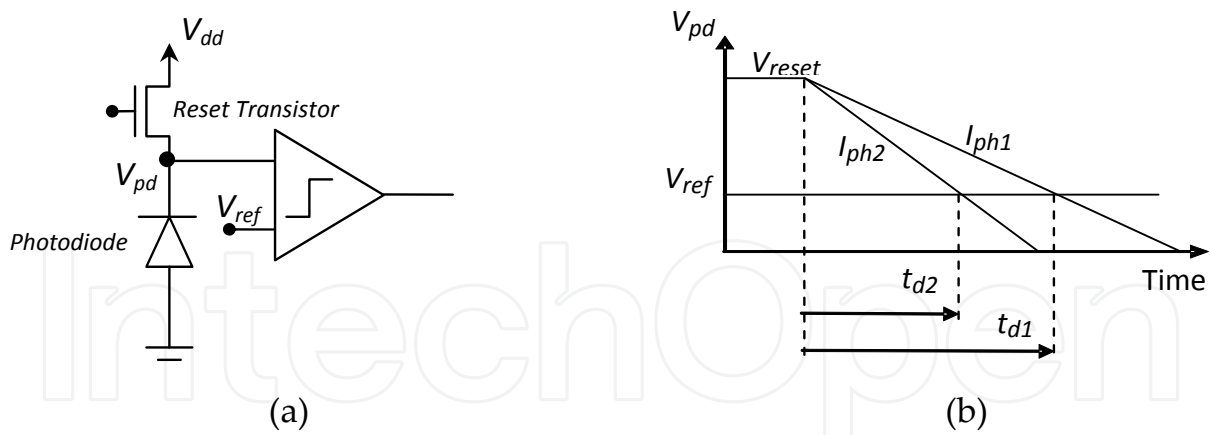


Figure 1. (a) Time-domain CMOS pixel; (b) main waveforms.

where C_{pd} is the photodiode's capacitance, I_{dark} is the dark current, I_{ph} is the photocurrent, V_{reset} is the initial photodiode's voltage and V_{ref} is the reference voltage.

Figure 2 shows the discharge time for different values of reference voltage assuming $C_{pd}=30fF$ and $I_{dark}=100fA$. As one can see, the discharge time is smaller for higher reference voltages. For photocurrent smaller than 100fA, the curve saturates due to the presence of the dark current.

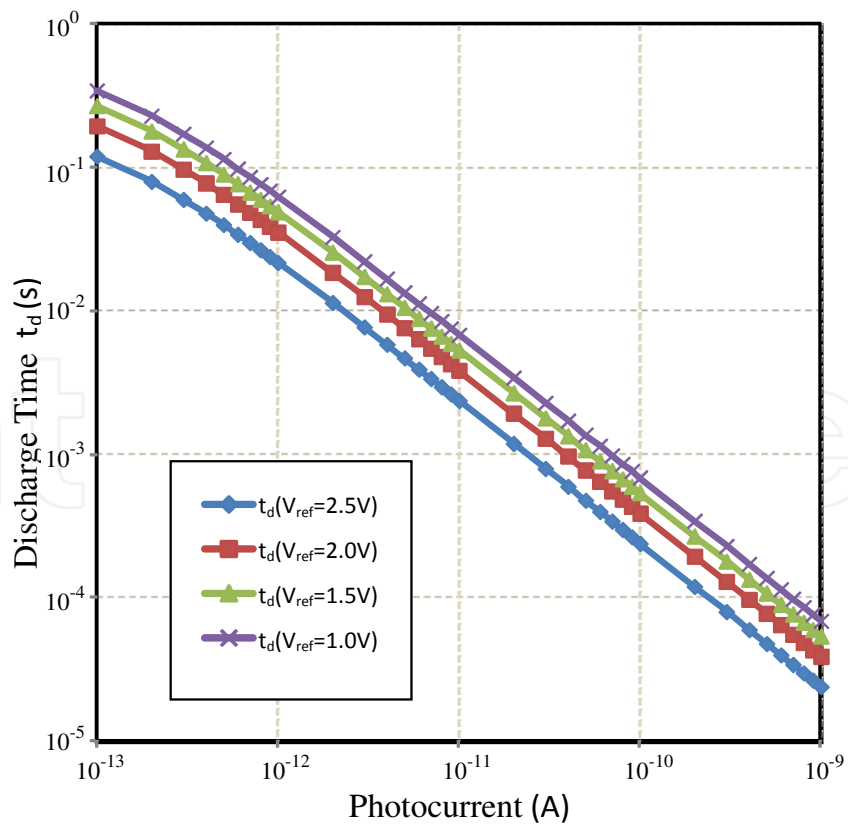


Figure 2. Discharge time of a time-domain CMOS sensor at different values of reference values.

3. Fixed-pattern noise in time-domain CMOS imagers

The fixed-pattern noise is defined as the variation of pixel's photoresponse in a matrix when a uniform light intensity focuses the matrix. Time-domain CMOS imagers have two main sources of variation that contributes to fixed pattern noise; (1) the variation of the reset voltage (ΔV_{reset}) due to threshold voltage variation of the reset transistor and (2) the offset voltage of voltage comparator (ΔV_{offset}). The threshold voltage variation causes a variation on the discharge time that can be written as

$$t_d + \Delta t_d = \frac{C_{pd}}{(I_{dark} + I_{ph})} (V_{reset} \pm \Delta V_{th} - V_{ref} \pm \Delta V_{offset}) \quad (2)$$

where Δt_d is the error reflected in the discharge time measured, ΔV_{th} is the variation introduced by the threshold voltage variation of reset transistor and ΔV_{offset} is the voltage variation introduced by the offset voltage of the voltage comparator. It is possible to demonstrate from the previous equation that the error reflected in the discharge time (Δt_d) can be written as

$$\Delta t_d = \frac{C_{pd}}{(I_{dark} + I_{ph})} (\Delta V) \quad (3)$$

where, $\Delta V = \Delta V_{th} + \Delta V_{offset}$.

According equation (3), the discharge time error is proportional to voltage error introduced (ΔV), and inversely proportional to photocurrent and. therefore the discharge time error varies according light intensities changes. Figure 3 shows the discharge time error as function of photocurrent assuming $C_{pd} = 30\text{pF}$, $I_{dark} = 100\text{fA}$ for three different values of voltage errors.

Manipulating equation (3), it can be demonstrated that the percentage of relative error is given by

$$\frac{\Delta t_d}{t_d} \% = \frac{\Delta V}{(V_{reset} - V_{ref})} 100\% \quad (4)$$

According to equation (4) the relative error of discharge time is independent of light intensity (photocurrent) and inversely proportional to reference voltage. Figure 4 shows the relative discharge time error for three different values of voltage error. As one can see, the relative discharge time error is smaller for small reference voltage values. It is smaller than 4% at $V_{ref} = 0.5\text{V}$.

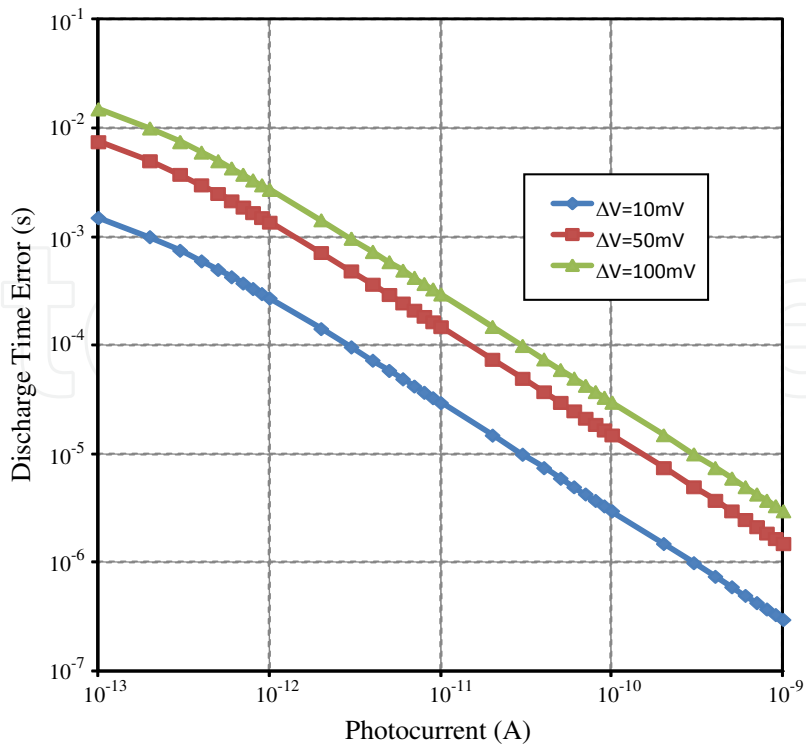


Figure 3. Discharge time error.

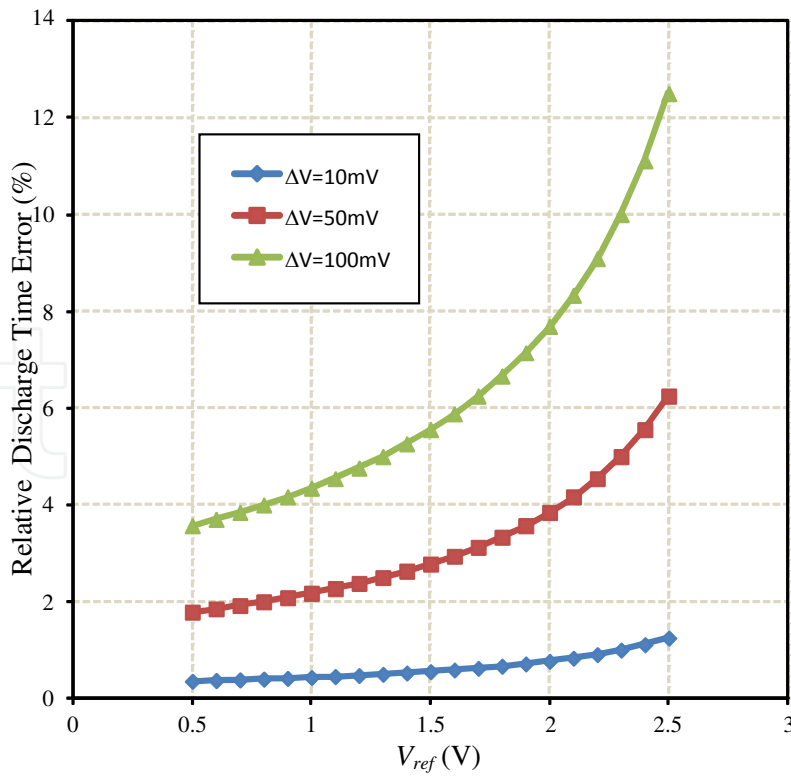


Figure 4. Relative discharge time error.

4. New readout method for time-domain with FPN reduction

In order to cancel the voltage error introduced (see equation 2), we propose to measure the discharge time between the comparisons with two reference voltages as shown in Figure 5.

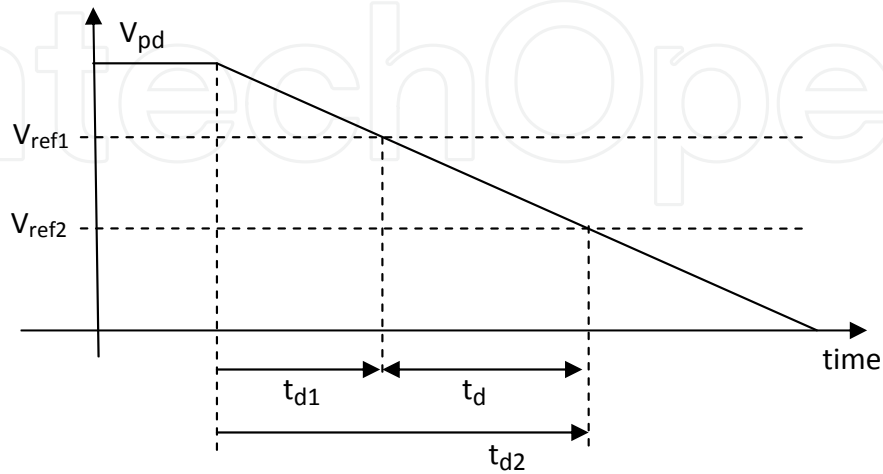


Figure 5. New readout method main waveforms.

The instant of comparison are two, t_{d1} and t_{d2} . For V_{ref1} the comparison time is given by

$$t_{d1} = \frac{C_{pd}}{(I_{dark} + I_{ph})} (V_{reset} \pm \Delta V_{th} - V_{ref1} \pm \Delta V_{offset}) \quad (5)$$

For V_{ref2} the comparison time is given by

$$t_{d2} = \frac{C_{pd}}{(I_{dark} + I_{ph})} (V_{reset} \pm \Delta V_{th} - V_{ref2} \pm \Delta V_{offset}) \quad (6)$$

The discharge time is now given as the interval time between t_{d1} and t_{d2} . Subtracting equations (5) of (6), it is possible to demonstrate the discharge time given by

$$t_d = t_{d2} - t_{d1} = \frac{C_{pd}}{(I_{dark} + I_{ph})} (V_{ref1} - V_{ref2}) \quad (7)$$

According to equation (7) the new discharge time is independent of the source of fixed-pattern noise because it is independent of reset voltage and the offset voltage of voltage comparator. However, the same comparator must be used in order to achieve the offset voltage cancelling.

Figure 6 shows the transfer function graph of t_d for $V_{ref1}-V_{ref2}=2V$, $C_{pd}=30fF$ and $I_{dark}=100fA$. The characteristic of time versus photocurrent is the same of conventional time-domain CMOS imager as can be seen in Figure 3.

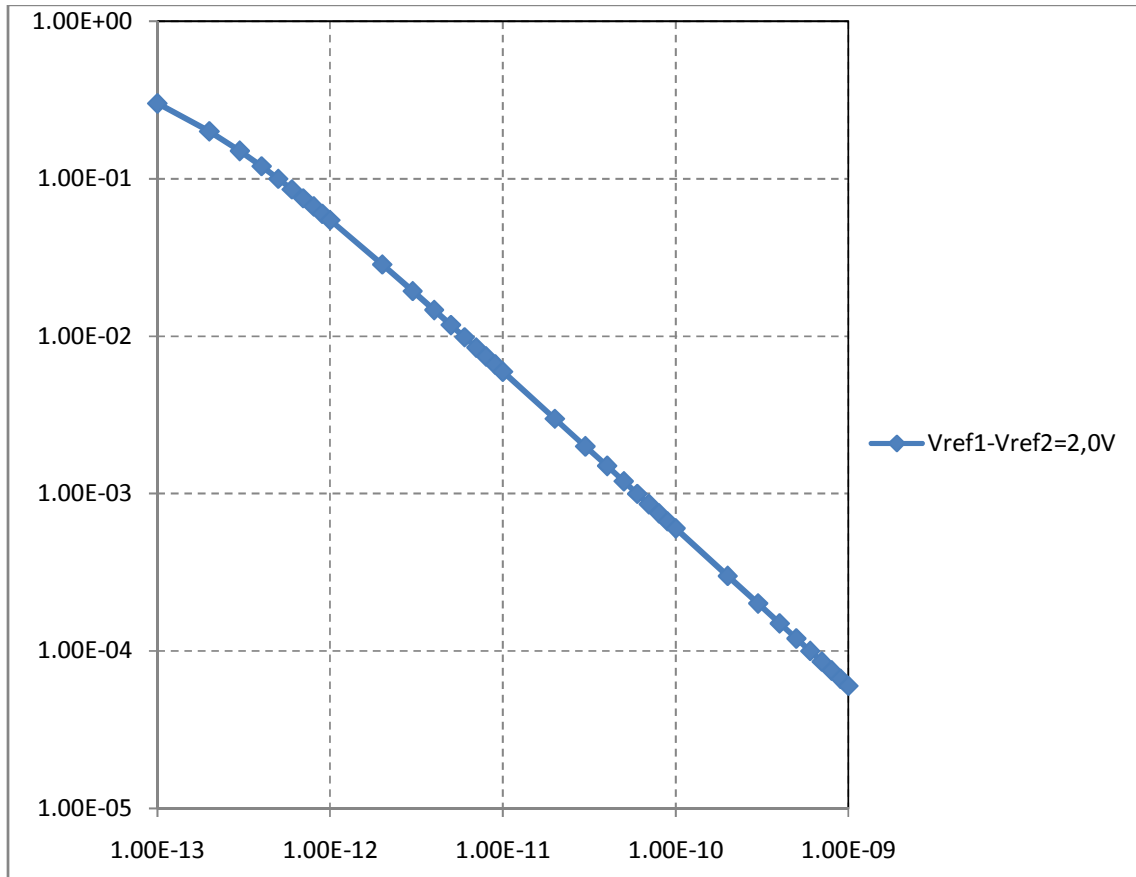


Figure 6. Discharge time (s) versus photocurrent (A).

5. Simulation results

5.1. FPN time-domain characteristic without FPN cancellation

Figure 7 shows the equivalent circuit of the CMOS sensor image used for simulations. The simulated pixel is comprised of a reset transistor and capacitance and a source current as equivalent circuit of photodiode. We assume that the photocurrent is constant and independent of voltage as usual in the literature. For simulations we used a design kit of a $0.35\mu m$ 3.3V CMOS technology.

In order to achieve the transfer characteristic time versus photocurrent simulated, we use a constant reference voltage of 1.5V, reset voltage of 3.3V and a typical capacitance of 30fF. By varying the photocurrent different comparison times for reference voltage of 1.5V were found

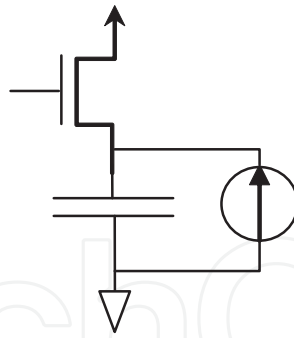


Figure 7. Discharge time (s) versus photocurrent (A).

and the obtained transfer characteristic is shown in Figure 8. Our analysis indicates that the simulation results are in agreement with equation (1).

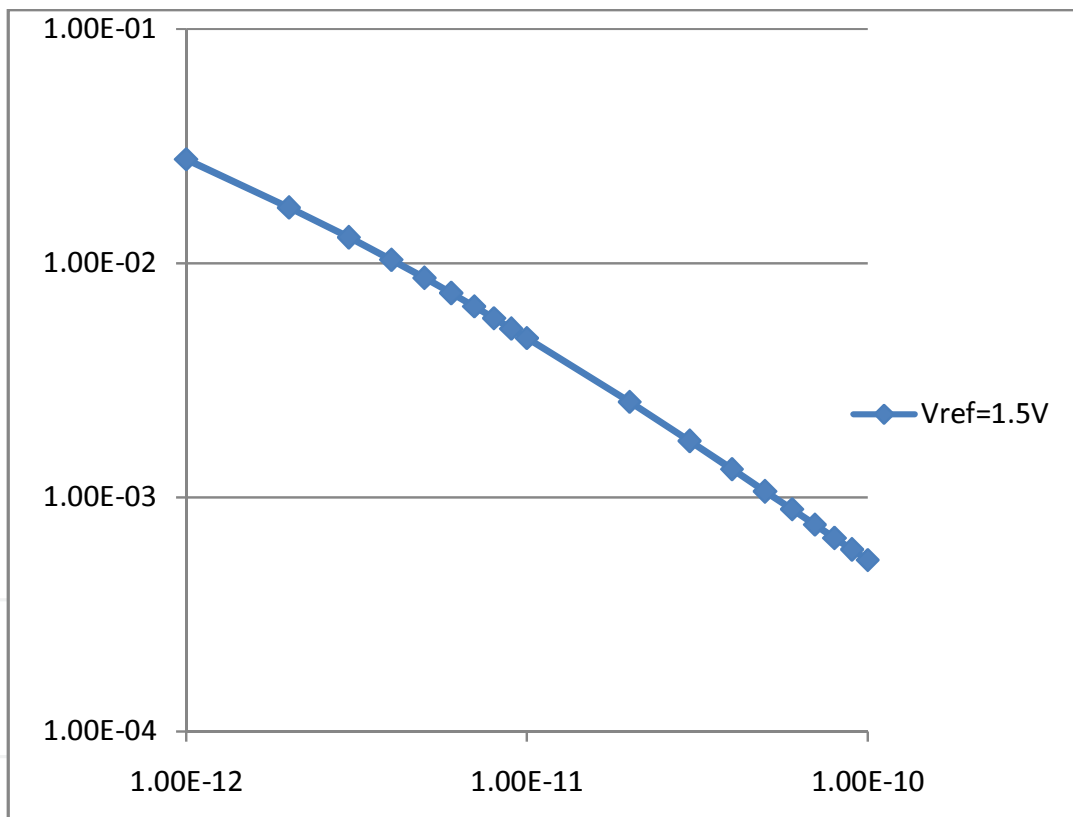


Figure 8. Discharge time (s) versus photocurrent (A).

For simulating the error voltage introduced by circuits, we choose to change the reset voltage (initial voltage) from 3.3V to 3.2V. Therefore, we simulate a error voltage of 100mV caused by the variation of the threshold voltage of the reset transistor and/or by the offset voltage of the comparator. Using a reference voltage of 1.5V and changing the initial voltage in the simulations we found a comparison time error from 6% to 10% as shown in Figure 9.

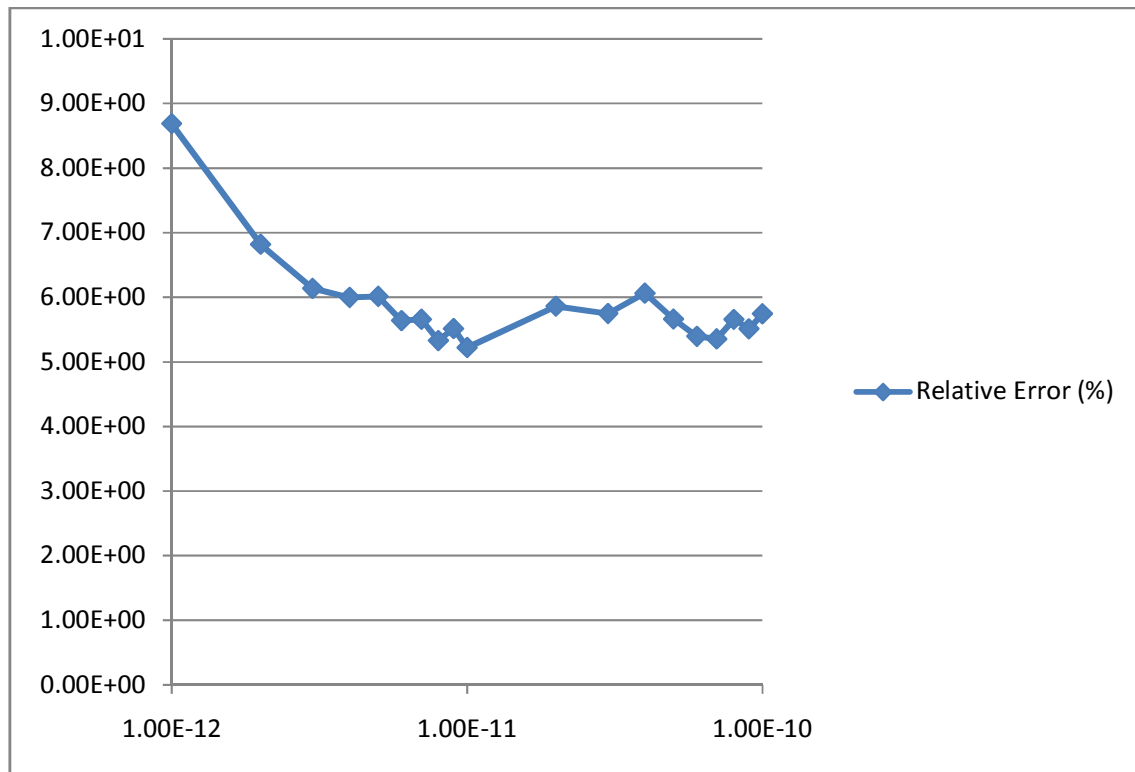


Figure 9. Relative error (%) versus photocurrent (a) for 100mV of variation in reset voltage.

This result indicates that the FPN in time domain for an entirely pixel matrix is less than 10%. The error is calculated as

$$error(\%) = 100 * \frac{t_d(3.3V) - t_d(3.2V)}{t_d(3.3V)} \quad (8)$$

5.2. FPN time-domain characteristic with FPN cancellation

Two references voltages are used for FPN cancellation. We use $V_{ref1}=2.5V$ and $V_{ref2}=2.0V$ as reference voltages. For this case, the transfer characteristic discharge time versus photocurrent is shown in Figure 10. The discharge time t_d was measured as the difference between the discharge time to V1 and the discharge time to V2 ($t_d=t_d(2.5V)-t_d(2.0V)$). Our analysis indicates that the transfer characteristic indicated in Figure 10 is in agreement with equation (7).

A simulation with 100mV of error introduced again was performed and the error was calculated as equation (8). For this case, the relative error found is shown in Figure 11. This simulation result indicates that the relative error is less than 2% percent. Therefore, the simulation result shows that this technique can reduce the FPN in time-domain imagers.

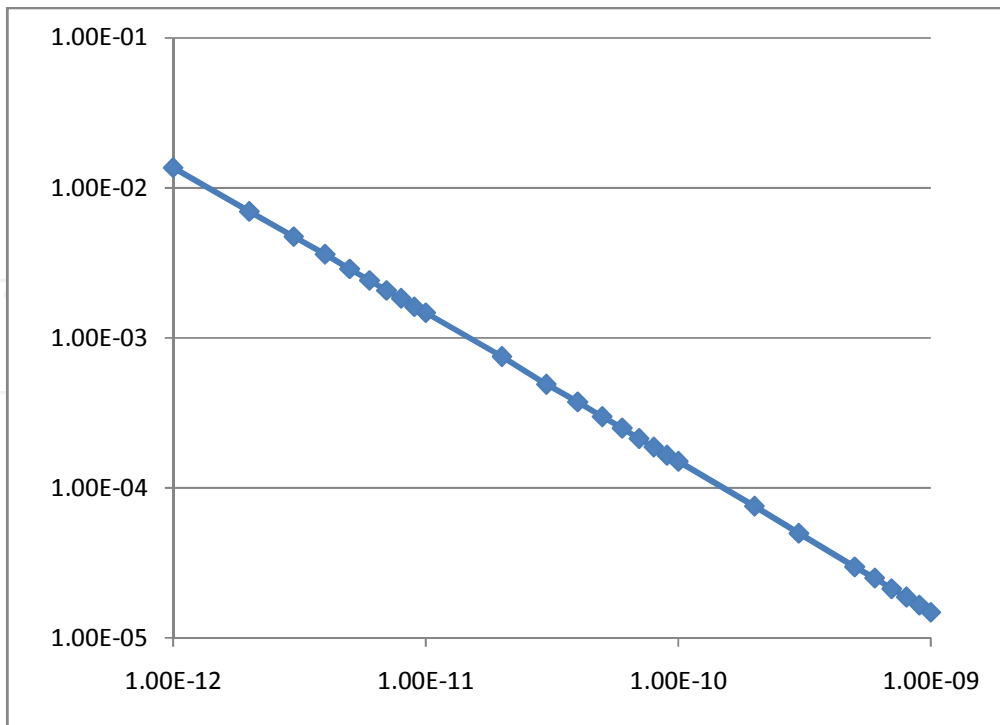


Figure 10. Discharge time (s) versus photocurrent (A) for $V_{ref1}=2.5V$ and $V_{ref2}=2.0V$.

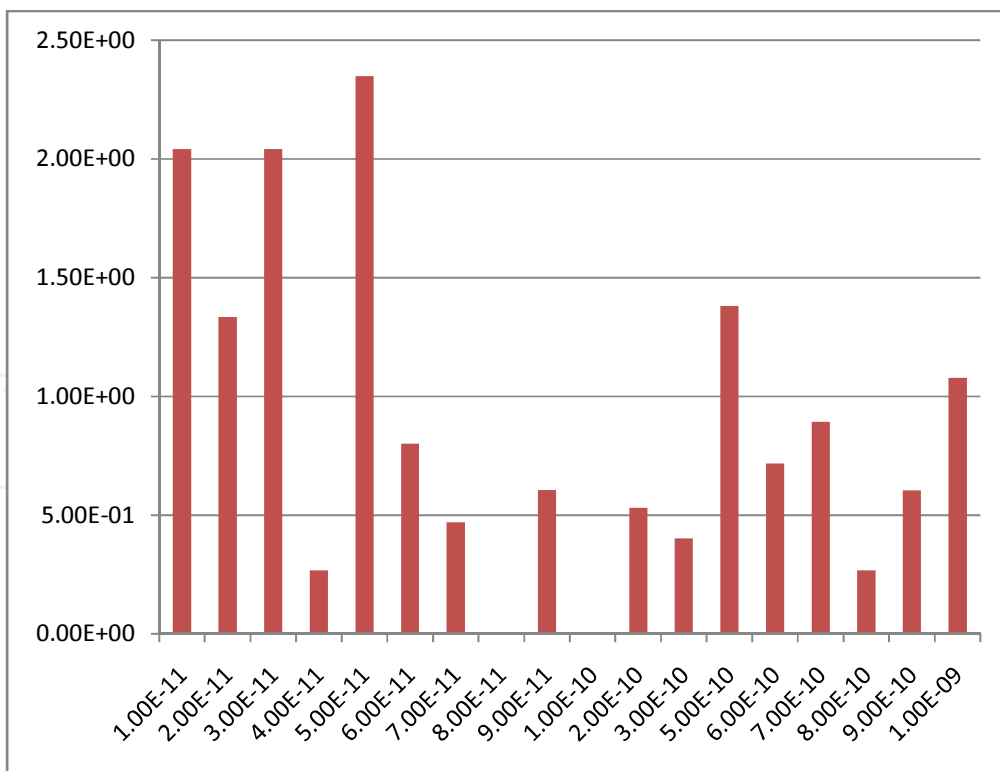


Figure 11. Relative error (%) versus photocurrent (A).

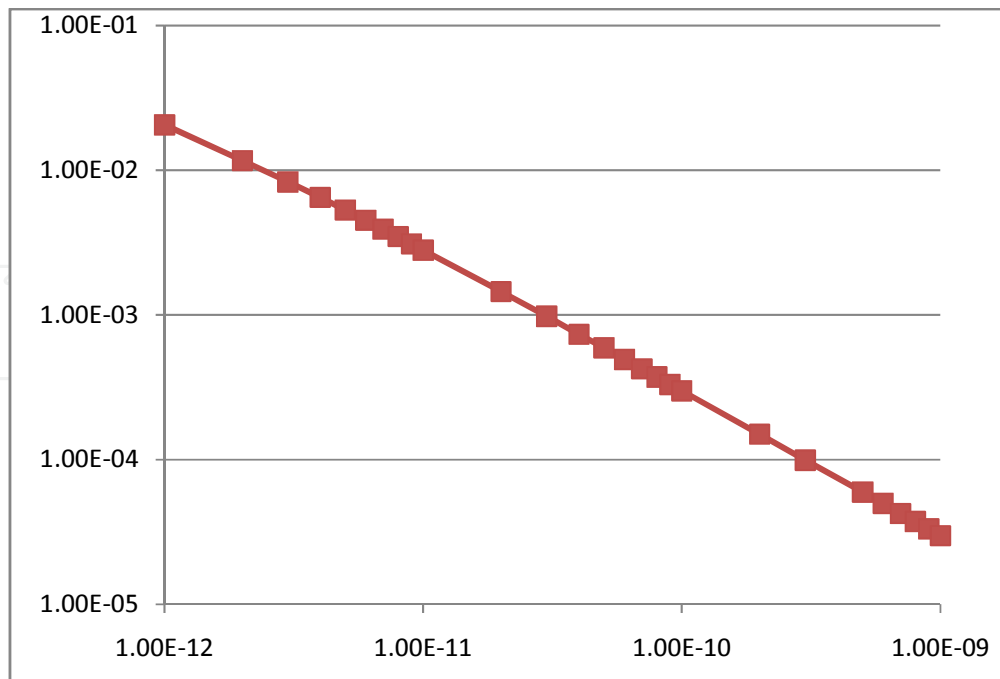


Figure 12. Discharge time (s) versus photocurrent (A) for $V_{ref1}=2.5V$ and $V_{ref2}=1.5V$.

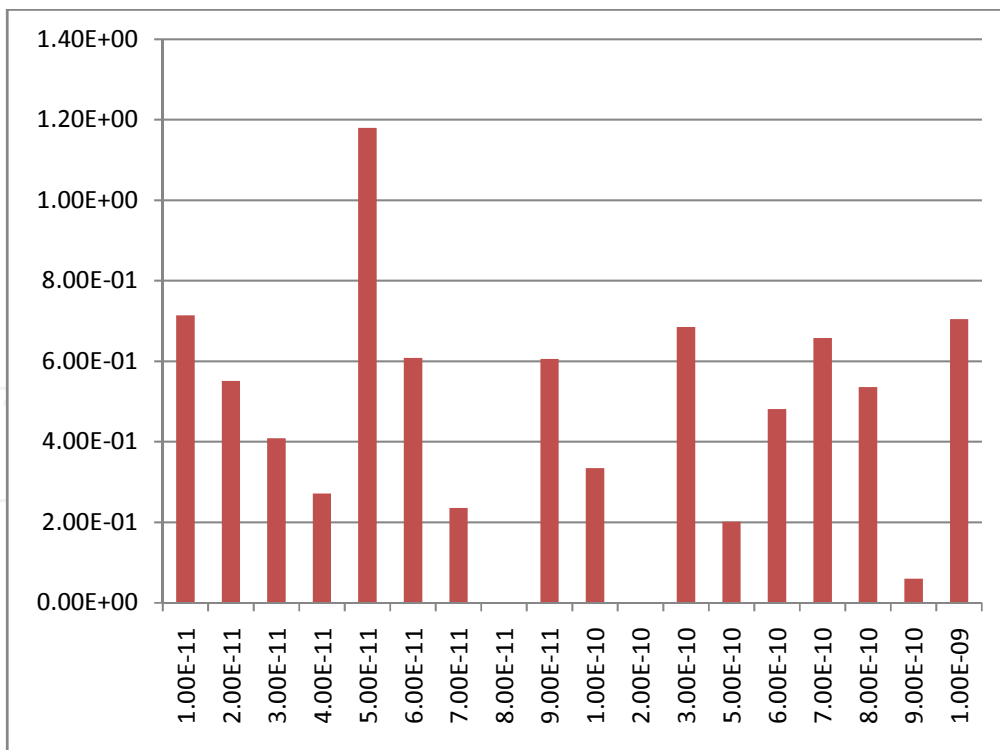


Figure 13. Relative error (%) versus photocurrent (A).

In order to confirm the results, we decide to simulate using reference voltages of $V_1=2.5V$ and $V_2=1.5V$. As one can see in Figure 12, for this case the transfer characteristic is in agreement with equation (7) and the transfer characteristic in Figure 10.

For this case, an error of 100mV was introduced in the circuit simulated as stated before. The relative error found in this case is shown in Figure 13. Again the relative error is less than 2% showing that the technique can reduce the FPN.

6. Electronic circuit for time domain FPN cancellation

The challenge in this technique implementation is to develop a circuit that uses the same comparator (same offset voltage) to compare two reference voltages. For this purpose we propose the circuit shown in Figure 14.

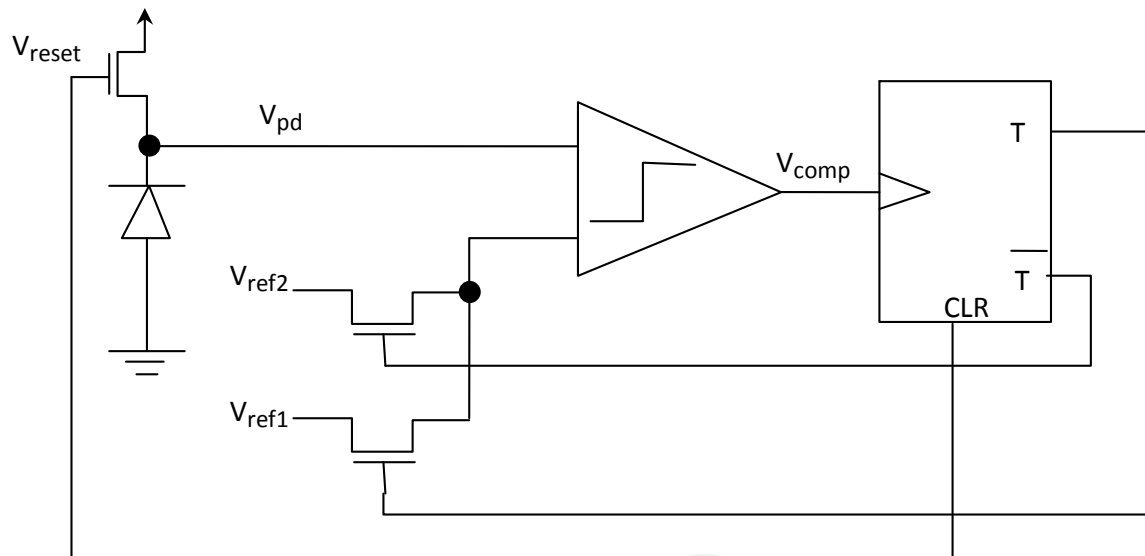


Figure 14. Electronic circuit of new FPN cancelling for time-domain imagers.

The circuit is composed of a comparator, two selector transistors (switches), and a T Flip-Flop. The main waveforms of signal are shown in Figure 15. First, the reset signal used to reset the pixel is also used to reset the flip-flop and the counter. Initially at low, the output of flip-flop control the two switches selecting only one of the reference voltages (V_{ref1}). After reset, and during the beginning of integration time, the V_{ref1} reference voltage is selected for comparison. At instant of comparison, when the output pixel is V_{ref1} , the output comparator triggers the flip-flop that changes to high. At this moment, the switches are biased disconnecting V_{ref1} and connecting V_{ref2} . The output of the comparator goes low again but the output of the flip-flop remains high. When the output pixel voltage reaches V_{ref2} the comparator output pulses again trigger the flip-flop output to low. At this moment the counter stops and the reference voltage V_{ref1} returns to be connected to the comparator input.

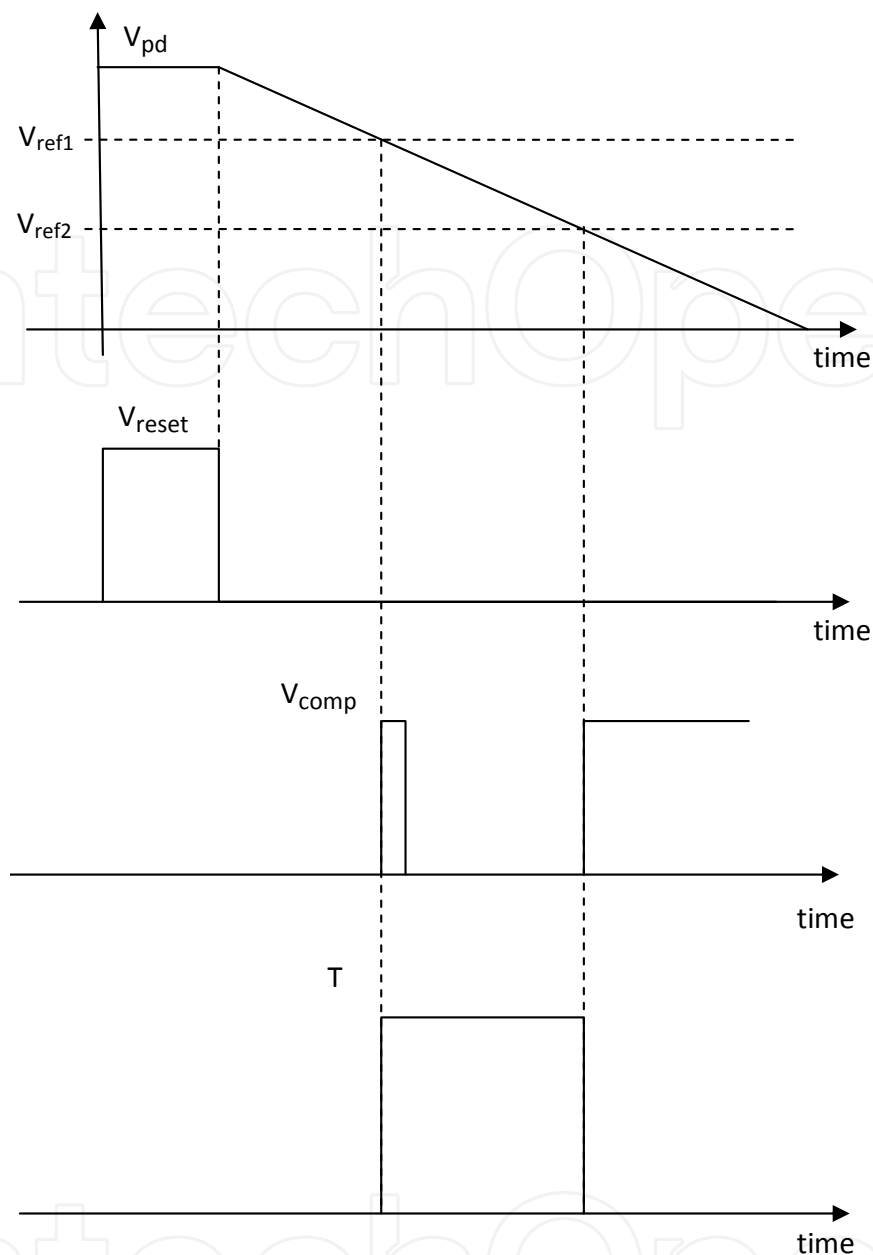


Figure 15. Electronic circuit main waveforms.

7. Conclusions

High dynamic range imager CMOS image sensors are one of the most important applications of CMOS image sensors. Most of the high dynamic range CMOS image sensors proposed in the literature neglect the fixed pattern noise, which is one of the major drawbacks of CMOS image sensors compared to CCDs. In this work, a fixed-pattern noise reduction technique is presented for high dynamic range CMOS image sensors operating in time domain. According to simulation results, the new technique can reduce the fixed pattern noise down to 2%.

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References

- [1] A. Belenky, A. Fish, A. Spivak, and O. Yadid-Pecht, "A snapshot CMOS image sensor with extended dynamic range," *IEEE Sensors Journal*, vol. 9, pp. 103-111, 2009.
- [2] F.S. Campos, O. Marinov, N. Faramarzpour, F. Saffih, M.J. Deen, J.W. Swart, "A multisampling time-domain CMOS imager with synchronous readout circuit," *Analog Int. Cir Signal Proc*, vol. 57, pp. 151-159, 2008.
- [3] D. Park, J. Rhee, and Y. Joo, "A wide dynamic-range CMOS image sensor using self-reset technique," *IEEE El Dev Lett*, vol. 28, no. 10, pp. 890-892, 2007.
- [4] L.G. McIlrath, "A low-power low-noise ultrawide-dynamic range CMOS imager with pixel-parallel A/D conversion," *IEEE J. Solid-State Circuits*, vol. 36, pp. 846-853, 2001.
- [5] D. Yang, A. El Gamal, B. Fowler, and H. Tian, "A 640x512 CMOS image sensor with ultra wide dynamic range floating point pixel level ADC," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1821-1834, 1999.
- [6] S. Decker, R.D. McGrath, K. Brehmer, and G. Sodini, "A 256x256 CMOS imaging array with wide dynamic range pixels and column parallel digital output," *IEEE J. Sol-St Cir*, vol. 33, pp. 2081-2091, 1998.
- [7] M.-W. Seo, T. Sawamoto, T. Akahori, Z. Liu, T. Iida, T. Takasawa, T. Kosugi, T. Watanabe, K. Isobe, and S. Kawahito, "A low-noise high-dynamic-range 17b 1.3-Megapixel 30-fps CMOS image sensor with column-parallel two-stage folding-integration/cyclic ADC," *IEEE Trans. Electron Devices*, vol. 59, no. 12, Dec. 2012.
- [8] Z. Ignjatovic, D. Maricic, M.F. Bocko, "Low power, high dynamic range CMOS image sensor employing pixel-level oversampling $\Sigma\Delta$ analog-to-digital conversion," *IEEE Sensors Journal*, vol. 12, no. 4, pp. 737-746, April 2012.
- [9] M.W. Seo, et al., "A low-noise high intrascene dynamic range CMOS image sensor with a 13 to 19b variable-resolution column-parallel folding-integration/cyclic ADC," *IEEE J Sol-St Cir*, vol. 47, no. 1, pp. 272-283, Jan 2012.

- [10] Y.C. Chae, J.M. Cheon, S.H. Lim, M.H. Kwon, K.S. Yoo, W.K. Jung, D.H. Lee, S.H. Ham, and G.H. Han, "A 2.1 M pixels, 120frames/s CMOS image sensor with column-parallel $\Delta\Sigma$ ADC architecture," *IEEE J. Solid-State Circuits*, vol. 46, no.1, pp. 236-247, Jan. 2011.
- [11] J. H. Park, S. Ayoama, T. Watanabe, K. Isobe, and S. Kawahito, "A high-speed low noise CMOS image sensor with 13-b column-parallel single-ended cyclic ADCs," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2414-2422, Nov. 2009.
- [12] M. Furuta, Y. Nishikawa, and S. Kawahito, "A high-speed, high-sensitivity digital CMOS image sensor with a global shutter and 12-bit column-parallel cyclic A/D converter," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 766-774, Apr. 2007.

