Chapter 10

SiGe Based Visible-NIR Photodetector Technology for Optoelectronic Applications

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1. Introduction

This chapter covers recent advances in SiGe based detector technology, including device operation, fabrication processes, and various optoelectronic applications. Optical sensing technology is critical for defense and commercial applications including telecommunications, which requires near-infrared (NIR) detection in the 1300-1550 nm wavelength range. [Here we consider the NIR wavelength band to span approximately 750-2000 nm; the upper portion of this band, e.g., 1400 nm and longer wavelengths, is sometimes elsewhere designated short-wave infrared (SWIR).] Although silicon (Si) photodetectors have been widely used to detect in the visible to short NIR wavelength regime, the relatively large Si band gap of 1.12 eV, corresponding to an absorption cutoff wavelength of ~1100 nm, hinders the application of Si photodetectors for longer wavelengths vital for medium-and long-haul optical fiber communications.

Group III-V compound semiconductors possess the advantages of high absorption efficiency, high carrier drift velocity, excellent noise characteristics, and mature design and fabrication technology for optical devices, and are commonly used in IR detection related devices [1]. InGaAs based IR photodetectors have been developed for NIR (up to ~1700 nm) applications, InSb for 3-5 μm applications, and HgCdTe for 1-3, 3-5 and 8-14 μm applications [2]; the spectral responses of these and various other IR detector material systems are shown in Figure 1. While it is possible to integrate III-V semiconductor materials on Si by wafer bonding or epitaxy [3], III-V based detectors normally require cooling (typically down to 77 K), and incorporating III-V materials into the prevalent silicon process is at the expense of high cost and increased

complexity. In addition, there is the potential of introducing doping contaminants into the silicon, since III-V semiconductors act as dopants for Group IV materials [4].

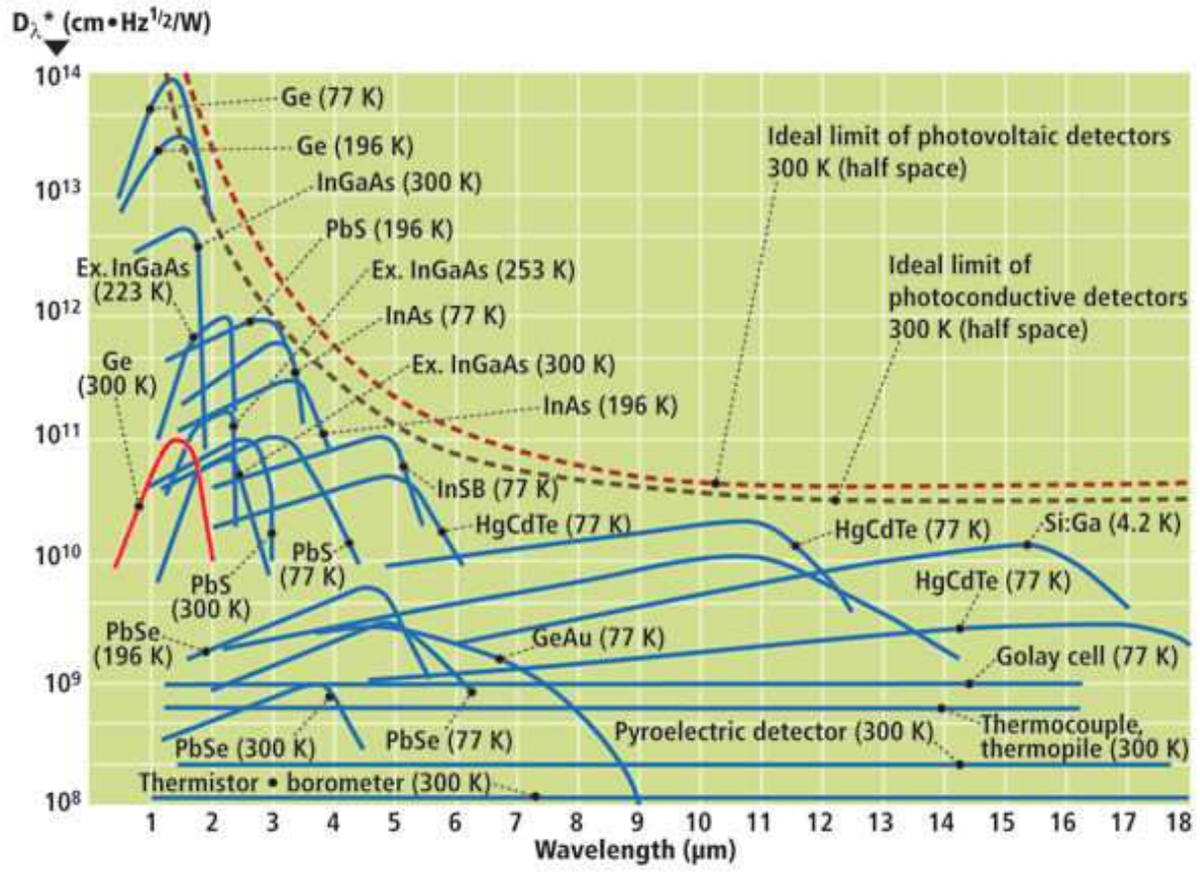

Figure 1. Spectral response characteristics of various IR detectors of different materials/technologies. Detectivity (vertical axis) is a measure of signal-to-noise ratio (SNR) of an imager normalized for its pixel area and noise bandwidth [5].

Germanium (Ge) is a Group IV material as is silicon, and thus avoids the cross contamination issue [6]. Ge, which can now be produced with extremely high purities, has an absorption spectrum similar to that of InGaAs, and can be alloyed with Si to improve the mobility and/or velocity of mobile carriers [7]. Ge forms a covalent bond with Si, and a number of SiGe based alloys involving the addition of hydrogen or oxygen are known. Amorphous alloys such as *a*-$Si_xGe_yH_z$ are characterized by the absence of long-range order, but often possess a considerable degree of short-range order which is referred to as chemical ordering. A useful table listing Si and Ge bond and defect energies is found in Ref. [8]. One property of Ge that is of particular interest is the nature of its band gap. Though Ge like Si is predominately an indirect band gap (E_g=0.66 eV) material, it has a direct band gap of 0.80 eV that is only 140 meV above its indirect band gap [9]. This enables Ge to transform from an indirect gap material towards a direct gap material through the incorporation of tensile strain, as will be discussed in more detail in Section 5.2.

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Consequently, strained absorption layers composed of Ge/SiGe can provide much higher optical absorption and enhanced transport properties over the ~1300-1600 nm wavelength range than layers of pure Si, enabling SiGe based photodetectors with extended NIR capabilities. (Although potential drawbacks of Si-Ge integration exist including lattice mismatch between the materials and a relatively low thermal budget for Ge, the growth processes can be adjusted to compensate in each case.) While detectors based on Ge crystals have been used for NIR detection for many years, these have required cooling down to 77 K, making them expensive and limiting their use [10]. Detectors incorporating epitaxially grown Ge/SiGe on Si substrates can operate at room temperature (RT), thus offering substantially reduced cost and size, weight, and power (SWaP). Furthermore, SiGe photodetectors can be designed to exhibit low dark currents (nA range) and dark current densities comparable to those of large area Group III-V detectors, with accordingly high signal-to-noise ratios (SNRs) [11]. Consequently, SiGe based devices have become promising and practical candidates for many applications requiring detection of radiation at visible to NIR wavelengths.

Perhaps the most important advantage of SiGe based devices is that SiGe epitaxial growth processes are compatible with both front-and back-end silicon complementary metal-oxide-semiconductor (CMOS) fabrication technologies. Consequently, SiGe detector devices can be heterogeneously combined with CMOS circuitry using widely installed manufacturing infrastructure used for production of CMOS integrated circuits (ICs). In addition, SiGe photodetectors and Si CMOS receiver circuits can be simultaneously fabricated and then monolithically integrated [12]. Fabricated SiGe detectors can be incorporated directly with low noise Si readout integrated circuits (ROICs) to yield low-cost and highly uniform IR focal plane arrays (FPAs) to maximize the fill factor, as will be discussed in Section 7. This allows SiGe detector based imaging devices to be produced much less expensively and with less difficulty than those based on III-V detectors. An attractive feature of CMOS-compatible SiGe IR detectors/imagers is that they can be fabricated on large diameter (up to 450 mm) Si wafers [13], further decreasing costs and maximizing production output.

2. Applications of SiGe detector technology

2.1. Telecommunications

The relatively recently realized capability of growing Ge epitaxially on Si has enabled the incorporation of Ge in an expanded variety of detector applications. A primary application for SiGe NIR detectors involves optical telecommunications networks. Due to fundamental physical advantages over copper as well as improved bandwidth, power dissipation, cost, and noise immunity, fiber optic based communications have been utilized to enhance available bandwidths for services such as internet, cable television, and telephone, e.g., using fiber-to-the-premises (FTTP) network architectures [14]. By replacing electrical wires with optical fibers, data rates can be enhanced from 10 Mb/s up to the order of 10 Gb/s with much lower power budgets [15].

Monolithic integration of optics with Si electronics is a primary means to realize low-cost and high performance interconnections, and Ge is a promising material to bridge low-cost electronics with the advantages of optics [12]. Unlike their Si based counterparts, photodetectors with tensile strained Ge/SiGe layers can provide high optical absorption over the entire C band (1530-1565 nm) and most of the L band (1565-1625 nm). The L band is commonly utilized by dense wavelength division multiplexing (DWDM) systems, and it has been determined that expanding the detection limit from 1605 nm to 1620 nm can enable 30 additional channels for long-haul optical telecommunications [16]. The performance of SiGe based photodetectors operating at extended NIR wavelengths is now comparable to or in some cases exceeds the performance of InGaAs based devices that have traditionally been used in telecommunications networks [10].

2.2. Optical interconnects

Conventional copper interconnects become bandwidth limited above 10 GHz due to frequency-dependent losses such as skin effects and dielectric losses from printed circuit board substrate materials [18]. In addition, RC delay and heat dissipation issues originating from metal interconnects on Si ICs have become increasingly problematic as feature sizes continue to shrink in accordance with Moore's Law [15]. Consequently, recent years have seen a rapid advancement in the adaption of Si based optical interconnects from rack-to-rack and board-to board to chip-to-chip as well as to on-chip applications. The latter two applications require a large number of high-speed, low-cost photodetectors densely integrated with Si electronics [12].

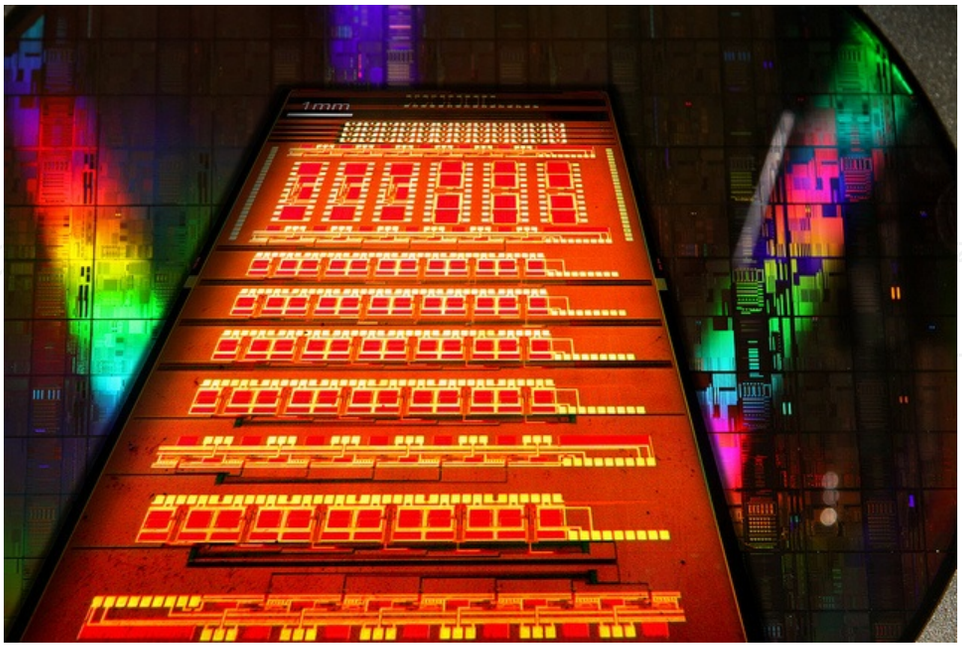

Figure 2. The compatibility of SiGe technology with standard CMOS processing makes new types of optoelectronic ICs possible. Shown here is a new IC technology from IBM designated *CMOS Integrated Silicon Nanophotonics* [17].

While compound semiconductor devices offer high performance due to their excellent light emission and absorption properties, the process of integrating them in optical interconnects is generally very complicated, as well as costly due to the overhead associated with manufacturing in a separate facility combined with the costs associated with packaging and assembling [19]. On the other hand, SiGe based photodetectors have been demonstrated that provide nearly all of the characteristics desirable for integrated optoelectronic receivers [20]. SiGe detectors offer high speeds (10 Gb/s and greater), high sensitivity, a broad detection spectrum, and the potential for monolithic integration with IC CMOS fabrication technology as will be discussed in Section 7.2. Thus, SiGe technology holds much promise for optical interconnects in next generation ICs (Figure 2) to overcome bottlenecks inherent in conventional microelectronic devices.

2.3. Further commercial and military applications

The detection of visible-NIR radiation offered by SiGe based sensors and imaging devices operating at RT make them useful for a variety of additional industrial, scientific, and medical applications. Applications requiring low-cost NIR capable sensors include medical thermography for cancer and tumor detection during diagnosis and surgery, machine vision for industrial process monitoring, sorting of agricultural products, biological imaging techniques such as spectral-domain optical coherence tomography, and imaging for border surveillance and law enforcement [21]. SiGe based NIR sensors/imagers also provide a low-cost solution for a wide range of military applications. These military applications include, but are not limited to, day-night vision, soldier robotics, plume chemical spectra analysis, biochemical threat detection, and night vision for occupied and autonomous vehicles [13].

An additional military application of particular significance is hostile mortar fire detection and muzzle flash (Figure 3). Muzzle flashes, which approximate a blackbody spectrum from 800 K to 1200 K [22], consist of an intermediate flash and, unless suppressed, a brighter secondary flash [23]. Such incendiary events produce large amounts of energy in the NIR spectral region. The ability to image flashes from hostile fire events combined with target detection capability [e.g., by using spectral tags (chemical additives) for identification of friendly fire] provides a vital function in the battlefield that can be key to saving the lives of soldiers as well as making good strategic decisions such as knowing when and where to attack [24]. The realization of small and low-cost SiGe devices that can detect hostile fire sources therefore has the potential to greatly benefit our armed forces.

Another commercial application in view involves very small form factor SiGe based visible-NIR cameras. Since imaging has become a core feature to most mobile phone users and manufacturers, the industry puts much effort into related performance improvements and optimization of camera manufacturing methods. Wafer-level packaging of CMOS image sensors and wafer-level optics provide a cost-effective means of potentially equipping future generations of camera smartphones with visible-NIR imaging capability with smaller form factors [26]. Developing such miniature cameras based on SiGe integrated CMOS technology will require demonstrating small pixel and format NIR detector arrays that enable wide field-of-views. Producing a practical NIR imager will likewise involve further refining the thermal,

Figure 3. SiGe technology is associated with a number of military applications involving NIR sensitivity, including muzzle flash detection [25].

mechanical, and optical analyses of encapsulation and optical materials to enable compatibility with NIR FPA manufacturing.

3. SiGe sensor performance modeling

3.1. Performance model overview

This section deals with modeling of SiGe NIR FPA imaging performance over a wide range of light levels that can occur for day-night operation [13]. The model predicts detector dark currents, photocurrents, and readout and background noise associated with a novel small pixel, low-cost SiGe visible-NIR prototype camera. This type of imager, based on the ability to grow NIR-sensitive SiGe layers on silicon to form pixels utilizing existing high quality and low-cost semiconductor and electronic architectures, is intended to provide NIR night vision capability in addition to visible operation.

A fairly large matrix of variables, which include NIR background, pixel size, focal length, *f*-number, integration time, spectral bandpass, dark current level, and readout noise level, require a significantly complex model to perform the necessary design trade studies. This model predicts values for sensor noise equivalent intensity (NEI) and SNR, and also generates simulated 30 and 60 Hz NIR image sequences. The model was designed to assist in the

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development of miniature NIR or visible-NIR cameras and FPA designs and predict NEI and SNR performance of image or video quality (resolution and noise), so as to aid in the design of SiGe detector based camera optics, FPA formats, readout electronics, and pixel size.

3.2. Variable NIR background

The NIR background radiance between overcast dark night and full daylight varies by about eight orders of magnitude, spanning approximately 0.1 mlux to 25,000 lux. For daytime operation, spectral filtering, aperture reduction, and/or integration time reduction are required to prevent saturation of an FPA. The night radiance over the visible-NIR wavelength range spanning 400-1750 nm can also be quite varied: ~1.0×10^{-9} W/cm^2 for overcast rural settings, ~1.5×10^{-9} W/cm^2 for overcast urban conditions, ~1.2×10^{-8} W/cm^2 for clear night sky rural conditions, and up to ~3.1×10^{-8} W/cm^2 for clear moonlit night skies.

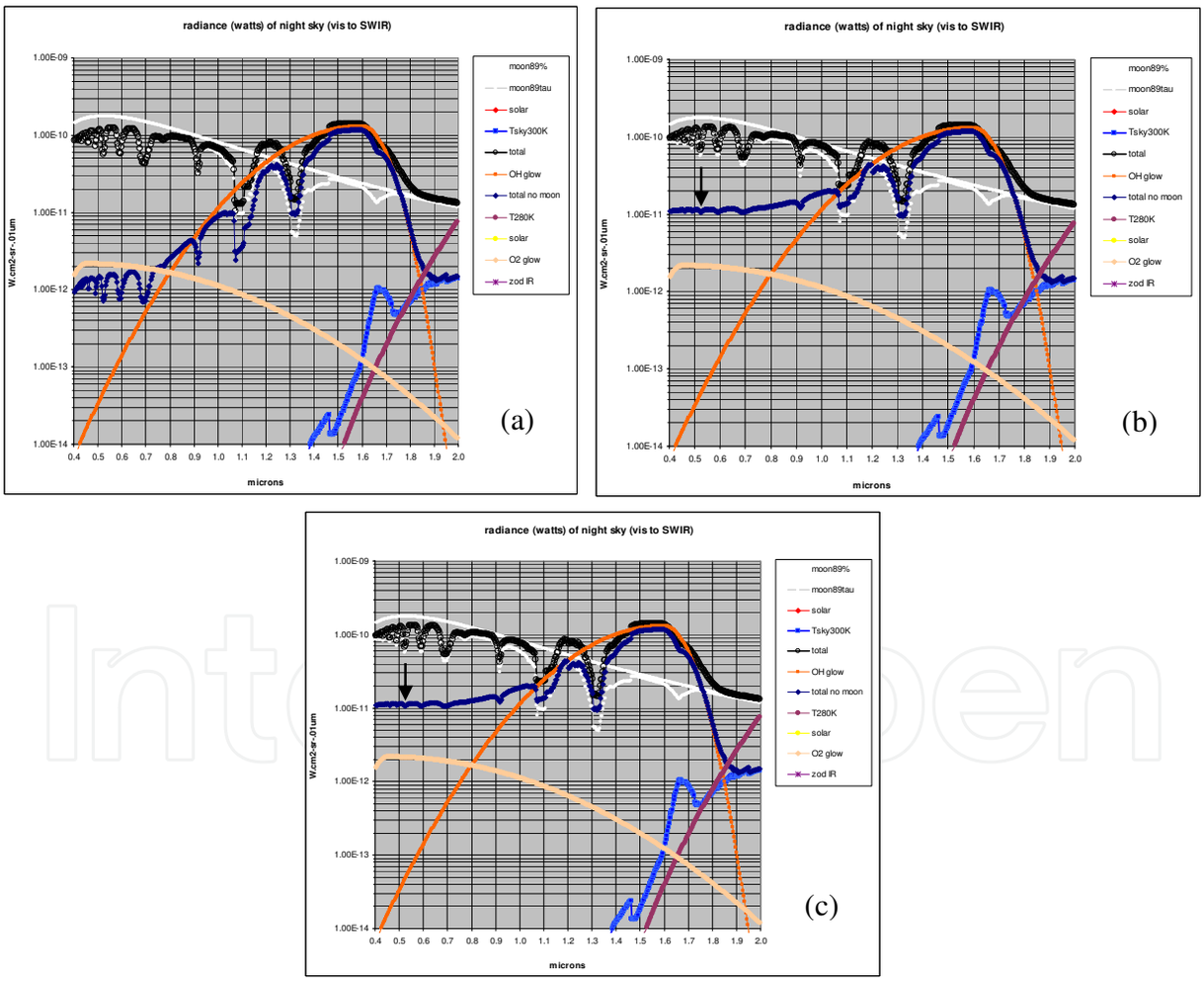

Figure 4. Visible to NIR spectral radiance of night sky based on astronomical data [27] along with data from M. Vatsia [28] plotted in (a), and data from R. Littleton [29] plotted in (b); in (c), radiance includes light pollution (Toronto). In these plots, airglow is shown in orange, moonlight in white, zodiacal IR in beige, lower atmosphere radiance in light blue, total radiance transmitted to ground in black, and total radiance to ground from airglow alone in dark blue.

Since the primary source of illumination in the NIR regime is upper atmosphere airglow, the imaging performance NIR cameras typically degrades when used in dark night overcast conditions or under a thick canopy. Moonlight and light pollution that exist in more urban settings can also help to illuminate terrain, but such illumination occurs mostly at shorter wavelengths. This situation is shown in Figure 4 in which the lunar radiance is mainly significant in the 400-1200 nm region, and is particularly evident in Figure 4(c) which shows the effects of city light pollution (where the radiance level is derived from a Toronto, Canada based spectral measurement). These spectral radiances have been modeled in order to determine the electron noise level in NIR FPAs for a given FPA pixel size, spectral band, integration time, and set of optics. This provides the background limited performance (BLIP) conditions to which dark currents and the readout noise must be added.

Basic atmospheric transmittance and path radiance capabilities have been included in the model. The percent cloud cover, which attenuates the airglow and celestial sources as well as the specified solar scattering level, can be taken into account along with aerosol visibility (5 km or 23 km). The transmittance from scene to sensor assumes a horizontal path at the earth's surface. The attenuation effects of the atmosphere on the images were computed, and subsequently a path radiance based on the ambient NIR background was reinserted into the images. This effectively compensated for the loss of scene brightness and contrast with attenuation and the overall increase in brightness due to path radiance. The images in Figure 5 illustrate the loss of contrast with increasing range.

Figure 5. Atmospheric effects on clear night sky. NIR images at distances of 1, 10, and 15 km (left to right) for 5 km visibility conditions.

3.3. Image quality metrics

Figure 6 displays images from a simulated camera to illustrate the effects of resolution and SNR on image quality and potential image identification. For 30 or 60 Hz image sequences, the eye can integrate some of the frames which allows for slightly better identification than is seen in these single images. Motion of an object over the field-of-view also aids in identification, since the eye can compensate for pixilation when viewing a moving object.

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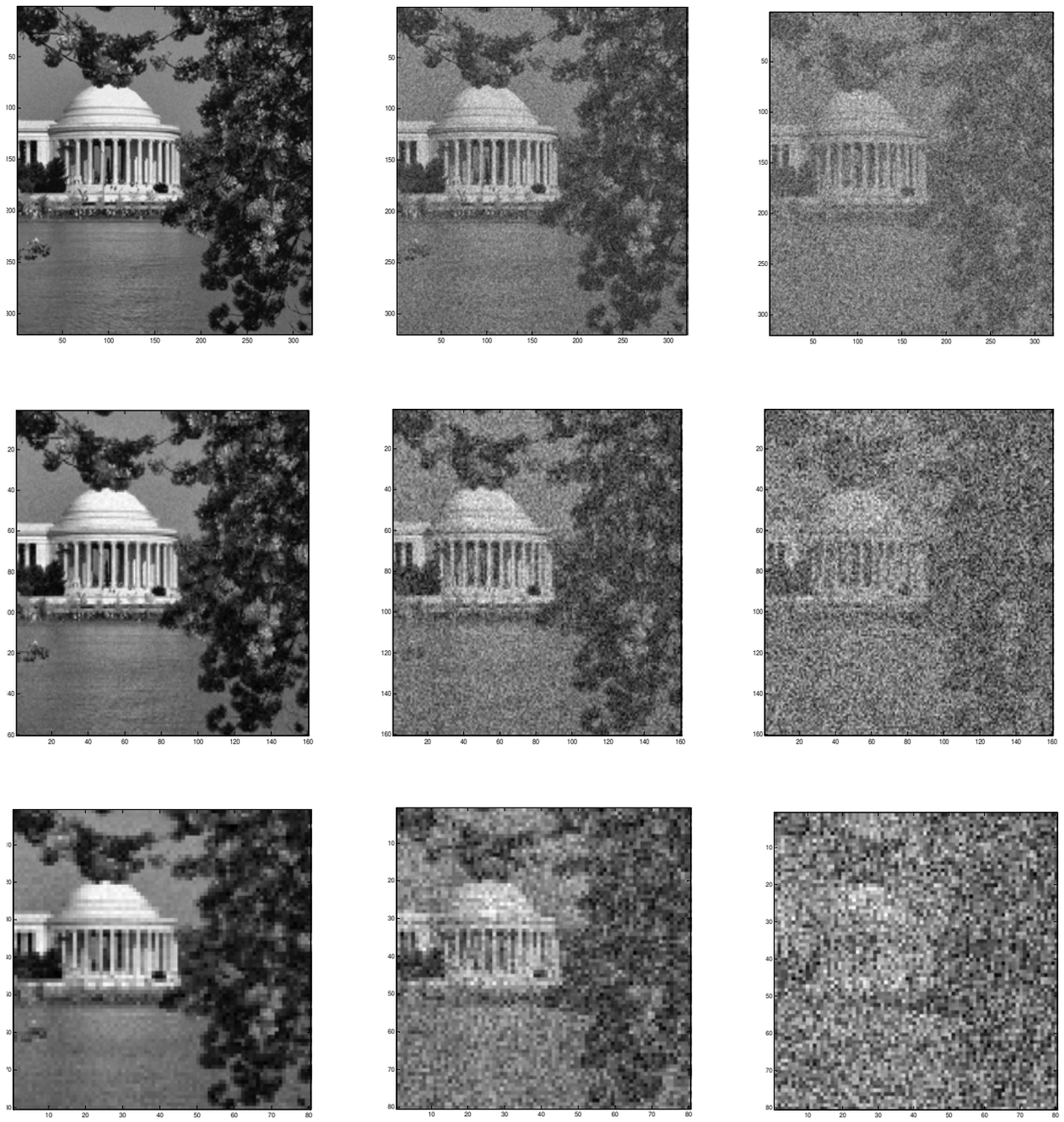

Figure 6. Effects of SNR and resolution on imagery; middle column is typical of an *f*/1.5, 60 Hz, 15 μm pixel broadband NIR imager. The rows (top to bottom) show reduction in resolution (1X, 2X, and 4X). The columns (left to right) show no noise, SNR=3.5 or NEI=2.2×10^{10} photons/s-cm^2, and SNR=1 or NEI=7.7×10^{10} photons/s-cm^2.

3.4. Maximizing the signal

The available signal is determined based on the FPA integration time, quantum efficiency (QE), optics *f*-number (defined as the ratio of lens focal length to diameter of the entrance pupil), and visible-NIR background in the chosen spectral band. The general SNR is calculated as [13]:

$$\mathrm{SNR} = \frac{e_{sig}}{\tilde{e}_{noise}} = \frac{e_{bk,NIR}}{\sqrt{e_{n,bk}^2 + e_{n,read}^2 + e_{n,dark}^2}} \tag{1}$$

where the noise level consists of background, read, and dark current noise. The signal as measured by collected electrons e_{sig} is given by

$$e_{sig} = t_i G \tau_o f \eta \frac{A_{det}}{4F_{\#}^2} \int_{\lambda_1}^{\lambda_2} \Phi_{bk} d\lambda \tag{2}$$

where t_{i} is the integration time, G is the gain, τ_{o} is the optics transmittance, f is the fill factor, η is the QE, A_{det} is the detector area, $F_{\#}$ is the f-number, and Φ_{bk} is the visible-NIR background in photons/sec-cm^2. The background consists of airglow, moonlight and light pollution sources:

$$\int_{\lambda_1}^{\lambda_2} \Phi_{bk} d\lambda = \int_{\lambda_1}^{\lambda_2} \left[t_a \left(\Phi_{airglow} + \Phi_{moon} + \Phi_{solar} \right) + \Phi_{lightpol} \right] d\lambda \tag{3}$$

where the transmittance τ_{a} occurs from ground to space.

3.5. Minimizing noise

The NIR camera noise is a combination of the background noise, readout noise (typically consisting of a few electrons to tens of electrons), and dark current noise. In designing the optics and setting the parameters of the FPA, the dark current and readout noise must be maintained below the background noise. The f-number is the metric for signal and background level noise; however, the focal length required for identifying the object of interest at the desired range must first be specified before the f-number can be determined. It is necessary to know the focal length along with the f-number in order to obtain an adequately accurate SNR for the specific night sky background, which in turn is used to determine the required optical aperture.

The readout noise $e_{\mathrm{n,read}}$ is normally in the range of 10-50 electrons. The background noise is simply the square root of the background electrons collected:

$$e_{n,bk} = \sqrt{t_i G \tau_o f \eta \frac{A_{det}}{4F_{\#}^2} \int_{\lambda_1}^{\lambda_2} \Phi_{bk} d\lambda} \tag{4}$$

Likewise, the dark current noise may be expressed as

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$$e_{n,dark} = \sqrt{\frac{t_i G I_{dark}}{q}} = \sqrt{\frac{t_i G J_{dark} A_{det}}{q}} \tag{5}$$

If the dark current, which is a function of the bias voltage, is further reduced by decreasing the negative bias, uniformity and responsivity may be degraded.

In addition to these basic temporal noises, NIR cameras exhibit spatial noise. Although calibrations usually reduce the spatial noise to levels below that of the temporal noise, spatial noise varieties such as random pattern noise, fixed row and column noise, temporal row and column noise, and frame fluctuation noise all can be observed in the images. The model incorporates all the noise types described in a three-dimensional (3D) noise model, the concept of which is illustrated in Figure 7.

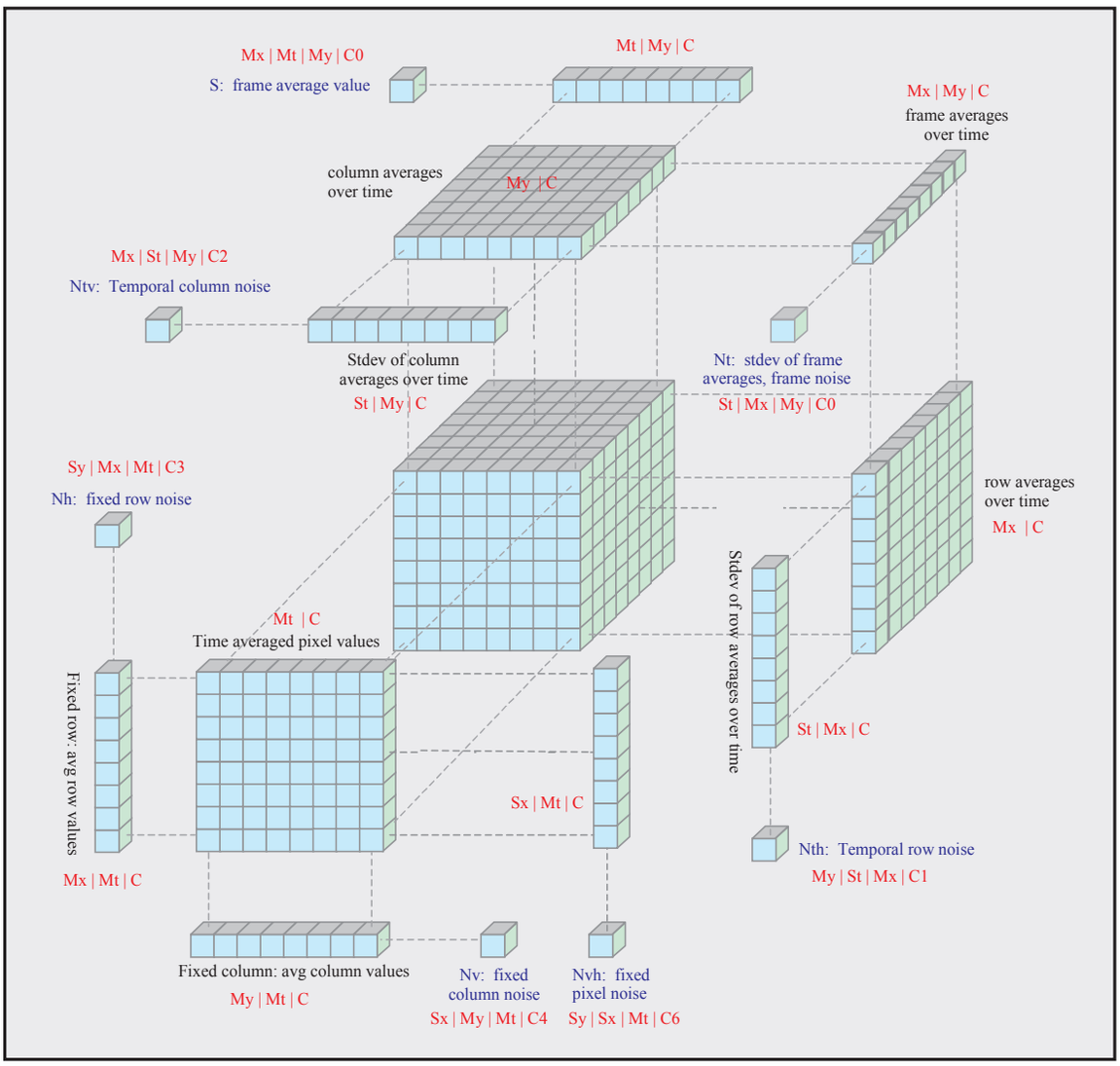

Figure 7. Method of deriving 3D noise from the model illustrated.

The background SNR formula for specific dependencies is expressed as

$$SNR_{bk} = \sqrt{t_i G \tau_o f \eta \frac{A_{det}}{4F_\#^2} \int_{\lambda_1}^{\lambda_2} \Phi_{bk} d\lambda} \tag{6}$$

while the dark current SNR is given by the formula

$$SNR_{dark} = \frac{\sqrt{q t_i G A_{det}} \tau_o f \eta}{4F_\#^2 \sqrt{J_{dark}}} \int_{\lambda_1}^{\lambda_2} \Phi_{bk} d\lambda \tag{7}$$

The sensor NEI condition is

$$\int_{\lambda_1}^{\lambda_2} \Phi_{bk} d\lambda = NEI = \frac{\sqrt{e_{n,read}^2 + e_{n,bk}^2 + e_{n,dark}^2}}{t_i G \tau_o f \eta \frac{A_{det}}{4F_\#^2}} \tag{8}$$

Typical NEIs are in the 8×10^8 to 5×10^9 photon/s-cm^2 range and vary with integration time and *f*-number, where nominal values are in the ranges of 16 to 33 ms and *f*/1.0 to *f*/1.5, respectively. The SNRs in view are for single frames. As was noted, ability of the human eye/brain to integrate some of the frames when perceiving 30 to 60 Hz imagery improves detection and identification performance compared to single static frame viewing. The improvement for random temporal noise dominated images generally varies with the square root of the number of frames the eye can integrate. Eye integration is complicated and varies with light level, resolution, and other factors. This improvement is not only limited by the temporal duration of the eye integration, but also by the underlying spatial noise of the sensor image. Since the level of spatial noise including row and column noise is often marginally below the level of the temporal noise, the eye integration improvement ceases when temporal noise abatement becomes equal to the spatial noise.

The SNR can also be improved by spatially binning pixels, but this is at the expense of sacrificing spatial resolution. This SNR improvement is generally proportional to the square root of the number of binned pixels. Thus, implementing 2×2 binning improves the SNR by a factor of 2. Adding these two phenomena to the previously derived SNR gives:

$$SNR = \frac{e_{sig}}{\tilde{e}_{noise}} = \frac{e_{bk,swir} N_{fs} N_{ps}}{\sqrt{N_{fs} N_{ps} [e_{n,bk}^2 + e_{n,read}^2 + e_{n,dark}^2]_{temporal}} + N_{fs} N_{ps} e_{n,spatial}} \tag{9}$$

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This expression shows the improvement in SNR with the square root of the product of summed pixels and summed frames for the temporal noise part, and demonstrates the ineffectiveness of summing toward improving the SNR of spatial noise dominated imagery.

3.6. Predicting NEI and SNR

NEI vs. operating temperature for pixel sizes of 30, 20, 10 and 5 μm is shown plotted in Figure 8 using a diffusion expression derived from low dark current density data. For these simulations, the following parameters were employed: integration time of 33 ms, gain of unity, read noise of 10 electrons rms, dark current residual nonuniformity calculated for a temperature delta of 0.1 K, optics with *f*/1.25, QE of 80%, and wavelength range spanning 1000-1750 nm. It can be seen that the NEI due to dark current (blue squares) increases as the pixel size is decreased, since the dark current noise is a function of linear pixel size while light collection is a function of pixel area. The NEI improves with pixel size because the number of photons collected increases with detector area while the BLIP noise increases in proportion to the square root of the detector area. For the sensor modeled, the BLIP NEI for 30 μm pixels is 1.5×10^9 photons/s-cm^2, significantly lower than the value of 9×10^9 photons/s-cm^2 determined for 5 μm pixels.

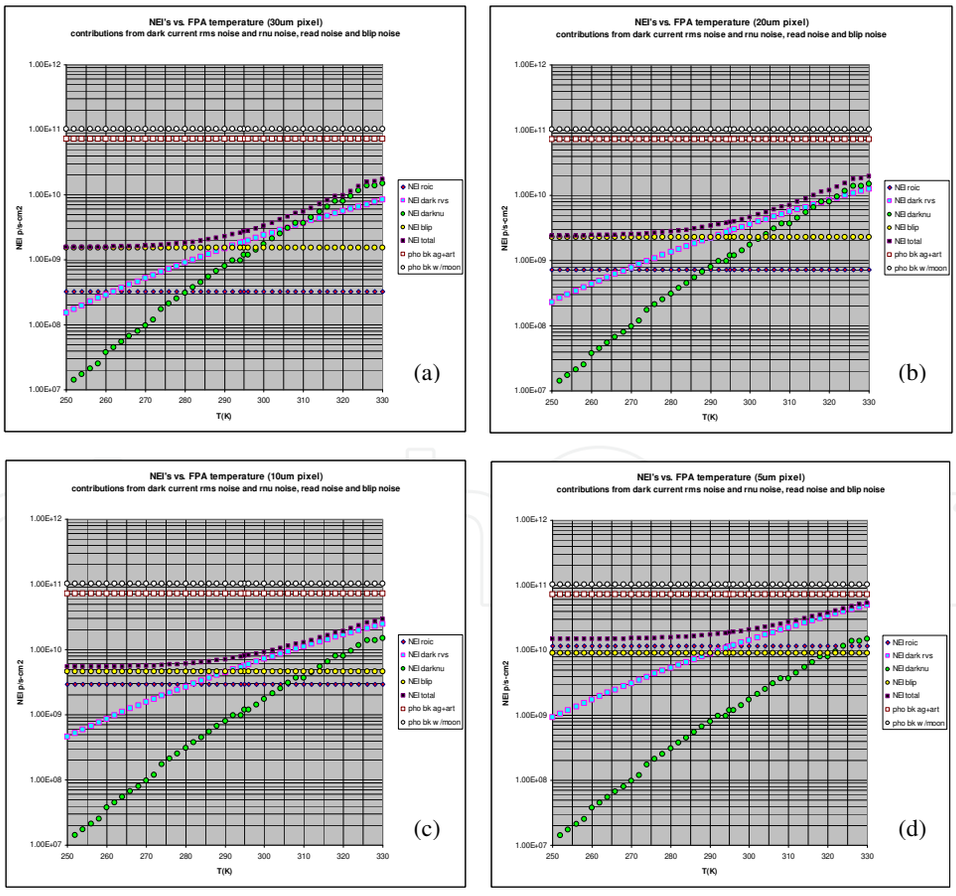

Figure 8. NEI vs. operating temperature for visible-NIR sensors with various pixel sizes: (a) 30 μm, (b) 20 μm, (c) 10 μm, and (d) 5 μm.

Minimizing dark current in SiGe detectors, especially for those with smaller pixels, is a driving requirement. Figure 9 shows the SNR vs. dark current density for 7.5 and 12 μm pixels as a function of dark current density. The level lines are the readout and background SNRs and the slanted lines are the dark current SNRs. The background SNR is the best attainable SNR. The intersection of the lines thus signifies the dark current level where the dark current SNR is equal to the readout or background SNR. In Figure 9(a), the yellow lines signify the background or BLIP SNRs for clear skies with no moonlight for the two pixel sizes, with the upper yellow line showing the SNR for 12 μm pixels and 0.89 moonlight conditions. In Figure 9(b), the readout noise SNR (red squares) has been added for both large and small pixels (based on 10 noise electrons per integration).

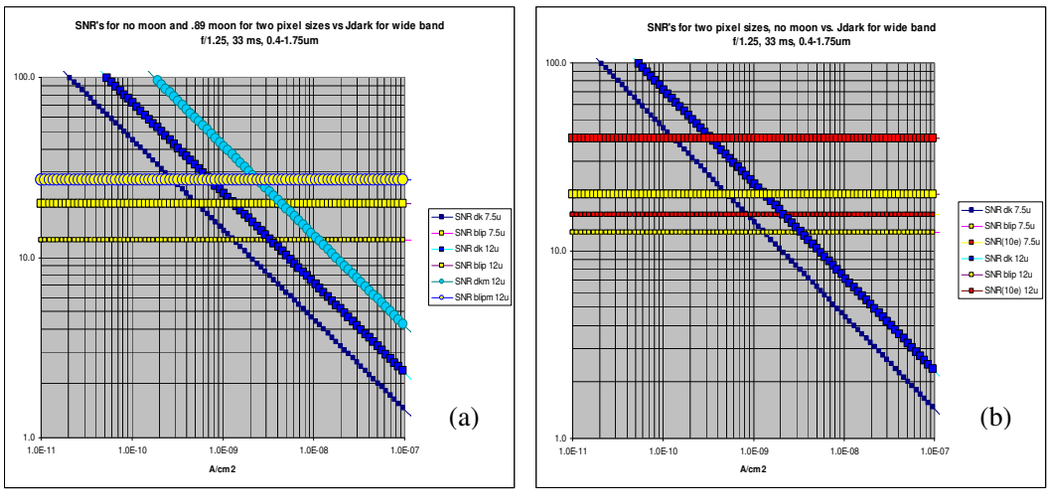

Figure 9. (a) SNR vs. dark current density for 7.5 and 12 μm pixels for dark sky, 0.89 moonlight conditions, *f*/1.25, 33 ms integration time, and 400-1750 nm bandpass; (b) shows the addition of read noise based SNR (10 electrons).

Dark current appears to be the performance limiting factor for small pixel NIR FPAs operating at RT. The performance can be improved by compensating for the dark currents using lookup tables, though nonuniformity due to uncompensated variance in dark current over the FPA must also be characterized. While utilizing lookup tables should smooth out most of the nonuniformity, there will be residual nonuniformity as a result of the FPA pixels' dark current to temperature difference ratios at RT in combination with the temperature increment used in the lookup tables. The dark current residual nonuniformity must be kept below the average dark current noise level to preserve the performance, as illustrated in Figure 9.

3.7. SiGe imager performance based on modeling results

Miniature SiGe detector based FPAs that can be incorporated into handheld cameras or inserted into smartphones require *f*/2 to *f*/3 optics and pixels approximately 5-7 μm in size. These detectors will consequently have reduced light collection with relatively high dark currents at RT. Such higher *f*-numbers, which are about twice those characteristic of an ideal NIR camera, effectively reduce the signal and SNR by about a factor of four. While small optics of *f*/1 to *f*/1.5 are possible, these may require an increase in optics diameter. Another method

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to improve the SNR in dark current limited NIR sensors is to incorporate a microlens array (e.g., having 20 μm lens centers) to focus light from the scene onto 5-7 μm detector pixels. This maintains the signal strength while reducing detector dark current, enabling small pixel sizes within a larger cell that allows for extra on-chip signal processing electronics.

Predictions based on the modeling that has been detailed in this section are summarized as follows: Imaging under rural night sky conditions becomes challenging for small pixel, small optics designs, and dark currents can significantly impact performance in an uncooled NIR camera. A small NIR camera will respond well to minimal amounts of illumination from a direct NIR source, such as one imaged in indoor or shorter-range outdoor environments. In addition, the performance limitations of small uncooled NIR cameras are not found to be problematic for live fire detection and identification applications. Overall, these findings indicate that low-cost, small pixel, uncooled detectors based on growth of SiGe on Si are potentially advantageous for imaging in indoor or low light level outdoor environments.

4. Operation and performance of SiGe photodetectors

A photodetector may be basically defined as a device that converts an optical signal (photons) into an electrical one (electrons). There exist three primary classes of semiconductor based photodetectors: avalanche photodiodes (APDs), metal-semiconductor-metal (MSM) detectors, and p-i-n (*pin*) detectors. [An additional type of detector device, known as a metal-insulator-semiconductor (MIS) photodetector featuring an insulator layer inserted between metal and semiconductor layers [30], has been developed as well but is not that common.] Detector devices of each of these three main classifications based on SiGe technology have been demonstrated. For the visible-NIR detection applications in view, SiGe based MSM and *pin* devices are the best suited, with each having associated advantages and disadvantages that will be discussed in some detail throughout the remainder of this section.

4.1. Avalanche Photodiodes (APDs)

APDs, which are commonly employed in high bitrate optical communication systems, achieve high built-in gain through avalanche multiplication, and require high bias voltages (~20 V/μm) to achieve desired ionization rates and provide detection of low power signals with high sensitivity [12]. Under sufficiently high external bias, the electrical field in an APD's depletion region causes photogenerated electrons from the absorption layer to undergo a series of impact ionization processes. This enables a single absorbed incoming photon to generate a large number of electron/hole pairs (EHPs), which effectively amplifies the photocurrent and improves the sensitivity, providing a QE potentially greater than unity. SiGe APDs typically have separate absorption-charge-multiplication (SACM) structures (see Figure 10), in which light is absorbed in an intrinsic Ge film and electrons are multiplied in an intrinsic Si film; such structures allow optimization of both QE and multiplication gain [10].

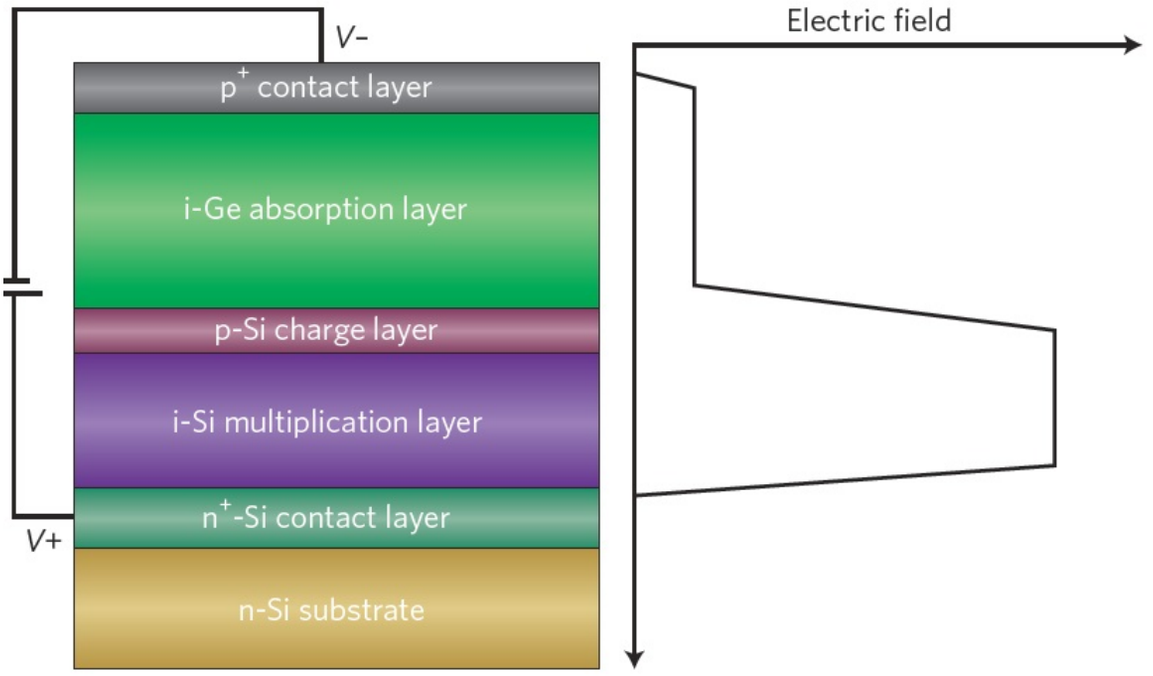

Figure 10. Schematic cross-section of a SiGe based APD device with a separate absorption-charge-multiplication (SACM) structure and its internal electric field distribution [10].

The most important performance metrics for APDs are ionization ratio (which should be minimized), internal electric field distribution, excess noise factor, gain-bandwidth product, and sensitivity [4]. The device structure of a basic APD is similar to that of a *pin* photodetector. Compared with their *pin* counterparts, APDs offer 5-10 dB better sensitivity and higher SNR due to their internal multiplication gain, as well as high bandwidth-efficiency products [4,31]. However, the comparatively low operation bandwidths and the requirement of very high bias voltages limit the integration potential of SiGe based APDs into practical CMOS-based devices.

4.2. Metal-Semiconductor-Metal (MSM) photodetectors

MSM photodetectors comprise two back-to-back Schottky contacts and feature a closely spaced interdigitated metal electrode configuration on top of an active light absorption semiconductor layer [32]. The material, physical, and electrical properties of MSM devices are depicted in Figure 11(a), (b), and (c), respectively. MSM detectors are photoconductive devices not functional under zero bias, and require sufficient external bias for the semiconductor layer to become fully depleted. The Schottky junctions present in MSM detectors exhibit rectified current-voltage (I-V) characteristics as do *pn* junctions, but occur at the metal-semiconductor rather than semiconductor-semiconductor interfaces. Also, while *pn* junctions allow both electrons and holes to flow under forward bias, Schottky junctions allow only majority carriers to flow.

Advantages of MSM detectors include low capacitance and consequent low RC delay, which enables high-speed operation. Detection bandwidths for SiGe based MSM devices are comparatively high, making them suitable for fast optical fiber communications. In addition,

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since MSM detectors are inherently planar and require only a single photolithography step, they are relatively easy to fabricate, boosting their potential for practical integration. However, the external QE and effective responsivity in MSM devices are generally lower than those in *pin* detectors due to shadowing of the metal electrodes, which typically occupy 25-50% of the surface area [18].

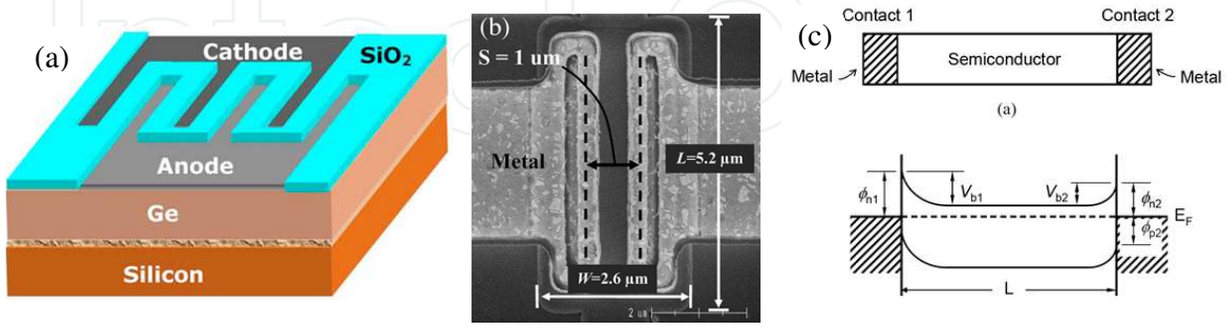

Figure 11. (a) Cross-section of MSM photodetector fabricated on Ge layer grown on Si substrate [33]. (b) Scanning electron microscope (SEM) image of an evanescent waveguide-coupled Ge-on-SOI MSM photodetector [34]. (c) Schematic diagram of MSM structure and corresponding energy band diagram at thermal equilibrium [12].

In addition, high dark current associated with SiGe based MSM devices, primarily as a result of hole injection over the Schottky barrier [35], is a significant problem that raises the noise floor and increases standby power consumption [10]. This dark current may include current associated with thermally generated electron-hole pairs and carrier injection over the Schottky barriers, since SiGe MSM detectors typically have poor Schottky contacts with Ge [12]. While techniques to suppress dark current in MSM devices, such as dopant segregation and utilizing an intermediate layer of amorphous Ge and SiC, have suppressed dark current in detection devices significantly [36], MSM detectors generally still exhibit higher levels of dark current than comparable SiGe based *pin* devices [37] often resulting in an inferior level of performance [4].

4.3. *Pin* photodetectors

As their name may suggest, *pin* photodetectors consist of an intrinsic (*i*) region sandwiched between heavily doped $p^+$and n^+semiconductor layers. A typical *pin* photodetector design cross-section is depicted in Figure 12(a). The p^+/n^+regions may be formed by implantation, *in situ* doping, or consist of a highly doped monocrystalline Si substrate [15,38]. The depletion layer in which all absorption occurs is almost entirely defined by the thicker highly resistive intrinsic region. This is in contrast to a common *pn* photodiode, in which the width of the depletion region (usually thinner than that in *pin* devices) is governed by the applied external electric field.

SiGe based *pin* photodetector structures can exhibit significant built-in electric fields of several kV cm^{-1} inside the *i*-Ge/SiGe layers, which overcome recombination processes at lattice defects, improving the device quality and enabling smaller devices [10]. The uniform electric field *F* in the intrinsic region in a *pin* photodetector is given approximately by [41]:

$$F = \left(V_{bi} - V\right) / w_D \tag{10}$$

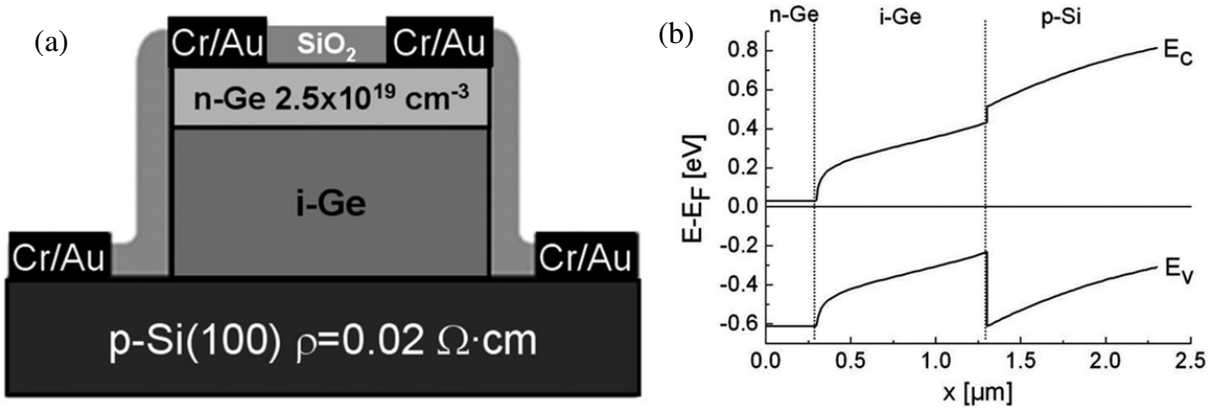

Figure 12. (a) Cross-sectional schematic view of SiGe based *pin* photodetector structure [39]. (b) Band diagram of *pin* Ge/Si heterojunction [40].

where V is the applied voltage, V_{bi} is the built-in voltage, and w_D is the thickness of the depletion or intrinsic region. Upon absorption of a photon in the intrinsic region of energy $h\nu > E_g$, EHPs are created and immediately separated by the external electric field resulting from reverse biasing the device, leading to generation of photocurrent. Absorption outside the intrinsic region will also result in photocurrent if the minority carriers manage to diffuse to the intrinsic region. Since there are few charge carriers in the intrinsic region, the space charge region reaches completely from the *p*-type to the *n*-type region. Figure 12(b) shows the energy band diagram of a *p*-Si/*i*-Ge/*n*-Ge heterojunction.

The intrinsic/depletion region thickness, which is normally made substantially larger than that of the $p^+$and n^+regions, can be tailored to optimize detector performance [4]. Having a relatively thick depletion region with a strong internal electric field causes most of the generated EHPs to be transferred to the p^+/n^+regions and collected as a result of carrier drift rather than diffusion. (Since the valence band offset is much larger than the conduction band offset, the higher barrier in the valence band limits the movement of holes, so the conductivity in *pin* heterojunctions is due to electrons in the conduction band [40].) This in turn results in less carrier recombination at dislocations or point defects, leading to higher collection efficiency [10]. Because of this as well as other factors, a thicker depletion region in a *pin* photodetector is associated with higher responsivity and QE. On the other hand, having a thinner intrinsic region in a *pin* detector reduces the transit time, thereby enhancing the response bandwidth [4]. However, a thinner intrinsic layer also effects a larger capacitance, which produces greater RC delay that can have a limiting effect on the detector speed of operation [12].

There are two main classifications of SiGe based *pin* photodetectors structures: normal incidence (NI) and lateral. As might be expected, in the former type of device light is incident vertically or normal to its top or bottom surface, while in the latter type the photons are incident horizontally or laterally. In addition, a substantial portion of SiGe *pin* detectors now have

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waveguide-coupled (WC) designs, which circumvent alignment issues by featuring either evanescent coupling or butt-coupling between integrated SiGe detectors and Si optical waveguides. Practically all lateral (and some NI) *pin* photodetectors are WC. The advent of practical WC SiGe *pin* photodetectors was relatively recent— virtually all such detector devices have been reported within the past decade. While lengths of early WC *pin* photodetectors were typically on the order of 100 μm to ensure full absorption of light around 1550 nm [4], more recent devices are have been designed smaller (~10X) to reduce the RC delay and maximize potential bandwidths [42].

4.4. Reported performance of SiGe *pin* photodetectors

Due to their comparative ease of fabrication, performance advantages, and prevalence, the focus throughout the remainder of this chapter centers primarily on SiGe based *pin* photodetectors and associated technology. Performance specifications reported for NI and WC *pin* SiGe photodetectors are given in Table 1 and Table 2, respectively. In Table 3 and Table 4, typical ranges of performance results for MSM detectors and typical APD specifications, respectively, are presented for comparison.

WL (μm)	Resp. (A/W)	DC Dens. (mA/cm^2)	DC (μA)	BW V_{Bias} (V)	BW (GHz)	V_{Bias} (V)	Pub. Year	1st Author	Ref.
1.3	0.13	0.2	0.2	-1	2.3	-3	1998	S. Samavedam	[43]
1.55	0.33	30	12	-1	~0.4	-4	2000	L. Colace	[20]
1.55	0.75	15	0.14	-1	2.5	-1	2002	S. Fama	[44]
1.55	0.035	100	0.31	-1	38.9	-2	2005	M. Jutzi	[37]
1.55	0.56	10	0.79	-1	8.5	-1	2005	J. Liu	[15]
1.55	—	375	0.075	—	39	-2	2006	M. Oehme	[45]
1.3	0.45	6.4	0.20	-1	8.8	-2	2006	M. Morse	[46]
1.55	0.28	180	0.57	-1	17	-10	2006	Z. Huang	[47]
1.55	0.20	~200	~10	-1	10	-1	2006	L. Colace	[48]
1.55	0.037	27	0.035	-1	15	-1	2007	T. Loh	[49]
1.55	1.0	130	~0.1	-1	49	-2	2009	S. Klinger	[50]
1.55	0.8	—	0.042	-1	36	-3	2009	D. Suh	[51]

Table 1. Reported performance specifications of NI *pin* SiGe photodetectors.

Compared to NI detectors, WC SiGe *pin* photodetectors generally have similar bandwidths (up to 47 GHz), higher responsivity and QE, and dark currents and dark current densities that are comparable in magnitude. Among *pin* WC detectors, lateral structures have demonstrated higher QE values compared to NI devices due to less light consumption in the highly doped region, while achieving similar response speeds [42].

Resp. (A/W) @ 1.55 μm	DC Dens. (mA/cm²)	DC (μA)	BW V_{Bias} (V)	BW (GHz)	V_{Bias} (V)	Pub. Year	1st Author	Ref.
0.87	1.3×10^3	0.9	-1	7.5	-1	2007	D. Ahn	[54]
0.89	51	0.17	-2	31.3	-2	2007	T. Yin	[55]
1.0	0.7	0.0002	-1	4.5	-3	2008	M. Beals	[56]
0.65	—	0.06	-1	18	-1	2008	J. Wang	[42]
1.0	60	~1	-1	42	-4	2009	L. Vivien	[57]
1.1	1.6×10^4	1.3	-1	32	-1	2009	D. Feng	[52]
0.8	—	0.072	-1	47	-3	2009	D. Suh	[58]
1.1	28	1.3	-1	36	-3	2010	D. Feng	[59]
0.78	40	0.003	-1	45	-1	2011	C. DeRose	[60]
0.8	71	0.025	-1	45	0	2013	L. Virot	[61]

Table 2. Performance specifications of WC *pin* SiGe photodetectors.

In comparison to SiGe based MSM devices, SiGe *pin* detectors offer high bandwidths, low noise, and high responsivities. Responsivities reported for some *pin* devices are as high as ~1 A/W (and even greater for certain WC detectors), and typically are substantially better than those of MSM devices [50,52]. SiGe *pin* detectors generally also offer higher responsivities and lower dark currents than SiGe APDs. SiGe *pin* detector devices have demonstrated responsivities at 1310 and 1550 nm that are similar to those of commercially available InGaAs photodetectors [53].

Parameter	Best	Typical	Worst
Responsivity @ 1.55 μm	0.8-1.2 A/W	0.53-0.75 A/W	0.10-0.14 A/W
Dark Current Density	85-100 mA/cm²	0.6-2.0 A/cm²	650-1000 A/cm²
Dark Current	0.011-0.020 μA	4-10 μA	90-4000 μA
Bandwidth	36.5-40.0 GHz	10-25 GHz	1.0-4.3 GHz

Table 3. General performance specification ranges of MSM type SiGe photodetectors.

Bandwidths of Ge/SiGe *pin* photodetectors have improved from several gigahertz to close to 50 GHz in recent years, and are presently comparable to those of MSM devices. Currently the highest *pin* detector bandwidth is 49 GHz at-2 V reverse bias as reported by Klinger *et al.*, and three reported WC detectors can operate above 45 GHz, fast enough to accommodate future 40 Gb/s telecommunications applications [50]. Techniques considered to enhance bandwidths further include limiting the thickness of the Ge/SiGe intrinsic layers in *pin* photodiodes to reduce carrier transition times, and altering the device structure to limit undesirable parasitic effects.

Parameter	Best	Typical	Worst
Responsivity @ 1.55 μm	0.80 A/W	0.40 A/W	0.17 A/W
Dark Current	~10 μA	~50 μA	~100 μA
Bandwidth	~35 GHz	~12 GHz	~5 GHz
Gain-bandwidth Product	350 GHz	105 GHz	50 GHz

Table 4. General performance specifications of SiGe APDs.

Reported dark currents and dark current densities in SiGe *pin* detectors are both on average approximately two orders of magnitude lower compared to those of MSM devices, with dark current densities of certain *pin* devices as low as in the μA/cm^2 range [42]. The dark current and dark current density results presented were almost entirely measured for devices biased at 1 V. To minimize dark current and operating power further, there has recently been increasing research interest in the development of lower bias or even zero-bias *pin* photodiodes. Zero-bias SiGe *pin* photodetectors have demonstrated responsivities at 0 V bias nearly equivalent to the saturated value at 2 V bias [15], as well as 3 dB bandwidths as high as 25 GHz [38].

5. Design objectives of SiGe pin photodetectors

5.1. $Si_{1-x}Ge_x$ photodetector design parameters

While some early attempts to develop SiGe IR detectors concentrated on potential LWIR applications [62,63], in this chapter we focus solely the development of devices for applications involving detection in the NIR band (up to ~1700 nm). The most straightforward method by which to adjust the cutoff wavelength of a SiGe photodetector in order to tune its range of response is to modify the $Si_{1-x}Ge_x$ alloy composition. Si and Ge have the same type of crystallographic structure and the materials can thus be alloyed with varying Ge concentrations. For $Si_{1-x}Ge_x$ alloys, the lattice constant does not exactly follow Vegard's law. The relative change of the lattice constant is given by [63]:

$$a_{Si_{1-x}Ge_x} = 0.5431 + 0.1992x + 0.0002733x^2 (\text{nm}) \tag{11}$$

The concentration of Ge in a layer of $Si_{1-x}Ge_x$ may be accurately measured using characterization techniques such as X-ray diffraction (XRD). As the Ge concentration is increased, the band gap of the material is reduced, and therefore the cutoff wavelength of a detector will increase (extending its operational wavelength range) assuming all other factors remain constant. However, from a practical device fabrication standpoint, depositing pure Ge or SiGe with very high Ge concentration entails certain technical challenges; for instance, as predicted by Equation (11), a higher Ge concentration of $Si_{1-x}Ge_x$ grown on Si results in a larger lattice

mismatch between the materials. This can lead to Stranski-Krastanov growth in which islands form to relieve the misfit strain, which in turn leads to rougher surfaces [12]. However, as will be discussed in the following section, the incorporation of even small amounts of tensile strain can be utilized to extend the operating range of a SiGe photodetector having an absorption layer of a given Ge concentration further into the NIR regime. In addition, modification of parameters such as the doping concentration and growth temperature can be undertaken to further fine-tune the spectral response of a device. Thus, there are multiple factors that more or less influence the operational wavelength range of a SiGe based detector. These must be properly balanced in the process of designing and developing a detector device that exhibits required and optimal performance characteristics for a given application(s).

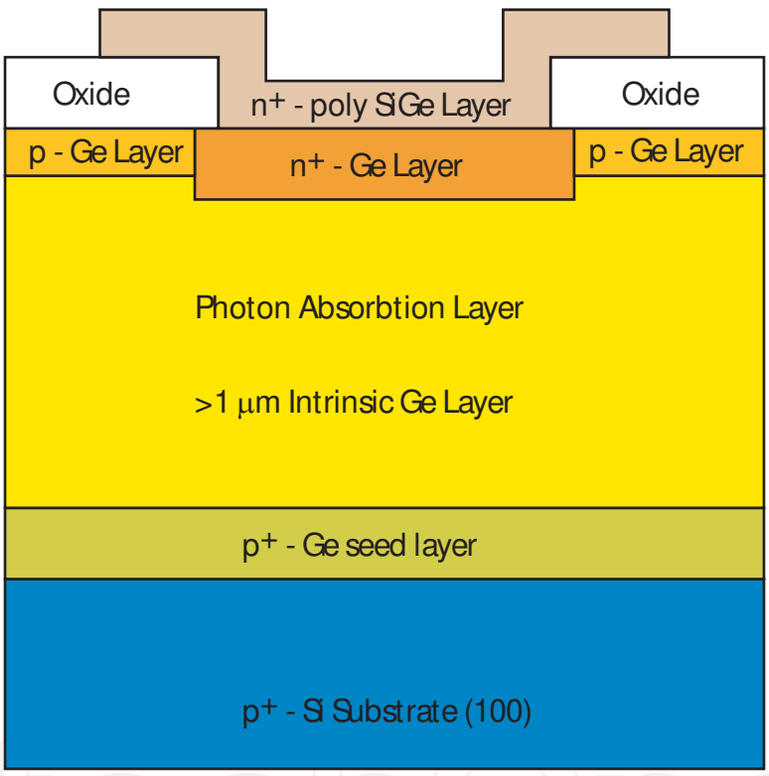

Figure 13. SiGe *pin* photodetector structure used to evaluate impact of various fabrication methodologies [64].

A diagnostic *pin* photodetector device structure designed to evaluate the impact of various fabrication methodologies to reduce leakage currents and produce higher detector performance is shown in Figure 13 [64]. The structure, from the bottom up, consists of a p^+Si substrate, thin p^+Ge seed layer, thicker *i*-Ge layer, and top n^+polysilicon layer with an underlying n^+doped Ge region. The polysilicon layer covers sections of oxide deposited on the sides of the top surface of the cylindrical detector, under which shallow *p*-Ge regions may form. This structure can be used to help to assess the following: ability to grow high quality/low defect density Ge on Si; layer thicknesses necessary for minimal topological and defect density requirements; and isolation of defect states at the Ge/oxide interface from the signal carrying layers. Also of relevance is the determination of the optimum doping level and thickness of the lighter doped

p-type Ge regions under the oxide to isolate interface states and lateral leakage current that could result between the highly doped n^+Ge region below the polysilicon and the p^-Ge regions.

5.2. Incorporating strain to improve NIR detection

Strains and consequent stresses normally arise during epitaxial growth of thin films on substrates of different compositions and/or crystal structures. Internal strains and stresses can result from a mismatch in the lattice constants of the individual layers, which is illustrated in Figure 14. If the lattice mismatch between two materials is less than ~9%, the initial layers of film will grow pseudomorphically, i.e., the films strain elastically in order to maintain the same interatomic spacing. As the film grows thicker, the increasing strain will create a series of misfit dislocations separated by regions of relatively good fit.

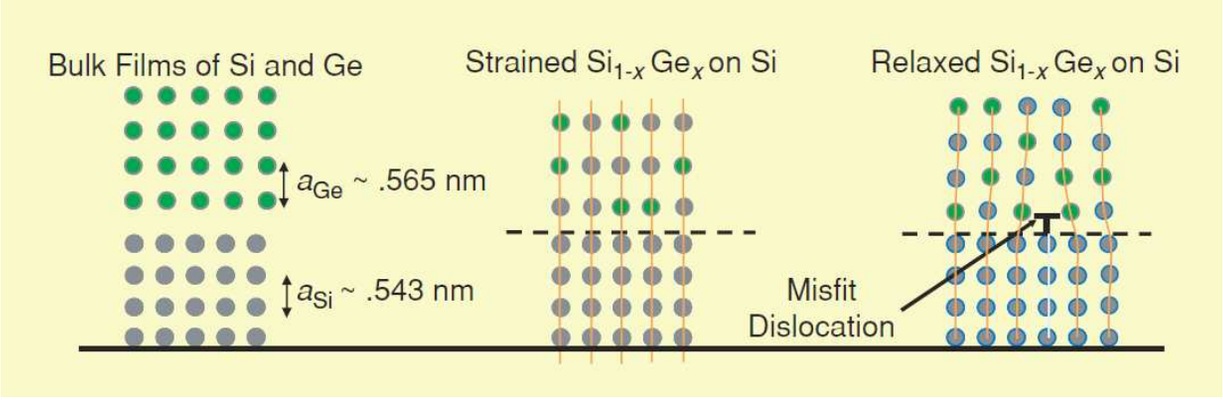

Figure 14. Relationship between lattice mismatch of Si and Ge and misfit dislocations that degrade detector performance [18].

Since the lattice constant of Ge exceeds of that of Si by 4.18%, very thin $Si_{1-x}Ge_x$ ($x > 0$) layers grown on a Si substrates are initially compressively strained. Near perfect epitaxial growth of such a strained heteroepitaxial layer can be achieved if its thickness does not exceed a critical thickness for stability. Since the pseudomorphic critical thickness for growth of Ge on Si with strain due to lattice mismatch is less than 1 nm, a Ge layer that is grown with a thickness that is substantially larger than this limit will relax through the formation of misfit dislocations [7,10].

However, the difference in thermal expansion coefficients between the layers can also play a significant role in the development of strain following epitaxial growth. Since Ge has a larger thermal expansion coefficient than Si, when the temperature cools to RT after growth the consequent reduction in the lattice constant of a deposited Ge/SiGe layer will be suppressed by the Si substrate [65]. This results in the generation of residual tensile strain in the Ge/SiGe layer normally within the range of 0.15-0.30% [9,66]. The changes in band gap energy and absorption that occur with the introduction of strain are depicted in Figure 15(a) and (b), respectively.

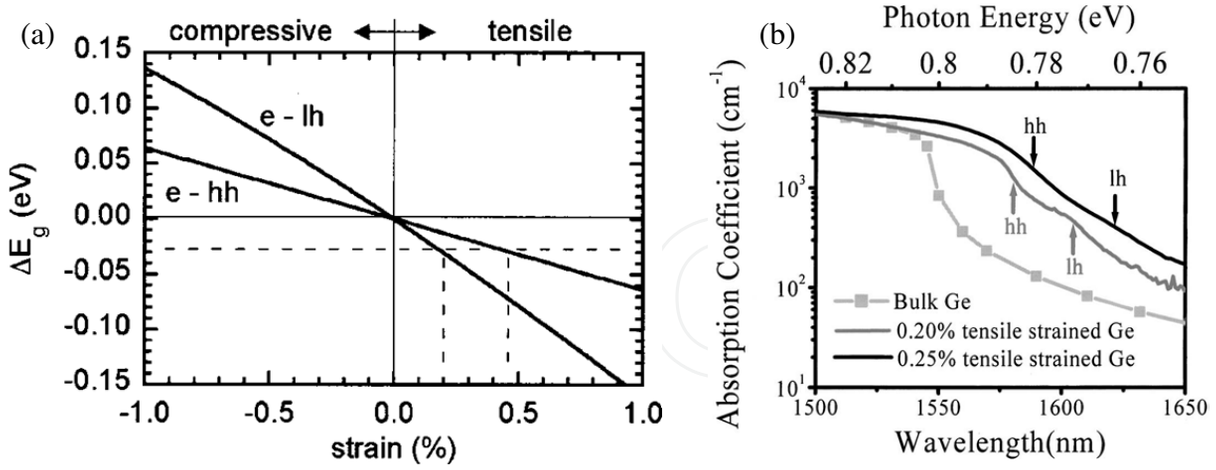

Figure 15. (a) Calculated change in direct band gap energy as a function of strain in Ge [65]. (b) Absorption spectra of bulk Ge, and 0.20% and 0.25% tensile strained Ge [53].

The presence of this biaxial tensile stress in Ge causes the valence subbands to split, where the top of the valence band comprises the light hole band. The light hole band energy increases and consequently both the direct and indirect gaps shrink, with the direct gap shrinking more rapidly. Thus, with the increase of tensile strain, Ge transforms from an indirect gap material towards a direct gap material. This stress-induced shift in valence subbands is depicted in Figure 16(a).

Upon application of tensile strain, e.g., of 0.2%, the direct band gap of Ge reduces from 0.80 eV for unstrained material to ~0.77 eV, which effectively increases the corresponding cutoff wavelength from 1550 to 1610 nm [15,65]. As shown in Figure 16(b), this provides greater sensitivity for sensor operation at NIR wavelengths of 1600 nm and above due to the higher absorption coefficient (~5X) and recombination rates of the strained Ge over this range [9]. This extended operational range is very useful for telecommunications, since strained layer SiGe based sensors can operate over most or all of the L band spanning 1560-1620 nm, as well as for other applications requiring detection of longer wavelengths in the NIR regime.

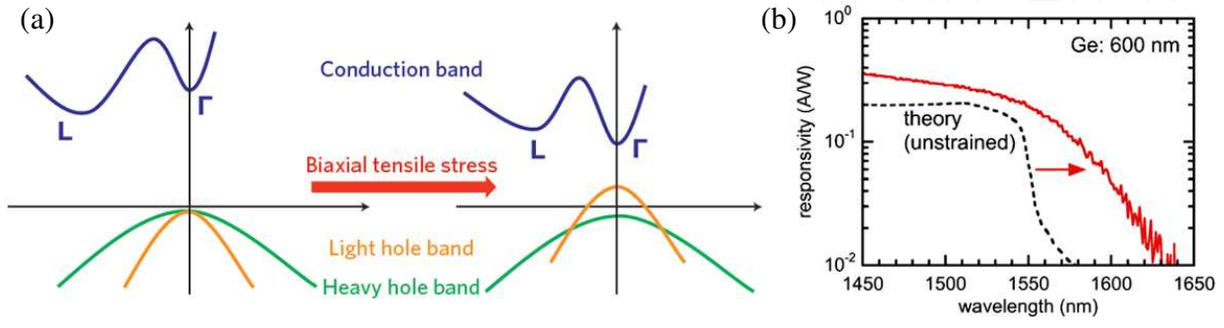

Figure 16. (a) Shift of Ge from indirect gap toward direct gap material with application of tensile strain [10]. (b) Comparison of responsivity spectra for *pin* photodetectors having unstrained and strained Ge layers [67].

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5.3. Reducing dark current

The growth of Ge on Si can be characterized as Stranski-Krastanov growth, an example of which is shown in Figure 17(a). For film thicknesses below the critical thickness, a 2D wetting layer is formed, beyond which a transition to 3D islanding growth mode occurs to relieve the built-in strain in the Ge layers [66]. Defects and threading dislocations arising during Stranski-Krastanov growth typically form recombination centers. At RT, dark current in *pin* photodetectors, i.e., the current measured under reverse bias with no illumination, is mainly due to generation current through such traps [68]. Higher levels of dark current result in increased power consumption that reduces detector performance, and shot noise associated with this leakage current can also degrade the SNR [5] and lower sensitivity for NIR systems [1]. Figure 17(b) shows typical I-V characteristics SiGe devices where the dark current at negative bias increases proportionally to device size.

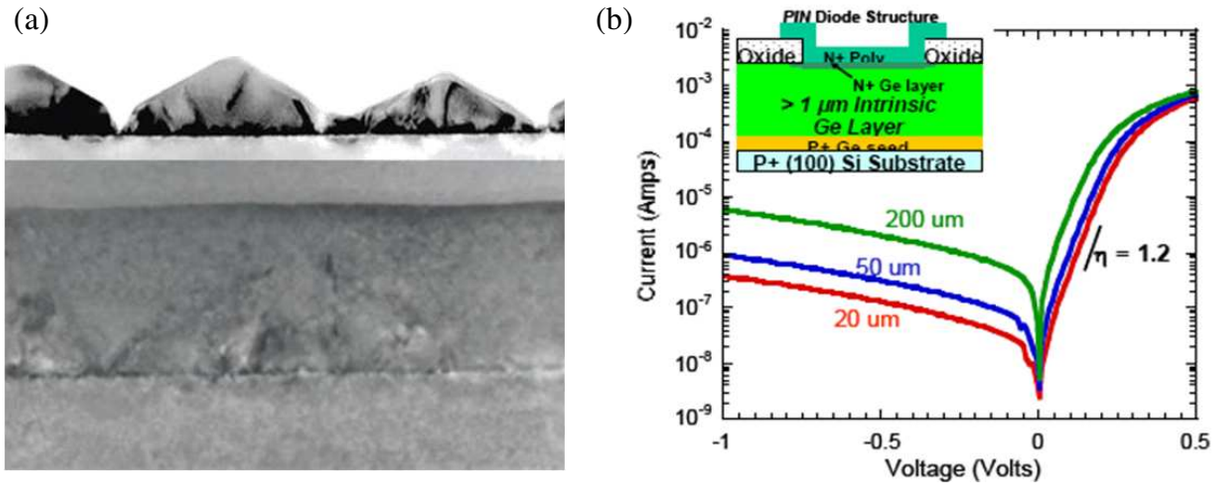

Figure 17. (a) Ge-on-Si Stranski-Krastanov epitaxial growth [10]. (b) Measured RT I-V characteristics for large area diodes with 20, 50 and 200 μm unit cells; the inset shows a schematic of the device cross-section [24].

Since dark current can be particularly high in SiGe based photodetectors, a major research thrust has been to reduce the dark current to the greatest extent possible in order to enhance sensitivity and boost overall device performance. (It is noted that in SiGe *pin* photodetectors dark current increases with applied electric field and does not saturate, and thus the measured dark current is usually specified at a given reverse bias, e.g.,-1 V.) The goal is to limit the dark current to levels acceptable for high-speed operation usually considered to be not more than 1 μA [54] (or dark current densities of 1-10 mA/cm^2), above which the transimpedance amplifier noise will be exceeded [35] and the SNR reduced [1]. However, a precise value of the required dark current is dependent upon the particular speed of operation and the amplifier design. Thermionic emission limits the dark current density in SiGe photodetectors down to ~10^{-2} mA/cm^2 at RT, which is around two orders of magnitude higher than that of standard InGaAs based photodetectors [10].

Various approaches have been proposed to further reduce the dark current in SiGe detectors by several orders of magnitude, including superlattice structures [24], incorporation of quantum dots [63], use of buried junctions [69], and graded compositional layer designs [68]. Dark current generally scales with device area, so reducing the overall size of SiGe detector devices is one means of limiting leakage current for a given photodetector design. For the fabrication of SiGe *pin* detectors, a two-step growth process and high temperature anneal (which will be covered in Section 6) can reduce threading dislocations and thus resultant dark current and dark current density [43,70]. The effects of a buffer layer grown by two-step growth and high temperature annealing on dark current density are shown in Figure 18(a) and (b), respectively. The splitting of the valence bands in Ge due to the presence of tensile strain also lowers the density of states for holes, leading to reduction of intrinsic carrier density that can likewise contribute to reduced reverse dark current in devices [65]. Further methods to effect reductions in dark current include improving surface passivation and/or utilizing smaller selective growth regions during device fabrication [63].

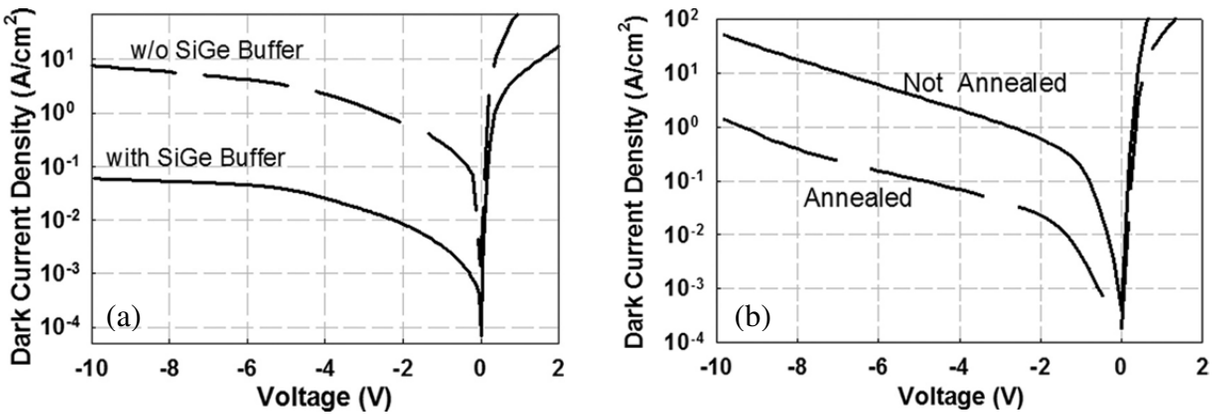

Figure 18. Effect of (a) buffer layer grown by two-step growth, and (b) high temperature annealing, on dark current density characteristics [68].

6. Fabrication of SiGe *pin* photodetectors

6.1. SiGe detector growth methods

Epitaxial growth of Si/SiGe using gas precursors has been utilized for the past three decades [10]. Selective growth of Ge/SiGe epitaxial films, using mask layers such as SiO_2 and Si_3N_4, generally requires the formation of vertical sidewalls [usually by reactive ion etching (RIE)] to minimize faceting and enhance trench filling [9]. An early method for growing Ge on Si, first proposed by Luryi *et al.* in 1984 [71] and later optimized by other groups, involved using graded SiGe buffer layers to reduce the density of threading dislocations arising in the Ge layer. Such graded structures lead to an optimized relaxation of the graded layers, where existing threading dislocations are more effectively utilized to relieve stress [43]. However, this method requires significant time and resources as well as necessitates films at least 6 μm

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thick that are associated with large residual surface roughness, which are problematic for the fabrication of practical, cost effective-devices [4,72].

In recent years the most prevalent and useful method to deposit Ge/SiGe layers to form functional *pin* detector devices has involved a two-step growth process where the growth temperature is ramped up between the growth steps. This technique was first applied to epitaxial grown Ge on Si by Colace *et al*. in 1998 [73], and it has since been commonly adopted for Ge epitaxial growth. This method most often involves deposition of Ge/SiGe on intrinsic Si, but growth of Ge on silicon-on-insulator (SOI) surfaces has also been demonstrated [20].

6.2. Two-step growth process overview

The two-step growth process commonly used for fabricating NI *pin* detectors consists of initial low temperature (LT) epitaxial growth of Ge/SiGe to form a thin strain-relaxed layer, followed by relatively high temperature (HT) growth to form the thicker absorbing film, and a subsequent HT anneal [16,70,74]. In general, the growth steps are primarily designed to prevent islanding. The first LT growth step is crucial in governing the film crystalline quality and the surface morphology and also the final strain state in the Ge films [66]. Ge/SiGe films grown using this process have been shown to have reduced rms surface roughness of less than 1 nm [15,70]. In addition, the HT anneal reduces threading dislocations arising from lattice mismatch between the Si and Ge to enable a higher quality Ge film with reduced dark current [9]. Figure 19(a) shows a cross-sectional view of a Ge layer grown on Si with a close-up view of the Ge-Si interface, while Figure 19(b) comprises a top view of the fabricated *pin* photodetector.

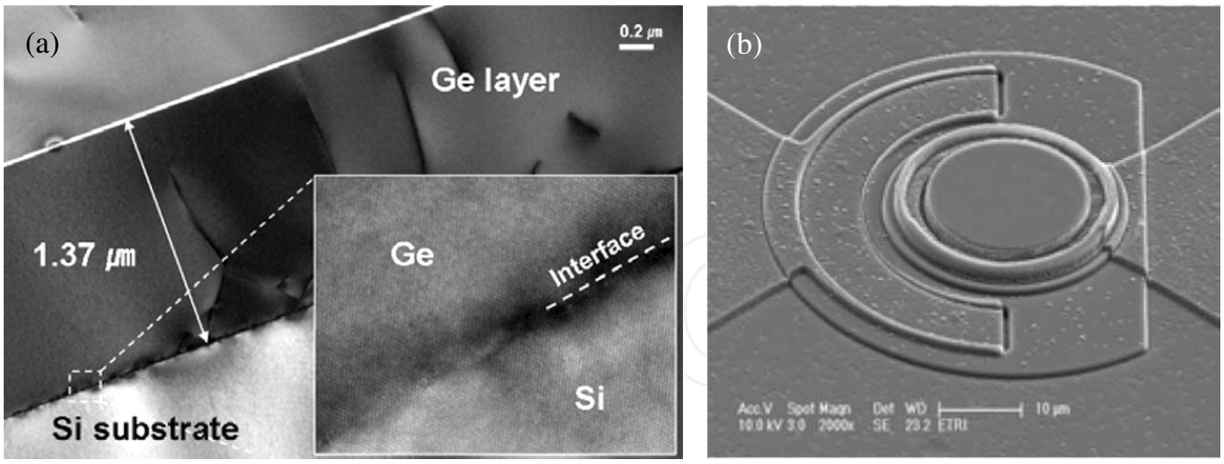

Figure 19. (a) Cross-sectional transmission electron microscope (TEM) image of Ge grown on Si substrate, where the inset shows Ge atoms coherently matched up to the Si substrate on a lattice scale; and (b) top view SEM image of fabricated Ge *pin* photodetector device [51].

The epitaxial growth in this two-step process is usually performed using a variant of the chemical vapor deposition (CVD) method. The most commonly employed variant is ultrahigh vacuum CVD (UHV-CVD) [53,75], in which the operating pressures are high enough to control oxygen background contamination levels. However, SiGe based devi-

ces have also been grown using low-pressure CVD (LP-CVD) [74] more broadly utilized by industry [7], low-energy plasma-enhanced CVD (LEPE-CVD) [48], reduced pressure CVD (RP-CVD) [46], and rapid thermal CVD (RT-CVD) [40]. These CVD based methods enable high control of layer and multi-layer thickness and suitability for future large wafer-scale fabrication. The two-step process is likewise compatible with the molecular beam epitaxy (MBE) method, which has been employed in fewer but still a considerable number of instances [37,45,70,76]. Primary advantages of MBE are allowance of lower thermal budgets [66] and tight control over doping profiles [1].

6.3. LT growth

In the first LT (slower growth rate) step of this low/high temperature growth process, fully planar homoepitaxial deposition of a thin Ge/SiGe seed or buffer layer on a Si wafer is performed to ensure smooth surface morphology and to avoid islanding of the film [10]. Si wafers with (100) orientation are associated with lower leakage currents than (001) oriented wafers [1]. The Ge seed layer is deposited on the surface of the substrate, which is often highly doped to facilitate the future requirement of low resistance ohmic contacts. This seed layer is designed to prevent strain release from undesirable 3D island growth, reduce surface roughness, and enhance the migration of threading dislocations (Figure 20) to decrease their proliferation. Buffer/seed layer thicknesses in the range of 30-75 nm are most optimal to withstand the temperature ramp and homoepitaxially grow Ge films with smooth surface morphologies [77] with reduced threading dislocation densities [68]; for layers less than 30 nm thick, islanded surfaces have a tendency to form [74]. The first ~0.7 nm (i.e., below the critical thickness) of the buffer layer will be strained due to the 4.18% lattice mismatch between it and the underlying Si substrate, after which a progressive strain relaxation takes place, and a fully strain-relaxed Ge epilayer is produced for growth beyond a few additional nanometers [66]. Therefore, this layer, assuming it is of sufficient thickness, is initially predominately relaxed.

The seed layer growth temperature influences adatom processes on the surface, crystalline growth, surface morphology, abruptness of doping transitions, and relaxation processes [68]. Temperatures employed for seed layer deposition are predominately in the 300-400°C range, and usually from 320-360°C [9]. Depositing seed layers at temperatures below 300°C can lead to crystallographic defect formation, while temperatures above 400°C have been found to produce surface roughening due to increased surface mobility of Ge [7]. At such relatively low growth temperatures, the low surface diffusivity of Ge kinetically suppresses undesired islanding that can otherwise result [10].

In situ doping (e.g., with boron) of this layer can be utilized to enhance the seed growth rate and lower the Ge/Si interfacial oxygen level [7]. Seed layer doping has been found to scale linearly with boron doping levels up to 10^{20} cm^{-3} [74]. It has also been determined to reduce series resistance under forward bias and lower dark current under reverse bias [63].

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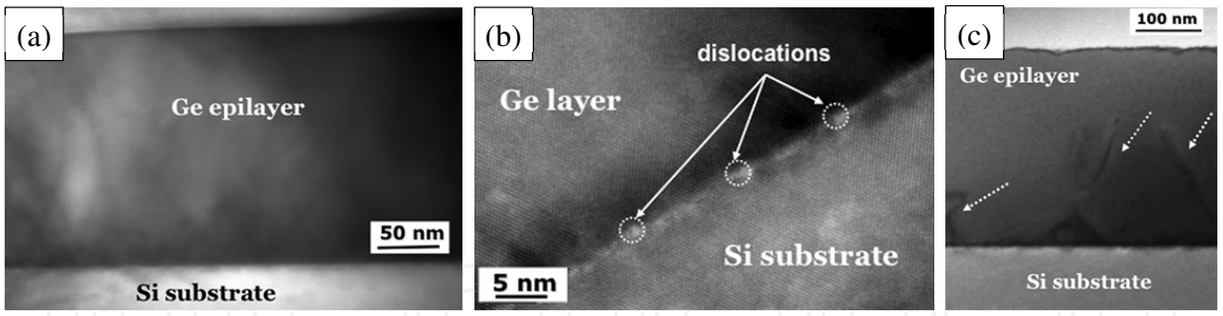

Figure 20. (a) Cross-sectional TEM image of Ge layer grown on Si; (b) enlargement of layer in (a) near the interface region, showing a high density of misfit dislocations; and (c) TEM image of the Ge layer grown following a two-step growth process, where threading dislocations are less evident [66].

6.4. HT growth

In the subsequent HT step of the growth process, a layer of intrinsic Ge or SiGe serving as the *pin* detector absorption region is grown in the temperature range of 500-800°C above the relaxed buffer/seed layer. The growth temperatures utilized are most commonly in the 600-700°C range, which has been found to produce a satisfactory growth rate and sufficient degree of tensile strain while also providing a smooth high crystal quality Ge/SiGe film [10]. Using a layer composed of Ge (rather than SiGe) maximizes the potential cutoff wavelength of device, but high Ge content $Si_{1-x}Ge_x$ ($x \geq 0.8$) can likewise be effective. In general, as this *i*-Ge/SiGe layer is made thicker, the transit time increases which reduces the device bandwidth, while the responsivity rises due to higher absorption and junction capacitance is reduced [15]. However, topological and defect density concerns limit the *i*-layer thickness for practical *pin* devices to 2 μm or less [64]. The doping level of this intrinsic SiGe layer is typically three to four orders of magnitude lower than that of the highly doped $n^+$and p^+layers of a *pin* detector [76]. Upon cooling following the HT growth, this layer becomes strained due to the difference in the thermal expansion coefficients between the Ge/SiGe layer material and the Si substrate. In one instance the level of strain present after cooling was found to rise as the layer thickness increased up to ~150 nm, and then remain essentially constant as its thickness grew further [66].

6.5. HT anneal

Following the LT/HT growth steps, HT *in situ* annealing, often cyclic in nature, is usually performed. The cyclic annealing process enables a reduction in sessile threading dislocation density by transforming sessile threading dislocations to glissile ones, which due to thermal stress glide effectively annihilate dislocations [78]. This annealing process is intended to reduce the threading dislocation density by up to two orders of magnitude (e.g., from 10^9 to 10^7 cm^{-2} [9]) and thereby diminish resultant dark/leakage currents, and also to enhance the strain/stress of the *i*-Ge layer [48]. To have an optimal effect, the high anneal temperature is usually chosen to be marginally less than the Ge melting temperature (939°C), with the low temperature at least 50°C below high anneal temperature and above ambient [78]. Typical cyclic anneal temperatures span the 700-900°C range.

Cyclic annealing for up to 10 cycles compared to a single cycle was found in multiple cases to further reduce the dislocation density by a significant degree [70]. On the other hand, a single anneal cycle can result in lower boron diffusion out from the p^+SiGe layer while still maintaining acceptably low dislocation density [47]. High and low cyclic annealing durations are most commonly 10 min; however, a single anneal lasting up to 2 h has been found to be equally effective in certain cases [68]. As the anneal time increases, Ge/Si interdiffusion can become an issue and limit tensile strain [66]. An alternate approach involves a hydrogen ambient, by which annealing at ~800ºC for 30 min can effectively reduce surface roughness and threading dislocation density attributed to enhanced atomic mobility from the annealing [79].

6.6. Subsequent fabrication steps

Following selective two-step LT/HT growth and annealing, additional processing steps are required in the development of a practical Ge/SiGe *pin* photodetector device. The top contact of the detector can comprise a thin (100-200 nm) layer of polysilicon deposited on the intrinsic Ge/SiGe layer, *in situ* doped with phosphorus [53]. This forms the n^+layer that provides a conductive path to the opposite site of the detector. Free-carrier absorption, which can be significant in Si at NIR wavelengths, was modeled using the Drude equation [18] for a polysilicon layer of 200 nm thickness with dopant concentration of 10^{19} cm^{-3}, and was found to have an acceptably minor impact on performance. However, if the doping level is increased significantly the layer thickness will need to be reduced, and vice versa, in order to prevent free-carrier absorption from significantly degrading detector performance.

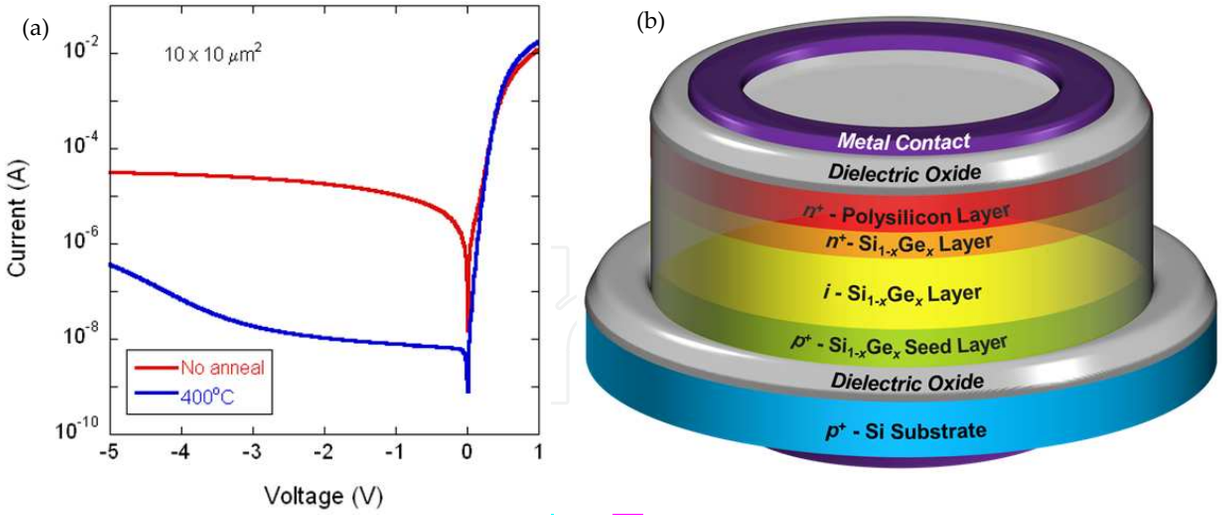

Figure 21. (a) I-V characteristics for 10×10 μm² SiGe *pin* detector devices with and without 400°C post-metallization anneal in N_2; at-1 V, the dark current is reduced by ~1000X with 400°C by the annealing [24]. (b) Schematic showing composition of a prospective SiGe *pin* photodetector device after fabrication.

Following deposition of the polysilicon layer, an activation anneal can be performed, which serves to out-diffuse dopant atoms from the polysilicon layer into the underlying Ge/SiGe to form a vertical *pin* junction [63]. A passivation layer (e.g., of SiO_2) may then be deposited at

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relatively low temperatures using a CVD based process, which serves to reduce leakage currents and isolate active elements [1]. This oxide layer can be patterned using a photolithographic process to open a window to the underlying $Si_{1-x}Ge_x$ surface. The next prospective step in this process, nearly completing the photodetector design, involves sputter depositing metal (e.g., aluminum or titanium) to form low resistance top and bottom contacts. Silicidation annealing may subsequently be performed at temperatures in the 600-900°C range to ensure highly conductive ohmic contacts enabling higher photocurrent [53]; this has also been observed to marginally increase the tensile strain in the Ge/SiGe layer [16]. Following this metallization process, the samples may be annealed in nitrogen, as shown in Figure 21(a), which has been found reduce dark current by up to three orders of magnitude for small area Ge/SiGe *pin* photodetectors [24]. A potential design layout of a fabricated SiGe *pin* photodetector device having undergone these processing steps is depicted in Figure 21(b).

7. Practical integration SiGe detectors for imaging arrays

7.1. IR FPA and ROIC technology

Because of the compatibility of Ge growth methods with standard silicon based CMOS processes, photodetectors developed through selective epitaxial growth of Ge/SiGe can be heterogeneously integrated with CMOS circuitry using manufacturing infrastructure already widely installed for the production of BiCMOS and CMOS integrated circuits. In addition, unlike charge-coupled device (CCD) based imagers that require specialized and relatively complicated processing techniques, CMOS based imagers can be built on fabrication lines designed for commercial microprocessors. This has enabled the resolution of CMOS imagers to continue to increase rapidly due to the ongoing transition to finer lithographies as predicted by Moore's Law. This in turn has led to higher circuit density and levels of integration, better image quality, lower voltages, and lower overall system costs for CMOS devices in comparison with traditional CCD based solutions [80].

The term *focal plane array* (FPA) refers to a 2D assemblage of individual detector pixels located at the focal plane of an imaging system [21]. FPAs convert optical images into electrical signals that can then be read out and processed and/or stored in digital format. Staring array FPAs, in which the associated optics serve solely to focus the visual image onto the detectors in the array, are scanned electronically usually using circuits integrated with the arrays. The electrical output from the array can be either an analog or digital signal, which in the latter case requires the inclusion of analog-to-digital conversion electronics. CMOS based silicon addressing circuits, the dominant technology for large scale arrays, are mature with respect to fabrication yield and attainment of near-theoretical sensitivity.

Readout integrated circuits (ROICs) enable a FPA to be fully functional by accumulating photocurrent from each pixel to provide parallel signal processing circuitry for readout. ROIC functions include pixel deselecting, antiblooming on each pixel, subframe imaging, and output preamplification [80]. In monolithically integrated ROICs, both detection of light and signal readout (multiplexing) is performed in the detector material in the spacing between the pixels

rather than in an external readout circuit [75]. Advantages of this approach include reduced number of processing steps, increased yields, and reduced costs. Another common architecture for IR FPAs uses a hybrid based approach, in which the individual pixels are directly connected with readout electronics providing for multiplexing [21]. Some benefits of this method are the potential for near 100% fill factor, increased signal processing area, and the ability to optimize the detector and multiplexer independently.

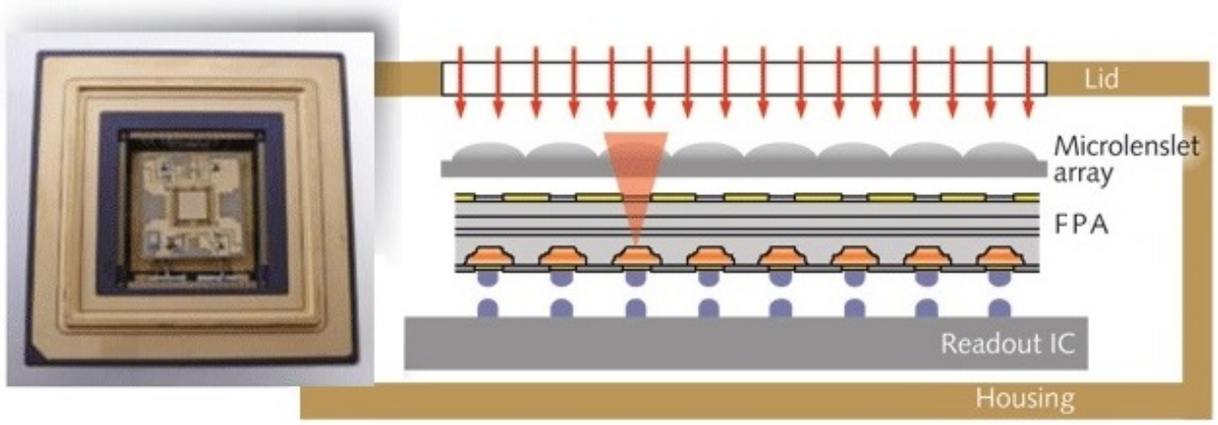

Figure 22. Photograph and schematic of a focal plane array (FPA) consisting of a hybridized chip stack with readout integrated circuit (ROIC), pixel array, and microlens array [81].

ROICs comprise input cells or unit cells, which in the case of hybrid FPAs consist of the areas located directly under each pixel that are connected to the pixels through indium bumps that bond the aligned FPA and ROIC together [82]. This procedure allows multiplexing the signals from thousands of pixels onto a few output lines. FPAs can utilize either frontside illumination, where photons pass through the ROIC, or backside illumination, where photons pass through a transparent detector array substrate; the latter is often the most advantageous since ROICs typically have areas of metallization and other opaque regions that effectively reduce optical area of the structure [21]. ROICs are processed in standard commercial foundries, and can be custom designed to feature any type of circuit that will fit in the unit cells, though this space is often quite limited. Microlenses deposited above each pixel arrays concentrate incoming light into photosensitive regions, and thus offer a means of further improving sensitivity for devices having relatively low fill factors. A typical indium bonded hybrid architecture FPA utilizing a microlens array is depicted in Figure 22.

7.2. Integration of SiGe technology in CMOS processes

The progressing technological development of low dark current SiGe detector arrays has made possible the fabrication of high density large format SiGe NIR FPAs. The frontside illumination process flow shown sequentially in Figure 23 was developed by DRS Technologies and provides various potential steps for the processes for fabrication and integration of FPA pixels with SOI wafers [63]. In this process, the SOI wafers have a thin, high quality Si layer on top, and a buried oxide layer below. The detector p^+base layer and intrinsic (i) layer are deposited

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by SiGe epitaxy (*Step 1*). Vias into SiGe are then etched by RIE, where the buried oxide layer provides the etch stop (*Step 2*). Next, an oxide layer is deposited to provide dielectric isolation for the via structure. Doped polysilicon deposition completes the top n^+layer of the *pin* photodiode structure and provides a conductive path to the opposite site of the detector (*Step 3*). A Si handle is bonded to the detector wafer (*Step 4*) to provide support during the etching and thinning. The Si wafer is then etched (*Step 5*), where the buried oxide layer again provides an etch stop (selectivity > 1000:1). Next, vias are opened though the oxide to access the top n^+detector layer and the p^+base layer (*Step 6*). This step is followed by via metal fill. The detector wafer will then be ready for direct CMOS bonding to interconnects (*Step 7*); this enabling technology is associated with low temperatures, high density, ultra-small pitch, and pixel scale reductions. Following bonding, the handle wafer is removed (*Step 8*). Finally, a pixel isolation etch completes the detector array (*Step 9*).

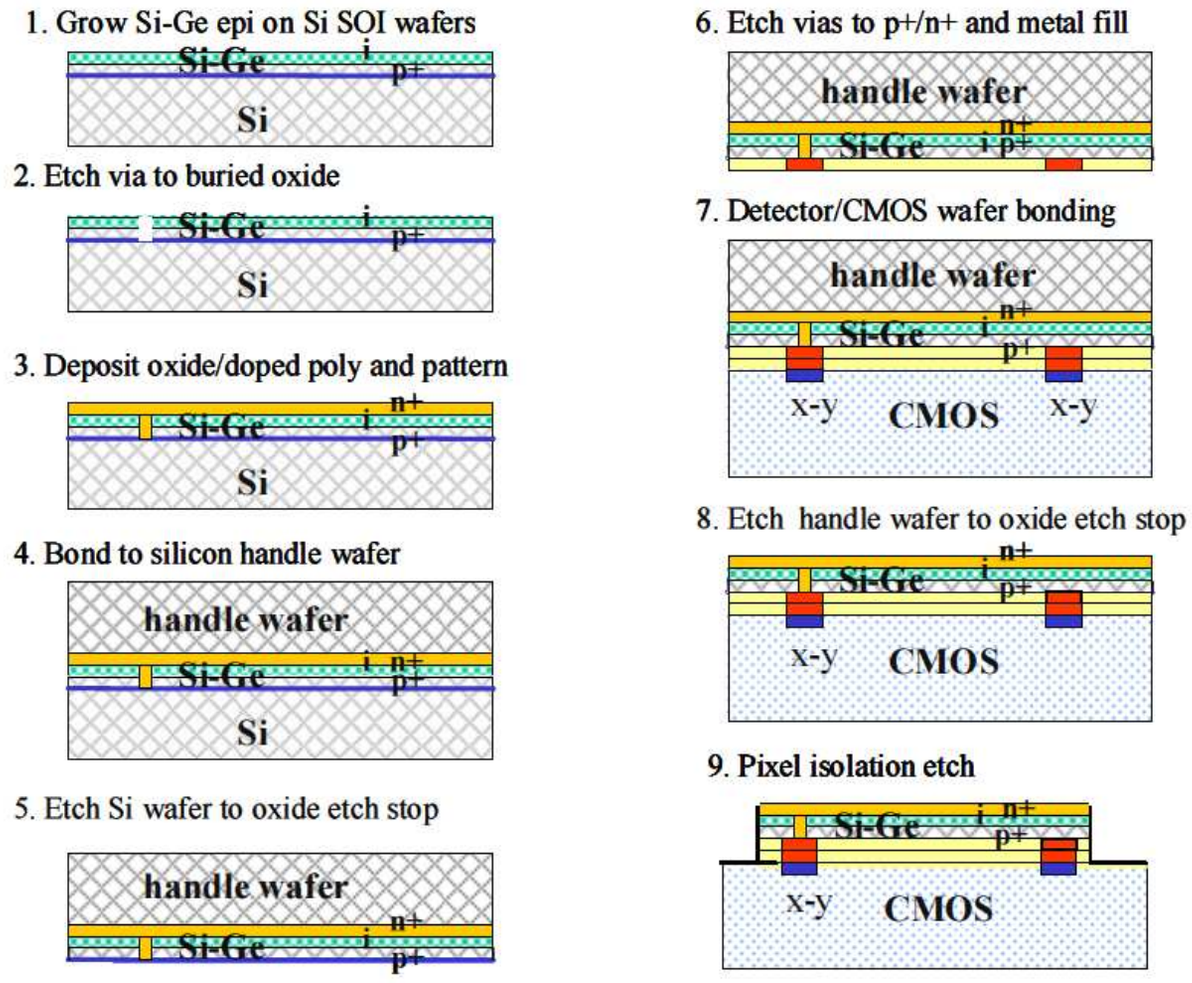

Figure 23. Process flow for fabrication of NIR front side illuminated SiGe FPA and CMOS ROIC for SiGe detection and imaging applications [63].

The first monolithic integration of Ge NIR photodetectors in a CMOS process that produced multichannel, high-speed optical receivers was reported by Masini *et al*. in 2007 [83]. With this approach, the Ge epitaxy step was integrated at the end of the frontend processing and before the contact module. RP-CVD deposition of Ge at a temperature of 350ºC without HT annealing was performed to avoid potential damage resulting from high temperature epitaxy. Since high temperatures are necessary for gate oxide growth, the Ge module was inserted after the gate processing. The integrated WC *pin* detectors, which are depicted with the Si CMOS circuit in Figure 24, operated at 1550 nm at a bandwidth of 10 Gb/s with sensitivity greater than-14 dBm.

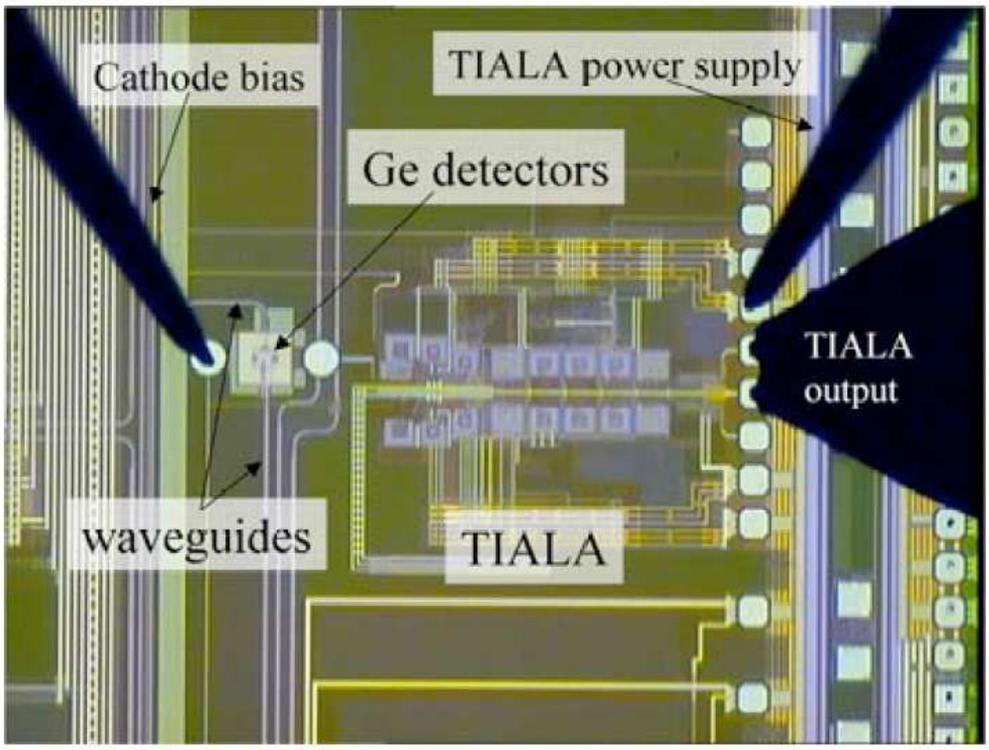

Figure 24. Integration approach for monolithic fabrication of a Ge pin photodetector and Si CMOS circuit on a common SOI platform [83].

In 2010, Ang *et al*. [19] developed and monolithically integrated highly efficient WC *pin* Ge-on-SOI photodetectors with a CMOS circuits. They utilized an "electronic-first, photonic-last" approach to avoid Ge degradation and cross contamination to fabricate both vertical and lateral devices, where the former were found to offer superior performance in relation to bandwidth and dark current density. A closely matched integrated CMOS inverter circuit was demonstrated capable of performing logic functions. A high temperature (800°C) prebake treatment was used before the Ge epitaxy growth, which was found to not have any observable detrimental impact on the operation of the CMOS devices. The vertical *pin* detectors achieved a responsivity of 0.92 A/W at 1550 nm, QE of 73%, bandwidth of 11.3 GHz, and dark current of 0.57 μA. Figure 25(a) and (b) show the design of the evanescent coupled Ge photodetectors in vertical and lateral *pin* configurations, respectively, while Figure 25(c) shows the integration approach for monolithically fabricating the Ge *pin* photodetector and Si CMOS circuit.

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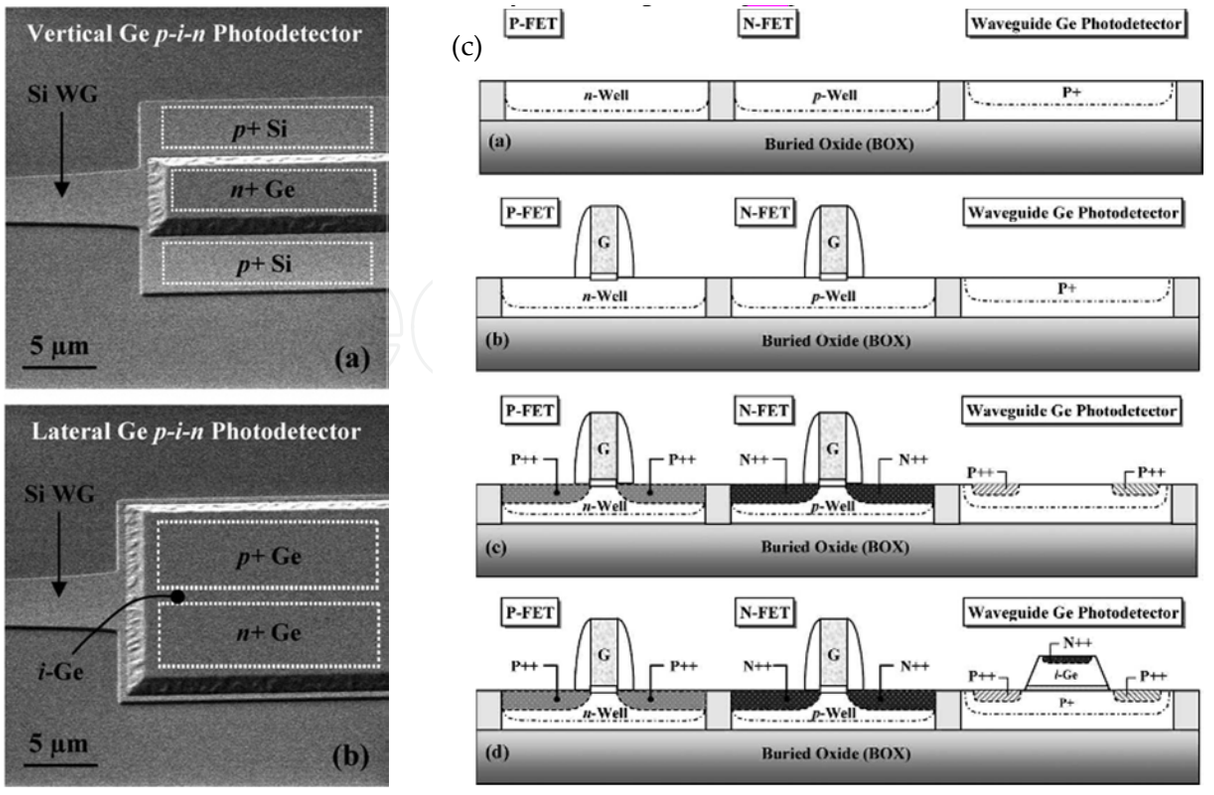

Figure 25. (a) SEM micrograph showing design of evanescent coupled Ge photodetector featuring vertical *pin* configuration; (b) Ge photodetector design with lateral *pin* configuration; and (c) schematic showing "electronic-first and photonic-last" integration approach for monolithically fabricating the WC Ge *pin* photodetector and Si CMOS circuit on a common SOI platform [19].

7.3. Development of SiGe detector arrays for imaging

IR FPAs have traditionally been based on conventional materials utilized for IR detection including HgCdTe, InSb, InGaAs, and VOx [64]. SiGe FPAs for NIR detection are relatively new to the scene. SiGe based FPAs with associated ROICs can leverage low-voltage, deeply scaled, nanometer class IC processes that enable high yield of low-power, high-component density designs with large dynamic, on-chip digital image processing (for SWaP-efficient sensor designs) and high-speed readouts. A common objective is to produce large format NIR FPAs that are very compact.

Colace *et al*. in 2007 [6] demonstrated an optoelectronic chip incorporating a fully functional 2D array of 512 polycrystalline heterojunction Ge pixels integrated on CMOS electronics and operating in the NIR. The ROIC was serial and made use of an 8-bit data bus and 9-bit address bus. In order to compensate for a significant level of dark current, the chip was equipped with offset control and a dark current cancellation circuit. It also featured addressing and signal processing electronics including 64 analog-to-digital converters. This integrated circuit, which operated up to and above 1550 nm, was found to exhibit good photoresponse and could acquire simple images. The chip, its architecture, and its cross-section are illustrated in Figure 26.

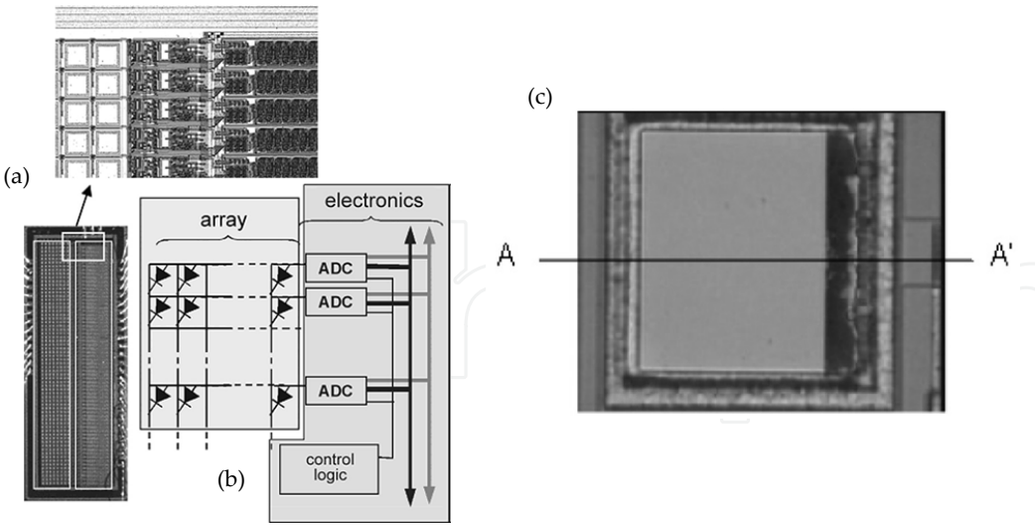

Figure 26. (a) Photograph of optoelectronic chip featuring 2D Ge photodetector array, showing zoomed-in image of a portion of the array; (b) chip architecture, comprising readout electronics; and (c) photograph of individual pixel [6].

In 2010 Vu *et al*. [75] developed arrays of both vertical and lateral *pin* photodetectors that were integrated into electronic-photonic FPAs. Layers of metal were employed to connect the detector electrodes to transimpedance amplifiers and CMOS circuits, and light signals were then coupled from waveguides or inserted directly into the side of the Ge intrinsic layer via optical fibers. A responsivity of 1.11 A/W at 1550 nm, bandwidth of 15 GHz, and dark current density on the order of 100 nA/cm^2 were achieved for the NI photodetectors. The integrated chips were produced in a standard CMOS foundry, where the fabrication processes was optimized for manufacturability.

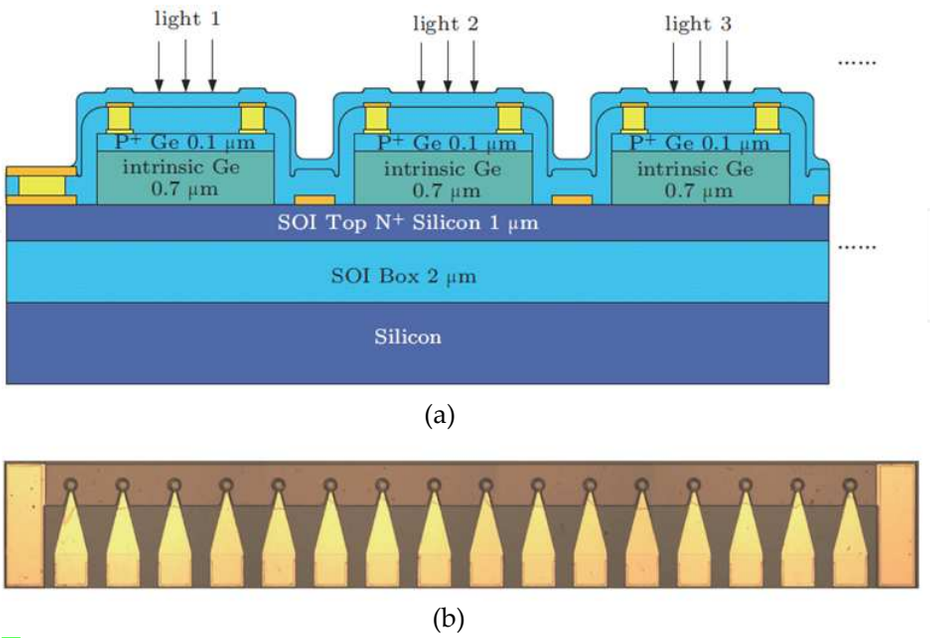

Figure 27. (a) Schematic cross-section, and (b) top view, of a linear photodetector array consisting of 16 detectors [84].

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In 2014, Chong *et al.* [84] reported a parallel system of 16 element *pin* photodetector arrays, shown in Figure 27, for parallel optical interconnect applications. The detectors comprised Ge absorption layers epitaxially grown on a SOI substrate by UHV-CVD using the two-step LT/HT growth process, and incorporated a plasma etched double mesa vertical structure to reduce parasitic capacitance. The array featured responsivities of 0.38 and 0.23 A/W at 1310 and 1550 nm, respectively, with a very low dark current density of ~5 mA/cm^2 with no applied bias and a bandwidth of up to 8 GHz.

8. Optoelectronic properties of Si/Ge based nanostructures

8.1. Quantum confinement and strain in Si/Ge nanostructures

A growing number of optoelectronic devices including photodetectors are being developed that employ low-dimensional nanostructures (NSs), particularly quantum wires (Q-wires) and quantum dots (QDs), to enhance their performance. NSs offer unique optical and electronic properties resulting from the quantum confinement of electrons and holes. Such quantum confinement in NSs, which is directly affected by their dimensions, has a substantial impact on band gap energy. The quantum confinement effect (QCE) causes the band gap of crystalline Si and Ge Q-wires and QDs to increase as their diameters are reduced according to the relation $E_g \sim 1/R^a$, where E_g is the band gap and a falls between 1 and 2 [85]. Figure 28(a) and (b) show a comparison of band gap energy reported by various groups as a function of QD diameter in crystalline Si and Ge QD structures, respectively, where it can be seen that the band gap energies of the Si QDs follow a much more uniform and predictable pattern than those of their Ge counterparts. As a result of larger exciton energy, the QCE effect is stronger in Ge than in Si, and the electronic properties Ge QDs can thus be more easily modulated by the QCE than can those of Si QDs [85,88]. In addition, making the length scale in NSs small enough produces uncertainty in the momentum **k** vectors that consequently allows the **k** selection rules to be broken, causing the band gap to change from indirect toward direct that allows electron-hole recombination to take place without the need of phonons [86].

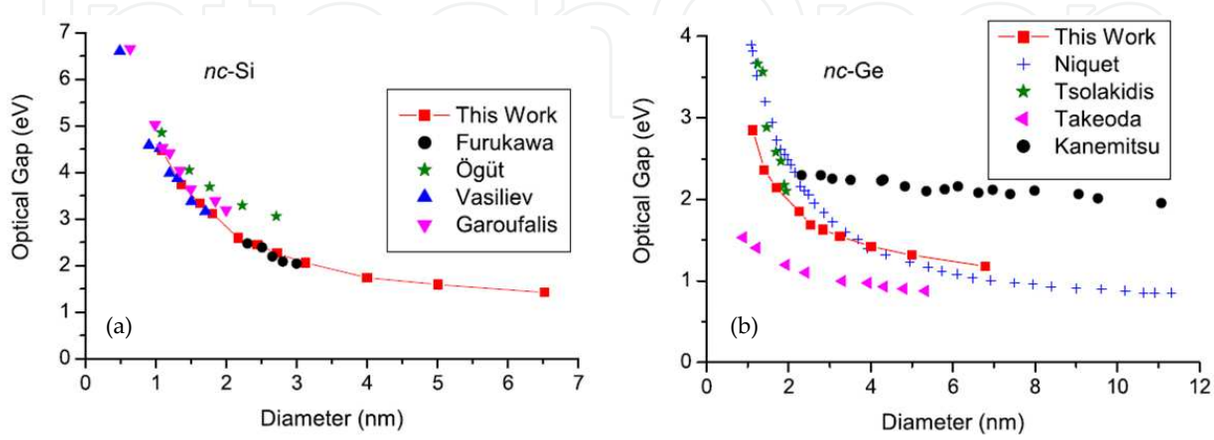

Figure 28. Comparison of band gap energy as a function of QD diameter for (a) Si and (b) Ge [87].

As was shown to be the case with bulk SiGe alloys, strain alters the intrinsic interatomic distances and thus affects the band gap energy, and also impacts the effective masses and mobility [85]. However, their reduced dimensionality and small size allow NSs to tolerate relatively large stress and strain without introducing significant dislocations or other defects that could undermine their electrical properties. Due to the nature of their geometry, NWs—especially the core-shell variety—experience tensile stress due to bending in addition to that caused by lattice mismatch [86]. By applying an external tensile strain of around 2.8% to Si-core/Ge-shell NWs, a transformation from direct band gap to indirect one can likewise be achieved [89].

8.2. Photodetectors based on SiGe nanowires and quantum dots

In addition to the enhancement of performance properties due to the QCE and strain, detectors based on one-dimensional Q-wires [i.e., nanowires (NWs)] offer potentially greater sensitivity primarily due to larger surface-to-volume ratios [90]. There is still progress to be made in this area, however, as Ge NW based photodetectors currently have significantly longer photocurrent rise and decay kinetics and associated time constants than those based on bulk Ge/SiGe. As illustrated in Figure 29(a), the optical absorption of $Si_{1-x}Ge_x$ NWs is largely affected by the material concentration, with the band gap (and thus SiGe NW based photodetector response) shifting to lower energies and longer wavelengths as x increases. As might be expected based on the previous discussion on QDs, a shift to lower energies was observed with increasing NW diameter for both Si and Ge NWs, again evidencing the potential for tuning the optical properties of NS based photodetector devices by varying the constituent NS sizes.

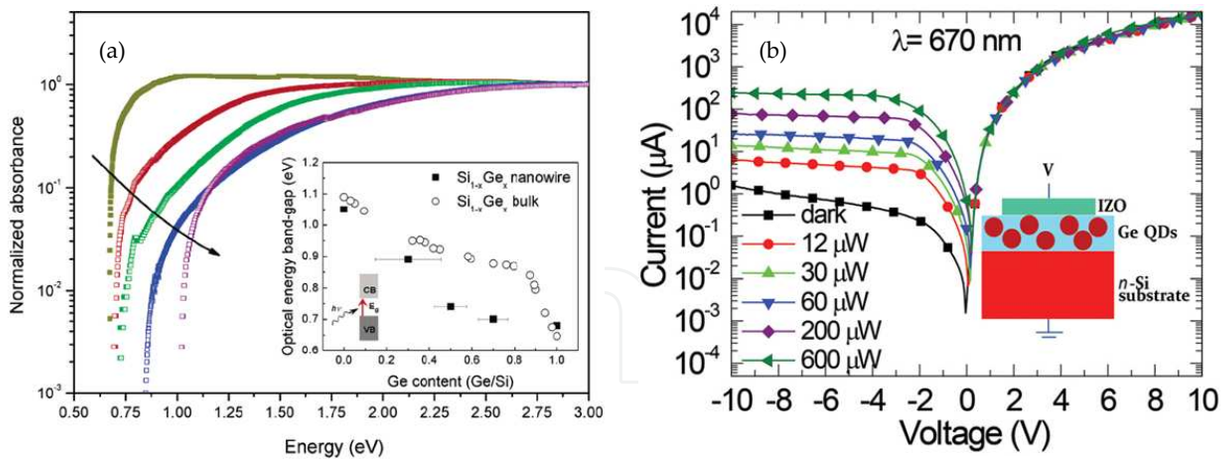

Figure 29. (a) Optical absorption spectra vs. band gap energy of $Si_{1-x}Ge_x$ NWs of five representative compositions (following the arrow, the spectrum corresponds to Ge, $Si_{0.3}Ge_{0.7}$, $Si_{0.5}Ge_{0.5}$, $Si_{0.7}Ge_{0.3}$, and Si NWs, respectively); the inset summarizes variation of optical band edges with the known values from bulk $Si_{1-x}Ge_x$ crystals [91]. (b) I-V characteristics for amorphous Ge QD photodetector at different illumination powers; the inset shows a schematic of the device [92].

In the past few years, a number of detector devices comprising QDs, which exhibit quantum confinement in all three dimensions, have been developed. QD detectors offer the advantages of increased sensitivity to normally incident radiation as a result of breaking of the polarization

selection rules, large photoelectric gain associated with a reduced capture probability of photoexcited carriers due to suppression of electron-phonon scattering, and small thermal generation rate resulting from the zero-dimensional character of the electronic spectrum that renders improved SNR [93]. Compared to Si QDs, Ge QDs have higher absorption coefficients due to localized defect states [92]. SiGe QD detectors have been reported that operate up to the LWIR regime; however, the responsivity of these devices is typically much greater at NIR wavelengths, i.e., below 2000 nm [93]. The response at NIR wavelengths of photodetectors comprising Ge QDs grown on SiGe has been attributed to interband transitions between electrons in Ge/SiGe layers and holes in the Ge QDs. Figure 29(b) shows the I-V characteristics of a Ge QD photodetector exposed to different intensities of visible illumination. Ge QD based photodetectors have recently demonstrated peak responsivities as high as 4 A/W at-10 V bias and response times down to ~40 ns [92].

9. Summary

This chapter has covered the operation, design, fabrication, and applications of SiGe based photodetector technology. A model to predict SiGe sensor performance over a wide range of light levels has been presented, which indicates that a low-cost, small pixel, uncooled SiGe based detector will respond well to small amounts of illumination from a direct NIR source. The operation and relative performance characteristics of Ge based avalanche photodiodes (APDs), metal-semiconductor-metal (MSM) detectors, and *pin* detectors have been discussed. SiGe *pin* photodetectors offer performance advantages including high responsivities, high bandwidths, low bias voltage requirements, and low dark current compared to other types of SiGe detectors. The impact of detector dark current and techniques for reducing it in *pin* photodetector devices have been examined. The nature and impact of strain and stress on extending SiGe based detector response to longer NIR wavelengths were also discussed.

Installed infrastructure and heterogeneous integration can be leveraged to fabricate small feature CMOS-compatible SiGe based *pin* detector array devices exhibiting optimal properties for NIR detection. A common fabrication process for SiGe based *pin* photodetectors incorporating two-step low/high temperature epitaxial growth of Ge/SiGe layers on Si substrates followed by a high temperature anneal and additional processing steps has been outlined, which was found to reduce threading dislocation density and thereby improve device quality. In addition, fabricated SiGe detectors can be directly integrated with low noise Si readout integrated circuits to yield low SWaP, low cost, and highly uniform IR focal plane arrays (FPAs) that can function as imaging devices. Various integrated SiGe based FPA imagers have been demonstrated that exhibit enhanced functionality and performance characteristics. Finally, the impact of the quantum confinement effect and strain on band gap in low dimensional nanostructures was analyzed, and the characteristics of photodetectors based on quantum dots and nanowires were discussed.

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