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Nanotechnology for Packaging

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1. Introduction

The use of implantable microelectronic devices for treatment of medical conditions, e.g. movement disorders, deafness and urinary incontinence has increased steadily over the years [1]. These devices use microelectronic components to sense biological activities in the implanted patient. The microelectronic components must be protected from the surrounding tissue using insulating (hermetic) packaging material. This packaging prevents the aqueous saline environment of the body from corroding, short-circuiting and contaminating the internal electronics. Microelectronic packages must incorporate some electrically conducting elements that bridge through the protective packaging to allow the internal microelectronics to sense (or stimulate) the surrounding external environment. These conductive elements are called interconnects or feed-throughs.

First generation implantable electronic devices, such as the first cardiac pacemakers, had few, relatively large interconnects. To this day, many of these interconnects are constructed using labor intensive, manual assembly techniques. Electrode contacts are tack-welded to conductive leads, and then the entire assembly is laid inside a mold and encased in silicone insulation. The insulated wires are then released from the mold, flashing is removed and the final assembly is quality tested.

Next generation devices could have as many as 1000 interconnects condensed in a similar cross-sectional surface area of the device packages. At this scale, hand laid and molded wires in silicone will not suffice. Simple but accurately repeatable processes must be developed to create functional feed-throughs. Existing feed-through designs and fabrication processes will not be appropriate and will warrant new strategies to prevent the penetration of mobile ions such as K^+ , Na^+ and Cl^- from surrounding body fluid [2, 3].

The hermeticity of a package is its ability to prevent ion migration across (or through) its structure. Research and development in this area has accelerated significantly [4]. Simply put the hermeticity of different materials classes can be ordered as follows: polymers (least hermetic) < glass < polycrystalline metals/oxides (most hermetic). Interfaces between two different materials can serve as an avenue for contaminant ions to migrate as can grain boundaries between crystals of the same, polycrystalline material. Helium leak testing is currently the gold standard for evaluating hermeticity.

A number of research groups are trying to overcome existing issues with fabrication of hermetic packages for implantable microelectronics [5-8]. Since these implanted devices must remain hermetic for the lifetime of the patients, many important factors should be considered in their design, including the location of implantation, dimensional constraints, materials constraints (e.g. biocompatibility, conductivity, etc.), and selection of an appropriate fabrication process technology

Our group has investigated using electrochemical plating to fill cylindrical channels in channeled substrates. Our theoretical approach is to take a two-dimensional substrate with penetrating channels orthogonal to the planar surfaces, and fill these channels with electrochemically deposited metal. The resulting "assembly" of conducting elements embedded in the insulating substrate, can then be bump-bonded to a microchip, and the chip can then be encased in a gas-filled, brazed hard casket or embedded in a conformal coating.

This approach has been successful using larger channeled ($\approx 200 \mu\text{m}$) substrates, like the U.S. Naval Research Labs channel glass, with electroplated copper and chromium interconnects [9]. However, electrochemically depositing non-porous, continuous interconnects made from implantable electrical stimulator metals (e.g. platinum, iridium or their alloys) cannot be achieved due to solubility and deposition rate challenges. As a result, our group proposed and developed a strategy of electroplating several adjacent high-aspect ratio nano-channels, in nano-channeled substrates, with precious metal solutions. Once deposited, adjacent embedded nanowires can be electrically connected in parallel to create larger conducting elements.

Figure 1 depicts two schematics illustrating how this type of assembly would work. Here, metallic nanowires are deposited into a nano-channeled substrate, forming hermetic feed-throughs. Instead of using a single conducting element bump-bonded to each single contact on the chip, an array of co-deposited nanowires forms a single conductor unit through the substrate.

Fabricating these assemblies is achieved using a commonly used approach by nanowire researchers, called the "template synthesis" approach [10]. In this method, metallic ions in solution (plating solution) are electrochemically reduced at a working electrode surface that has been applied to the base of the channels of a nano-channeled substrate.

Using this template synthesis approach to deposit nanoscale elements provides distinct performance advantages. By confining the metal deposition to nanometer dimensions inside the channel, mass transport gradients that cause dendritic deposition and growth no longer occur. Further, by completely filling the channels, we are able to develop a dense interconnect from platinum and iridium that spans the substrate material.

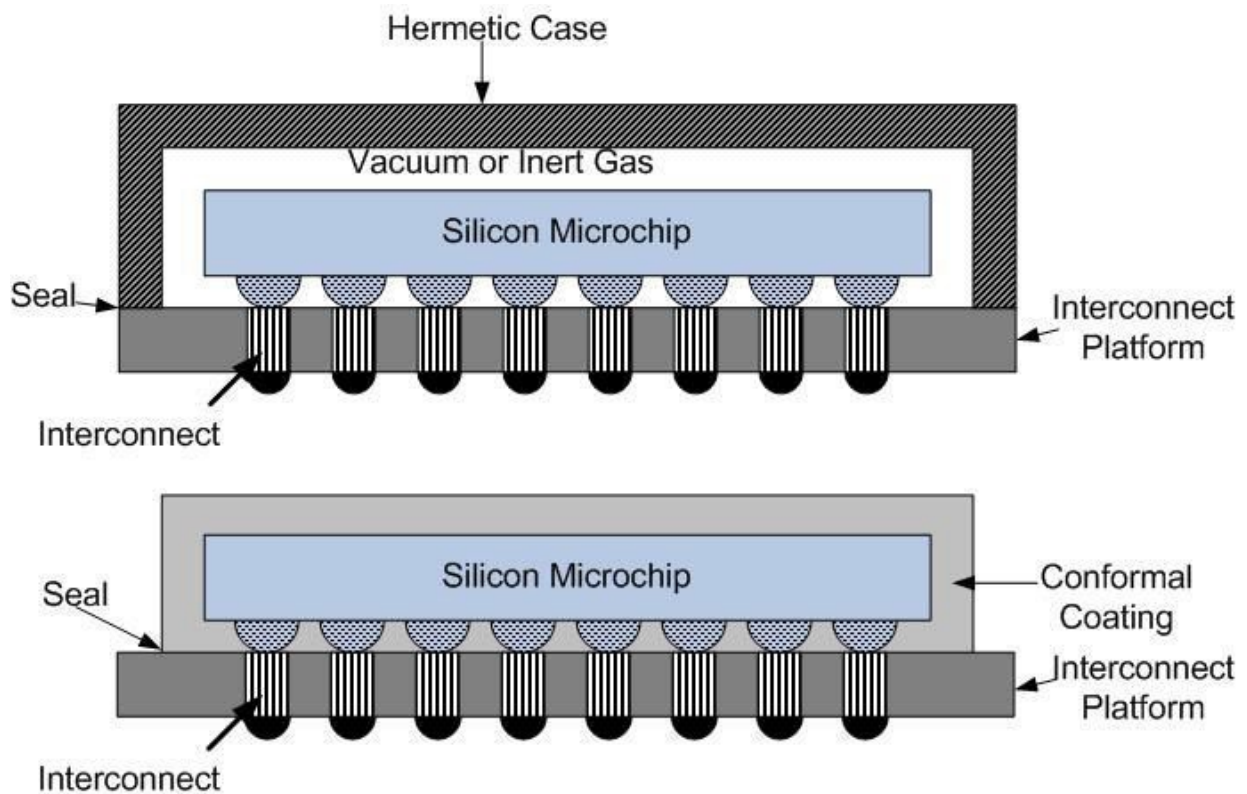


Figure 1. The top diagram shows an interconnect substrate with a case bonded over the top of the chip. Bumps on both the chip and the interconnect substrate facilitate electrical connections. This interconnect substrate could also be used with conformal coating technology (bottom). Drawing not to scale.

This approach also provides several key commercialization advantages. First, electroplating is a cost-effective processing technique. Second, unlike many nano-fabrication processes, template synthesis can be performed at ambient temperature and pressure. Lastly non-equilibrium phases can be produced by electrodeposition, a result that cannot be achieved using thermal processing techniques [11].

To date, no study has reported fabrication of ultra-high-density platinum-iridium nanowire arrays using a template synthesis approach. Only a handful of reports have been published on platinum nanowires synthesis. Approaches reported include focused ion beam [12], photoreduction in mesoporous silicides [13-17], colloidal synthesis [18, 19], self-assembly [20, 21], and nano-channel filling by electrochemistry [22-24],

This study focuses on the fabrication and evaluation of nonporous, platinum-iridium dense nanowires with improved electrical and mechanical properties to be used, embedded in their original template substrate, as a novel feed-through technology in hermetically packaged implantable microelectronics. Here we report on the fabrication process, the material properties of the isolated nanowires, and lastly an assessment of the performance characteristics of the nanowire-in-template assembly as a hermetic feed-through platform.

2. Materials and methods

2.1. Platinum–Iridium nanowire electrodeposition

Figure 2 is a schematic detailing the key steps involved in the template synthesis approach used to fabricate our platinum-iridium nanowires and nanowire-template assemblies. Prior to deposition, a conductive thin film layer must be applied to one side of the filtration membrane to 1) seal the base of the pores, thus allowing them to be filled with plating solution, and 2) to provide an electrically conducting base to serve as the working electrode at which metallic ions in solution are reduced and “grown” through the template as a metallic nanowire.

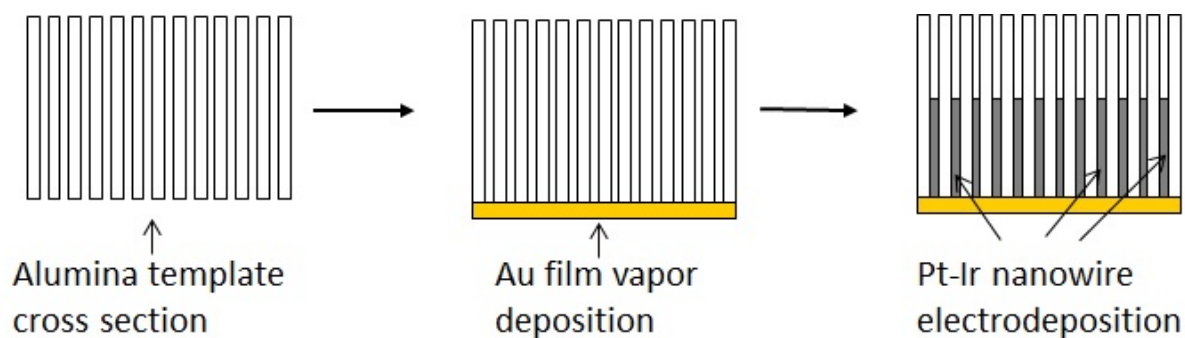


Figure 2. Schematic of the fabrication processes of metallic nanowires in AAO nanopores. Drawing not to scale.

Anodisc[®] nanoporous anodized aluminum filtration membranes (Whatman Inc., UK) were used as substrates for nanowire template synthesis. The templates have an approximate thickness of 60 μm and a diameter of 47 mm. For ease of membrane handling all templates were fitted with a plastic annular ring attached to one side of each membrane.

SEM inspection of both sides of the membranes revealed that the pore aperture sizes were different on one side versus the other. The pore apertures on the side with the plastic ring attached were approximately 20 nm in diameter. On the other side the pore apertures were approximately 200 nm in diameter, randomly distributed and with larger spaces between the pores. Cross-sectional analysis (through the membrane thickness) revealed that the large 200 nm channels continued down the majority of the template thickness, and that in the final 50 nm of thickness, the channels bifurcated into series of smaller finger-like channels with 20 nm diameters. Au thin films ($h = 80$ nm) were e-beam vapor-deposited on the side of the AAO membranes with the smaller pore apertures to create the sealed, electrical contact base for the working electrode.

Nanowires were electrodeposited using a three-electrode electrochemical cell which contained a larger, vertically-oriented cylindrical channel and a smaller diameter cylindrical chamber were machined into a Teflon[®] block along with horizontal small via to create a Luggin capillary between the two Figure 3. The larger channel's base was sealed by placing (in the following order,): an O-ring against the Teflon[®] block, followed by the AAO membrane with the uncoated side in contact with the O-ring, followed by a thick ($h = 40$ mm) copper plate. These

components were fixated in place using a spring clamp. Once assembled, the electrochemical plating solution was filled into the larger chamber and the reference electrode was inserted into the smaller chamber.

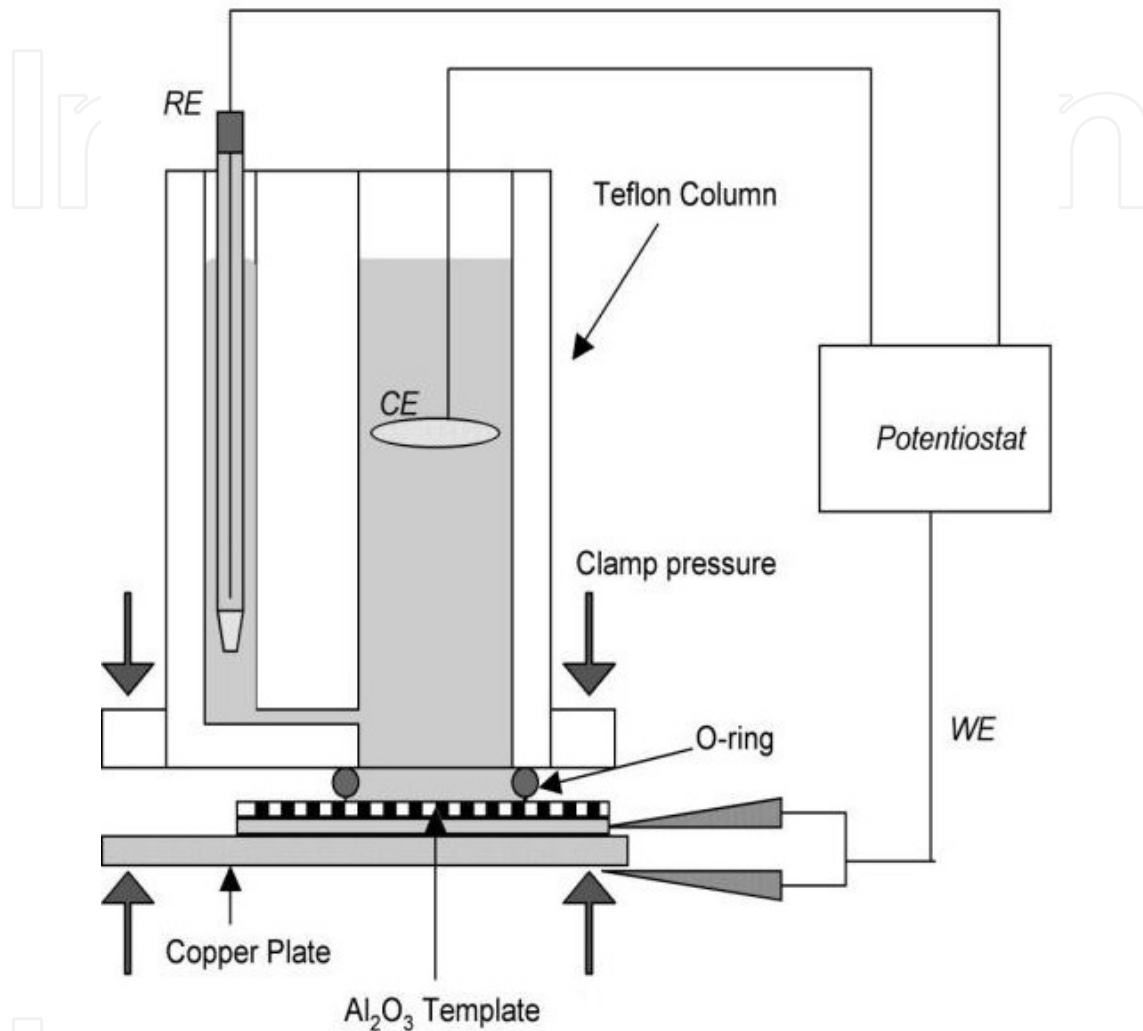


Figure 3. Electrochemical cell used for nanowire deposition in nano-channeled aluminum oxide (Al₂O₃) template.

Electrochemical deposition was performed using a software controlled, programmable potentiostat (Gamry). Electrical contact was made to the base copper plate, via alligator connector, thus making the sputtered Au thin film serve as the working electrode (WE). A silver-silver chloride (Ag/AgCl) electrode was used as the reference electrode (RE) and a spiral wound platinum wire ($\varnothing = 1$ mm) was placed in the larger chamber as a counter electrode (CE).

Nanowires were electrochemically deposited from a platinum-iridium plating solution that our group has developed and reported elsewhere [25]. In this work, two key parameters were controlled to affect deposition properties: pH and deposition potential. The pH of the initial plating solution is approximately 1.8 to 2.5, depending on the desired final properties of the

deposited alloy, and in this study, was varied from pH = 1.8 to 5.0 by carefully titrating the solution with 3M NaOH (aq) solution. With respect to deposition potential, a potentiodynamic program was used to drive deposition. Previous studies by our group have shown that changing the potential range impacts the compositional ratio of Pt:Ir [25]. Specifically the potential range was cycled over a 150mV potential range, e.g. between $U = 0.0$ V to -0.15 V vs. Ag/AgCl. The ranges used are listed in Table 1.

2.2. Nanowire isolation

Nanowires were isolated from the AAO templates, Figure 4, for further analysis of the nanowire properties. The electrodeposited AAO templates with embedded nanowires were immersed in an aqueous solution of 3M NaOH(aq) to dissolve the oxide membrane. The nanowire suspension was allowed to stand, to settle the nanowires out of the basic solution. Excess solution (supernatant) was carefully pipetted off and DI water was added to the vial to neutralize the remaining supernatant's pH. This process was repeated three times until a neutral solution was achieved. Nanowires in suspension were then pipetted onto either fresh, un-sputtered AAO filters to capture for SEM or onto TEM mesh grids for TEM analysis.

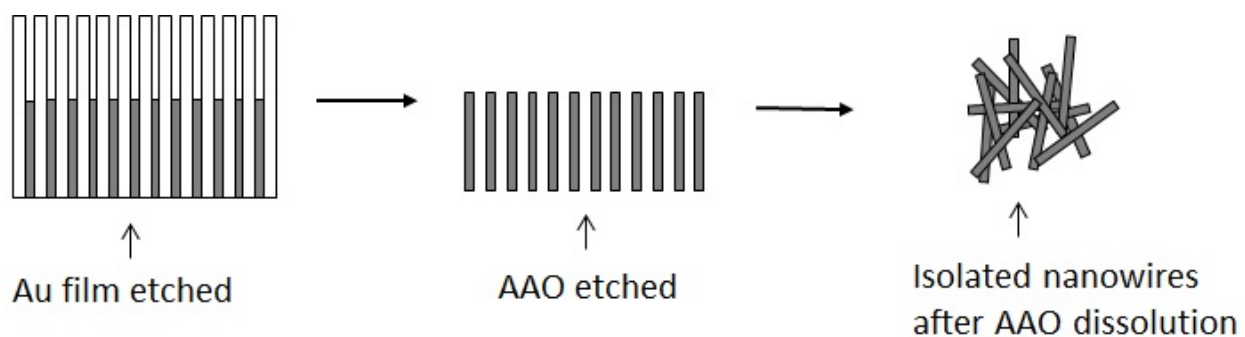


Figure 4. Schematic of the isolation process used to separate electrodeposited nanowires from AAO templates. Drawing not to scale.

2.3. Electron microscopy (SEM & TEM) characterization

All scanning electron microscopy imaging was performed using a field emission scanning electron microscope (ZEISS 1550VP) with an accelerating voltage of 4 kV.

Transmission electron microscopy was used to further characterize nanowire morphology and microstructure. Isolated nanowires were captured on carbon coated copper grids with 300-mesh size (Ted Pella Inc.) and imaged using a JEOL 2100 (Japan) TEM. Brightfield and darkfield images as well as diffraction patterns were captured. Images were taken on the edges of the nanowires, at the thinner branches (≈ 20 nm) to ensure transmission of the electron beam through the samples. Diffraction patterns were taken using beam widths smaller than the width of the nanowires, to minimize probability of outside contributions to measured patterns.

2.4. Nanowire conductivity

Electrical conductivity measures were taken on individual nanowires trapped across lithographically patterned electrical contacts [26]. In this process, a silicon wafer is masked with photoresist that has been patterned into an array of source-sink contact strip pairs. A source-sink pair consist of two, macro-scale, square contacts, each with a single lead approximately 4 mm in thickness and 10 mm in length extending towards the complimentary pad. The two parallel whiskers are separated by a 2 mm gap of patterned photoresist.

To prepare a single sample for testing, a suspension of nanowires in methanol is pipetted onto the substrate surface and the solvent is allowed to evaporate. Nanowires stick preferentially to the photoresist mask and not to the silicon wafer surface. Once dried, each source-sink pair is reviewed via SEM imaging to identify if any source-sink pair has a single nanowire trapped on the photoresist and also is bridged between the source lead whiskers and the sink lead whisker, Figure 5. Successful preparations are labeled, and the whole wafer is then sputter coated with Ti ($h = 5$ nm) adhesion and Au ($h = 50$ nm). After metalization, photoresist is lifted off, leaving behind the source-sink leads/contacts in gold, with bridging nanowires pinned between the Ti/Au layer and the silicon wafer.

Once prepared a voltage bias was applied across the contacts and current was measured through the leads. Electron transport measurements were performed using an Agilent 4156B semiconductor parameter analyzer. Current-voltage curves were generated to characterize nanowire resistivity.

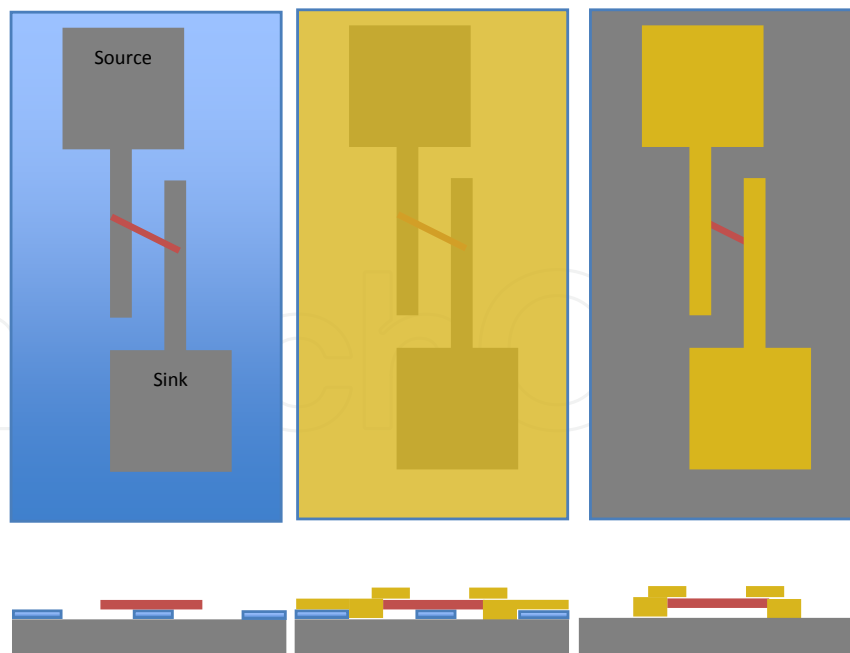


Figure 5. Schematics showing three steps used to MEMS fabricate nanowire resistivity test system. A photoresist mask (blue) is spin coated and patterned onto a silicon substrate (gray) and nanowires are dispersed from suspension until a source/sink pair trap a wire. Metallization (center) with a gold layer followed by liftoff (right) leaves patterned leads holding the nanowires in place for testing.

2.5. Helium leak testing

Helium leak tests are a standard method for assessing electronic package hermeticity. Here we use helium leak tests to provide a preliminary assessment on whether our nanowire-template assemblies have hermetic properties worthy of microelectronics packaging applications.

In practice, helium leak tests are performed by subjecting two-dimensional test samples to vacuum on one side, while helium gas is introduced on the opposite side via gas gun. The vacuum side uses a mass spectrometer to measure any helium that has penetrated through the substrate/interconnects as a result of the applied vacuum. Helium concentrations detected can be correlated to leak rates.

Helium leak tests were performed using an ASM 182-TD (Alcatel, Inc.) helium leak detector with capability of detecting helium leak rates down to 5×10^{-12} mbar L s⁻¹. Typically, values below 1×10^{-11} mbar L s⁻¹ are considered hermetic for microelectronics applications [4, 27, 28]. A custom, sample mounting fixture was designed for testing the nanowire embedded membranes. The fixture has an ultra-fine polished surface to ensure a proper seal between the test membrane and the fixture. The fixture was mounted to the inlet aperture of the leak detector using a standard vacuum seal and clamp. Samples are placed over top of a small circular inlet in the center of this fixture and held in place by the applied vacuum, a small amount of vacuum oil is applied to a polymer O-ring which is placed between the surface of the fixture and the sample to ensure a good seal.

To take measurements samples are mounted and vacuum applied until the flow rate settles below 1×10^{-11} mbar L s⁻¹. A continuous small dose of helium was sprayed from a gas spray gun on the top side of the sample exposed to ambient air. Helium gas was sprayed at the sample surface at a distance of 10cm with a pressure of 20 lbs for 10 seconds. After helium exposure, the highest observed leak rates were measured and recorded. Leak rate measurements were repeated three times for each sample. After each measurement, a time delay was given in order to return the leak rate to re-equilibrate.

3. Results and discussion

3.1. Platinum–Iridium nanowire electrodeposition

A series of nanowire-template samples were prepared using different plating solution pH: 1.8, 3.1 and 5.0. Subsequently, nanowires were isolated and examined via SEM to identify what pH produced preferred morphologies. For our application, high-aspect ratio and non-porous wires are desirable. Figure 6 shows a series of representative SEMs of isolated nanowires prepared from solutions of different pH, specifically (from top to bottom): pH = 1.8, 3.1 and 5.0.

Nanowires were first deposited at pH = 1.8, Figure 6a, isolated nanowires showed some mechanical compliance, evidenced by their visible bending in images. However, analysis of

image series confirmed that at this pH, high aspect ratio nanowires could not be achieved. It is unclear what the root cause may be. Typically, at such low pH, hydrogen co-deposition played some role in impacting deposition. It is also possible that template dissolution under such high acidity may be taking place.

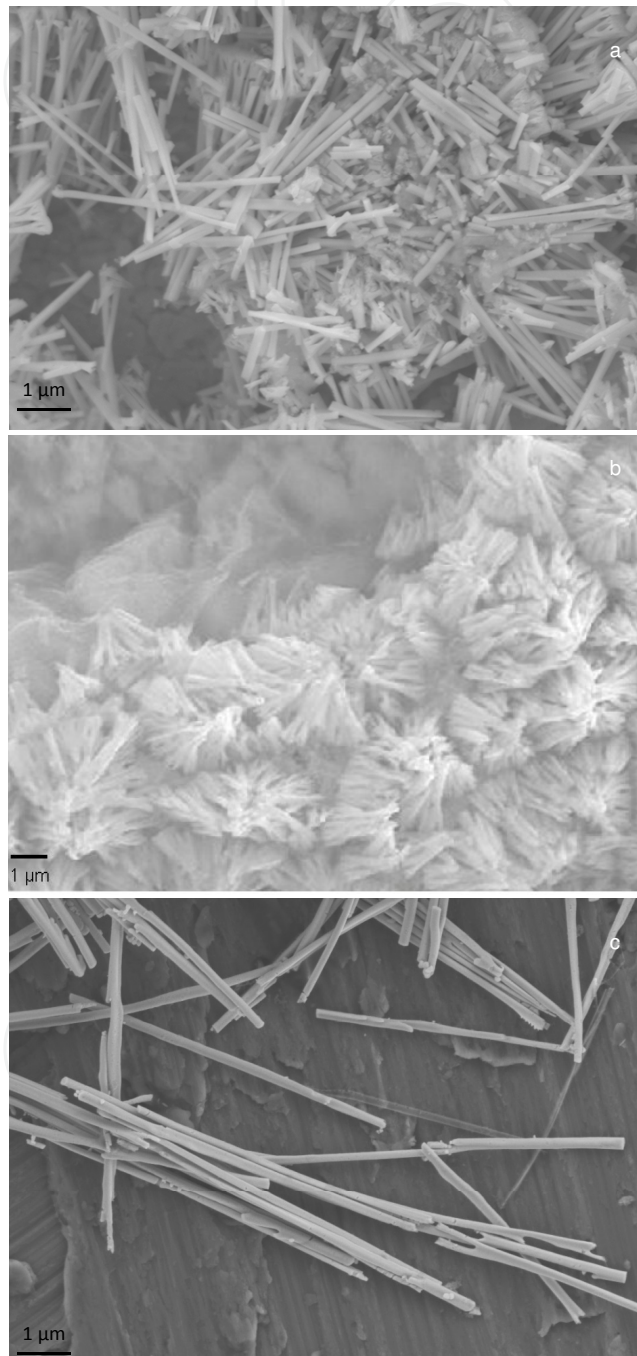


Figure 6. a) SEM micrograph of isolated nanowires with shorter lengths electrodeposited at pH=1.8, (b) SEM micrograph of isolated nanowires with brittle structures electrodeposited at pH=5 and (c) SEM micrograph of isolated dense nanowires with dense structures electrodeposited at pH= 3.1.

At pH = 5.0 Figure 6b, isolated nanowires were fragmented also with small aspect ratio. Porosity within the individual segments could not be confirmed, however, we suspect that either the nanowires themselves are brittle and fragment post-isolation, or that the deposition results in porosity which leads to fragmentation, once the structural support of the template is removed. It is unclear at this time what the mechanism for the resulting microstructure may be.

In contrast to both previous samples, high-aspect ratio nanowires were successfully synthesized using a plating solution with pH = 3.1, Figure 6c. Image analysis showed that aspect ratios from 20:1 to more than 50:1 were achievable using this approach. More work is needed to better understand what mechanisms are responsible for controlling the transport mechanisms taking place in the nano-channels. From these data, we determined pH = 3.1 would be capable of producing nanowires with preferred morphological structure.

3.2. Controlling Pt: Ir composition with potential

Co-deposition of binary alloys and multilayer nanowires has been reported elsewhere [29-31]. Here, platinum (Pt) and iridium (Ir) metal atoms are deposited through the AAO channels by electrochemically reducing from platinum ions $[\text{PtCl}_6]^{4-}$ and iridium ions $[\text{IrCl}_6]^{4-}$ in solution. By cycling the potential in a range below the equilibrium potentials for both ion complexes, the kinetics of deposition can be modulated to ensure that both elements are deposited in desirable quantities.

For this study, the potential range that produces a desirable Pt:Ir composition was unknown. We therefore selected five different potential ranges, Table 1, and prepared nanowires using each cycling range. All five potential ranges spanned 250 mV of potential but used different starting potentials (U_o) from $U_o = -0.5\text{V}$ to $U_o = 0.2\text{V}$ vs. Ag/AgCl.

| Potential range (V) vs. Ag/AgCl | Average Pt:Ir ratio (%) |
|---------------------------------|-------------------------|
| $\Delta U = 0.20$ to -0.15 | 68:32 % |
| $\Delta U = 0.02$ to -0.15 | 67:33 % |
| $\Delta U = 0.00$ to -0.15 | 62:38 % |
| $\Delta U = 0.00$ to -0.20 | 68:32 % |
| $\Delta U = -0.05$ to -0.15 | 85:15 % |

Table 1. Deposition potential ranges and resulting PtIr nanowire fractional composition

Following deposition, nanowires were isolated and composition was tested using energy dispersive spectroscopy (EDS). Results in Table 1 show compositional fractions ranging from 62:38% to 85:15% platinum were attained by varying chemistry. While the exact mechanisms responsible for the differences in concentration are not well understood at this stage, we do know that shifting the potential range used for deposition affects the deposition kinetics inside the nano-channels.

It has been reported that platinum-iridium with 60:40 composition shows preferred properties for neurostimulation applications, e.g. highest electroactivity [32]. We therefore focused on further characterization of nanowires prepared with this deposition range ($\Delta U = 0.00$ to -0.15).

3.3. TEM characterization

TEM analysis was performed on 60:40% Pt:Ir nanowires to further characterize material properties. Figures 7a and 7b are bright-field and dark-field TEM images of platinum nanowires, respectively, deposited at the optimal conditions for creating hermetic AAO-feed-through assemblies.

Figure 7a shows a gross image of a single isolated nanowire. Due to thickness and low magnification, no structural information (grain size, orientation, etc.) is distinguishable. At higher magnification and in dark field mode, however, grain boundaries and morphology can be distinguished. In Figure 7b, we estimate average grain size in the range of 5-10 nm, and they show no preferential growth orientations. There is some contrast observed between grains along the perimeter of the wire versus grains occurring within the central axis of the nanowires. This may suggest that contact with the AAO nanochannel surfaces may direct grain growth in some preferred orientations, however more studies are needed.

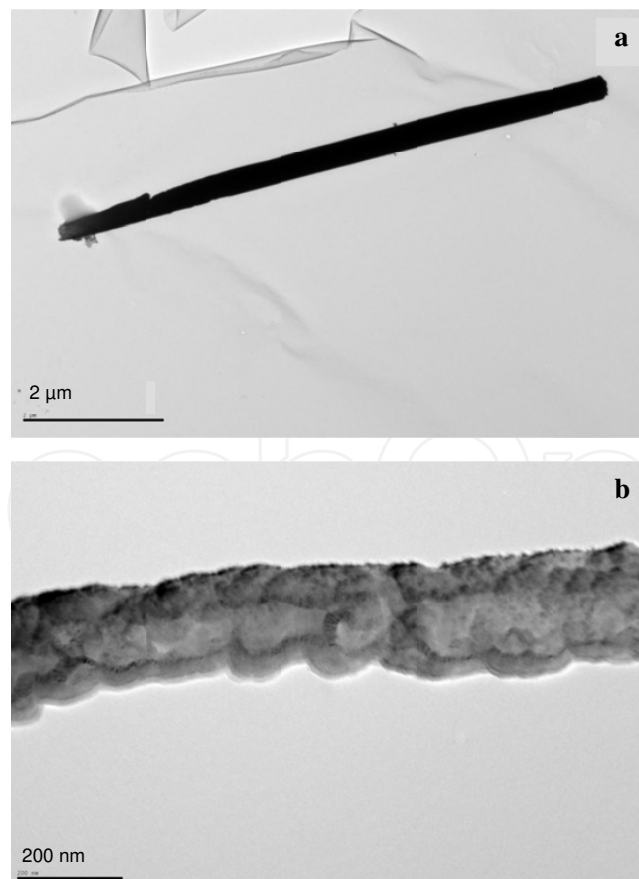


Figure 7. Bright-field (a) and dark-field (b) images of platinum nanowires.

TEM diffraction patterns of the deposited nanowires, Figure 8, showed concentric ring patterns, confirming the dark field observations that the nanowires were deposited with a polycrystalline structure, with no preferred orientation, and with an average grain size of 3-5 nm. Grain sizes calculated from x-ray diffraction patterns using Scherrer formula may underestimate grain size, as strain effects can impact patterns. The radius(r) of the diffraction rings varies with h, k, l as shown in equation (1):

$$r \propto \sqrt{h^2 + k^2 + l^2} \quad (1)$$

where h, k and l are the Miller indices that represent the crystallographic plane. The results of the calculations using equation (1) showed that the rings correspond to the planes (111), (200), (220) and (311) which represent a typical face-centered cubic (FCC) structure (Figure 10).

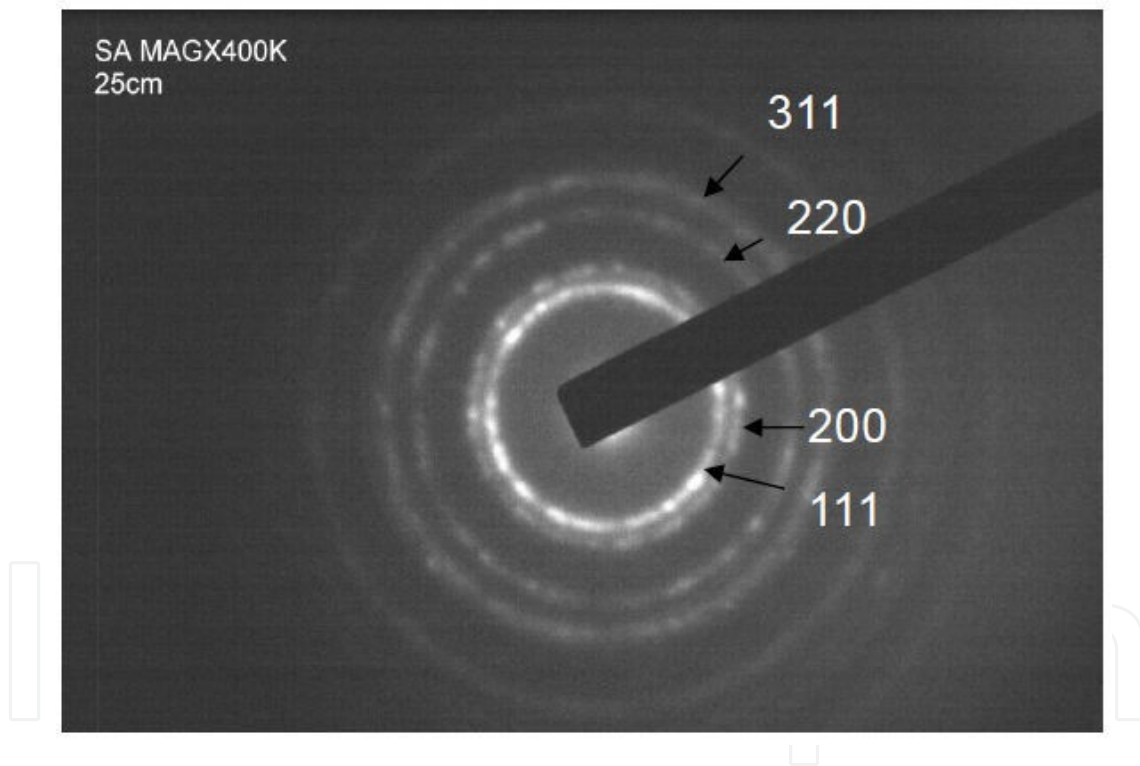


Figure 8. Electron beam diffraction pattern of platinum-iridium nanowire with fcc structure.

A HRTEM image of an individual platinum-iridium nanowire is shown in Figure 9. Since the values of the lattice parameters of platinum and iridium are too close to each other, the $(-1-1\ 1)$, $(1\ 1\ 1)$ and $(0\ 0\ 2)$ planes labeled in Figure 11 represent the FCC crystal structure that may belong to either platinum or iridium (JCPDS 04-0802) or an alloy of the two. Consequently, the twin at the grain boundary might be due to the effect of a platinum or iridium alloying grain, indicating a bimetallic particle [33].

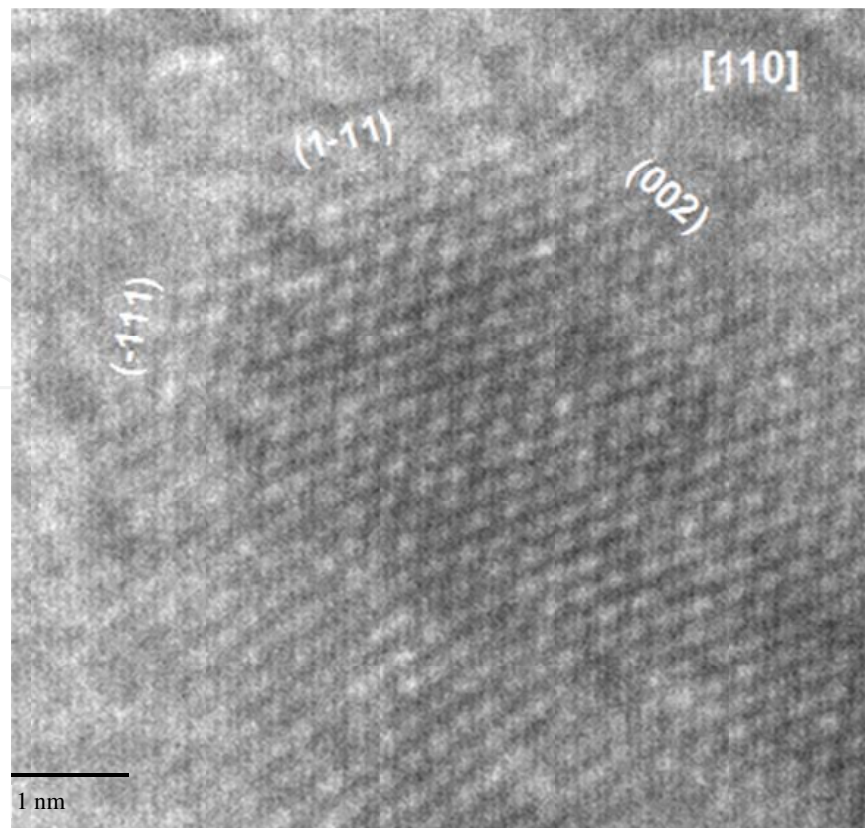


Figure 9. HRTEM image of an individual platinum-iridium nanowire

3.4. Conductivity measurements

Single nanowire, conductivity measurements were also performed on 60:40 Pt-Ir nanowires and compared against platinum nanowires prepared by a similar method. Figure 10a and 10b show scanning electron micrographs of lithographically fixated platinum and platinum-iridium nanowires, respectively, fixed between two lithographically patterned Au contacts. Platinum nanowires were used as a comparator as this is the only other known method of synthesizing similar nanoscale feed-through constructs. The method for their synthesis is described elsewhere [24]. Resistivity measurements were taken across the nanowire bridge and lead resistivity was subtracted out based on the bridging nanowire's location on the source and sink contact strip (approximately 2 μm for both samples).

Three representative current-voltage plots for both nanowire species are plotted in Figure 11. The slopes of these plots are inversely related to resistance [$I = (1/R)V$], therefore smaller slope magnitude suggests reduced resistance. For the six nanowires tested here we can calculate almost 2-fold improvement in conductivity for the Pt-Ir nanowires vs. pure platinum, which is consistent with known intrinsic properties for both metals ($\rho_{Pt} = 105 \text{ n}\Omega \text{ m}$ and $\rho_{Ir} = 47.1 \text{ n}\Omega \text{ m}$, respectively). More investigations are needed in this space.

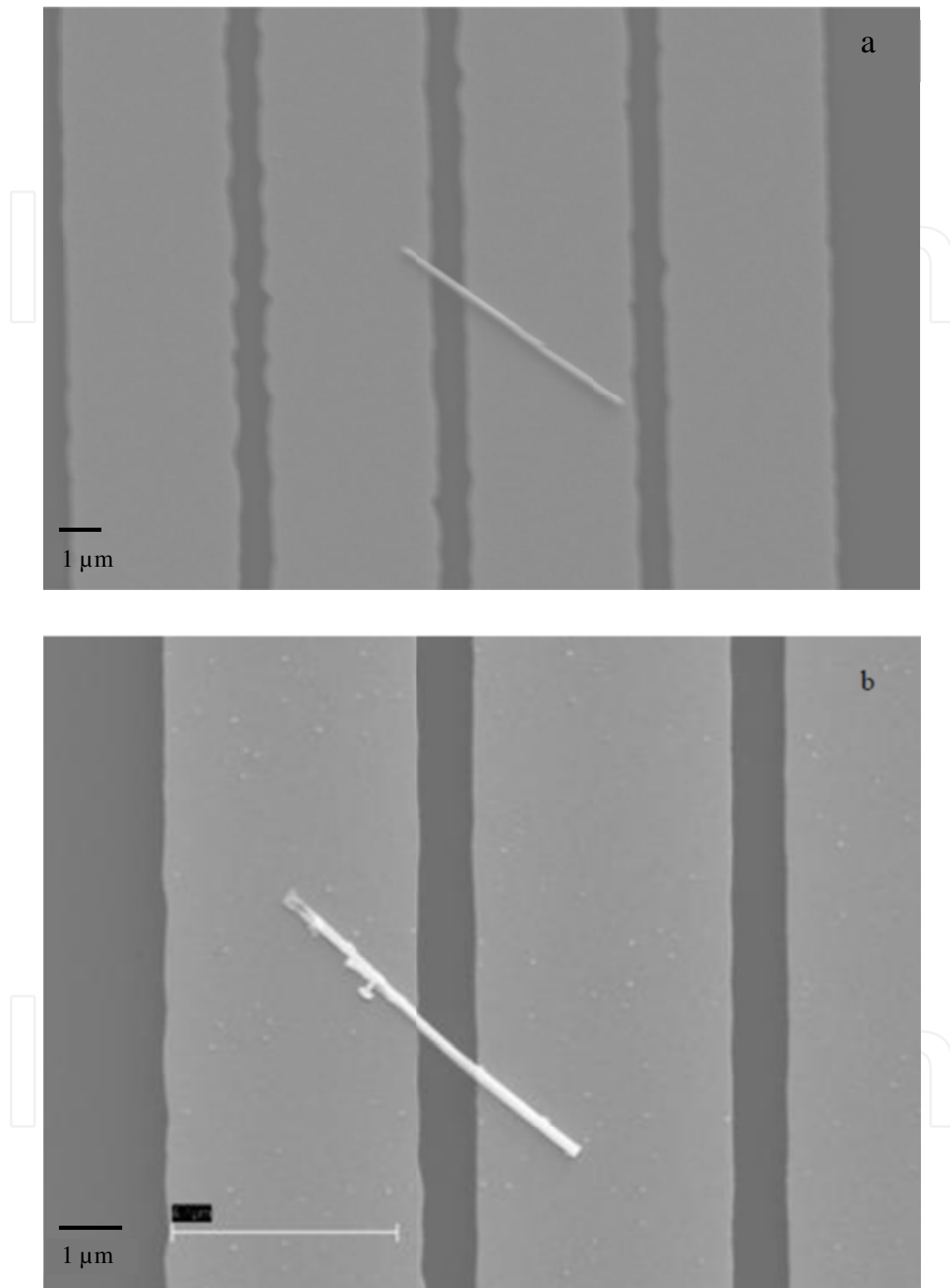


Figure 10. SEM micrograph of the testing device used for electrical conductivity measurement of a) single platinum nanowire and b) single platinum-iridium nanowire.

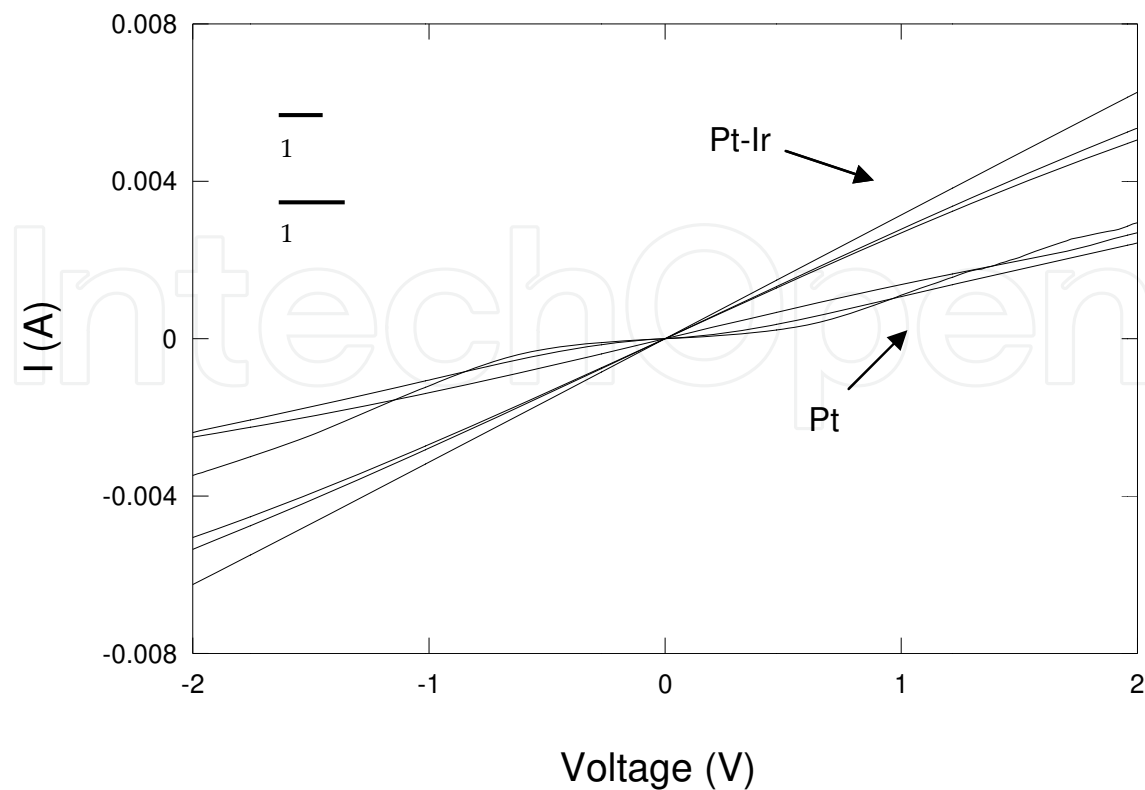


Figure 11. Current vs. voltage plots demonstrating the improved conductivity of platinum-iridium nanowires.

3.5. Helium leak testing

Pt-Ir nanowire in template assemblies were prepared with 60:40 (Pt:Ir) composition, and subjected to helium leak testing. Figure 12 shows a cross-sectional SEM micrograph of a fractured AAO template following platinum-iridium nanowire deposition. The conductive metallic nanowires are clearly seen as white, high-aspect ratio elements surrounded by the nano-channeled AAO (darker surrounding material). The right side of the image shows the 20 nm aperture side of the template and some of the bifurcations and branching can be resolved. The left side of the image shows the 200 nm aperture side of the template. Here it can be seen that complete filling of the channels has not been accomplished in this sample.

Helium leak testing results for these samples were taken an averaged 1.5×10^{-11} mbar L sec⁻¹ (variance not calculated). These results suggest that these structures would meet industry standards for hermetic leak rates [27, 28], which have been reported at values as high as 2×10^{-10} mbar L sec⁻¹. For comparison, samples prepared using other potential ranges were also tested and found to be one to two orders of magnitude more leaky. These results suggest that it may be possible to fabricate hermetic feed-throughs using these types of nano-scaled constructs, however care must be taken to ensure that the metal deposition procedure produces non-porous, high-aspect ratio conducting elements.

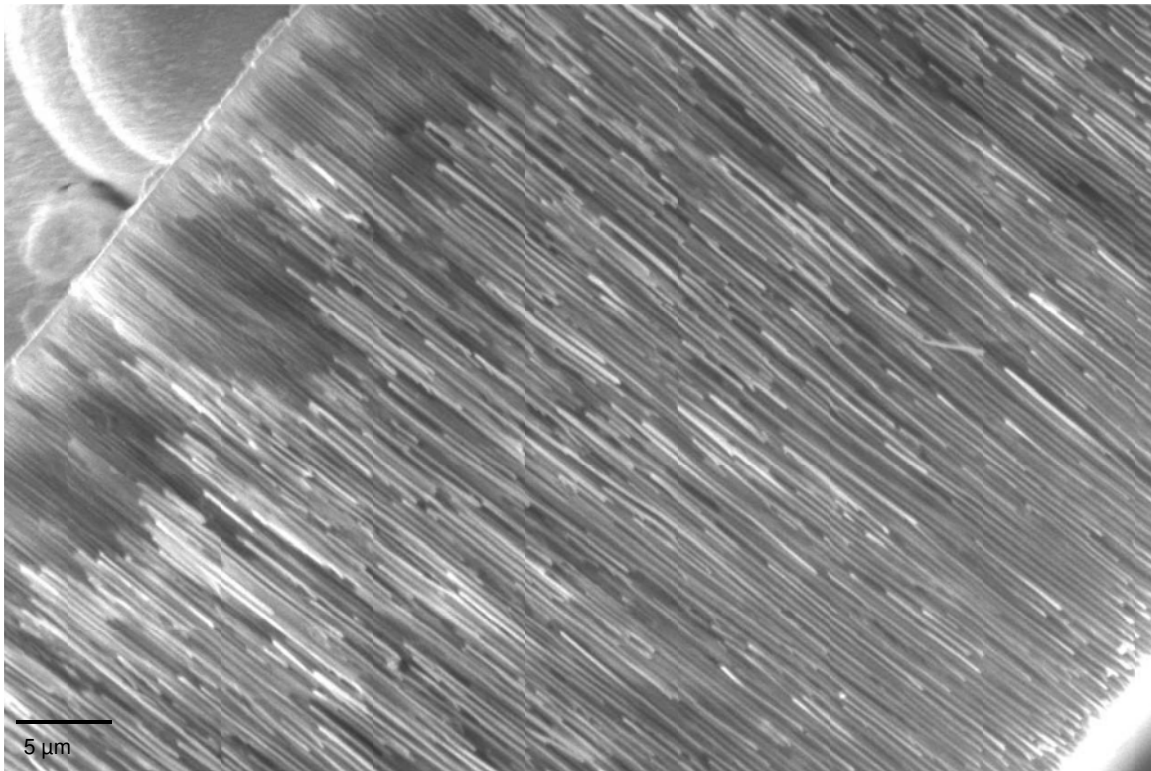


Figure 12. SEM micrograph of the cross section of platinum-iridium nanowires grown in AAO pores.

4. Conclusions

Platinum, iridium and alloys of the two will continue to play a significant role in biomedical devices due to their biocompatibility, resistance to corrosion, and electrochemical properties under physiological conditions. Processing challenges for these metals will continue to drive research and development to discover novel and efficient ways to create structures and components that meet technological demands. Namely, simpler and more reliable ways to fabricate components will always drive innovation in this space.

Hermetical packaging for implantable microelectronics will continue to use platinum and iridium feed-throughs embedded in non-reactive, electrically insulating templates/substrates. As the size of microelectronic devices decreases, and the number of feed-throughs per unit area of package increases, novel approaches to fabricating feedthrough technologies in an effective and economical way will be required.

Here we report on platinum-iridium alloy nanowires electrochemically deposited in nanoporous aluminum oxide using a template synthesis technique. We believe that series of nanowires, connected in parallel, can be used substituted for single conducting elements of equivalent cross-sectional area. However a careful understanding of how solution chemistry, deposition potential, and other parameters affect nanowires composition and morphology as well as feed-through hermeticity.

Hermeticity test results, as well as conductivity measurements, suggest that platinum-iridium nanowires may prove a viable platform for developing novel feed-through technologies. More investigation is needed to better correlate material properties of the deposited nanowires with resulting performance results. Additional work is also needed to develop ways of integrating these assemblies into entire chip package designs. However these results are promising.

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