Chapter 2

Radio Frequency IC Design with Nanoscale DG-MOSFETs

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Additional information is available at the end of the chapter

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1. Introduction

Today's nanochips contain billions of transistors on a single die that integrates whole electronic systems as opposed to sub-system parts. Together with ever higher frequency performances resulting from transistor scaling and material improvements, it thus become possible to include on the same silicon chip analog functionalities and communication circuitry that was once reserved to only an elite class of compound III-V semiconductors. It appears that the last stretch of Moore's scaling down to 5 nm range, only limited by fabrication at atomic dimensions and fundamental physics of conduction and insulation, these systems will only become more capable and faster, due to novel types of transistor geometries and functionalities as well as better integration of passive elements, antennas and novel isolation approaches. Accordingly, this chapter is an example to how RF-CMOS integration may benefit from use of a novel multi-gate transistors called FinFETs or double-gate MOSFETs (DG-MOSFETs). More specifically, we hope to illustrate how radio frequency wireless communication circuits can be improved by the use of these novel transistor architectures.

1.1. CMOS downscaling to DG-MOSFETs

As device scaling aggressively continues down to sub-32nm scale, MOSFETs built on Silicon on Insulator (SOI) substrates with ultra-thin channels and precisely engineered source/drain contacts are required to replace conventional bulk devices [1]. Such SOI MOSFETs are built on top of an insulation (SiO_2) layer, reducing the coupling capacitance between the channel and the substrate as compared to the bulk CMOS. The other advantages of an SOI MOSFET include higher current drive and higher speed, since doping-free channels lead to higher carrier mobility. Additionally, the thin body minimizes the current leakage from the source

to drain as well as to the substrate, which makes the SOI MOSFET a highly desirable device applicable for high-speed and low-power applications. However, even these redeeming features are not expected to provide extended lifetime for the conventional MOSFET scaling below 22nm and more dramatic changes to device geometry, gate electrostatics and channel material are required. Such extensive changes are best introduced gradually, however, especially when it comes to new materials. It is the focus on 3D transistor geometry and electrostatic design, rather than novel materials, that make the multi-gate (i.e double, triple, surround) MOSFETs as one of the most suitable candidates for the next phase of evolution in Si MOSFET technology [2]- [5].

Being the simpler and relatively easier to fabricate among the multigate MOSFET structures (MIGFET, ΠI-MOSFET and so on) the double gate MOSFET (DG-MOSFET) (Fig. 1) is chosen here to explore these new circuit possibilities. The DG-MOSFET architectures can efficiently control the channel from two sides of instead of one as in planar bulk MOSFETs. The advantages of DG-MOSFETs are as follows [6]:

- Reduced Short Channel Effects (SCE) due to the presence of two gates and ultra-thin body.
- Reduced subthreshold leakage current due to reduced SCE.
- Reduced gate leakage current due to the use of thicker oxide. Lower SCE in DG devices and the higher driver current (due to two gates) allows the use of thicker oxide in DG devices compared to bulk-CMOS structures.

Due to the reasons stated above, the last decade has witnessed a frenzy of design activity to evaluate, compare and optimize various multi-gate geometries, mostly from the digital CMOS viewpoint [7], [8]. While this effort is still ongoing, the purpose of the present chapter is to underline and exemplify the massive increase in the headroom for CMOS nano-circuit engineering of RF communication systems, when the conventional MOSFET architecture is augmented with one extra gate.

The great potential of DG-MOSFETs for new directions in tunable analog and reconfigurable digital circuit engineering has been explored before in [9]. The innate capability of this device has also been explored by others, such as the Purdue group led by K. Roy [6], [7] has demonstrated the impact of DG-MOSFETs (specifically in FinFET device architecture) for power reduction in digital systems and for new SRAM designs. Kursun (Wisconsin & Hong Kong) has illustrated similar power/area gains in sequential and domino-logic circuits [10]. A couple of French groups have recently provided a very comprehensive review of their DG-MOSFET device and circuit works in a single book [8]. Their works contain both simulation and practical implementation examples, similar to the work carried out by the AIST XMOS and XDXMOS initiative in Japan [11]-[13] as well as a unique DG-MOSFET implementation named FlexFET by the ASI Inc [14], [15]. Recently, Intel has announced the most dramatic change to the architecture of the transistor since the device was invented. They will henceforth build transistors in three dimensions, which they called the 3D-MOSFET [4], a device that corresponds to FinFET/DG-MOSFET.

1.2. RF/Analog IC design

In addition to features essential for digital CMOS scaling such as the higher I_{ON}/I_{OFF} ratio and better short channel performance, DG-MOSFETs possess architectural features also

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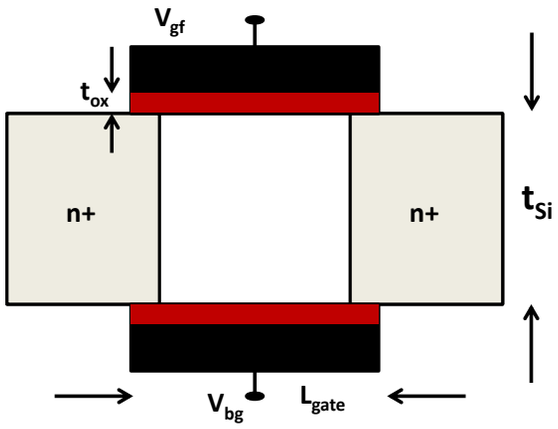


Figure 1. Generic DG MOSFET structure.

helpful for the design of massively integrated radio frequency analog and adaptive systems with minimal overhead to the fabrication sequence. Given the fact that they are designed for sub-22nm technology nodes, the DG MOSFETs can effectively handle GHz modulation, making them relevant for the RF/Analog/Mixed-Signal system-on-chip applications and giga-scale integration [16], [17].

The two most important metrics for RF CMOS/DG-CMOS circuits are the transit frequency f_T and the maximum oscillation frequency f_{max}. The former is defined as the frequency at which the current gain of the active device is unity, while the latter is the frequency for which the power gain is unity. Both these quantities relate the achievable transconductance to "parasitics" as gate-source and gate-drain capacitances (C_{gs} and C_{gd}). In case of f_{max} the gate resistance R_G is also considered as it deals with power dissipation. The f_T increases with decreasing gate lengths and for a DG-MOSFET at 45 nm it is obtained around 400 GHz [18].

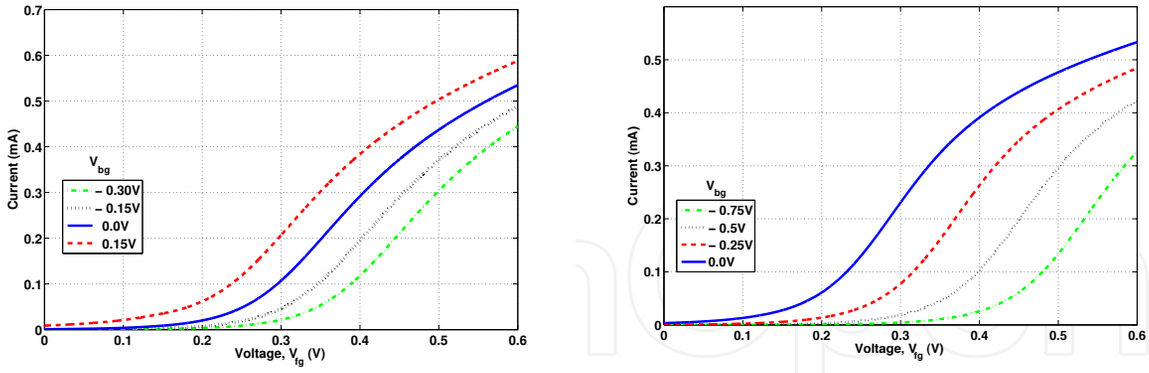
Also, they have reduced cross-talk and better isolation provided naturally by the SOI substrate, multi-finger gates, low parasitics and scalability. However, the DG-MOSFET's potential for facilitating mixed-signal and adaptive system design is highest when the two gates are driven with independent signals [19]. It is the independently-driven mode of operation that furnishes DG MOSFET with a unique capability to alter the front gate threshold via the back gate bias. This in turn leads to:

- Increased operational capability out of a given set of devices and circuits.
- Reduction of parasitics and layout area in tunable or reconfigurable circuits.
- Higher speed operation and/or lower power consumption with respect to the equivalent. conventional circuits.

2. DG MOSFET modeling and simulation

2.1. ASU PTM for FinFETs

The widely available compact models for SOI-based single-gate MOSFETs can not be used for the DG-MOSFETs, for which new surface-potential based models are developed [20]-[23].



(a) (b)

Figure 2. The I_D - V_{fg} characteristics of an n-type DG-MOSFETs at different back-gate bias conditions as observed in a) ASU PTM 32 nm DG FinFET b) ASU PTM 45 nm DG-FinFET technology with Synopsys HSPICE RF simulation.

Instead either physically-rigorous demanding TCAD simulations or approximate SPICE models utilizing two back-to-back MOSFETs mathematically coupled for improved accuracy may be used. In this chapter, most of the circuits investigated use this latter approach. We have used the ASU Predictive Technology Model for 45 nm & 32 nm DG FinFETs [24] for our simulations for most of the circuits. The circuit simulator used for the design and analysis is the industry standard Synopsys HSPICE RF. The reliability of these two ASU technology models are evident from the typical transfer characteristics of an n-type DG-MOSFET with independent back-gate biasing as shown in Figs. 2a & b. It is obvious that the front gate threshold can be tuned via the applied back-gate voltage, which is sufficient for us to confirm the tunable functionality and carry out a comparative study. This 'dynamic' threshold control is crucial to appreciate the tunable properties of the oscillator and amplifier circuits.

2.2. UFDG SPICE

The UFDG model is a process/physics and charge based compact model for generic DG MOSFETs [25]. The key parameters are related directly to the device physics . This model is a compact Poisson-Schrodinger solver for DG MOSFETs that physically accounts for the charge coupling between the front and the back gates. The UFDG allows operation in the independent gate mode and is applicable to FD SOI MOSFETs. The quantum mechanical modeling of the carrier confinement, dependent on the Ultra Thin body (UTB) thickness (t_{Si}) as well as transverse electric field is incorporated via Newton Raphson iterations that link it to the classical formalism.

The dependence of carrier mobility on Si-film thickness, subject to the QM confinement and on transverse electric field is also accounted for in the model. The carrier velocity overshoot and dependence on carrier temperature is characterized in the UFDG transport modeling to account for the ballistic and quasiballistic transport in scaled DG MOSFETS [26]. The channel current is limited by the thermal injection velocity at the source, which is modeled based on the QM simulation. The UFDG model also accounts for the parasitic (coupled) BJT (current and charge) which can be driven by transient body charging current (due to capacitive coupling) and/or thermal generation, GIDL [27] and impact ionization currents, the latter of which is characterized by a non-local carrier temperature-dependent model for the ionization rate integrated across the channel and the drain.

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The charge modeling which is patterned after that is physically linked to the channel-current modeling. All terminal charges and their derivatives are continuous for all bias conditions, as are all currents and their derivatives. Temperature dependence for the intrinsic device characteristics and associated model parameters are also implemented without the need for any additional parameters. This temperature dependence modeling is the basis for the self-heating option, which iteratively solves for local device temperature in DC and transient simulations in accord with a user defined thermal impedance.

The Relaxation Oscillator and the RF-Mixer analysis are carried with this simulator.

3. Transmitter design

The transmitter (Fig. 3) consists of an oscillator, modulator, power amplifier and finally an antenna. A matching network (Z_0 in Fig. 3) which maximizes the power transfer and minimizes the reflection losses generally precedes the 50 Ω antenna. In this article, the components that have been investigated with DG-MOSFET technology include a Relaxation Oscillator, LC Oscillator, an OOK Modulator and two different topologies of Power Amplifier. It is to be noted that the oscillators are also part of the receiver design and has its use in RF Mixer and Phase Locked Loops (PLLs).

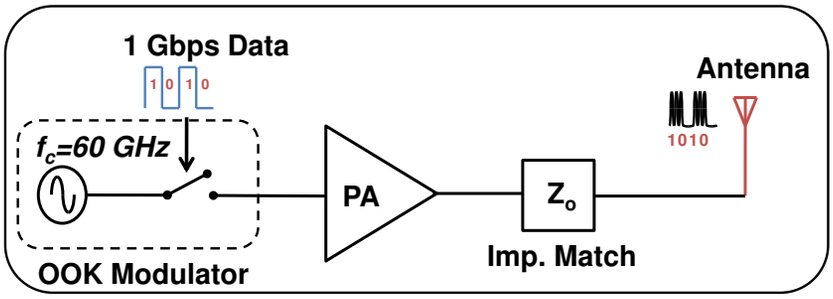
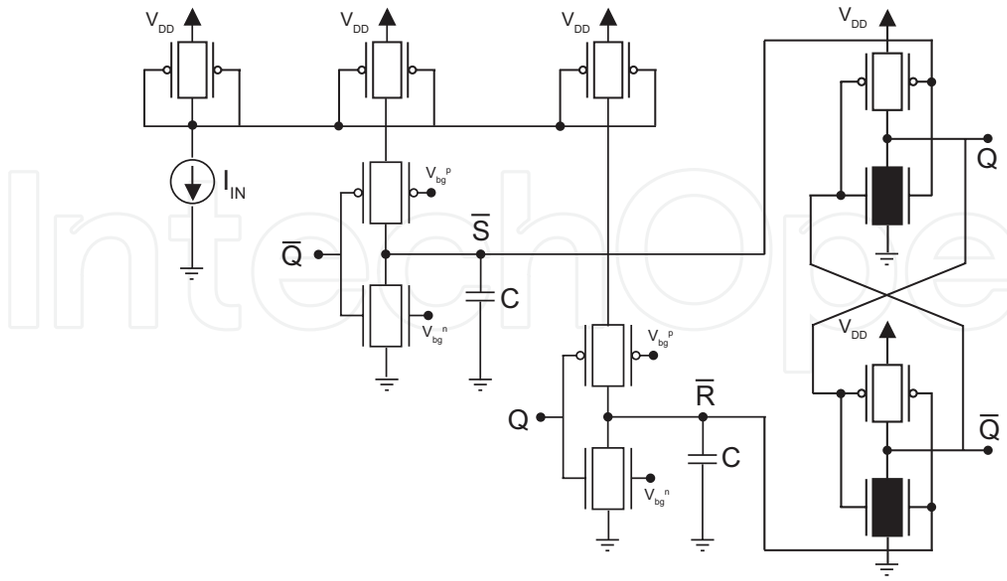


Figure 3. The transmitter block consisting of the oscillator, modulator and power amplifier and other passive devices/circuits.

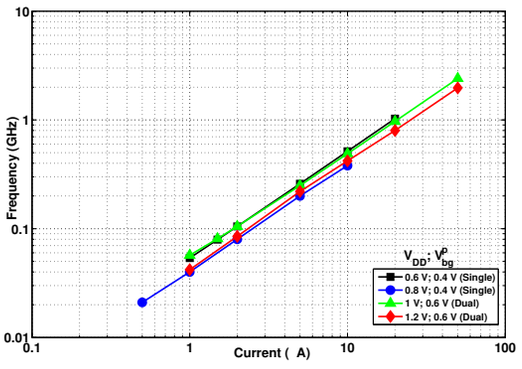
3.1. Relaxation oscillator

Relaxation oscillator is an inductorless non-resonant oscillator that is either current controlled or voltage controlled. The second circuit in [28] implements a dual input S/R latch. As illustrated in Fig. 4a the NOR gates used to construct the latch consist of only four DG-MOSFET as opposed to eight required in conventional CMOS architecture. This serves to save circuit area and a decent amount of power dissipation. The two inverters are biased with equal copies of the input current, I_{IN}, from the current mirrors implemented with three pMOS. The back gate of the two inverters are tuned in voltage to vary the frequency.

The DG-MOSFET implementation also has two advantages, firstly it can be used also as a VCO by virtue of the back gate bias and secondly it operates more efficiently with a higher upper limit as a result of very high transconductance of DG-MOSFETs [29]. Although the accessible frequency range in the VCO mode is dwarfed in contrast to massive ICO response given in logarithmic scale, the operation as a VCO provides the circuit with an extra degree of freedom in tuning. Specifically, the voltage operated fine 'vernier' frequency tuning sets a frequency with precision after it has been 'coarsely' selected by the current operated crude logarithmic tuning.



(a)



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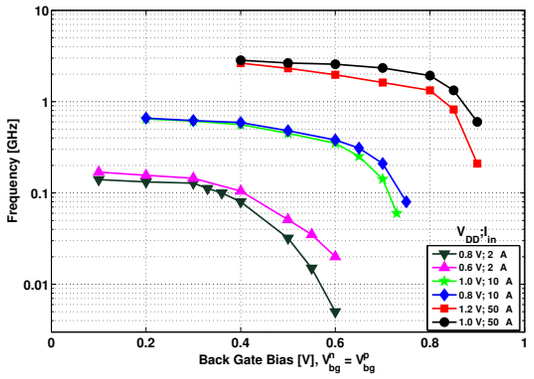


(c)

Figure 4. a)The current/voltage controlled relaxation oscillator in DG-MOSFET technology. b) The 'crude tuning' of the relaxation oscillator with varying current. c) The fine tuning in frequency with back gate bias when $V_{bg}^{p} = V_{bg}^{n}$ of the relaxation oscillator.

In Fig. 4b, we can verify the frequency has a log-log relationship with the current. The frequency ranges from 30 MHz to a few GHz for a change in current supply from 0.4 μA to 50 μA. This coarse tuning in frequency is supported via back gate fine tuning of the DG MOSFET inverters. For a constant current and voltage supply, the frequency can be tuned to vary in the order of MHz, as the inverter back gate voltage varies from 0.1 V to 1 V. It is observed, a higher V_{DD} results in a slower oscillation at a fixed input current, because the SR Latch takes longer time to reach a higher switching threshold ($\sim 1/2V_{DD}$) as V_{DD} is increased. The Fig. 4c demonstrates these facts with three different current sources and supply voltage. The phase noise of the oscillator is -104 dBc/Hz at 1 MHz offset. All these analysis are carried with 45 nm DG-MOSFET using UFDG SPICE.

3.2. LC oscillator and OOK modulator

LC oscillators consists of inductors and capacitors connected in parallel. Although inductors consume a lot of area when compared to the inductorless oscillator described above oscillators, it is a must in RF Design to use inductors because of two primary reasons [30]. They are as follows:

- The resonance of inductors with capacitors allow for higher operational frequency and lower phase noise.
- The inductor sustains a very small DC voltage drop which aids in low supply operation.

We have chosen the differential negative resistance voltage controlled oscillator (VCO) variant of the LC oscillator (Fig. 5a) for the investigation. The latch circuit in the differential mode serves as negative resistance to nullify the effects of a positive resistance arising out of the imperfect inductor. The Q factor determines the undesired resistance value (R) of the inductor (L) at the resonance frequency, ω. Modeling the resistive loss in the inductor, L by the parallel resistance (R) we can write [30]:

$$Q = \frac{R}{\omega L} \tag{1}$$

The LC tank achieves a frequency that is much higher and has a phase noise that is much lower than that of the relaxation oscillator. This is primarily because of the resonance of the circuit.

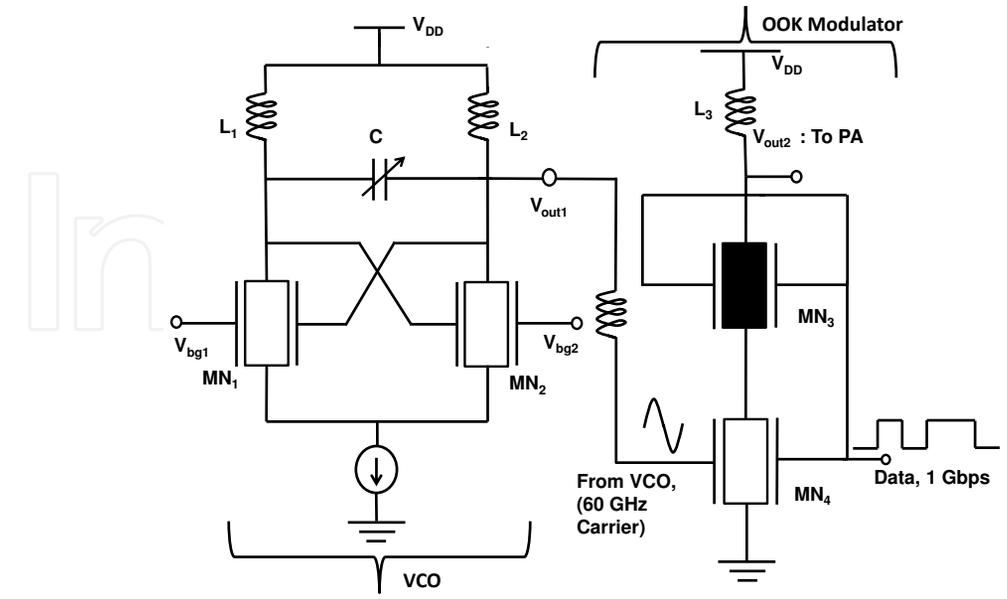
The OOK Modulation is a non-coherent modulation scheme that modulates the carrier only when the circuit is in the 'ON' state. It is the special case of Amplitude Shift Key (ASK) modulation where no carrier is present during the transmission of a 'zero'. The bit error rate for OOK modulation without the implementation of any error correcting scheme is given by [31]

$$BER = \frac{1}{2}exp(\frac{-E_b}{2N_0}) + \frac{1}{2}Q\sqrt{\frac{E_b}{N_0}} \tag{2}$$

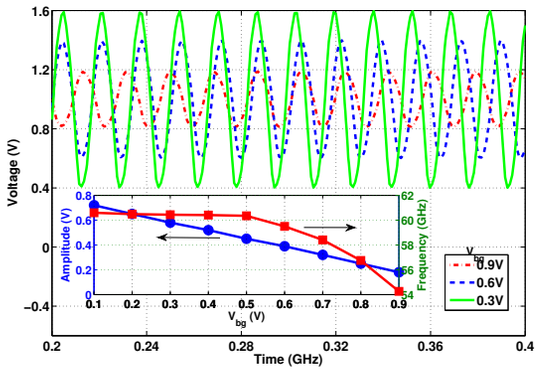
Although, the associated bit error rate of OOK modulation is inferior to that of other coherent modulation schemes, simple OOK modulation scheme is implemented to avoid the complicated carrier recovery circuit and for their ability to modulate very high frequency signals in extremely long-life battery operated applications. The non-coherent OOK demodulation generally employs an envelope detector in the receiver which saves the power, area, cost and complexity since no local oscillator (LO) or carrier synchronization scheme is involved.

3.2.1. Design and simulation

The DG-MOSFET based VCO can be tuned from the back gate for controlling the rms voltage (V_{rms}). Fig. 5b illustrates this interesting tunable feature of the DG MOSFET VCO. Without any change in the supply, the V_{rms} can be controlled via back gate bias (V_{bg}), which can have



(a)



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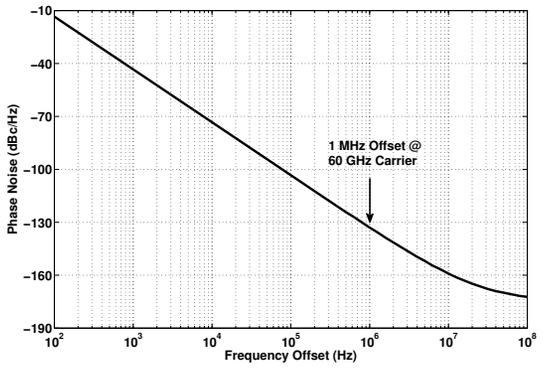

(c)

Figure 5. a) The OOK Modulator circuit with the VCO. The proposed OOK Modulator uses only two DG-MOSFET for modulation and switching. b) The variation of VCO output amplitude at different V_{bg}. Inset: Amplitude and frequency variation for different V_{bg}. c) The phase noise of the VCO at 60 GHz. The phase noise at 1 MHz offset is observed at -133 dBc/Hz in time variant Hajimiri-Lee model [32].

application in many adaptive low power wireless systems. The bias at the back gate can also be tuned to change the oscillation frequency after a certain threshold (0.5 V) (Fig. 5b inset). Although DG-MOSFET is not reputed for its noise performance, the phase noise of the 60 GHz VCO is found to be -133 dBc/Hz at 1 MHz offset (Fig. 5c) which is comparable to that of bulk CMOS [33]. As expected, the phase noise is dominated by the process dependent flicker noise of slope $\sim$ -30 dB/decade. The corner frequency f_{cor} is obtained around 10 MHz.

The proposed novel DG-MOSFET based OOK Modulator [34] consists of only two DG-MOSFETs making it ideal for use in ultra low power systems (Fig. 5a). The modulator can

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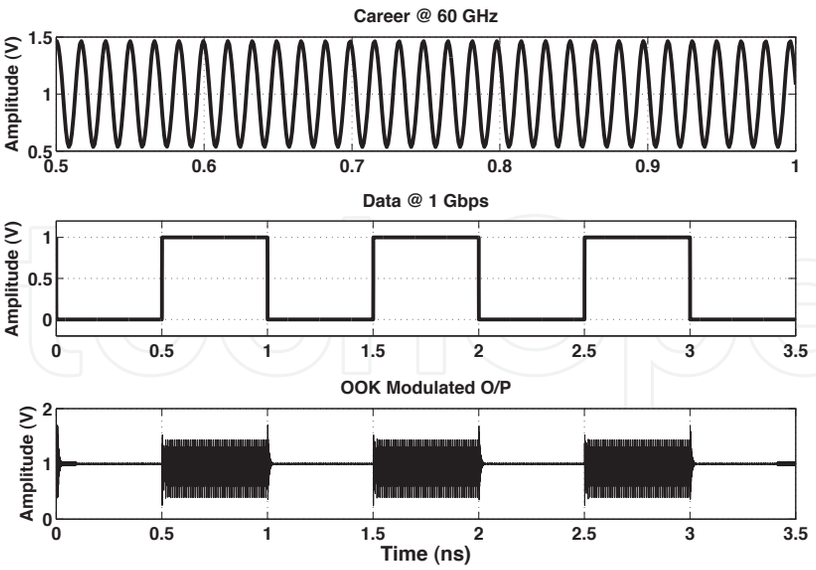

Figure 6. The OOK Modulated output for a carrier frequency of 60 GHz and data rate of 1 Gbps. The input data sequence resembles 50% duty cycle.

work up to a data rate of 5 Gbps without any discernible distortion for 60 GHz carrier. The DG-MOSFET MN_4 acts as the key OOK modulating device. The 60 GHz sinusoidal carrier from the VCO is fed into one of the gates of the transistor whereas the pulsed digital data is input to the other gate. The charge capacitive coupling of the two gates provided by the thin Si body determines the modulation, and therefore depends on the bias conditions of the two gates as well as device dimensions. The modulation occurs when the device operates in the saturation or in cut-off region, that is when there is either a '1' or '0' respectively emanating from the pulsed digital data. In other words, the modulation takes place at all instants of time. The symmetric DG-MOSFET MN_3 acts as the switch and is kept at a high threshold voltage (filled) for better electrostatics and keying and to maximize the I_{ON}/I_{OFF} ratio. The MN_3 is turned on at the 'HIGH' state of the pulsed data and remains off at the 'LOW' state, maintaining the principle of OOK Modulation scheme. The modulated output is obtained at the drain of MN_3. This is illustrated in Fig. 6. All these analysis are carried in 32 nm ASU PTM FinFET technology.

3.3. Power Amplifier

The Power Amplifier (PA) is the final stage of transmitter design before signal transmission through antenna. They are responsible for amplifying the power level of the transmitted signal several times so that the received signal is above the sensitivity of the receiver which is calculated from the link budget analysis. The PAs are divided into various classes such as A, B, AB, C D, E, F etc. Among these classes A, B, AB and C incorporate similar design methodologies differing only in the biasing point. Among these Class A amplifier is the most linear and is widely used in RF transmitter design although they have the least Power Added Efficiency (PAE). Several acclaimed literatures [35], [30] are available for interested readers on these concepts. This book chapter focusses on the design of tunable DG-MOSFET Class A PA.

The design of the wide band and high gain PA is a challenging task, especially in ultra-compact MOSFETs with low output impedance. Consequently, in [36], we simply adapted two recent single-gate implementations with competitive features in the GHz range, which allows a more fair performance comparison to be made between different devices. In the first PA topology [37], we modify the architecture slightly for the DG-MOSFET to explore its gain and bandwidth characteristics as well as its tunability. The second topology reported here is a three stage single-ended, common-source (CS) PA similar to the one reported by Yao et al. [38] for conventional CMOS. The basic difference over the published topologies in both cases is the length of the DG-MOSFET devices (45 nm) that is substantially smaller. There are a number of reasons for this gate length choice. Firstly, the proposed PAs are essentially designed for low-power highly compact Si mixed-signal radio applications where the range and area will be typically quite limited. Secondly, the DG-MOSFET architecture is inherently a narrow width device technology in which very large number of fingers needed to obtain large W/L ratios. Finally, we wish to implement a PA for ultra-compact wide-band RF CMOS applications such as vehicular anti-collision radar. Given that DG-MOSFET technology is aimed for sub-22 nm digital technologies, 45 nm is a good compromise for analog circuit implementation.

The next two sections will discuss in detail about these design modifications and provide their simulated response including gain tuning, peak gain, bandwidth and linearity. Interested readers can compare the performances of these power amplifiers with a few other conventional designs in [36].

3.3.1. Topology A - Design and simulation

The circuit topology of the first wide band (3-33 GHz) DG-MOSFET PA is shown in Fig. 7a, which consists of three DG-MOSFETs in a Darlington cascode arrangement. The common source transistor MN_1 operates in the symmetric mode while the two transistors MN_2 and MN_3 are configured for independent mode operation. The width of MN_1 is taken to be 1 μm while the width for transistors MN_2 and MN_3 are kept higher at 2.4 μm for better input return loss and optimized gain performance. MN_3 is biased at 2.6 V (V_{b1}). The back gate of the transistors MN_2 and MN_3 are biased for gain tuning. The resistors R_1 and R_2 complete a self biasing network for Class A operation. This modified DG-MOSFET darlington configuration is divided into two stages. The first stage is the series peaking stage and inter-stage matching, and the second stage is the output power stage.

The series peaking circuit consisting of R_3 and L_1 increases the output load pull impedance, and also provides the peaking impedance for feeding forward signals. The inductor L_3 along with the source degeneration circuit consisting of R_4 and L_2 yields in real part wide band inter-stage impedance matching for maximizing the power transfer between the stages. The common source transistor MN_2 and MN_3 are connected in cascode. The transistor MN_3 acts in common gate configuration and one of its gate is grounded with the aid of the peaking inductor L_4 and a bypass capacitor C_1 [30]. Along with achieving a near constant gain by maintaining the flatness, the bandwidth of the amplifier is also increased with the aid of this peaking inductor. A high pass L-network (L_5 & C_3) is used as the matching circuit.

Our simulation verifies the forward gain (S_{21}) to vary from 3 to 33 GHz, while maintaining a desired flatness (Fig. 7b). The gain changes by less than 20% in this frequency range, attesting to the extreme flatness. The peak gain is observed at 24.5 dB. The input and output return

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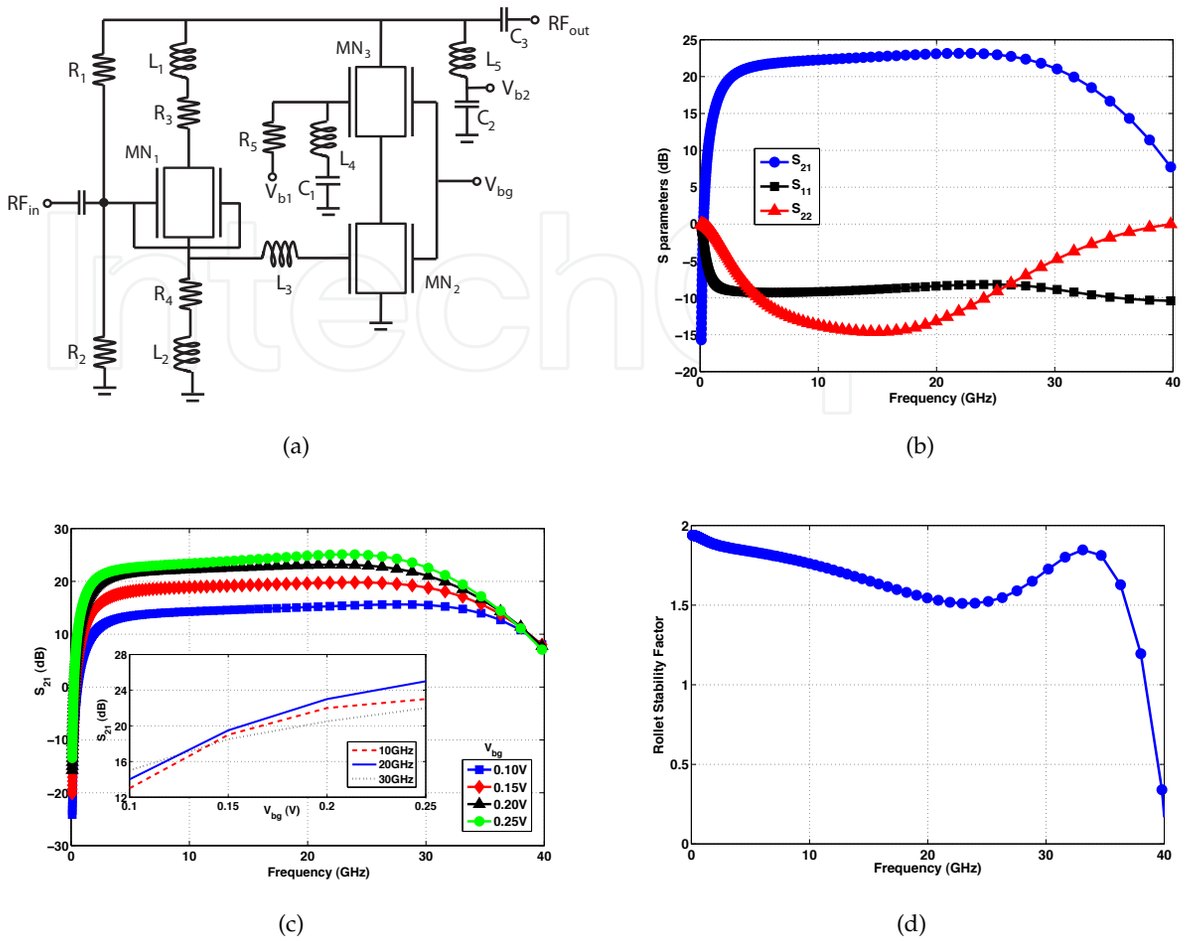

Figure 7. a) The DG MOSFET based power amplifier circuit in modified darlington cascode configuration. Transistors MN_1 operates in the symmetric mode while MN_2 and MN_3 operate in independent mode with the back gates used for dynamic tuning. b) The S parameters which provide the gain (S_{21}) and reflection losses (S_{11} & S_{22}) of the power amplifier. This is measured for V_{bg} = 0.2 V. c) The back gate dependence of the gain is clearly evident. The gain changes by $\sim$ 10 dB in the tuning range of V_{bg}. Inset: Gain variation with V_{bg} at different frequencies. d) The rollet stability factor (K) is above unity in the operating range of 2 - 32 GHz verifying the amplifier to remain unconditionally stable in this range. K drops below unity beyond $\sim$ 38 GHz.

losses (S_{11} & S_{22}) are also obtained from the simulation. Fig. 7c shows these S parameters at a V_{bg} of 0.2 V which is applied at the back gate of the transistors MN_2 and MN_3. The back gate voltage (V_{bg}) is varied from 0.1 V to 0.25 V for the operating frequency range during which the gain of the amplifier increases considerably. The range of gain tuning is observed to be limited to almost 10 dB. The inset of the figure shows the gain variation with V_{bg} at different frequencies. The unconditional stability of the amplifier is verified measuring the rollet stability factor, K which is given as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\triangle|^2}{2|S_{12}S_{21}|} \tag{3}$$

$$\triangle = S_{11}S_{22} - S_{12}S_{21} \tag{4}$$

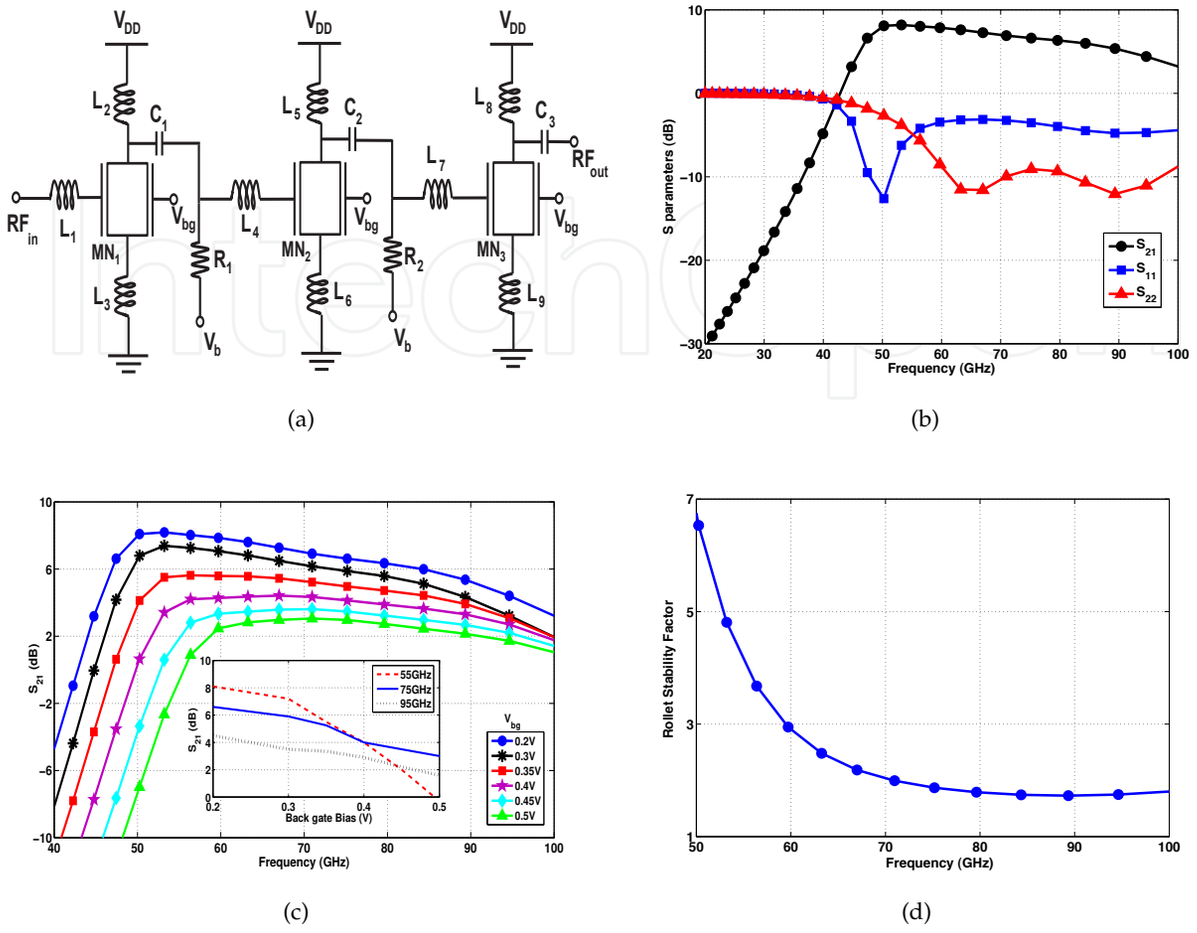

Figure 8. a) The three stage DG MOSFET based power amplifier circuit. All the three transistors operate in the independent mode. b) The S parameters which provide the gain (S_{21}) and reflection losses (S_{11} & S_{22}) of the power amplifier. This is also measured for V_{bg} = 0.2 V. c) The back gate dependence of the gain is clearly evident. The gain changes by $\sim$ 6 dB in the tuning range of V_{bg}. Inset: Gain variation with V_{bg} at different frequencies. d) The rollet stability factor (K) is well over unity in the operating range of 60 - 90 GHz verifying the amplifier to remain unconditionally stable in the range.

The value of K is observed to be above unity in the operating frequency range indicating the unconditional stability of the amplifier (Fig. 7d). The back gate tuning of the PA is verified from Fig. 5. The 1 dB compression point (P_{1dB}) and the 3rd order Input Intercept Point (IIP_3) are found to be 11.9 dBm and 27.5 dBm, respectively, indicating the suitability of the circuit. The 15.6 dB difference between P_{1dB} and IIP_3 can be attributed to the scaling down of DG MOSFET to 45 nm [35]. The power added efficiency (PAE) and the fractional bandwidth (FB) of the amplifier is $\sim$12% and 176% respectively.

3.3.2. Topology B - Design and simulation

In the second topology, the DG-MOSFET Class A amplifier is implemented in three stages (Fig. 8a). Although the earlier cascode topology has higher & flatter gain, and larger output impedance, the CS configuration is advantageous in terms of the lower supply voltage required, leading to higher efficiency. All the transistors in this topology operate in the

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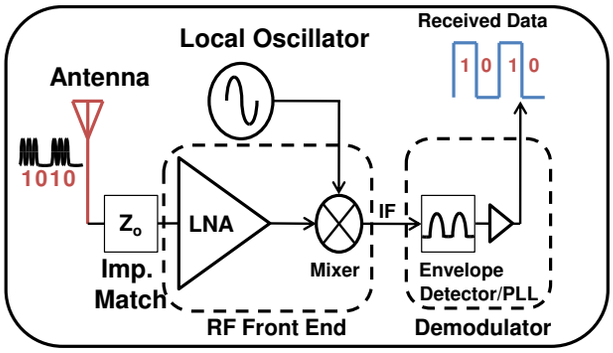


Figure 9. The receiver block consisting of the RF Front End (LNA & RF Mixer) and the Demodulator (Envelope Detector, for non-coherent detection or PLL, for coherent detection).

independent mode. The source degeneration inductors L_3, L_6 and L_9 along with the inter stage inductors L_4 and L_7 maximizes the power transfer and improves linearity [35]. The width of the three transistors are kept fixed at 1.2 μm. The source and the bias voltage (V_b) are both kept at 1 V.

Although the 3-dB bandwidth is $\geq$ 50 GHz, as evident from Fig. 8b, for all cases of back gate voltages (Fig. 8c) a more realistic operating range of this amplifier can be considered to be in the range of 60 - 90 GHz. Once again, the inset of the Fig. 8 shows the gain variation with V_{bg} at different frequencies. The peak gain achieved is $\geq$ 8 dB. The rollet stability factor remains more than unity for this operating range as shown by simulated data in Fig. 8d. The P_{1dB} and the IIP_3 are found to be 7.2 dBm and 19.8 dBm respectively. The PAE and the FB of this amplifier is $\sim$14% and 40% respectively.

4. Receiver design

The front end of the receiver consists of a Low Noise Amplifier (LNA) and RF Mixer. To demodulate a non-coherent signal an Envelope Detector is used while to demodulate a coherent signal a Phase Locked Loop is generally used (Fig. 9). In this chapter, we have designed an LNA, Envelope Detector and a Charge Pump Phase Frequency Detector (which is an essential component in PLL design) and analyzed an existing RF Mixer.

4.1. Low Noise Amplifier

The Low Noise Amplifier (LNA) is an essential component in the front-end of any communication/navigation receiver. The received signal at antenna is very weak and therefore it is necessary to amplify the signal for demodulation and processing. At the same time the noise figure of the amplifier has to be very low because the received signal will eventually be passed to non-linear devices such as RF Mixers which add noise. Therefore LNA design optimizes to minimize the noise level at the first stage of the receiver i.e. at the LNA itself. Other characteristics that require from an LNA include high gain, impedance matching linearity and stability.

The circuit topology of the tunable 45 nm DG-MOSFET LNA implemented here is shown in Fig. 10, which consists of three DG-MOSFETs in a 2 stage common source cascode topology. The common source transistor MN_1 operates in the symmetric mode while the two transistors MN_2 and MN_3 are configured for independent mode operation. The common

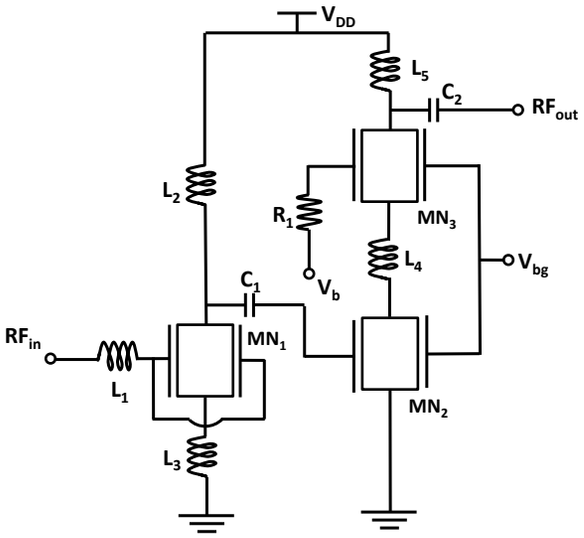
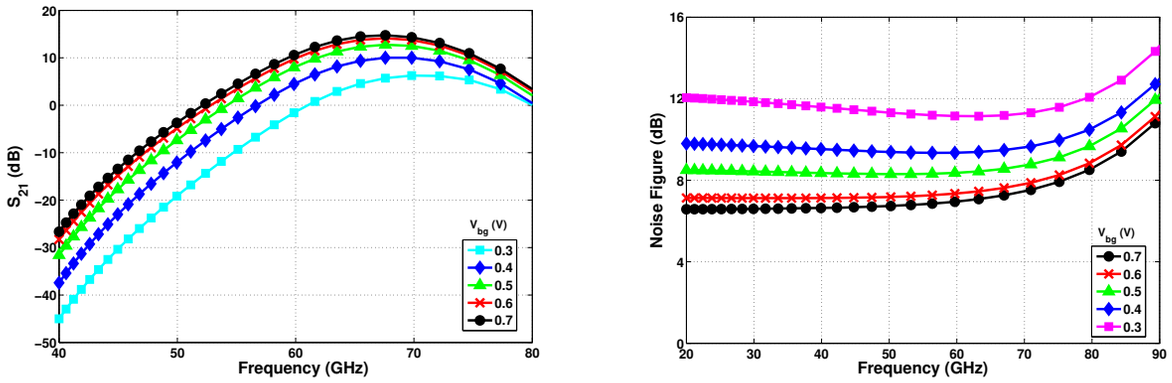


Figure 10. The DG MOSFET based LNA in common source cascode configuration. Transistors MN_1 operates in the symmetric mode while MN_2 and MN_3 operate in the independent mode with the back gates used for dynamic tuning.



(a) (b)

Figure 11. a) The gain (S_{21}) of the LNA varies with V_{bg}. This is measured for V_{bg} = 0.3 V to 0.7 V. b) The noise figure dependence on V_{bg} of the LNA is evident. The NF changes by 4.4 dB in the tuning range of V_{bg} at 65 GHz.

source transistor MN_2 and MN_3 are connected in cascode. The transistor MN_3 acts in common gate configuration. The width of MN_1 is taken to be 1 μm while the width for transistors MN_2 and MN_3 are kept higher at 2.4 μm for better input return loss and optimized gain performance. The supply, V_{DD} is kept constant at 1.2 V. MN_3 is biased at 2 V (V_b). The back gate of the transistors MN_2 and MN_3 are biased for gain tuning.

The series peaking circuit consists of an inductive load, L_2, that allows for low voltage operation and resonates with the inter stage capacitance, C_1, enabling a higher operating frequency [30]. The inductor L_1 is set to resonate with the gate source capacitance of MN_1. The source degeneration circuit consisting of L_3 yields (in real part) wide band impedance matching to maximize the inter-stage power transfer. The inductor L_4 tunes out the middle pole of the cascode, thus compensating for the lower f_T [39] of DG-MOSFET which is nearly 150 GHz at 45 nm.

The simulation shows the 3-dB bandwidth to be 15 GHz, ranging from 60 to 75 GHz. The forward gain (S_{21}) achieves a peak value of 15 dB at 65 GHz for V_{bg} = 0.7 V (Fig. 11a). Beyond this maximum operating voltage the gain gets saturated and is independent of V_{bg}. The peak gain reduces gradually as V_{bg} is reduced and drops to ∼5 dB for V_{bg} = 0.3 V. The power dissipated (P_{dc}) by the LNA also varies with V_{bg}, reaching 18 mW at V_{bg} = 0.7 V. Similarly, the LNA noise figure (NF) also depends upon the back gate bias, dropping to a minimum at peak gain as expected. It ranges from 7 dB at V_{bg} = 0.7 V to 11.4 dB at V_{bg} = 0.3 V (Fig. 11b). Clearly, the back gate tuning provides a convenient tool to optimize specific device performance parameters, setting up unique trade-offs such as that between power and gain.

The proposed LNA is unconditionally stable in the operating frequency range, verified from the simulated rollet stability factor, i.e. $K > 1$. The circuit is also simulated for linearity performance using a two tone frequency analysis near 60 GHz and the observed 3^{rd} order Input Intercept Point (IIP_3) is -5.2 dBm.

Overall, the DG-MOSFET implementations have impressive characteristics that either match or exceed the bulk MOSFET and even SiGe counterparts [40]-[42]. It is fair to point out that much of this response can be attributed to small gate length in our designs. However, a short gate length has also consequences for linearity and lower output impedance, with which this architecture appears to cope well.

4.2. RF mixers

The RF mixer is a non-linear electrical circuit that creates two new frequencies from the two signals applied to it. The new frequencies (sum & difference) are called the intermediate frequencies (IF). The sum frequency has its application on the up conversion whereas the difference frequency is used in the down conversion of an input signal. The conversion gain (CG) determines the mixing performance of the circuit [35].

4.2.1. DG-MOSFET mixers and methodology

DG-MOSFET mixer occupies a special status among analog applications given the compact and high performance nature of an active mixer using only one transistor which saves both power and area compared to conventional CMOS. Accordingly, there are already several literatures available focusing solely on this simple but promising circuit. For instance, a recent work by S. Huang et. al. [43] analyzes the RF Mixer based on the derivative superposition method. An earlier work [44] considers the evaluation of power consumption and area overhead of the DG-MOSFET for RF-mixer applications. W. Zhang et. al. [45] explored the use of multiple independent-gate FinFETs (MIGFETs) application and compares the spectral response of the single-and multiple-transistor (balanced) versions. Although this research provides valuable physical insights regarding the operational principles and behavior of the DG-MOSFET mixer, unfortunately the temporal resolution or the length of the transient data used in their Fast Fourier Transform (FFT) analysis, and the range of device parameters explored, are insufficient for a thorough study of the mixing performance in a methodical manner.

In contrast, in [46] we focus on the structural and operational parameters of DG-MOSFET in a methodical and accurate manner to optimize the biasing for maximum conversion

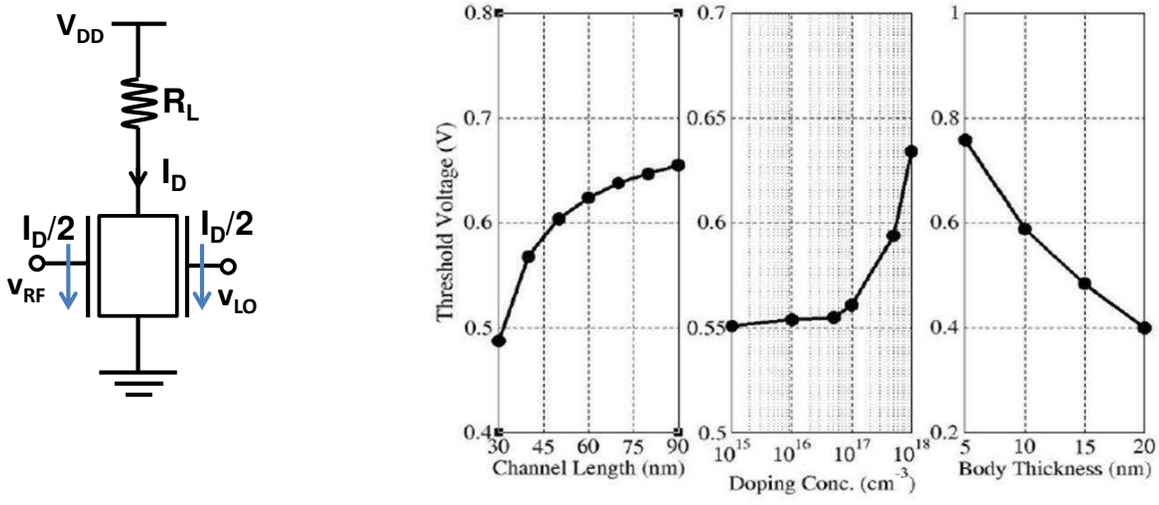


Figure 12. a) DG MOSFET RF Mixer circuit. b) The variation of V_T for the different device parameters L_{gate}, N_d and t_{Si}.

gain and power efficient design of the mixer circuit. Additionally, we also look into the correlation between conversion gain and the device parameters. In our methodology, we carefully considered the input RF and local oscillator (LO) signals' bias conditions while fairly comparing conversion gain recorded with different structural parameters, ensuring that gate over-drive (LO DC offset) has been kept the same.

The DG-MOSFET RF Mixer circuit (Fig. 12a) explored in [46] consists of a single double gate transistor. For a fair comparison of mixing performance obtained from varying important structural parameters, we first explore the dependence of threshold voltage (V_T) (Fig. 12b) on each of the device parameters, gate length (L_g), doping concentration (N_A) and body thickness (t_{Si}). The source voltage (V_{DD}) is kept at the typical value of 1 V and the circuit load, R_L, is kept at 6 kΩ for the analysis. The sinusoidal RF signal is considered at the frequency f_{RF} of 50 MHz while the sinusoidal local oscillator signal is chosen at a frequency f_{LO} of 10 MHz so to down convert the incoming frequency to 40 MHz. In this DG MOSFET based architecture, the RF input signal ((v_{RF} = (v_{rf} + V_{RF}) sin($2\pi f_{RF}$t)) is applied at one gate while the local oscillator (LO) signal (v_{LO} = (v_{lo} + V_{LO}) sin($2\pi f_{LO}$t) is applied at the another gate of the transistor. Here, v_{rf} and v_{lo} are the AC components of RF and LO signal respectively, while V_{RF} and V_{LO} are the respective DC bias components. The output signal (V_{out} = A_v[cos2πt(f_{RF} - f_{LO}) - cos2πt(f_{RF} + f_{LO})]) consisting of the two intermediate frequencies is observed at the drain of the DG MOSFET and A_v is (v_{rf} + V_{RF})(v_{lo} + V_{LO})/2. The conversion gain (CG) by definition, then becomes (v_{lo} + V_{LO})/2. However, this theoretical linear proportionality of CG on LO amplitude is not valid everywhere and there is a strong dependence on the device geometries and threshold as evident from this analysis, and this necessitates the requirement for bias optimization with quantum corrected simulations.

4.2.2. Non-linearity analysis

The DG-MOSFET Mixer's multiplicative/non-linear property has been analyzed here from Fig. 12a. The RF signal which is applied at the front gate is represented by small signal model. This is justified because the power level of RF signal is very small on reception at the antenna and remains small even amplified by the LNA. Therefore, the output voltage, V_{out} is

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given as:

$$V_{out} = g_m v_{RF} R_L \tag{5}$$

where g_m is the transconductance of the device at the front gate. The I-V characteristics of DG-MOSFET at saturation is modeled as [47]

$$I_D = K[(V_{gs} - V_T)^2 - K' e^{\frac{V_{gs} - V_0 - V_{ds}}{kT}}] \tag{6}$$

where K & K′ are process and device constants and V_0 is a second order term of V_T [47]. Here the drain current at the front gate is modeled by ignoring the exponential term assuming a large V_{ds} at saturation, where the numerator at the exponent goes negative.

$$\frac{I_D}{2} \simeq K(V_{gs} - V_T)^2 \tag{7}$$

The transconductance at the front gate is,

$$g_m = \frac{1}{2} \frac{\partial I_D}{\partial V_{gs}} \tag{8}$$

From eqns. (7) and (8) we can write,

$$g_m = 2K(V_{gs} - V_T) \tag{9}$$

Now from eqns. (7) and (9),

$$g_m = \sqrt{(2KI_D)} \tag{10}$$

A large signal model is assumed for the back gate as the LO signal is locally generated and usually has high amplitude levels,

$$I_D/2 = K(v_{LO} - V_T)^2 \tag{11}$$

implies,

$$I_D = 2K(v_{LO} - V_T)^2 \tag{12}$$

Therefore from eqns. (5), (10) & (12),

$$V_{out} = K''(v_{LO} - V_T)v_{RF} \tag{13}$$

Here K'' is a constant which include the process and device parameters and the resistor R_L. The eqn. (13) analyzes the DG-MOSFET device analysis for non-linear RF Mixer operation. The output voltage is the product of two input voltages. The process dependent parameter V_T can be eliminated if we consider a balanced/differential mixer mode. However, typically the balanced mode is avoided because in a receiver design the mixer follows the LNA which is generally single ended as it follows a single ended antenna. A balun which consumes a large area is thus required to construct before the mixer for the differential mode use.

4.2.3. Operating point analysis

After the FFT analysis (Fig. 13a inset) of the output at a very high temporal resolution, we observe significant spectral lines at the two intermediate frequencies of 40 MHz (f_{RF} - f_{LO}) and 60 MHz (f_{RF} + f_{LO}) indicating the appropriate double gate mixing performance and non-linearity. The presence of higher harmonics (such as at 100 MHz frequency) in the spectra indicates higher-order non-linearities and must be filtered out to work with the desired frequency. For the analysis purposes and simplification of the observed spectra, the LO signal used in our study is a pure sine-wave with a DC offset providing the operating point for the device, while the RF AC input at the another gate is held constant without a DC offset.

Our study indicates that the CG of the mixer rapidly changes with the amplitude of the LO rising to 200 mV (Fig. 13b), beyond which the increase is limited. Hence, for all L_{gate} values, the operating point of the mixer is chosen to be set around 120 mV for optimum power efficiency and CG. Similar results were also obtained for different N_As and t_{Si}s from corresponding analyses.

The CG is particularly sensitive to the LO DC bias (Fig. 13c) with an 'm-shape' dependence, where the middle dip could be as much as -80 dB. Hence, seemingly there are two bias conditions that provide similar performance in CG of the mixer (Fig. 13b). For instance, these two bias points are observed at 0.3 V and 1 V for L_{gate} = 30 nm and v_{lo} = 40 mV. Moreover, this m-shape is a very weak function of LO AC bias and L_{gate}. Data recorded with AC inputs of 40 mV with 120 mV shift mainly vertically with a large lateral similarity in terms of DC bias dependence. Likewise, the peak position shifts roughly 0.1 V only, as the gate length is varied from 90 nm to 30 nm. It is interesting to note that these optimum DC-bias ranges correspond to the least 'linear' sections of the device operation, as can be seen from the transfer characteristics and transconductance (g_m vs. I_d) curves in Fig. 13d. The current changes in a very non linear pattern around the optimum bias ranges and the g_m peak corresponds to the central dip in Fig. 13c. Clearly, the lower bias point ($\sim$ 0.3 V in Fig. 13c) should be preferred because of power efficiency and better stability indicated by the broader plateau. Similar analyses conducted for different N_A and t_{Si} of the DG-MOSFET mixer yield in similar results to our study of L_{gate}. A double-peaked LO-DC behavior persists in all cases. Summarizing results from these simulations, Tables 1, 2 and 3 list the optimum (lower) bias points for different structural parameters studied.

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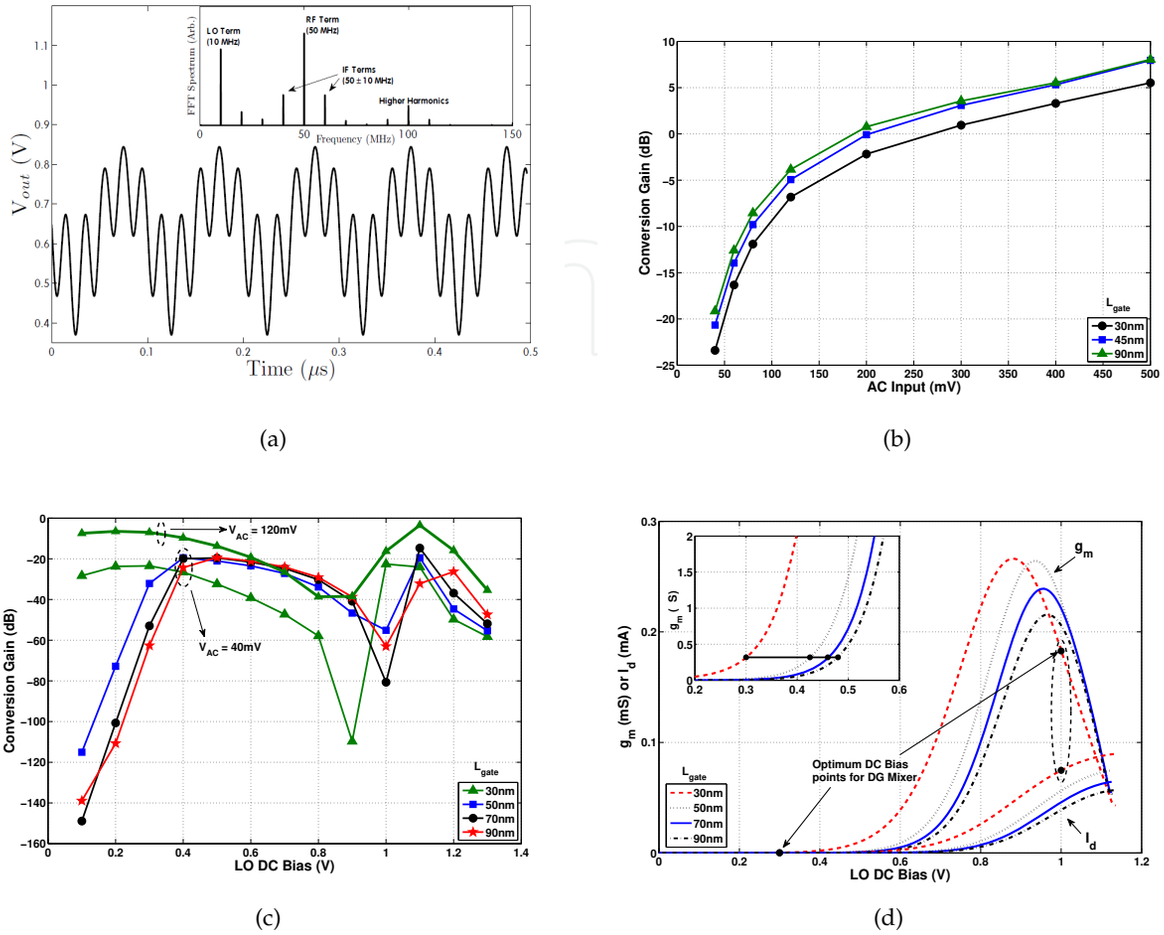


Figure 13. a) The FFT (inset) of the voltage at the mixer output (main panel) shows both the sum & difference terms as well as additional higher order harmonics. b) Variation of conversion gain with AC Input for different L_{gates}. The CG increases rapidly before 120mV, after which the performance of the conversion gain is limited. c) Variation of CG with DC bias at different L_{gate}s. Observation of two AC inputs (120 mV & 40 mV) shows their CG variation with DC bias is similar. d) Transconductance (g_m) & drain current (I_d) over DC bias for different L_{gate}s. Out of two optimum bias points, the lower one at 0.3 V (30 nm) is chosen for better stability and power efficiency.

L_{gate} (nm)	30	50	70	90
DC Bias (V)	0.30	0.41	0.45	0.47

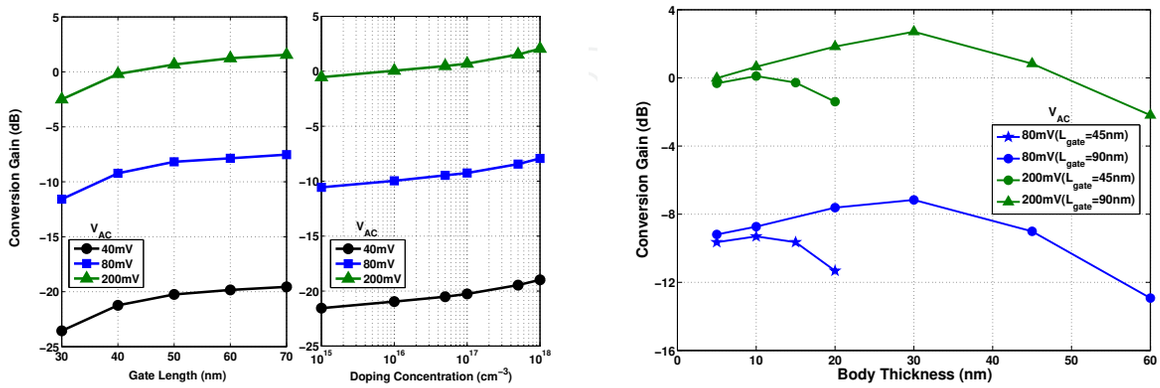
Table 1. Optimum LO DC bias for different gate lengths at $N_A = 10^{15}\ cm^{-3}$ & $t_{Si} = 5\ nm$

N_A (cm^{-3})	10^{15}	10^{16}	10^{17}	10^{18}
DC Bias (V)	0.45	0.47	0.48	0.50

Table 2. Optimum LO DC bias for different doping concentrations at $L_{gate} = 45\ nm$ & $t_{Si} = 5\ nm$

t_{Si} (nm)	5	10	20	30
DC Bias (V)	0.6	0.5	0.4	0.3

Table 3. Optimum LO DC bias for different body thicknesses at $N_A = 10^{15}\ cm^{-3}$ & $L_{gate} = 90\ nm$



(a) (b)

Figure 14. a) Dependence of CG on the gate length (L_{gate}) & doping concentration (N_A) for different AC Inputs. The weak correlation of these two parameters on the CG is clearly evident. b) Dependence of CG on the body thickness (t_{Si}) for different AC Inputs. CG varies with L_{gate} because of short channel effects.

4.2.4. Structural parameters

Next, we study the dependence of CGs recorded at the various LO AC amplitudes and at optimum DC (lower peak) bias conditions as a function of most significant structural parameters of the DG-MOSFET used for mixing. The results are summarized in Figs. 14a & 14b, which show the dependence of conversion gain with L_{gate}, N_A & t_{Si}. Clearly, the L_{gate} has almost no impact on the conversion gain at higher values while at lower value the impact becomes more pronounced. For N_A, the conversion gain almost remains constant at low doping levels whereas it slightly increases at very high (impractical) doping levels. However, from Fig. 14b we find that t_{Si} is a more significant parameter for conversion gain optimization. In a given gate length there appears to be an optimum body thickness that maximizes the CG. For example, at L_{gate} of 45 nm and 90 nm, the optimum body thickness is 10 nm and 30 nm, respectively. At either extreme of these values, the conversion gate is compromised due to the short channel effects in the higher end and quantum size effects at the lower end. Thus it is important to include both 2D/3D simulations and quantum corrections to optimize mixing performance in such nano-scale transistors, as with the case in this study.

We like to draw attention that the weak dependence of performance on the structural parameters here is a result of careful bias optimization. It also indicates that the choice of bias conditions, particularly the LO DC bias, is the most dominant handle in using DG-MOSFET active mixer. Admittedly, this observation may be counter intuitive, because the short channel effect are well known to adversely impact analog performance of the conventional MOSFETs in sub-100 nm regime. However, these adverse impacts are mostly related to the increase of the non-linearity in g_m which is certainly helpful for a mixer. In any case the well-scaled

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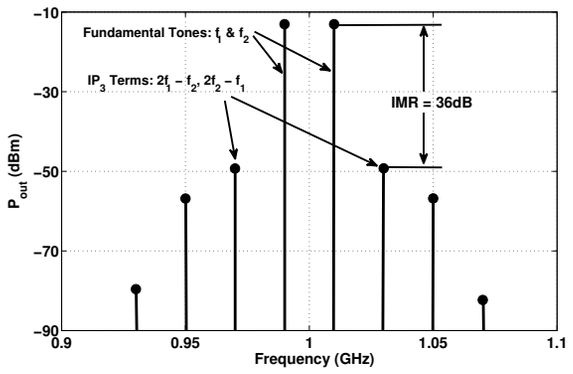

Figure 15. Computation of IP_3 using two tone frequency analysis (0.99 GHz and 1.01 GHz) around 1 GHz. The Intermodulation Ratio (IMR) gives level difference between the fundamental and the IP_3 terms and is used to obtain the $IIP_3 = P_{in}(f_1,f_2) + IMR/2$.

nature of the DG-MOSFET minimizes the emergence of strong short channel effects for the mixer performance.

Moreover, the apparent stability of mixer performance with device geometrical scaling could affect the phase noise in both positive and negative fashion. In terms of inter-device performance variations, the DG-MOSFETs will not suffer as much as the logic applications as the process variations in geometry does not appear to be a worry. However, since the LO-DC bias is the most important figure of merit, variations in threshold among devices and biasing errors/variations in circuits can be the main source of phase noise and limit the performance.

4.2.5. Linearity analysis

Finally, we examine the circuit for linearity implementing the two tone frequency analysis (Fig. 15). The 3rd order Input Intercept point (IIP_3) is found to be 15.9 dBm for 2 dBm LO power, indicating the suitability of the circuit [35].

4.3. Envelope detector

The demodulation of a non-coherent modulated wave requires an envelope detector. The envelope detector is basically a rectifier circuit that generates an envelope of the incoming high frequency carrier signal and strips off the carrier to recover the data.

In Fig. 16a, we have illustrated a 45 nm DG-MOSFET envelope detector circuit in which the output is inverted to that of binary input (Refer Fig. 6). The output signal needs further to be passed through an inverter for the recovery of the original signal. Although requires additional hardware, this circuit has an advantage over the straightforward recovery as the former has a better output swing over the latter [48]. The simulation (Fig. 16b) illustrates the recovered binary input information as same as that is shown in Fig. 6. The high frequency noise present with logic 1 data at the output can be easily filtered out.

4.4. Charge pump Phase Frequency Detector

The Phase Frequency Detector (PFD) is one of the two major components of a PLL, that is used for the demodulation of coherent modulated signal. The other being the local oscillator/VCO. It consists of two D Flip Flops and a reset circuit. The two D Flip Flops are implemented with eight NOR gates (four each) [49]. The reset path consists of another

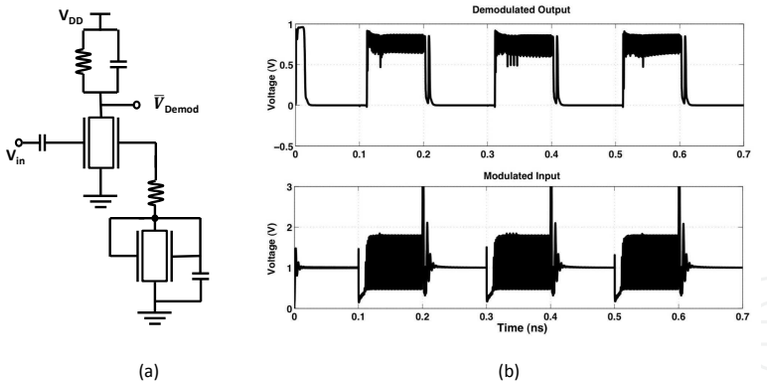

Figure 16. a) Envelope Detector Circuit with only two DG MOSFETs. b) The modulated input consisting of the both the carrier and data; the recovered demodulated output consisting only of data sans the carrier.

NOR gate. Here, each of the NOR gates are constructed with DG-MOSFETs. The circuit also consists of two DG-MOSFET NMOS switches implemented in regular V_T configuration (Fig. 17a).

4.4.1. DG-MOSFET NOR gate

The DG MOSFET NOR gate consists of only two DG transistors instead of four as in conventional CMOS architecture (Fig. 17b). This was first proposed by Chiang et. al [50]. The design employs the threshold-voltage (V_T) difference between double-gated and single-gated modes in a high V_T DG device to reduce the number of transistors by half.

The NOR logic with DG-MOSFETS is shown in Fig. 17c. One of the major advantages of using NOR gates using DG-MOSFETs is speed. The area and capacitance of the DG-MOSFET NOR gate is almost 2x less than the conventional CMOS due to reduced transistor count (half that of conventional CMOS) and associated isolation and wirings which lowers the capacitance and speeds up the circuit. In Fig. 17d we demonstrate this fact for different supply voltages. The advantage in higher speed is crucial for tiny phase error detection in PLL and is the subject of the following section.

4.4.2. Design and analysis

This analysis is carried with a supply of 1 V for $(W/L)_p$ = 4 μm / 45 nm and $(W/L)_n$ = 1 μm / 45 nm. The power consumed by the DG-MOSFET based Charge Pump PFD is 3.4 mW which is 21% less than that of the conventional CMOS under identical device dimensions and parameters. Although the drive current (I_{ON}) for DG-MOSFET is higher for both regular and high V_T configurations than that of a single gate MOSFET, the reduction in the number of transistor counts, reduces the power consumption decently. The area is also reduced almost by half resulting from this reduction.

The phase error between two pulses A and B can be correctly detected for both conventional CMOS and DG-MOSFET when the phase error between the two pulses (T_{pe}) is above a certain threshold. Now from our analysis at the previous section on speed enhancement of DG-MOSFET based NOR architecture we can deduce the rise time of the DG-MOSFET (T_{thDG}) is faster than that for rise time of conventional CMOS (T_{thSG}) to reach the desired threshold of logic 'HIGH' and thus we can write $T_{thDG} < T_{thSG}$. However, for low phase

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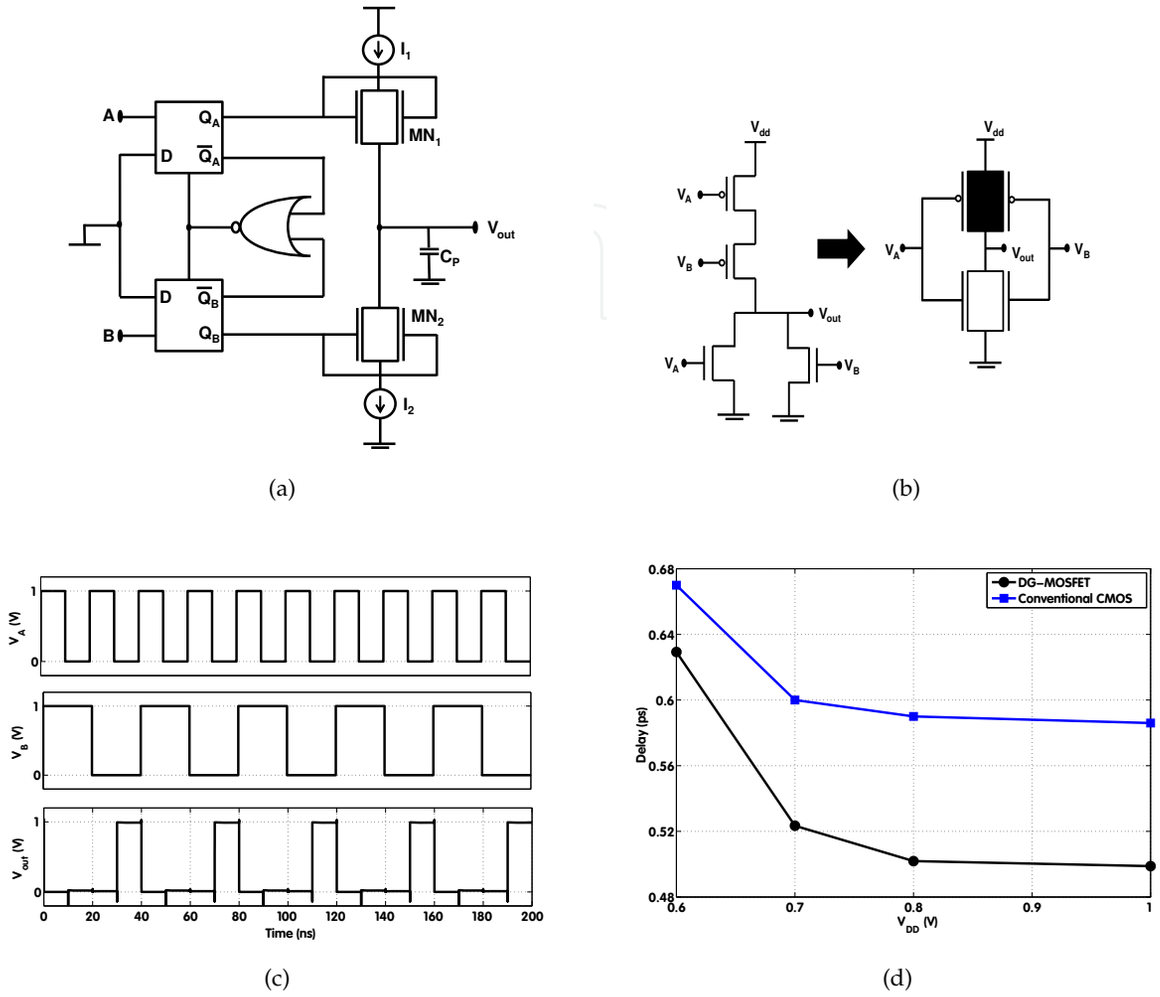

Figure 17. a) The Charge Pump PFD circuit implemented with DG-MOSFETs. b) 2-Input NOR Logic Gate in Conventional CMOS and its equivalent in DG-MOSFET. Two transistors are required in the DG-MOSFET. The PMOS in DG-MOSFET is kept at a high-V_T symbolized by a filled transistor. c) 2-Input DG-MOSFET NOR Logic simulated waveform for V_{DD} = 1 V. d) Delay comparison of 2-input NOR gate between conventional CMOS and DG-MOSFET for different supply voltages.

error applications, when $T_{thDG} \leq T_{pe} \leq T_{thSG}$, the PFD ceases to work correctly for the conventional CMOS. As observed from Fig. 18, for $T_{pe} = 80$ ps, the voltage at the output Q_A of the flip flop fails to reach the threshold to switch on the transistor MN_1 in the period when A is 'HIGH' and B is 'LOW'. The voltage *only* reaches the threshold when both A and B are HIGH. When B is high the voltage at Q_B also reaches 'HIGH' which turns the transistor MN_2 'ON'. Therefore, when both Q_A and Q_B are 'HIGH' (reaches the V_T) simultaneously, the current I_1 instead of charging the capacitor C_P passes through the switch MN_2. Thus the output voltage (V_{out}) remains nearly constant and changes only by a fraction of what should be in order to send the accurate message of phase error to the VCO, which follows the PFD in a PLL architecture. As a matter of fact, the V_{out} changes only by a meagre 0.005 mV for 100 ns. This is negligible and an incorrect feedback to the VCO. The V_{out} characteristics is verified from Fig. 19. This is the familiar dead zone condition where there is no or negligible charge pump current that contributes to no change in V_{out}.

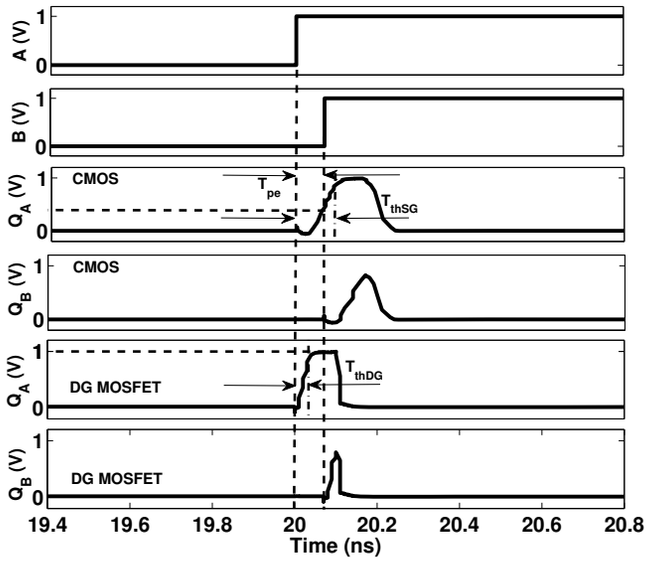

Figure 18. Phase error characteristics of two pulses A & B for conventional CMOS and DG-MOSFET for a phase error of 80 ps.

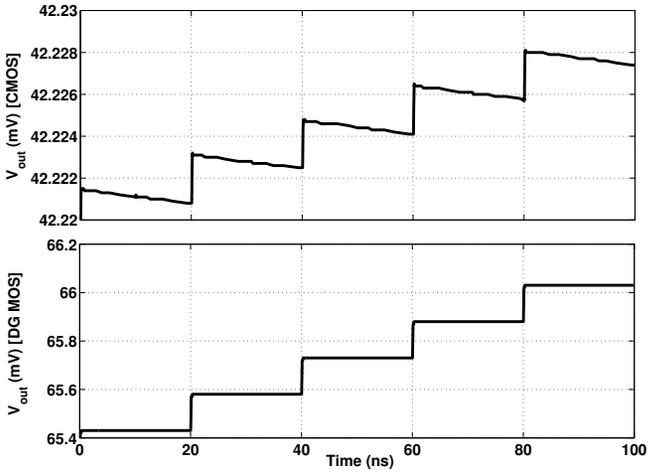

Figure 19. Charge Pump output voltage characteristics of Conventional CMOS and DG-MOSFET when $T_{thDG} \leq T_{pe} \leq T_{thSG}$

On the other hand, the advantage of DG-MOSFET is clearly evident from Fig. 18 where it can be confirmed that for the same period the threshold for the DG-MOSFET reaches the logic 'HIGH' when A is 'HIGH' and B is 'LOW'. Thus the current I_1 cannot escape through MN_2 and charges C_P instead. This is clearly because even when $T_{pe} \leq T_{thSG}$, the inequality $T_{pe} \geq T_{thDG}$, is still valid due to the fact that $T_{thDG} < T_{thSG}$ owing to the lower capacitance as discussed in the previous section. Thus the dead zone is avoided with the correct and significant change of 0.6 mV in V_{out} for the same duration as that of conventional CMOS (Fig. 19).

5. Summary and future prospects

The chapter has provided examples for unique and significant performance improvements available via a novel transistor architecture (FinFET or DG-MOSFET) in a wide collection of analog and mixed-signal circuits that can be used in today's integrated wireless communication, satellite navigation systems and sensor networks, verified through industry

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standard SPICE simulations. In particular, the chapter documents the tunable frequency response in relaxation and LC oscillators along with the gain tuning in wide-band PA and the LNA circuits. In all these cases, the performance improvements and tunable characteristics can be achieved via the availability of independently biased second gates in these new device architectures. In addition to gain tuning, the PA and the LNA performance parameters such as gain, bandwidth, linearity, NF are either comparable or better than some of the recent designs in conventional CMOS or III-V technologies. The fact that DG-MOSFET circuits utilize reduced transistor count compared to single gate CMOS is exemplified by relaxation oscillator, RF Mixer, OOK Modulator, Envelope Detector and Charge Pump PFD circuits. As obvious, the reduced transistor count aids in reducing area and may lower power dissipation. The biasing optimization technique of the RF Mixer described here maximizes the conversion gain of the RF Mixer with power efficiency. The DG-MOSFET Charge Pump PFD circuit avoids dead zone in PLL for low phase difference applications which is not possible in conventional CMOS as demonstrated here. The primary reason for this is reduced delay because of reduced area which in turn is achieved as a result of reduced transistor count.

With fabrication processes of DG-MOSFETs soon coming up with initiation from TSMC and rapidly expanding system-level efforts led by several national and international programs in US, Japan and Europe, along with several companies (such as Intel [4]) and academic centers focussing on these DG-MOSFET/FinFET/3DMOSFET technologies, we should expect a wide range of tunable analog RF circuits, reconfigurable logic blocks, on-chip power management blocks and mixed-signal system-on-chip applications to come into existence in the next few years.

Ultimately, with the ongoing nanotechnology revolution further performance improvements and architectural changes in devices are to be expected in the next decade and beyond. Our work here shows that such changes can be utilized by circuit engineering to result in very compact and capable systems, even when the actual change is to include merely an additional gate in the MOSFET architecture. This indicates that circuit engineering has a lot more to say not only in the final stretch of Moore's scaling, extending perhaps until 2020, but also in post-Moore area where fundamental fabric of building circuits may be altered significantly, and novel devices architectures and materials such as graphene, carbon nanotube, nanowire or molecular transistors are likely to play a significant role.

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