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Chapter 10

Tailoring Oxide/Silicon Carbide Interfaces: NO Annealing and Beyond

John Rozen

Additional information is available at the end of the chapter

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1. Introduction

We live in an energy-hungry world in which industrialization and globalization have accelerated the demand for resources that now doubles approximately every 40 years. Today, we consume about 18 TW (18×10^{12} Watts) which is equivalent to 97 billion barrels of crude oil yearly. While renewable energy sources offer an environmentally conscious alternative to fossil fuels, they account for only about 10% of this total [64]. In parallel to the advent of clean energy, an effort has to be made to curb consumption, which can in part be achieved by improving system efficiency. In this Section, we will discuss in such terms why high-volume sectors such as transportation, electricity generation, and distribution, can benefit from SiC-based electronics.

First, it should be recognized that the adoption of a new technology will be driven mainly by component cost and end-user benefits. Silicon carbide electronics is no exception and only makes sense if it can deliver on these fronts. A good example is the recent introduction of the pricier fluorescent light sources which make financial sense in the long term since they consume a fraction of the energy of incandescent bulbs and last some 20 times longer, proving that efficiency and reliability can justify the investment. So what are the key parameters that influence SiC device cost and efficiency?

Cost - Substrate size and availability have benefited from the boom in LED demand as III-nitride blue diodes can be fabricated on SiC. Indeed, the diameter of commercially available substrates has steadily increased from the release of two inch (50 mm) wafers in September 1997 to the recent unveiling of six inch (150 mm) wafers in August 2012 by Cree, inc., a very fast pace compared to Si evolution [100]. Also, tremendous quality improvements have been achieved together with increased process rate and uniformity. One of the many challenges facing SiC production has been the reduction of extended defects such as micropipes [29, 49]. Today, substrates are virtually free of such defects, optimizing device

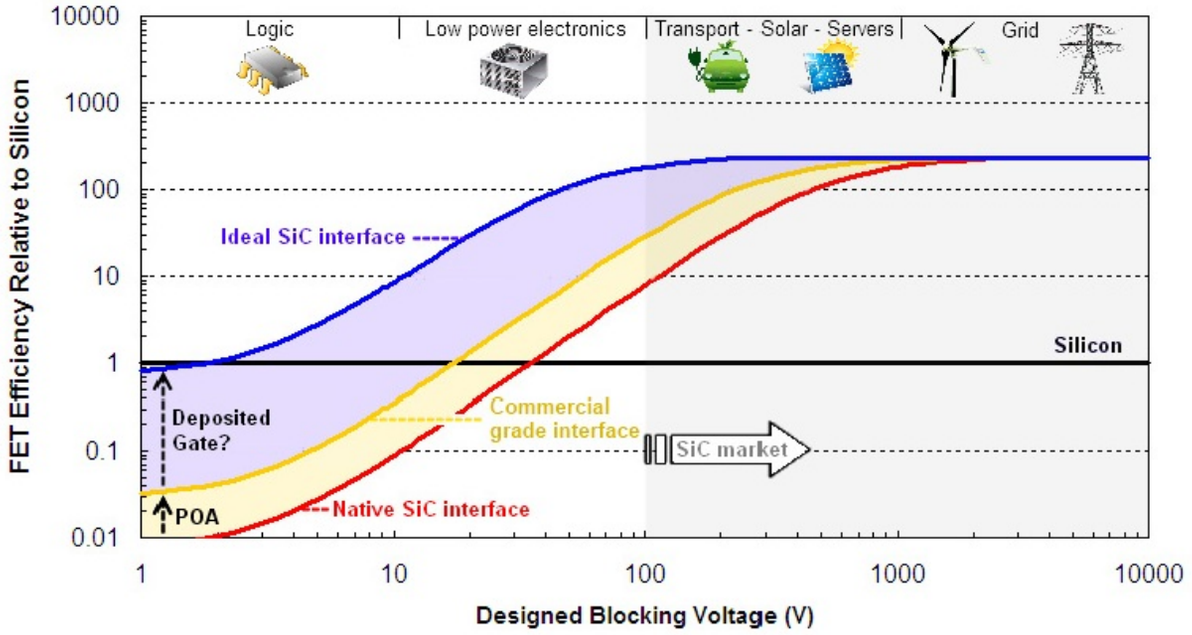

Figure 1. DC efficiency of SiC-based FETs relative to Si devices at given designed blocking voltages. While commercially available switches using NO-annealed thermal gate oxides have improved efficiency, one suggested route is the use of deposited oxides to achieve optimum properties [109].

yield. Demand and production costs have thus progressively driven down the price of the material, which has translated into cheaper and higher quality components for optoelectronic and high power applications.

Efficiency - While investment costs have diminished, SiC-based devices are still more expensive than their Si counterparts. Their efficiency is what can make them attractive in the long run. As illustrated in Fig. 1, the energy consumption of metal-oxide field-effect transistors (MOSFETs) can be orders of magnitude lower when using silicon carbide as a substrate to control high blocking voltages. Industries that would benefit from the widespread of such components include transportation, electricity distribution, grid coupling, high-performance computing, etc. Indeed, automakers have invested heavily in SiC research, targeting the implementation of SiC-based inverters in hybrid vehicles. To get an idea of how single device consumption will translate into system efficiency, let's take the example of photovoltaic (PV) power converters. PV inverters are used to convert the DC current from solar sources to feed it to the AC grid. They are made of power diodes and switches. A typical residential system has a nominal power of 5 kW at 400 V AC. Such Si-based converters can operate at over 95% efficiency but replacing Si components by commercially available SiC Schottky diodes and power MOSFETs can cut the loss by about 50%, yielding a saving of the order of $100 a year per household [22, 23]. Moreover, they can operate at higher temperature, so that limited cooling and volume requirements go in favor of system prices which can indeed prove beneficial over the years for the consumer choosing to adopt the new technology.

Further improvements in SiC device efficiency will make the case even stronger. Among the key building blocks at the device level is the oxide/semiconductor interface. Figure 1 highlights how it affects consumption, especially at low biases. In this Chapter, we will derive important parameters defining SiC devices from physical properties, and discuss the role and formation of the oxide/semiconductor interface, covering thermal oxides, post-oxidation annealing, and deposited dielectrics.

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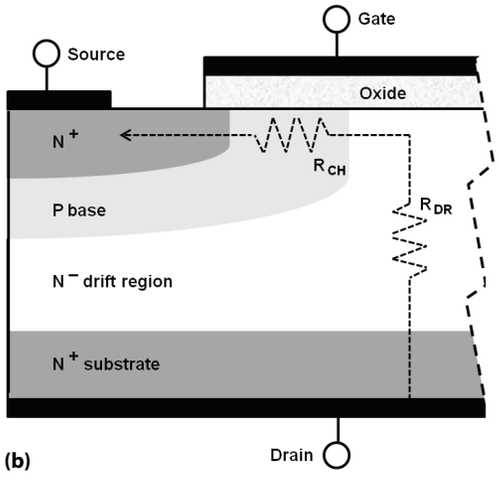
2. Breakdown field and device efficiency

Let us compare vertical double-implanted MOSFETs (DMOSFETs) designed to control the same bias, one Si-based, the other SiC-based, as shown in Fig. 2(b), using the constants of Fig. 2(a). The key differences between the two materials can be traced back to the Si-Si bond and the Si-C bond, respectively. The stronger interaction between silicon and carbon atoms is evidenced by the shorter bond length of 1.89 Å when compared to 2.35 Å for Si-Si. The proximity of atoms in SiC yield a more pronounced splitting of bonding and antibonding levels, which translates into a wider band gap in the periodic crystalline structures. The diatomic base of silicon carbide also explains the better thermal conductivity of the material because its vibration modes, i.e. phonons, are more energetic on average, as reflected in the Debye temperature. Ultimately, it is the phonon distribution that explains the higher critical field of silicon carbide, ξ_c, that can be used to derive a key parameter impacting device efficiency in high power electronics, the drift component of the specific ON resistance.

The breakdown field of a material is indeed not directly related to its band gap E_g. While, to first order, the free carriers need to reach a kinetic energy of at least $3/2\ E_g$ to induce the cascading impact ionization phenomenon, called avalanche, that multiplies the number of carriers and therefore the conductivity, the limiting factor in the bulk is phonon coupling [84, 86]. If the net velocity of carriers $\bar{v}$, proportional to the current, is smaller than or equal to the thermal velocity $v_{th} = \sqrt{3k_bT/m^*}$, the electron-phonon system is in equilibrium because of the ability of phonons to thermalize the carriers. In that regime, phonon scattering damps the energy gain of free carriers whose distribution in the bands can be visualized as a Fermi sphere slightly shifted in the direction of the electric field. However, if the field increases and reaches ξ_c, the rate at which carriers gain energy becomes too high to allow equilibrium with the lattice vibrations. Hot carriers then achieve phonon runaway. Their motion is no longer damped and they can accelerate freely from v_{th} to the critical speed $v_c \approx \sqrt{3E_g/m^*}$ allowing the avalanche process to start. It is worth noting here that in thin films, an additional constraint comes from the time the carriers take to accelerate to v_c, so that ξ_c can become larger than the bulk value, as illustrated in Fig. 3(a).

Constant	4H-SiC	Silicon
$Bandgap\ E_g\ (eV)$	3.26	1.12
$e^-\ mobility\ \mu_e\ (cm^2/V.s)$	1000	1400
$e^-\ effective\ mass\ (m^*/m_0)$	0.36	0.26
$Critical\ field\ \xi_c\ (MV/cm)$	2.2	0.3
$Dielectric\ constant\ (\epsilon/\epsilon_0)$	9.7	11.7
$Debye\ temperature\ T_d\ (K)$	1300	640
$Th.\ conductivity\ \theta\ (W/cm.K)$	3.7	1.5

(a)



(b)

Figure 2. (a) Properties of 4H-SiC and Si with 10^{15}-10^{16} cm^{-2} doping at 300 K [30, 65, 66, 84, 121]. (b) Vertical power DMOSFET.

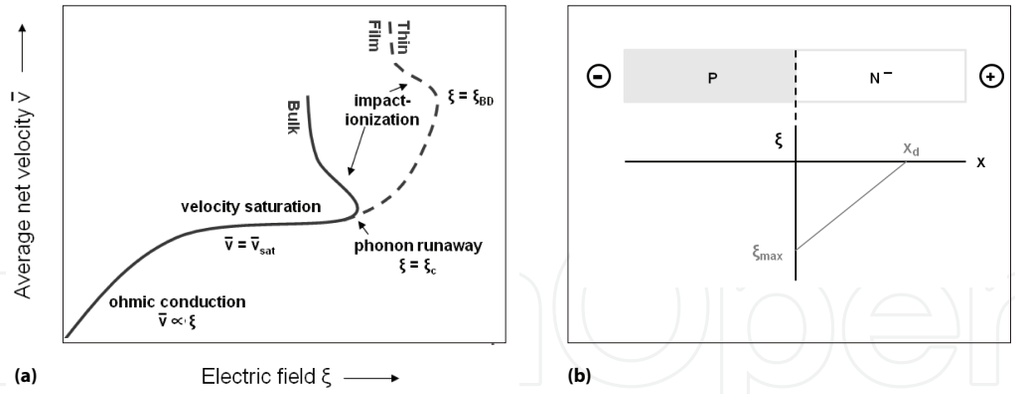


Figure 3. (a) Hot carrier velocity saturation and dielectric breakdown [105]. (b) Field distribution in a one-sided reverse-biased PN junction.

The critical field ξ_c of a semiconductor, can be used to design the most efficient device for a given blocking voltage V_d. When a DMOSFET is in the OFF state, the positive bias applied to the drain is entirely dropped in the N^- drift region [84, 124]. Indeed, together with the P base, it forms a reverse-biased one-sided PN junction, represented in Fig. 3(b). For a large blocking voltage, $V_d \gg E_g/q$, the extent of the depletion region on the lowly-doped side in the step-junction approximation is

$$x_d = \sqrt{\frac{2\epsilon_s V_d}{qN_d}} \tag{1}$$

where N_d is the density of donor atoms in the drift region, ϵ_s is the permittivity of the semiconductor, and q is the elementary charge. The peak electric field, at the boundary, being

$$\xi_{max} = 2\frac{V_d}{x_d} = \sqrt{\frac{2qN_d V_d}{\epsilon_s}} \tag{2}$$

The highest doping concentration that can sustain V_d is therefore

$$N_d^* = \xi_c^2 \frac{\epsilon_s}{2qV_d} \tag{3}$$

obtained by substituting for the critical field in Eq. (2). Then, from Eqs. (1) & (3), the minimum thickness of the drift region is given by

$$x_d^* = 2\frac{V_d}{\xi_c} \tag{4}$$

Accordingly, the drift region of a 4H-SiC DMOSFET can be substantially thinner and more highly doped than a Si-based device designed to control the same bias. Neglecting the current spread [9], the ratio of the optimal ON resistance components from the drift region can thus be estimated by

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$$\frac{R^*_{dr}\,|_{SiC}}{R^*_{dr}\,|_{Si}} = \left.\frac{N^*_d\,\mu_{dr}}{x^*_d}\right|_{Si} \left.\frac{x^*_d}{N^*_d\,\mu_{dr}}\right|_{SiC} = \frac{\mu_{dr}\,\epsilon_s\,\xi_c^3\,|_{Si}}{\mu_{dr}\,\epsilon_s\,\xi_c^3\,|_{SiC}} \tag{5}$$

where μ_{dr} is the drift mobility in the bulk of the semiconductor. Plugging the respective constants of the bulk semiconductors into Eq. (5) implies that in ideal devices the energy dissipated using 4H-SiC would be several hundred times lower compared to the Si equivalent for a given ON current [15].

In a real device, however, there are other components to the resistance such as the contact resistance and the channel resistance. Here we will discuss only the channel specific resistance which contains the contribution from the oxide/semiconductor interface of interest in this Chapter. It can be calculated using the long channel approximation as

$$R_{ch} = \frac{V_d}{I_{sat}}\,P^2 = \frac{LP}{nq\mu_{ch}} \tag{6}$$

where L is the channel length, P is the channel width, or the square cell pitch, μ_{ch} is the inversion mobility, and n is the minority carrier density [9]. The total specific ON resistance is then

$$R_{tot} = R^*_{dr} + R_{ch} = \frac{x^*_d}{N^*_d\,q\mu_{dr}} + \frac{LP}{nq\mu_{ch}} \tag{7}$$

which has the following dependence on designed blocking voltage according to Eqs. (3) & (4)

$$R_{tot} = \frac{4V_d^2}{\mu_{dr}\epsilon_s\xi_c^3} + \frac{LP}{nq\mu_{ch}} \tag{8}$$

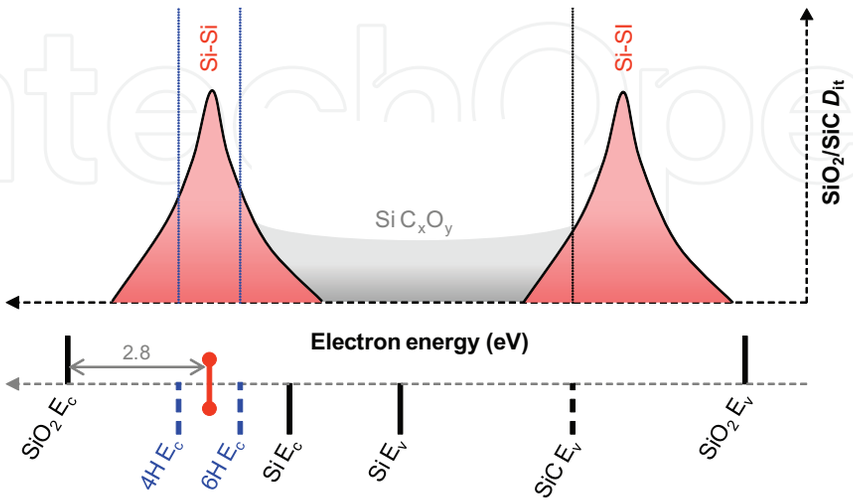

Figure 4. Schematic of the density of interface traps at the SiO_2/SiC interface.

From Eqs. (7) & (8), it can be seen that the smaller the designed blocking voltage, the smaller the width of the necessary drift region, and the larger the contribution from the channel resistance. In Si, that does not have a major impact in power devices because μ_{ch} can be as high as 50% of the bulk value μ_{dr}. However, SiC channels suffer from a mobility that can be less than 1% of μ_{dr} at the native SiO_2/4H-SiC interface. Therefore, interface quality can affect performance even in the kV range and the full potential of the SiC material cannot be reached. This is highlighted in Fig. 1, where the ratio of ON resistances was calculated using Fig. 2(a) constants, $L = 1\mu m$, $P = 10\mu m$, $n = 10^{15}$ cm^{-2}, and the following SiC μ_{ch}: 5, 50, and 500 cm^2/V.s. The significance of those mobility values are discussed in the next Sections.

3. Channel mobility and interface state density

Mobility is a measure of the ease a carrier can be moved in a solid under the application of an electric field ξ. It can be related to the speed of the carrier which is limited by scattering events occurring at average time intervals τ. Several types of scattering processes affect transport but the ones yielding the most frequent disturbances define the mobility value which can be written explicitly as

$$\frac{1}{\mu} = \frac{\xi}{\bar{v}} = \frac{m^*}{q} \sum_i \frac{1}{\tau_i} \tag{9}$$

where m^* is the effective mass, $\bar{v}$ is the net drift velocity, and τ_i corresponds to mean scattering times associated with various processes.

Because of the sudden termination of the semiconductor periodic lattice at the oxide interface, the channel mobility, μ_{ch}, is expected to be lower than the bulk mobility. Indeed, electrically active levels can appear in the band gap and act as recombination centers or Coulomb scattering centers. Moreover, the free carriers can interact remotely with charged border states in the oxide, further reducing τ_{Cb}. Other major damping mechanisms include surface-phonon and surface-roughness scattering represented by τ_{ph} and τ_{sr}, respectively. We note that the coupling of carriers to scattering effects depends strongly on their velocity such that Coulomb scattering dominates at low fields, while surface roughness scattering becomes dominant at higher fields. Because of these interface phenomena, the best SiO_2/Si devices display a channel mobility of about 700 cm^2/V.s, equivalent to 50% of the bulk mobility [78]. In the case of 4H-SiC however, the native oxide interface yields mobilities of about 5 cm^2/V.s, or less than 1% of the bulk value. So why is SiC so affected by the formation of a thermally grown interface? Let us discuss it from the point of view of Coulomb scattering, so that the question becomes: why is the density of interface traps (D_{it}) so much more prominent in SiC?

First, a down side of having a wider band gap is that it is sensitive to a wider range of defects. To first order, only the corresponding levels falling inside the band gap can be charged and yield Coulomb scattering. Since there is no evidence that SiO_2 formed on SiC is any different from thermally oxidized silicon [99], it can contain the same type of defects, some having energy levels affecting only SiC carriers. Let's take the example of the oxygen vacancy, detected by electron spin resonance (ESR) in both systems, which yields Si-Si bonds [75, 106]. The energy split of that dimer is inversely proportional to the proximity between

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atoms. Long Si-Si bonds, i.e. bigger than 2.35 Å, can have energy levels inside both the Si and SiC gaps. But the splitting between short Si-Si levels can be outside the silicon gap while being electrically active at a SiO_2/SiC interface [90, 130], as illustrated in Fig. 4. The same analysis is true when comparing defect levels in the 6H- and 4H-SiC polytypes which have energy gaps of 3 and 3.3 eV, respectively. Because their valence bands are lined up, the conduction band of 4H-SiC is 0.3 eV higher. This is why the major defect affecting 4H-SiC, located 0.1 eV below its conduction band, has a limited impact on 6H-SiC devices [114]. It is interesting to note that this defect corresponds to an energy of 0.4 eV above the Si conduction band and that a similar trap level has been observed in SiO_2 on Si even though it does not limit channel mobility [3, 4, 8].

The second reason explaining the large defect density at SiC interfaces is the oxidation process

$$2\,SiC\,+\,3\,O_2\,\rightarrow\,2\,SiO_2\,+\,2\,CO \tag{10}$$

Like silicon oxidation, it follows the Deal-Grove reaction-diffusion model, so that the thermal oxide thickness as a function of time can be written as

$$x[t]\,=\,-\frac{1}{2}\frac{B}{B/A}+\frac{B}{2}\sqrt{\frac{1}{(B/A)^2}+\frac{4(t+t_0)}{B}} \tag{11}$$

where B/A is the linear rate constant, B is the parabolic rate constant, and t_0 is an offset time constant [45]. For details on SiC oxidation kinetics and parameters corresponding to various orientations, pressures, and temperatures, see Refs. [43, 68, 98, 113, 122, 127, 135, 136]. But unlike Si oxidation, Eq. (10) implies the release of carbon. Because of this complex multi-step process, a variety of atomic defects involving C can result from oxide formation if CO molecules do not all find their way to the gas phase. [48, 71, 90]

Now that we have reviewed the impact and origin of defects at the SiO_2/SiC interface, a comprehensive picture of associated trap levels limiting inversion mobility can be put forward, as shown in Fig. 4. Thermal oxidation of silicon carbide results in a SiC_xO_y inter-layer that includes threefold and fourfold coordinated Si and C atoms [8, 44, 90, 130]. Some generate dangling bonds whose energy spreads across the band gap because it is determined by the environment surrounding the defects. Another stable configuration yielding a trap level in the gap is a split C interstitial. When substituting for a Si site in the semiconductor, it can be viewed as a small C-aggregate or "C-cluster" comprising 6 atoms. A carbon-rich interface has indeed been observed by techniques such as Rutherford backscattering (RBS) [46, 57, 89, 97], x-ray photoelectron spectroscopy (XPS) [54, 62, 67, 77, 128], electron energy-loss spectroscopy (EELS) [33–35], Raman spectroscopy [80], and in-situ spectroscopic ellipsometry [63]. The dominant defects however, are likely oxide-related. Indeed, Si-Si bonds of various lengths can extend into SiO_2 yielding interface and border traps [6, 17, 50, 72, 92, 112]. As mentioned before, the majority of corresponding bonding and antibonding states are located outside of the silicon gap but the former induce a distribution centered between the 4H and 6H-SiC conduction bands. The slightly smaller density of levels at lower energies is probably due to the majority of antibonding levels residing within the valence band of SiC whose edge is common in different polytypes [1]. The combination of trap levels associated with the SiC_xO_y inter-layer and Si-Si bonds, yields

the U-shaped D_{it} distribution. It rises sharply towards the SiC band edges because of the Si-related defects not dominant at silicon interfaces. Therefore, the efficiency of passivation techniques are expected to be very different at interfaces formed on the two semiconductors.

In the following Sections, we will discuss how to reduce D_{it} and its relationship with mobility. Although there is extensive literature dedicated to various orientations and polytypes, this overview is dedicated to devices fabricated on the (0001) Si-face of 4H-SiC.

4. Argon anneal

Oxidation conditions and post-oxidation annealing (POA) can affect the trap density at the SiO_2/4H-SiC interface. Both Ar anneal performed at growth temperature and re-oxidation at lower temperatures (e.g. 900 °C) have indeed proven to slightly reduce the amount of deep states [40, 129]. This can be explained by the removal of excess carbon without additional oxide formation, as corresponding atomic configurations yield defects populating interface states toward the middle of the gap. Since it does not reduce the density of levels close to the conduction band edge of 4H-SiC, Ar POA alone is not sufficient to enable efficient SiC devices. Nevertheless, it is typically used after thermal oxidation and before other annealing schemes.

5. Hydrogen passivation

Wet oxidation of 4H-SiC also yields a small reduction of interface states with energies away from the semiconductor band edges when compared to SiO_2 formation in dry oxygen [2, 26, 55, 90, 130]. It correlates well with the effects of H_2 POA. While at silicon interfaces hydrogen annealing yields a D_{it} from about 10^{11} to 10^{10} $cm^{-2}eV^{-1}$ in the middle of the gap and a mobility close to half the one of the bulk [20, 21], its impact at SiC interfaces is much less efficient, highlighting the differences between the two semiconductors [27, 58, 96]. Molecular hydrogen can indeed passivate Si- or C- dangling bonds, and insert long Si-Si bonds [28]. But it does not significantly affect split carbon interstitials and slow near interface states which populate the majority of the D_{it} at the 4H-SiC band edges. Like Ar annealing, wet oxidation and/or H_2 POA can be used together with other annealing techniques to optimize the trap density throughout the semiconductor band gap.

6. Nitridation

6.1. NO annealing

In 1997, the group of Prof. Dimitrijev, at Griffitth University in Australia, demonstrated that high temperature (1100 °C) nitric oxide (NO) annealing reduces the D_{it} at SiO_2/6H-SiC interfaces [76]. In 2000, Chung *et al.* published results on the effects of NO at the SiO_2/4H-SiC interface revealing that, in addition to removing deep states, it is also very efficient at reducing the density of slow states (by a factor of ≈ 10), and yields an order of magnitude increase in the channel mobility from about 5 to 50 cm^2/V.s along the Si-face [40, 41]. This breakthrough discovery, which originated from the joint effort between Auburn University and Vanderbilt University, led to the adoption of the NO process by the scientific and industrial communities as it enables the fabrication of high-quality oxide-based SiC power devices, facilitating their commercial release (Fig. 1).

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The benefits of NO annealing have been directly correlated with the incorporation of nitrogen, which is confined to the SiO_2/SiC interface, as detected by various techniques such as secondary ion mass spectroscopy (SIMS) [82, 106], nuclear reaction analysis (NRA) [81], electron energy loss spectroscopy (EELS) [33], and medium energy ion scattering (MEIS) [47, 137]. To study the impact of nitrogen, the amount incorporated can be tailored by the NO annealing time as illustrated in Fig. 5(a). The N density is then extracted by integrating SIMS interface peaks resulting from 1175 °C NO exposure of a dry thermal oxide for up to 2 hours. The nitrogen content is found to saturate around 6×10^{14} cm^{-2} or about a half monolayer coverage of the SiC surface. The nitridation kinetics result from a balance between N incorporation and removal. Indeed, at this temperature, NO decomposes partially into N_2 and O_2. While 1175 °C is required to enable NO diffusion to the interface and subsequent nitridation, the presence of oxygen limits its effect as interfacial nitrogen is unstable against the slow re-oxidation occurring in parallel [37]. Moreover, additional defect formation can also result from the presence of the excess oxygen.

Progressive reduction of the D_{it} across the 4H-SiC band gap corresponding to the tailored introduction of nitrogen has been measured in metal-oxide-semiconductor capacitors (MOSCAPs), as shown in Fig. 5(b). The density of states shows a strong correlation to the nitrogen content and is reduced by up to an order of magnitude close to the conduction band edge [82, 106, 108]. The sensitivity of the inversion mobility of electrons to the D_{it} reduction was studied in lateral field-effect transistors containing different amounts of nitrogen at the SiO_2/4H-SiC interface. From the results depicted in Figs. 6(a) & 10, the peak field-effect mobility is found to be inversely proportional to the density of charged states, which reveals a Coulomb-scattering-limited transport. It is important to note that this is true even in devices with the lowest D_{it} so that further defect passivation is projected to increase the mobility from 50 to more than 100 cm^2/V.s, which cannot be achieved by NO POA alone as nitrogen density becomes saturated. These conclusions are in agreement with separate mobility studies using Hall effect measurements on nitrided samples [13, 114, 125]. Such experiments also reveal that at higher fields, mobility becomes limited by surface-roughness scattering. Although NO POA has been shown to yield smoother interfaces [51], it is not clear what else can be done to further reduce that particular component.

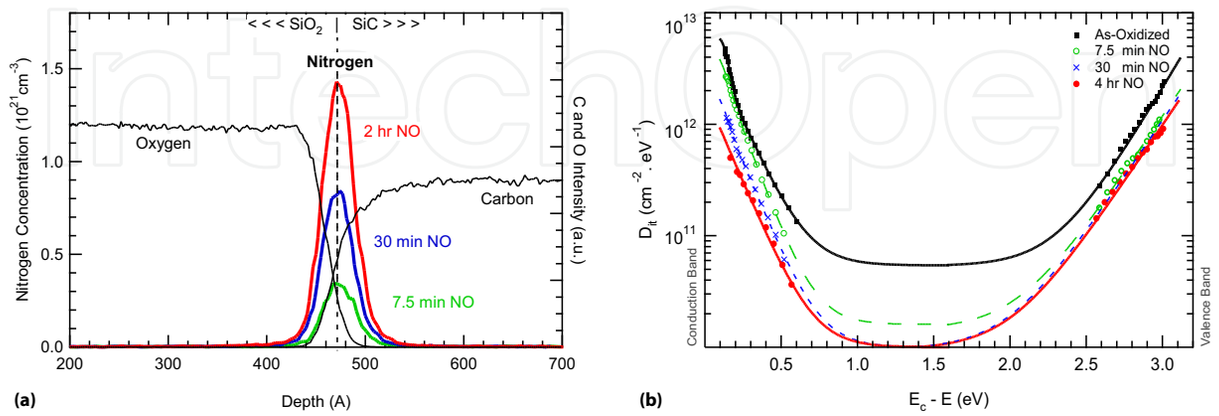

Figure 5. (a) SIMS Nitrogen profiles showing progressive accumulation at the SiO_2/SiC interface with increasing NO annealing time. Adapted from Ref. [106]. (b) Density of interface traps across the 4H-SiC band gap. Longer NO anneals yield lower D_{it}. Reproduced with permission from Ref. [108].©2011 IEEE

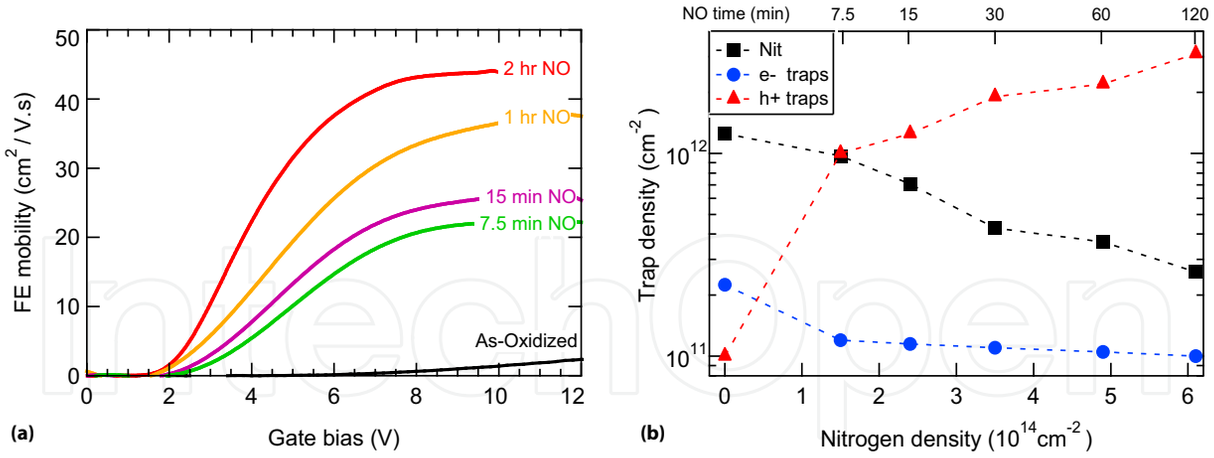

Figure 6. (a) Field-effect mobility extracted from lateral n-channel MOSFETs on 4H-SiC fabricated using different N doses. Reproduced with permission from Ref. [107]. ©2010 TTP (b) Dependence of integrated interface trap density (N_{it}), electron-generated levels, and positive oxide traps, on N content. Reproduced with permission from Ref. [107]. ©2010 TTP

The benefits of nitrogen incorporation also extend to the reliability of SiC devices when it comes to electron injection in the gate oxide, which is inherent to n-channel transistor operation, as the dielectric is exposed to leakage currents and charge tunneling from the inversion layer towards the biased gate contact [31, 32, 52, 73, 132]. While the resulting degradation can take a long time to develop under normal operation, accelerated techniques can be used to study device response to excess carriers penetrating the gate structure. To best simulate actual bias conditions, electrons were injected at low oxide fields (< 2 MV/cm) using a mercury lamp promoting carriers from the negatively-biased gate metal to the conduction band of 4H-SiC in MOSCAPs fabricated using dry oxidation followed by various NO annealing times [103, 106]. As shown in Fig. 7(a), the density of trapped negative charge, extracted from the flatband voltage shift of capacitance-voltage (CV) curves, can be plotted as a function of the integrated gate current, i.e. the injected electron density. If no nitrogen is present at the oxide/semiconductor interface, device characteristics continuously drift towards positive voltages. From the observation of hysteresis behavior of CV curves, this has been correlated to electron-induced acceptor state generation at the interface [5]. However, the presence of even the smallest amount of nitrogen can suppress the degradation, exposing the secondary component of the negative charge, the bulk electron traps in SiO_2 [103], Fig. 6(b).

When it comes to positive charge trapping however, the presence of nitrogen proves to be detrimental to device stability [73, 74]. This can be of concern even for n-channel transistors to which a negative gate bias can be applied to ensure that it is OFF in its idle state. Several methods have been used to accelerate hole exposure of the gate oxide such as x-ray irradiation [52], Fowler-Nordheim tunneling, and internal photoemission [104]. Figs. 6(b) & 7(b) show the positive trapped charge as a function of the injected hole carrier density using such a technique with samples containing different amount of nitrogen. There is a clear correlation between nitrogen content and oxide trap density. Because the nitrogen is contained at the interface and the charge is stable against bias reversal, it is attributed to near-interface traps in the SiON layer. ESR experiments have ruled out oxygen vacancies as the main positive trap in the oxide, another indication that atomic configurations involving

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nitrogen must be at play [106]. In fact, similar conclusions have been drawn from N-induced negative bias temperature instability (NBTI) on silicon which has been attributed to Si-N bonds [24, 25], which also suggests that the defects must originate from the SiO_2 conversion into a nitride.

From the impact of nitrogen incorporation on D_{it}, electron traps, and hole traps, summarized in Fig. 6(b), it is possible to paint a picture of what happens at the atomic level. First, it is important to note that although the term "passivation" is often used to describe the effects of nitrogen, the large density introduced by the NO process more likely yields a complete reconfiguration of the interface from SiO/SiC to SiON/SiC. But for simplicity, let us look at the effect of nitrogen on single defects. As mentioned previously, the majority of traps at the thermally grown interface are considered to be single and split carbon interstitials, as well as Si-Si bonds. Unlike hydrogen, nitrogen can reduce the energy of most of these atomic configurations by substituting for threefold-coordinated carbons or by inserting short suboxide bonds [90, 130]. While it can suppress acceptor levels close to the 4H-SiC conduction band edge, the donor nature of nitrogen and its 5 valence electrons can then yield states close to, or even within, the semiconductor valence band [104]. If the resulting atomic configurations are located on the oxide side of the interface, they can therefore act as stable hole traps. Let us take the example of a short Si-Si suboxide bond expected to have an unoccupied state close to the 4H-SiC conduction band. When inserted by NO, it yields a Si-NO-Si bridge and moves the trap level close the valence band. Theory suggests that the nitrogen lone electron pair leads to a partially occupied state that is a favorable hole trap, since giving away an electron makes the atomic configuration reduce its energy by a few eV. As mentioned earlier, nitrogen might not discriminate between defects and stoichiometric oxide sites as it indeed converts SiO to SiON. Therefore, the same configuration could result from N insertion in bridging Si-O-Si, which can create trap levels where there was none before.

In summary, the presence of nitrogen at the oxide/semiconductor interface is beneficial as it reduces D_{it}, increases mobility, and suppresses electron-induced interface state generation. But on the other hand, re-oxidation during NO POA limits the amount of N that can be inserted, and nitrogen generates a quantity of new traps by bonding in the near-interface

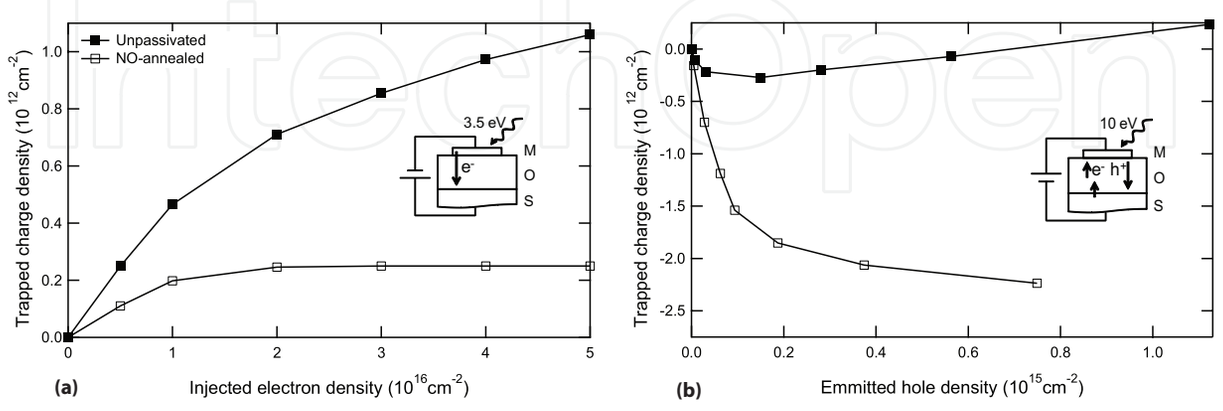

Figure 7. Effective trapped charge as a function of (a) injected electron density and (b) emitted hole density by internal photoemission. NO POA suppresses electron-induced interface state generation but increases the amount of hole traps in the oxide. Adapted from Refs. [103, 104]

region of the oxide. Since we have shown that more nitrogen would increase the mobility even further, other nitridation methods could maximize its density while confining it to the interface boundary.

6.2. N_2O and NH_3

Ammonia (NH_3) POA shows benefits as well in terms of D_{it} reduction close to the conduction band edge of 4H-SiC [39, 53, 133]. However, it yields unnecessary incorporation of nitrogen throughout the oxide, totalling a density ~ 100 times larger than NO POA. This compromises the integrity and reliability of the gate dielectric, as evidenced by the lowering of the breakdown voltage.

Nitrous oxide (N_2O) oxidation or POA also improves the properties of the oxide/semiconductor interface, but to a lesser extent than NO [12, 37, 70, 76, 81]. This is because it decomposes at high temperature into NO, O_2, and N_2. While the resulting NO incorporates nitrogen at the 4H-SiC/SiO_2 interface, the larger fraction of background oxygen mitigates this greatly. Indeed, since incorporated N is unstable against the slow re-oxidation occurring in parallel, N_2O POA yields about an order of magnitude less nitrogen than pure NO POA at similar process temperature. It reduces D_{it} by about a factor of 2 close to E_c and leads to a peak field-effect mobility of up to ≈ 25 cm^2/V.s in 4H-SiC transistors, as indicated in Fig. 10. However, nitrous oxide is sometimes preferred over NO for safety reasons as it comes with less demanding handling requirements.

6.3. N implants and radicals

Following the improvements induced by NO POA, other methods were developed to introduce N at the SiO_2/SiC interface. Although they may be more involved, they can yield NO-like properties for oxide-based devices formed on 4H-SiC and bring their own contribution to understanding the role of nitrogen.

One such nitridation technique is implantation. N^+ ions can be inserted in the top semiconductor layer that will subsequently be consumed by thermal oxidation, yielding the presence of nitrogen at the interface. The amount of N atoms can be tuned by implantation dose and energy. Studies have revealed that similarly to NO POA, the higher the nitrogen density at the thermally-formed interface, the lower the D_{it}, and the higher the field-effect mobility [42, 91, 93]. In fact, Poggi *et al.* have reported about an order of magnitude reduction of electrically active defects close to the conduction band edge of 4H-SiC and a room temperature field-effect mobility of up to 42 cm^2/V.s in lateral nFETs fabricated on the (0001) surface [94, 95], Fig. 10. While the progressive increase of μ_{FE} with N dose is consistent with the reduction of Coulomb scattering, Hall mobility measurements reveal that in devices with the higher nitrogen content, μ_{Hall} decreases with temperature. This implies that, unlike for the NO process, another dominant scattering mechanism appears following high implant doses. This has been attributed to induced damages in SiC and residual N interstitials left within the semiconductor [16]. Also, note that the process temperature can be kept at or below 1100 °C following implantation, to avoid activation that would convert N atoms into donors in SiC. But activation of a minority of dopants in the tail end of the implant can never be ruled out.

Another elegant way to introduce nitrogen is the exposure of thermal oxides to nitrogen radicals [116, 134, 137]. It can be achieved using a remote plasma generating highly reactive N^+ ions. SIMS measurements have shown that, like NO-POA, this results in nitrogen accumulation strictly at the interface between the oxide and the semiconductor. One advantage being that it can potentially occur without re-oxidation, allowing for N maximization. Studies on devices fabricated on the Si-face of 4H-SiC again show that the D_{it} is reduced proportionally to the amount of incorporated nitrogen, in line with results from NO POA. In fact, similar and even better performance in terms of peak field-effect mobility has been demonstrated using that technique. However, prolonged plasma exposure can also reduce the integrity of the gate oxide, implying that this promising nitridation method still requires optimization.

7. Phosphorus

In 2009, about a decade after the introduction of NO annealing, Okamoto *et al.*, from the Nara Institute of Science and Technology in Japan, proposed another post-oxidation annealing technique that significantly reduces D_{it} at SiO_2/4H-SiC interfaces. As mentioned in the previous section, implantation of nitrogen in SiC prior to oxidation has proved to be a beneficial nitridation technique. Hence, Prof. Yano and his group cleverly extended this logic to a screening method for various potential passivating species [87]. This is how phosphorus caught their attention as oxidation of P-implanted SiC also showed a lower density of electrically active defects than as-oxidized un-implanted interfaces. Following this discovery, they implemented a more gentle way to introduce P at the interface in order to avoid ion-induced damages and undesirable doping of the substrate, by flowing gas through a $POCl_3$ bubbler during a high temperature post-oxidation anneal.

When performed at 1000 °C on SiO_2, grown on the Si-face of 4H-SiC, $POCl_3$ POA leads to a D_{it} below 10^{11} $cm^{-2}eV^{-1}$ close to E_c, or several times lower than following NO POA [88]. This is reflected in the efficiency of lateral nFETs as the peak value of the field-effect mobility almost doubles compared to NO POA to about 90 cm^2/V.s. This has been correlated with the presence of phosphorus at the interface. Another proposed method to reach similar mobility values is exposing a thermal oxide to P_2O_5 extracted from a solid phosphosilicate glass (PSG) diffusion source [115]. Device properties following $POCl_3$ or PSG POA are reported in Figs. 8(a), 8(b) & 10.

Note that from SIMS analysis, it is found that both $POCl_3$ and PSG POA convert the dielectric into a phosphosilicate by yielding phosphorus throughout the gate. This compromises the reliability of the devices. Recently, forming a thin P-containing interfacial oxide, using $POCl_3$ and O_2, followed by dielectric deposition, was shown to reduce trapping by narrowing the phosphorus profile [11].

The benefits of phosphorus at SiO_2/SiC interfaces represent a milestone for silicon carbide research; not only because of mobility improvements, but also because it shines light on the nature of passivation at the atomic level. Indeed, both N and P are among the group V elements of the periodic table, possessing similar chemistry due to their 5 valence electrons. For example, it has fueled the discussion of the role of sub-surface SiC doping in improving device characteristics [36]. But while the physics of N and P binding at interfaces is still being debated, we are one step closer to a more comprehensive understanding of post-oxidation annealing mechanisms.

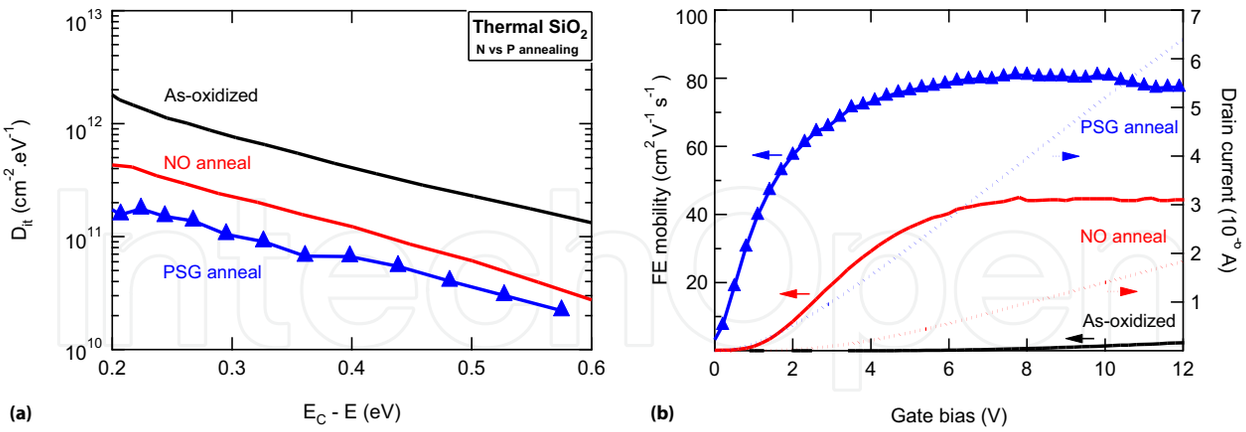

Figure 8. (a) D_{it} reduction compared to as-oxidized films using NO POA or a phosphorus source. Adapted from Ref.[115]. (b) Transfer characteristics and extracted field-effect mobilities showing the efficiency of P. Adapted from Ref.[115].

8. Deposited oxides

Considering all the efforts necessary to improve the interface, boasting that silicon carbide should be preferred over other wide band gap semiconductors because it can grow a stable thermal oxide may no longer be a valid argument. First, the dominating trap level close to the conduction band edge of 4H-SiC has been associated with slow near-interface defects most likely residing inside SiO_2, possibly oxygen vacancies. Second, evidence is mounting that the oxidation process itself, which creates C-related defects at the oxide/semiconductor interface, also yields a transition region that extends within SiC, potentially affecting transport properties inside the inversion layer of transistors [10, 17, 19, 117].

In particular, it has been proposed by the group of Prof. Kimoto, from Kyoto University in Japan, that thermal oxidation results in the emission of C atoms from the interface towards the bulk of the semiconductor [61]. Indeed, deep level transient spectroscopy (DLTS) measurements reveal a strong similarity between the effects of thermal oxidation and the ones of C implantation in irradiated samples, as both processes yield the suppression of a level labeled $Z_{1/2}$ thought to be associated with C vacancies in silicon carbide [69, 123]. A refined oxidation model including the kinetics of emitted atoms was then put forward by Prof. Hijikata's research group at Saitama University in Japan; it successfully models their in-situ ellipsometry observations of thermal oxide growth rate on silicon carbide in both the thin and thick film regimes [59].

Because of these drawbacks of thermal oxidation, it should not come as a surprise that using deposited oxides has yielded encouraging results. For example, chemical vapor deposition of a thin SiN buffer layer on the Si-face of 4H-SiC followed by SiO_2 deposition and N_2O annealing, has been reported to lower the D_{it} and increase the field-effect mobility to above 30 cm^2/V.s in lateral n-channel devices [85]. This is an improvement in efficiency compared to gates formed thermally in N_2O, highlighting the benefits of deposited dielectrics. In that particular case, thinning the SiN layer has also proven to be key as thick oxynitride films resulting from oxygen insertion can possess a high density of positive charges which lower mobility and move the threshold voltage to negative values.

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8.1. Alternate dielectrics

The versatility added in device fabrication from using deposited oxides allows to explore a variety of deposition techniques, temperatures, and most importantly the ability to use gate materials other than SiO_2. It is interesting to note that the reason for considering alternate dielectrics is to move away from thick thermal oxides to reach higher mobility, which is fundamentally different from the evolution of gate fabrication in silicon technology where the motivation comes from scaling and the need for physically thicker oxides at a given capacitance to maintain gate control while minimizing leakage, often at the expense of mobility [56, 131]. This has led to the development and integration of materials which possess a higher dielectric constant, or higher k, that are used in the new generations of Si electronics. Regardless of the dichotomy, it comes at a very opportune time for SiC device research which looks to take advantage of the acquired expertise in deposited gate dielectrics.

Another factor to consider when using high-k oxides on a wide band gap material like SiC however, is the reduced band offsets between the semiconductor and the dielectric. The conduction band offset relative to 4H-SiC for example goes from ≈ 3 eV with a SiO_2 gate to ≈ 1 eV with a HfO_2 gate [1, 102]. This has implications in terms of leakage current and reliability as such small barriers promote tunneling of carriers into the insulator, even more so that SiC devices are expected to perform at high temperature, which exacerbates the issue [105]. So if HfO_2 is to be considered as a gate material, a thin SiO interlayer is necessary to achieve reasonable leakage. Indeed, Afanas'ev *et al.* have demonstrated that such structures have good interface properties, without the need for nitridation, but that it comes at the expense of a maximum surface field of about 3 MV/cm in the semiconductor to ensure gate integrity, dangerously close to transistor minimum requirements [7]. Ultimately, a balancing act between SiO and HfO_2 thicknesses yields a compromise between performance and reliability [38].

But unlike Si technology, we are not aiming for the highest possible dielectric constant, so we can somewhat move away from this compromise as long as a quality dielectric can be obtained on SiC. A promising candidate in this respect is Al_2O_3; it has a dielectric constant close to 9 and a band gap only a few tens of eV narrower than SiO_2, yielding a conduction band offset relative to 4H-SiC that is still above 2 eV. Most importantly, it does not possess the same dominating trap level as SiO_2, so that high electron mobility can be achieved in n-channel devices. Indeed, peak field-effect mobility values measured at room temperature on the Si-face can exceed 100 $cm^2/V.s$ [60, 79]. A key observation is again that a thin thermal SiO or SiON layer is still required, not so much to reduce gate leakage but to increase efficiency by providing a progressive transition between the semiconductor and the deposited oxide. Since it acts as a passivating layer, it is no surprise that while it is needed, the thinner it is, the better, so that a good interface can be formed while reducing the impact of remote thermal oxide traps on channel transport properties. In practice, the stability of a high-k material on SiO has to be considered carefully to avoid intermixing of the atomic species during subsequent device fabrication steps. To mitigate this, a SiN barrier layer can be used between the thermal oxide and Al_2O_3, blocking Al diffusion to the interface [83], or the learning from Si technology can be extended to the use of low-temperature gate-last processing schemes [14].

8.2. Surface conditioning

In the previous Sections, we have shown that while moving away from a thermally-formed gate oxide improves transport properties in 4H-SiC devices, a thin SiO transition layer still brings a much-needed passivated interface. While this is also true for deposited dielectrics on Si, the remarkable difference is that the thinner the thermal oxide is, the better. The next logical step is therefore to avoid thermally-formed SiO entirely, circumventing the negative impact of oxidation-induced defects and near-interface traps. But how can this be done so that there is a clean transition between the SiC surface and the deposited oxide?

It all comes down to surface preparation of the semiconductor, which cannot simply end with a wet clean since atomic ordering and bonding are paramount. A common surface preparation technique that has been used prior to epitaxial deposition or graphene formation on SiC might provide part of the answer. Hydrogen exposure of the (0001) face of hexagonal SiC to high temperatures (e.g. 1350 °C) etches the surface, smoothing it and yielding atomic reconstruction [18, 101, 120, 126]. However, if a gate dielectric is deposited directly on it, there appears to be no reduction of the D_{it} when compared to an HF-last surface, which, as expected, is even worse than a thermally formed interface, at least when looking at SiO_2 deposition on 4H-SiC. But Shirasawa *et al.* observed on 6H-SiC that when high temperature H_2 exposure is directly followed by N_2 exposure at the same temperature, it results in an ordered surface terminated by a monolayer of SiN topped by a monolayer of SiO [118, 119]. These thin films have well defined band gaps, a sign of their electrical integrity, and are estimated to be stable without the existence of dangling bonds at the SiC surface.

Our group at the Central Research Institute of Electronic Industry, located in Yokosuka, Japan, then speculated that such a technique could be applied to 4H-SiC in order to form an ideal seed layer for subsequent deposition [110, 111]. Indeed, this "nitrogen conditioning" process is expected to yield an interface saturated by N atoms which are highly localized within a monolayer, a very promising scenario since we know that maximizing nitrogen content at the interface while limiting its presence in the oxide is key. Moreover, the single oxide layer formed by Si-O-Si bridges bonded to the nitrogen provides the bare minimum silicon oxide, while still offering a clean transition to a deposited layer.

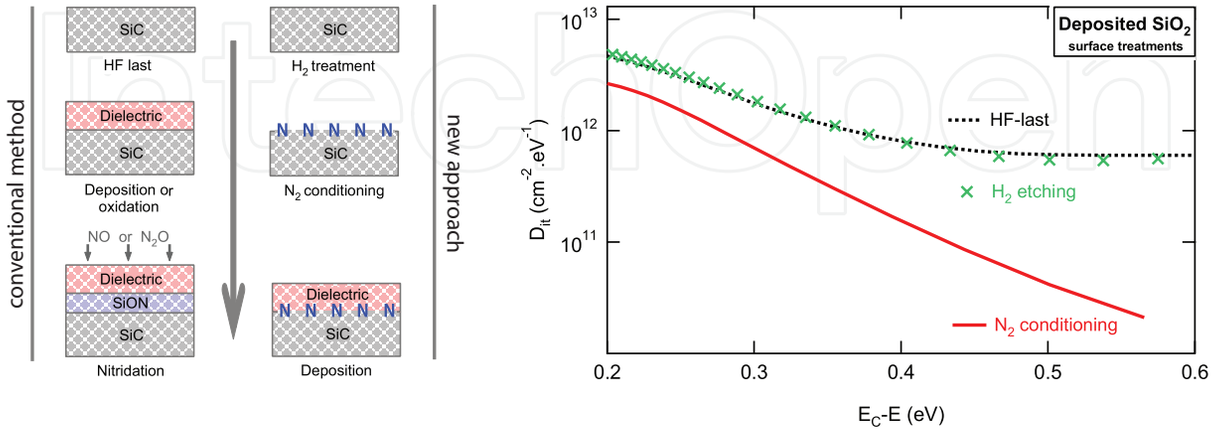

Figure 9. Schematic of the nitrogen conditioning technique for deposited oxides vs. conventional nitridation methods. On the right is the corresponding D_{it} from deposited SiO_2 on surfaces which were subjected to various treatments. Adapted from Refs. [110, 111].

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XPS and SIMS measurements confirm that a SiON layer can be formed using nitrogen conditioning on the Si-face of 4H-SiC. More importantly, we find that the nitrogen remains localized at the interface following 900 °C SiO_2 deposition by CVD. N is exclusively bonded to silicon, and no C-O, C-N, or N-O bonds are detected, which is consistent with the structure mentioned above, and atomically cleaner than interfaces resulting from either thermal oxidation or NO POA [77]. Electrical characterization shows that the density of interface states of a deposited oxide is lower than the one of a thermal oxide only when nitrogen conditioning is used, Fig. 9. While this is a notable improvement over as-deposited oxides on a HF-last surface, even better results are expected with alternate dielectrics and low temperature deposition methods such as atomic layer deposition (ALD). Indeed, if the seed layer can be kept intact and a quality oxide can be deposited, this smooth and clean interface should translate into higher inversion mobility because of reduced Coulomb and surface-roughness scattering.

9. Summary and conclusions

In order to realize the full potential of SiC-based devices across the voltage range depicted in Fig. 1, the quality of the oxide/semiconductor interface must be improved. Figure 10 summarizes both mobility and D_{it} from thermal oxide gates following the various annealing processes described in this Chapter. Despite increasingly efficient POA processes from N_2O, to NO, to phosphorus exposure, the wide band gap and complex oxidation process yield a large density of states that still limits the mobility in even the best oxide-based SiC transistors. While rigourous experiments have led to that conclusion, the trend depicted in Fig. 10 shows a clear dependence between carrier transport and interface states. It suggests that the significant increase in mobility compared to NO POA induced by PSG or $POCl_3$ annealing is

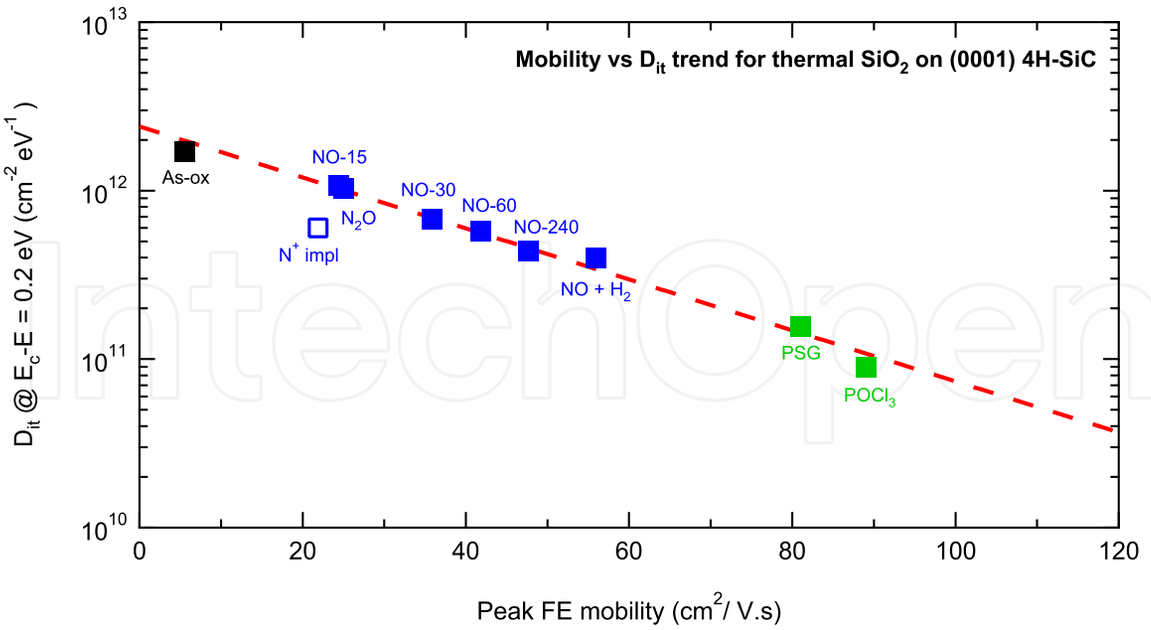

Figure 10. Peak field-effect mobilities extracted from lateral MOSFETs fabricated on (0001) 4H-SiC using thermal oxides with various POAs and the corresponding D_{it} @ 0.2 eV from the conduction band. The plot suggests that Coulomb scattering is the dominant mechanism affecting carrier transport. Further reduction of the interface trap density will keep improving device efficiency. Data gathered from Refs. [12, 88, 94, 106, 108, 115, 130].

still hampered by trap-induced Coulomb scattering. Moreover, it is another indication that if D_{it} can be decreased further, the mobility could potentially reach values well above 100 cm^2/V.s.

One can then speculate whether the best properties will be obtained from passivating a defective thermally-formed SiO_2/SiC interface or using alternate dielectrics like promising Al_2O_3 gate stacks that have demonstrated such high mobilities. Both of these top-down and bottom-up approaches come with their respective challenges going from process integration to device stability and reliability. Thermal oxide POA must optimize the density of passivating species while limiting their presence inside the oxide, indeed D_{it} is inversely proportional to the amount of nitrogen but the quantity of hole traps increases with it. As for alternate dielectrics, benefits could arise by moving away from pre- or post-deposition oxidation, using instead efficient surface preparation techniques.

If the steady progress made during the past couple decades is any indication, silicon carbide research, development, and technology, have a bright future ahead.

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Author details

John Rozen*

* Address all correspondence to: jrozen@us.ibm.com

IBM T.J. Watson Research Center, Yorktown Heights, NY, USA

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