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Advances in Resistive Switching Memories Based on Graphene Oxide

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1. Introduction

Memory devices are a prerequisite for today's information technology. In general, two different segments can be distinguished. Random access type memories are based on semiconductor technology. These can be divided into static random access memories (SRAM) and dynamic random access memories (DRAM). In the following, only DRAM will be considered, because it is the main RAM technology for standalone memory products. Mass storage devices are traditionally based on magnetic- and optical storage. But also here semiconductor memories are gaining market share. The importance of semiconductor memories is consequently increasing (Mikolajick et al., 2009). Though SRAM and DRAM are very fast, both of them are volatile, which is a huge disadvantage, costing energy and additional periphery circuitry. Si-based Flash memory devices represent the most prominent nonvolatile data memory (NVM) because of their high density and low fabrication costs. However, Flash suffers from low endurance, low write speed, and high voltages required for the write operations. In addition, further scaling, i.e., a continuation in increasing the density of Flash is expected to run into physical limits in the near future. Ferroelectric random access memory (FeRAM) and magnetoresistive random access memory (MRAM) cover niche markets for special applications. One reason among several others is that FeRAM as well as conventional MRAM exhibit technological and inherent problems in the scalability, i.e., in achieving the same density as Flash today. In this circumstance, a renewed nonvolatile memory concept called resistance-switching random access memory (RRAM), which is based on resistance change modulated by electrical stimulus, has recently inspired scientific and commercial interests due to its high operation speed, high scalability, and multibit storage potential (Beck et al., 2000; Lu & Lieber, 2007; Dong et al., 2008). The reading of resistance states is nondestructive, and the memory devices can be operated without transistors in every cell (Lee et

al., 2007; Waser & Aono, 2007), thus making a cross-bar structure feasible. A large variety of solid-state materials have been found to show these resistive switching characteristics, including solid electrolytes such as GeSe and Ag_2S (Waser & Aono, 2007), perovskites such as $SrZrO_3$ (Beck et al., 2000), $Pr_{0.7}Ca_{0.3}MnO_3$ (Liu et al., 2000; Odagawa et al., 2004; Liao et al., 2009), and $BiFeO_3$ (Yang et al., 2009; Yin et al., 2010), binary transition metal oxides such as NiO (Seo et al., 2004; Kim et al., 2006; Son & Shin, 2008), TiO_2 (Kim et al., 2007; Jeong et al., 2009; Kwon et al., 2010), ZrO_2 (Wu et al., 2007; Guan et al., 2008; Liu et al., 2009), and ZnO (Chang et al., 2008; Kim et al., 2009; Yang et al., 2009), organic materials (Stewart et al., 2004), amorphous silicon (a-Si) (Jo and Lu, 2008; Jo et al., 2009), and amorphous carbon (a-C) (Sinitskii & Tour, 2009; Zhuge et al., 2010) (Zhuge et al., 2011).

In last decades, carbon-based materials have been studied intensively as a potential candidate to overcome the scientific and technological limitations of traditional semiconductor devices (Rueckes et al., 2000; Novoselov et al., 2004; Avouris et al., 2007). It is worthy mentioning that most of the work on carbon-based electronic devices has been focused on field-effect transistors (Wang et al., 2008; Burghard et al., 2009). Thus, it would be of great interest if nonvolatile memory can also be realized in carbon so that logic and memory devices can be integrated on a same carbon-based platform. Graphene oxide (GO) with an ultrathin thickness (~1 nm) is attractive due to its unique physical-chemical properties. A GO layer can be considered as a graphene sheet with epoxide, hydroxyl, and/or carboxyl groups attached to both sides. GO can be readily obtained through oxidizing graphite in mixtures of strong oxidants, followed by an exfoliation process. Due to its water solubility, GO can be transferred onto any substrates uniformly using simple methods such as drop-casting, spin coating, Langmuir-Blodgett (LB) deposition and vacuum filtration. The as-deposited GO thin films can be further processed into functional devices using standard lithography processes without degrading the film properties (Eda et al., 2008; Cote et al., 2009). Furthermore, the band structure and electronic properties of GO can be modulated by changing the quantity of chemical functionalities attached to the surface. Therefore, GO is potentially useful for microelectronics production. Considering that although a large variety of solid-state materials have been found to show resistive switching characteristics, none of them can fully meet the requirements of RRAM applications, exploration of new storage media is still a key project for the development of RRAM (Zhuge et al., 2011). This review focuses on GO-based RRAM cells, highlighting their advantages as the next generation memories. Section 2 describes the basic concepts of resistive switching and resistance-switching random access memory and physical storage mechanisms. In section 3, the resistive switching mechanisms of GO thin films and memory properties of GO-based RRAM cells are presented. Detailed current–voltage measurements show that in metal/GO/metal sandwiches, the resistive switching originates from the formation and rupture of conducting filaments. An analysis of the temperature dependence of the ON-state resistance reveals that the filaments are composed of metal atoms due to the diffusion of the top electrodes under a bias voltage. Moreover, the resistive switching is found to occur within confined regions of the metal filaments. The resistive switching effect is also observed in GO/metal structures by conducting atomic force microscopy. It is attributed to the redox reactions between GO and adsorbed water induced by external voltage biases. The GO-based RRAM cells show an ON/OFF

ratio >100, a retention time >10^5 s, and switching threshold voltages <1 V. In section 4, the resistive switching mechanisms of conjugated-polymer-functionalized GO thin films and memory properties of corresponding RRAM cells are described. In this case, the resistive switching is ascribed to electron/hole transfer between graphene sheets and polymer molecules. The RRAM cells exhibit excellent memory performances, such as large ON/OFF ratio, good endurance, and high switching speed. In the last section, it is proposed that the realization of bidirectional or reversible electron transfer in graphene-based hybrid systems is expected to overcome the "voltage–time dilemma" (i.e., one could not realize high write/erase speed and long retention time simultaneously) in pure electronic mechanism-based RRAM cells (Schroeder et al., 2010). Pure electronic mechanisms in RRAM cells postulate the trapping and detrapping of electron in immobile traps as the reason for the resistance changes, also known as Simmons & Verderber model (Simmons & Verderber, 1967). While in graphene-based hybrid systems, the electron transfer occurs between graphene sheets and functional molecules covalently or non-covalently bonded to graphene, which may avoid the "voltage–time dilemma".

2. Resistive switching and RRAM

A resistive switching memory cell in an RRAM is generally composed of an insulating or resistive material sandwiched between two electron-conductive electrodes to form metal-insulator-metal (MIM) structure. By applying an appropriate voltage, the MIM cell can be switched between a high-resistance state (HRS or OFF-state) and a low-resistance state (LRS or ON-state). Switching from OFF-state to ON-state is called the SET process, while switching from ON-state to OFF-state is called the RESET process. These two states can represent the logic values 1 and 0, respectively. Depending on voltage polarity, the resistive switching behavior of an RRAM device is classified as unipolar and bipolar. For unipolar switching, resistive switching is induced by a voltage of the same polarity but a different magnitude, as shown in Fig. 1(a) (Waser & Aono, 2007). For bipolar switching, one polarity is used to switch from HRS to LRS, and the opposite polarity is used to switch back into HRS, as shown in Fig. 1(b) (Waser & Aono, 2007). A current compliance (CC) is usually needed during the SET process to prevent the device from a permanent breakdown. (Li et al., 2011)

In the simplest approach, the pure memory element can be used as a basic memory cell, resulting in a configuration where parallel bitlines are crossed by perpendicular wordlines with the switching material placed between wordline and bitline at every cross-point. This configuration is called a cross-point cell. Since this architecture will lead to a large parasitic current flowing through nonselected memory cells, the cross-point array has a very slow read access. A selection element can be added to improve the situation. A series connection of a diode in every cross-point allows to reverse bias all nonselected cells. This can be arranged in a similar compact manner as the basic cross-point cell. Finally a transistor device (ideally a MOS Transistor) can be added which makes the selection of a cell very easy and therefore gives the best random access time, but comes at the price of increased area consumption. Figure 2 illustrates the different cell type possibilities. For random access type memories, a transistor type archi-

tecture is preferred while the cross-point architecture and the diode architecture open the path toward stacking memory layers on top of each other and therefore are ideally suited for mass storage devices (Mikolajick et al., 2009; Pinnow & Mikolajick, 2004).
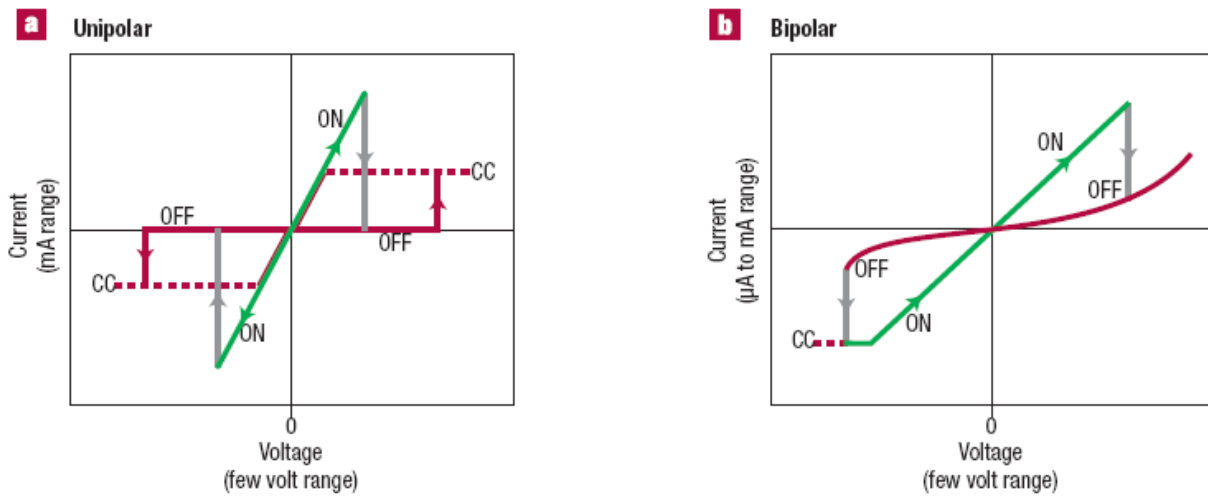

Figure 1. (a) Unipolar switching. The SET voltage is always higher than the voltage at which RESET takes place, and the RESET current is always higher than the CC during SET operation. (b) Bipolar switching. The SET operation takes place on one polarity of the voltage or current, and the RESET operation requires the opposite polarity. (Waser & Aono, 2007)
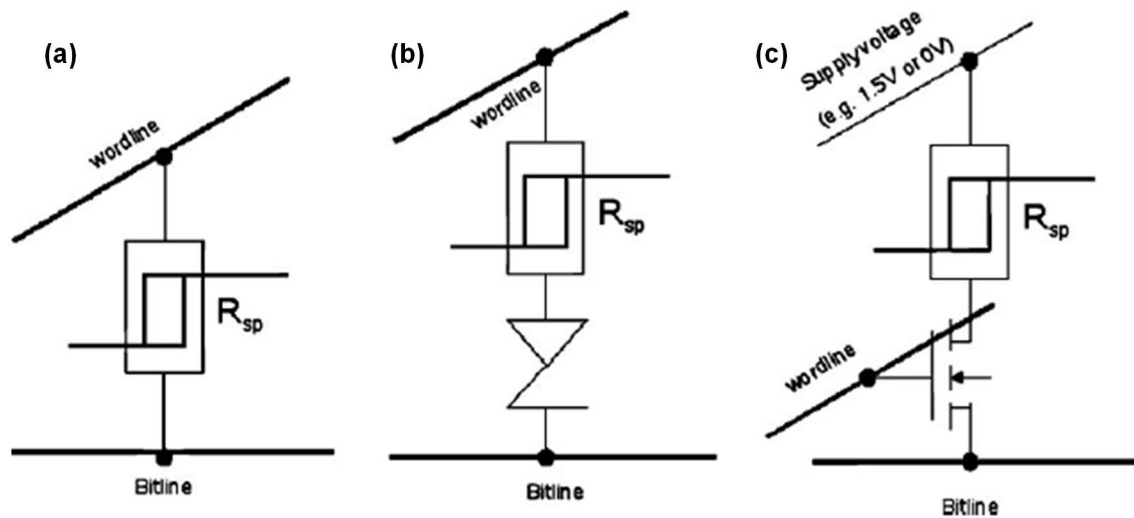

Figure 2. Three different cell architectures for RRAM cells: (a) cross-point cell, (b) diode cell, and (c) transistor cell together with their respective area consumption in F^2. F denotes the minimum feature size of the fabrication technology. (Mikolajick et al., 2009)

Based on the circuit requirements of high-density NVM today such as Flash and taking predictions about technology scaling of the next 15 years into account, one can collect a number of requirements for RRAM cells (Waser et al., 2009):

2.1. Write operation

Write voltages should be in the range of a few hundred mV to be compatible with scaled CMOS to few V (to give an advantage over Flash which suffers from high programming voltages). The length of write voltage pulses is desired to be <100 ns in order to compete with DRAM specifications and to outperform Flash which has a programming speed of some 10 ms, or even <10 ns to approach high-performance SRAM.

2.2. Read operation

Read voltages need to be significantly smaller than write voltages in order to prevent a change of the resistance during the read operation. Because of constraints by circuit design, read voltage cannot be less than approximately one tenth of write voltage. An additional requirement originates from the minimum read current. In the ON-state, read current should not be less than approximately 1mA to allow for a fast detection of the state by reasonably small sense amplifiers. The read time must be in the order of write time or preferably shorter.

2.3. Resistance ratio

Although an ON/OFF (R_{OFF}/R_{ON}) ratio of only 1.2 to 1.3 can be utilized by dedicated circuit design as shown in MRAM, ON/OFF ratios >10 are required to allow for small and highly efficient sense amplifiers and, hence, RRAM devices which are cost competitive with Flash.

2.4. Endurance

Contemporary Flash shows a maximum number of write cycles between 10^3 and 10^7, depending on the type. RRAM should provide at least the same endurance, preferably a better one.

2.5. Retention

A data retention time of >10 years is required for universal NVM. This retention time must be kept at thermal stress up to 85 ºC and small electrical stress such as a constant stream of read voltage pulses.

Despite a bursting body of experimental data that is rapidly becoming available, the precise mechanism behind the physical effect of resistive switching remains elusive. A few qualitative models have been proposed emphasizing different aspects: electric-field-induced defect migration (Baikalov et al., 2003; Nian et al., 2007), phase separation (Tulina et al., 2001), tunneling across interfacial domains (Rozenberg et al., 2004), control of the Schottky barrier's height (Jeong et al., 2009), etc., as shown in Fig. 3. A general consensus has emerged on the empirical relevance of three key features: (i) a highly spatially inhomogeneous conduction in the low resistive state, (ii) the existence of a significant number of defects, and (iii) a preeminent role played by the interfaces, namely, the regions of the oxide that are near each of the metallic electrodes which often form Schottky barriers. (Rozenberg et al., 2010)
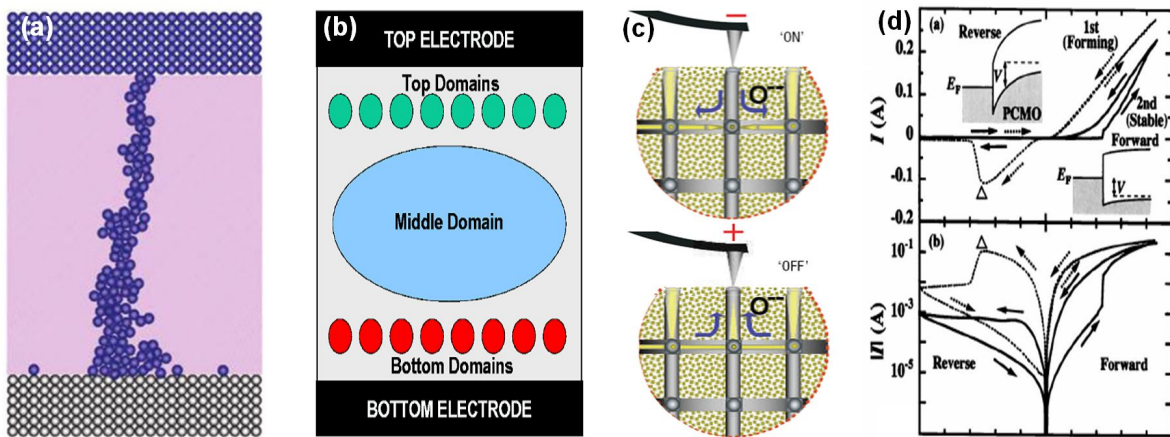
Figure 3. Reported several resistive switching mechanisms. (a) Filamentary model (Yang et al., 2009). (b) Domain model (Rozenberg et al., 2004). (c) Electrical field induced oxygen vacancy migration model (Szot et al., 2006). (d) Schottky barrier modulation model (Sawa et al., 2004).

3. Resistive switching and memory properties in GO-based RRAM cells

He et al. firstly reported reliable and reproducible resistive switching behaviors in GO thin films prepared by the vacuum filtration method on 2009 (He et al., 2009). The Cu/GO/Pt structure showed an ON/OFF ratio of about 20, aretention time of more than 10^4 s, and switching threshold voltages of less than 1 V, as shown in Fig. 4.
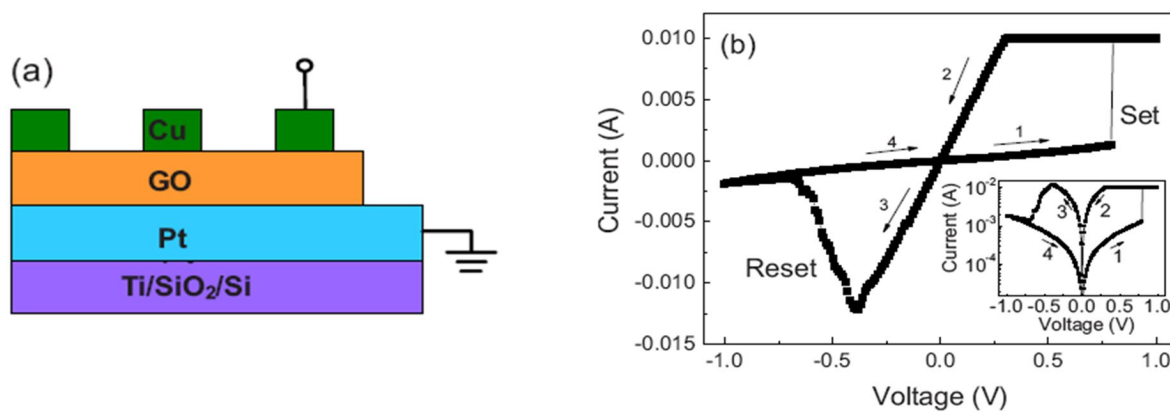

Figure 4. (a) A schematic configuration of the Cu/GO/Pt sandwiched structure. (b) I–V characteristics of the Cu/GO/Pt structure. The arrows indicate the sweep direction. The inset shows the I–V characteristics in semilogarithmic scale. (He et al., 2009)

It indicates that GO is potentially useful for future nonvolatile memory applications. At a later time, Zhuge et al. achieved larger ON/OFF ratios of more than 100 in metal (Cu, Ag, Ti,

and Au)/GO/Pt devices (Zhuge et al., 2011). They considered that the moisture in air affects the ON/OFF ratio of metal/GO/Pt memory cells severely. Furthermore, Jeong et al. present‐ ed a GO based memory that can be easily fabricated using a room temperature spin-casting method on flexible substrates and has reliable memory performance in terms of retention and endurance, as shown in Fig. 5 (Jeong et al., 2010). Therefore, the GO memory is an excel‐ lent candidate to be a memory device for future flexible electronics (Hong et al., 2010).
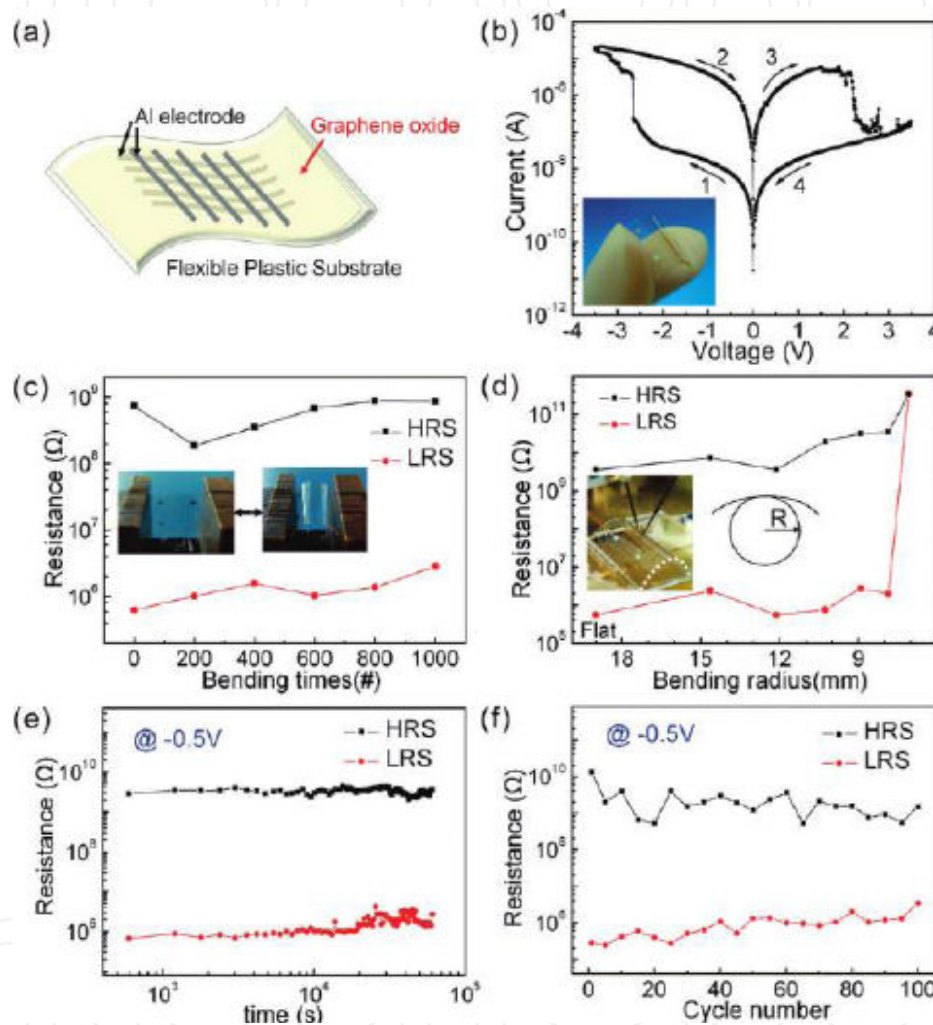

Figure 5. (a) A schematic illustration of a GO based flexible crossbar memory device. (b) Typical I–V curve of a Al/GO/Al/PES device plotted on a semilogarithmic scale. The arrows indicate the voltage sweep direction. The left in‐ set is a real photo image of a device. (c) Continuous bending effect of a Al/GO/Al/PES device. The insets show photo‐ graphs of repeated two bending states. (d) The resistance ratio between the HRS and LRS as a function of the bending radius (*R*). The inset is a photograph of an I-V measurement being performed under a flexed condition. (e) Retention test of Al/GO/Al/PES device read at –0.5 V. (f) Endurance performance of an Al/GO/Al/PES device measured during 100 sweep cycles. (Jeong et al., 2010)

As to the mechanism of the resistive switching effect in GO thin films, Zhuge et al. pointed out that in metal/GO/Pt sandwiches, the resistive switching originates from the formation and rupture of conducting filaments, as schematically shown in Fig. 6 (Zhuge et al., 2011).
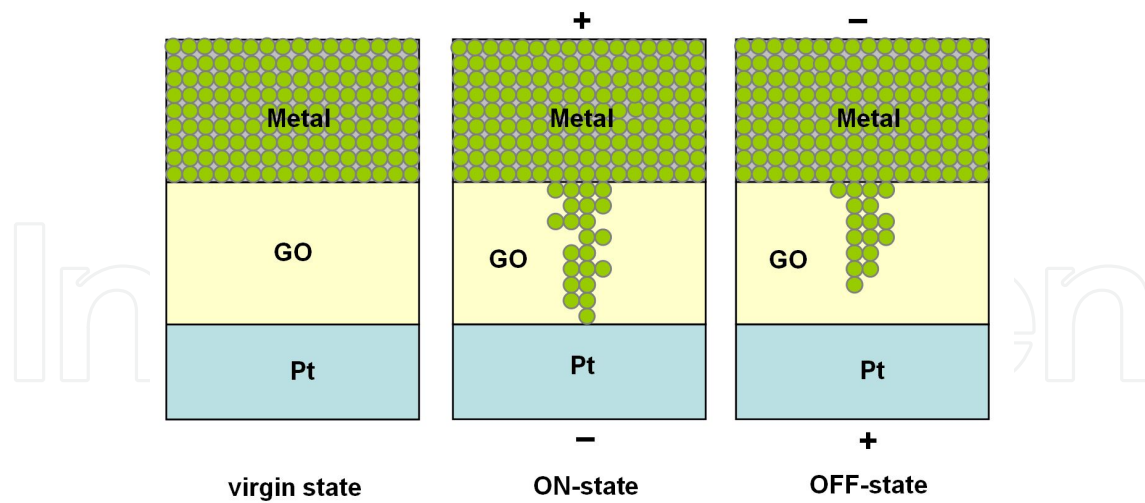
Figure 6. A schematic diagram for the mechanism of the resistive switching in metal/GO/Pt memory cells. (Zhuge et al., 2011)
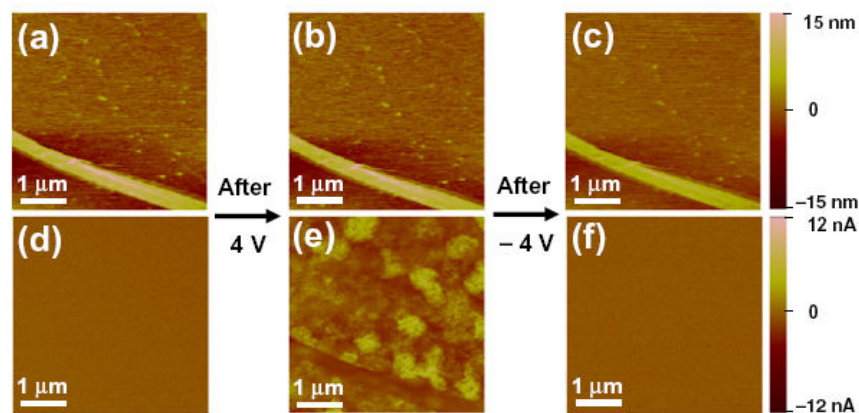

Figure 7. (a), (b) and (c) AFM images of virgin GO films, GO films in LRS, and GO films in HRS. The light-colored ribbons represent folded regions. (d), (e) and (f) the corresponding CAFM images under a read voltage of 1 V. (Zhuge et al., 2011)

An analysis of the temperature dependence of the ON-state resistance reveals that the filaments are composed of metal atoms due to the diffusion of the top electrodes under a bias voltage. Tsuruoka et al. pointed out that the formation of a metal filament is due to inhomogeneous nucleation and subsequent growth of metal, based on the migration of metal ions in the oxide matrix (Tsuruoka et al., 2010). Recently, they reported that the ionization of metal at the anode interfaces is likely to be attributed to chemical oxidation via residual water in the oxide layer, and metal ions migrate along grain boundaries in the oxide layer, where a hydrogen-bond network might be formed by moisture absorption (Tsuruoka et al., 2012). Moreover, the switching occurs within confined regions of the metal filaments. The RESET process is considered to consist of the Joule-heating-assisted oxidation of metal atoms at the thinnest part of the metal filament followed by diffusion and drift of the metal ions under

their own concentration gradient and the applied electric field, disconnecting the metal filament (Tsuruoka et al., 2010). Zhuge et al. also observed the resistive switching effect in GO/Pt structures by conducting atomic force microscopy (CAFM), as shown in Fig. 7 (Zhuge et al., 2011). It is attributed to the redox reactions between GO and adsorbed water induced by external voltage biases. While for Al/GO/Al memory cells, Jeong et al. attributed the bipolar resistive switching behavior to rupture and formation of conducting filaments at the top amorphous interface layer formed between the GO film and the top Al metal electrode, as shown in Fig. 8 (Jeong et al, 2010).
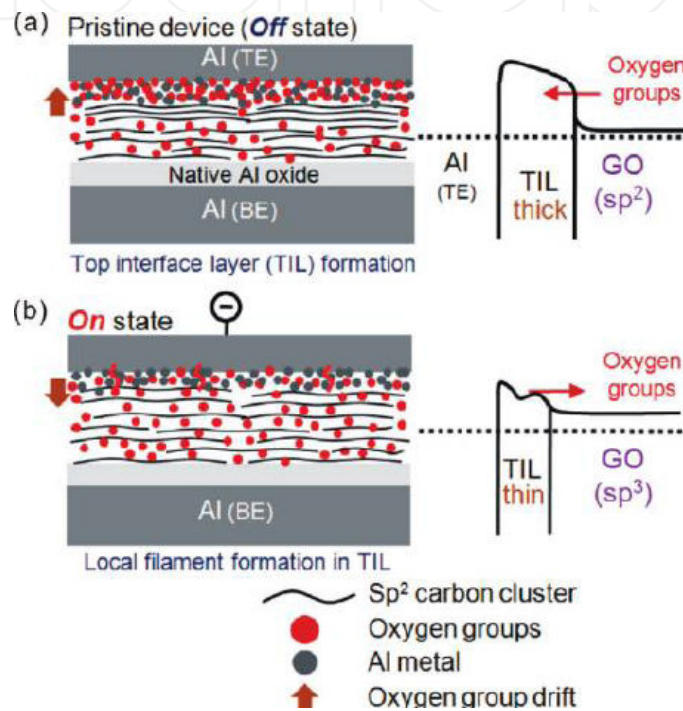

Figure 8. Schematic of the proposed bipolar resistive switching model for Al electrode/GO/Al electrode crossbar memory device. (a) The pristine device is in the OFF-state due to the (relatively) thick insulating top interface layer formed by a redox reaction between vapor deposited Al and the GO thin film. (b) The ON-state is induced by the formation of local filaments in the top interface layer due to oxygen ion diffusion back into the GO thin film by an external negative bias on the top electrode. (Jeong et al., 2010)

Furthermore, Hong et al. pointed out that for Al/GO/metal memory devices, the resistive switching operation is governed by dual mechanism of oxygen migration and Al diffusion (Hong et al., 2011). The Al diffusion into the graphene oxide is the main factor to determine the switching endurance property which limits the long term lifetime of the device. The electrode dependence on graphene oxide RRAM operation has been analyzed as well and is attributed to the difference in surface roughness of graphene oxide for the different bottom electrodes, as shown in Fig. 9 (Hong et al., 2011). Interestingly, Panin et al. observed both diode-like (rectifying) and resistor-like (nonrectifying) resistive switching behaviors in an Al/GO/Al planar structure, as shown in Fig. 10 (Panin et al., 2011). Electrical characterization of the Al/GO interface using the induced current identifies a potential barrier near the interface and its spatial modulation, caused by local changes of resistance at a bias voltage,

which correlated well with the resistive switching of the whole structure. Recently, Wang et al. found that the speed of the SET and RESET operations of the Al/GO/ITO resistive memories is significant asymmetric (Wang et al., 2012). The RESET speed is in the order of 100 ns under a –5 V voltage while the SET speed is three orders of magnitude slower (100 μs) under a 5 V bias. The behavior of resistive switching speed difference is elucidated by voltage modulated oxygen diffusion barrier change, as shown in Fig. 11 (Wang et al., 2012).
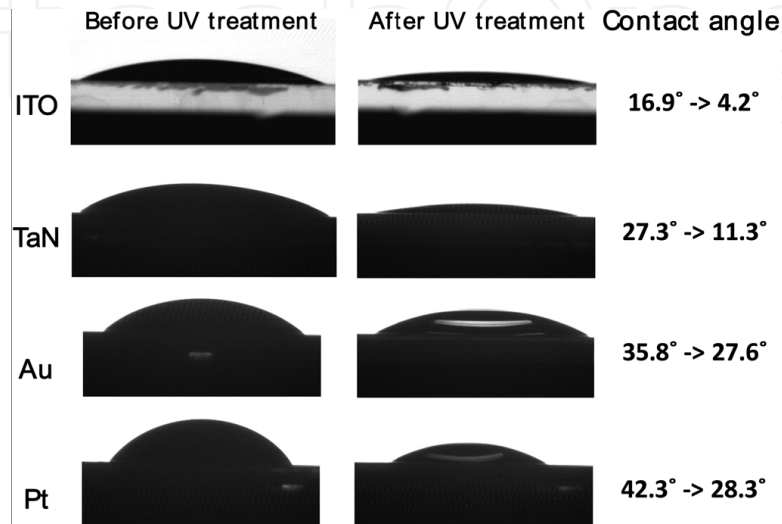

Figure 9. The contact angles of graphene oxide solution on four different surfaces of ITO, TaN, Su, and Pt. UV treatment is done to promote adhesion. (Hong et al., 2011)
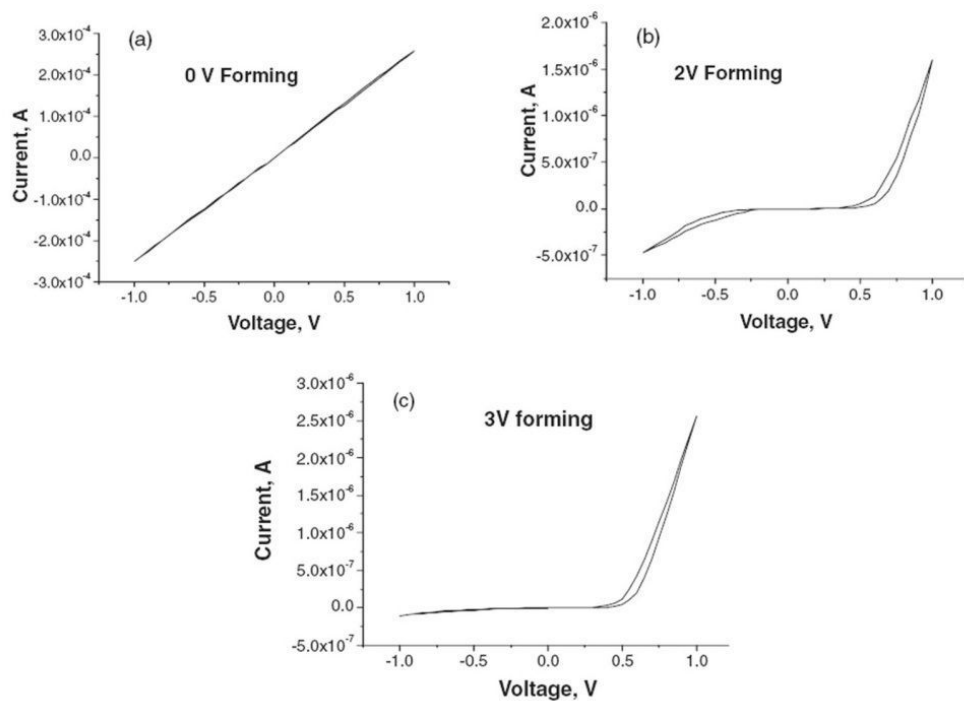

Figure 10. I–V curves of Al/GO/Al structures pre-formed at different forming voltages. (Panin et al., 2011)
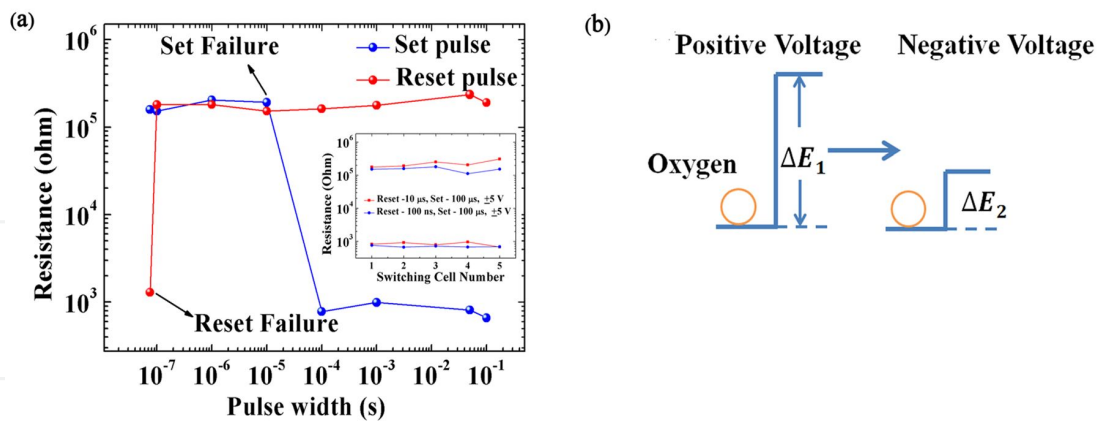
Figure 11. Pulse behavior of the Al/GO/ITO/PET memory cell, HRS and LRS is read at 0.3 V. (a) the SET and RESET operations of the devices with different pulsing width at ±5. The HRS and LRS of the devices are measured at 0.3V and the SET operation is found to be three orders of magnitude slower than the RESET operation; (b) a schematic of oxygen hopping barrier change model. (Wang et al., 2012)

4. Resistive switching and memory properties in GO-polymer hybrid RRAM cells

Liu et al. prepared a solution-processable and electroactive complex of poly(*N*-vinylcarbazole)-derivatized graphene oxide (GO-PVK) via amidation of end-functionalized PVK, from reversible addition fragmentation chain transfer polymerization, with tolylene-2,5-diisocyanate-functionalized graphene oxide (Liu et al., 2009). The Al/GO-PVK/ITO device exhibits bistable electrical conductivity switching and nonvolatile rewritable memory effects. The resistive switching is attributed to electron transfer between GO and PVK, as shown in Fig. 12 (Liu et al., 2009).
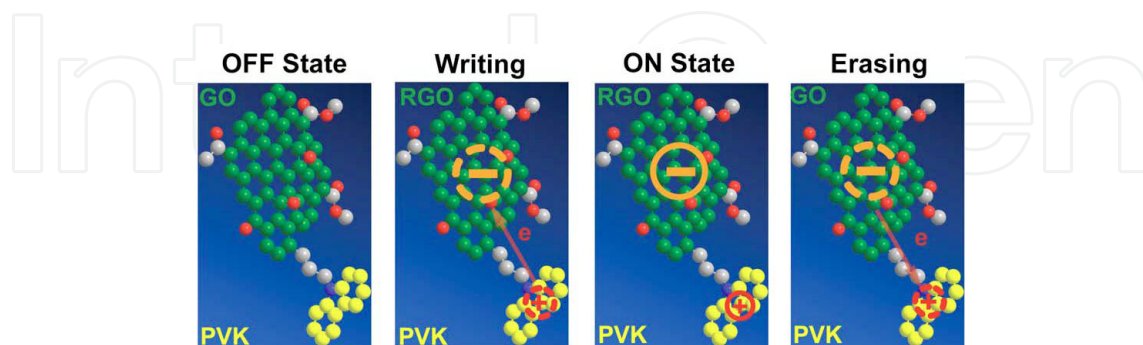

Figure 12. Plausible switching mechanism of GO-PVK. RGO stands for reduced graphene oxide. (Liu et al., 2009)

Zhuang et al. synthesized a novel conjugated-polymer-modified graphene oxide (TPAPAM-GO), which was successfully used to fabricate a TPAPAM-GO-based RRAM device (Zhuang et al., 2010). The device exhibits a typical bistable electrical switching and nonvolatile rewrit-

able memory effect, with a SET voltage of about–1V and an ON/OFF ratio of more than 10^3, as shown in Fig. 13 (Zhuang et al., 2010).
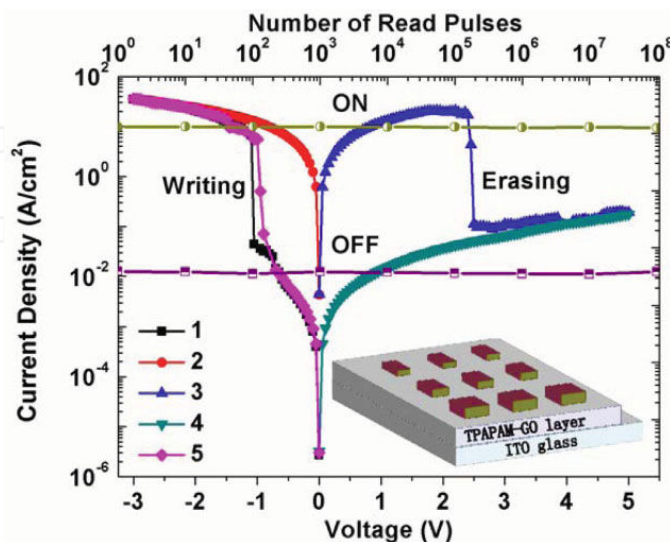

Figure 13. J–V characteristics and stability tested in either ON- or OFF-state under stimulus by read pulses of a 0.16-mm² ITO/TPAPAM-GO/Al device. Inset: schematic diagram of the single-layer memory devices. (Zhuang et al., 2010)

Both the ON- and OFF-state are stable under a constant voltage stress and survive up to 10^8 read cycles at a read voltage of –1 V. As to the switching mechanism, they deduced that at the switching threshold voltage, electrons transit from the hole transporting (electron donating) polymer TPAPAM (highest occupied molecular orbital, HOMO) into the graphene monoatom layer (lowest unoccupied molecular orbital, LUMO) via intramolecular charge-transfer (CT) interaction (Ling et al., 2008). The transferred electrons can delocalize effectively in the giant p-conjugation system, and reduce graphene oxide to graphene (Elias et al., 2009; Robinson et al., 2008). Upon electrochemical reduction of the functionalized graphene oxide, electrons can propagate with less scattering, giving rise to a substantially enhanced room temperature conductivity (~10^2 S m^{-1}) of the composite material (Robinson et al., 2008; Stankovich et al., 2006). Along with the increase of CT interaction, dual-channel charge-transport pathways will form via interplane hopping in graphene films and switch the ITO/TPAPAM-GO/Al device from the OFF-state to the ON-state (Ling et al., 2008). The application of a reverse positive bias to the device can, however, extract electrons from the reduced graphene nanosheet, returning it to the initial less-conductive form and programming the device back to the OFF-state (Zhuang et al., 2010). Wu et al. fabricated GO-polyimide (PI) hybrid RRAM cells, as shown in Fig. 14 (Wu et al., 2011). The functionalization of GO sheets with PI enables the layer-by-layer fabrication of a GO-PI hybrid resistive-switch device and leads to high reproducibility of the memory effect. The current-voltage curves for the as-fabricated device exhibit multilevel resistive-switch properties under various reset voltages. The capacitance-voltage characteristics for a capacitor based on GO-PI nanocomposite indicate that the electrical switching may originate from the charge trapping in GO sheets. The high device-to-device uniformity and unique memory properties of the device make it an at-

tractive candidate for applications in next-generation high-density nonvolatile flash memories (Wu et al., 2011). Yu et al. reported bistable resistive switching characteristics for write-once-read-many-times (WORM) memory devices using a supramolecular hybrid route to hydrogen-bonded block copolymers (BCP) and GO as charge storage materials (Yu et al., 2012). The ITO/7 wt% GO composite/Al device exhibits a one-time programmable effect with an ON/OFF ratio of 10^5 at –1.0 V, a retention of 10^4 s and a 10^8 read pulse of –1.0 V, as shown in Fig. 15 (Yu et al., 2012). The switching phenomena were attributed to the charge trapping environment operating across the BCP/GO interface and from the GO intrinsic defect. Controlling the physical interaction of BCP and functional GO sheets can generate a well-dispersed charge storage composite device for future flexible information technology.
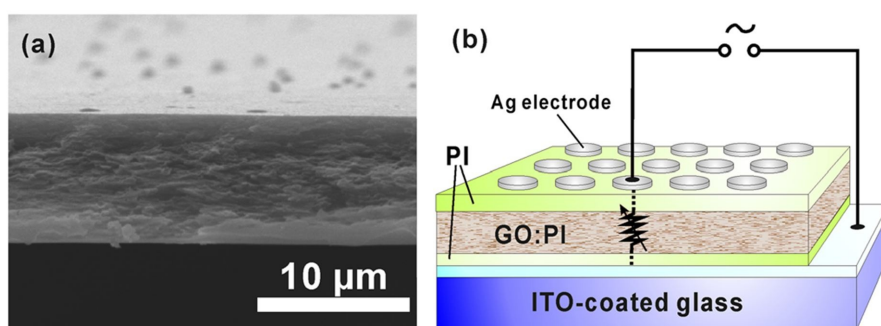

Figure 14. (a) FE-SEM image of the cross sectional view for the GO-PI film. (b) Schematic of Ag/PI/GO:PI/PI/ITO memory device. (Wu et al., 2011)

Recently, Hu et al. prepared a novel RRAM device based on reduced GO noncovalently functionalized by thionine (Hu et al., 2012). The device shows nonvolatile resistive switching behaviors with an ON/OFF ratio of more than 10^4, fast switching speed of <5 ns, long retention time of >10^5 s, and good endurance. The resistive switching in such memory device is attributed to electron transfer reaction between reduced graphene oxide sheets and thionine molecules.

Noting that besides GO, graphene can also be used for resistive switching memory devices. Standley et al. developed a nonvolatile resistive memory element based on graphene break junctions which demonstrates thousands of writing cycles and long retention times (Standley et al., 2008). They proposed a model for device operation based on the formation and breaking of carbon atomic chains that bridges the junctions, as shown in Fig. 16 (Standley et al., 2008). Recently, He et al. reported a planar graphene/SiO2 nanogap structure for multilevel resistive switching (He et al., 2012). Such two-terminal devices exhibited excellent memory characteristics with good endurance up to 10^4 cycles, long retention time more than 10^5 s, and fast switching speed down to 500 ns. At least five conduction states with reliability and reproducibility were demonstrated in these memory devices, as shown in Fig. 17 (He et al., 2012). The mechanism of the resistive switching was attributed to a reversible thermal-assisted reduction and oxidation process that occurred at the breakdown region of the SiO_2 substrate.
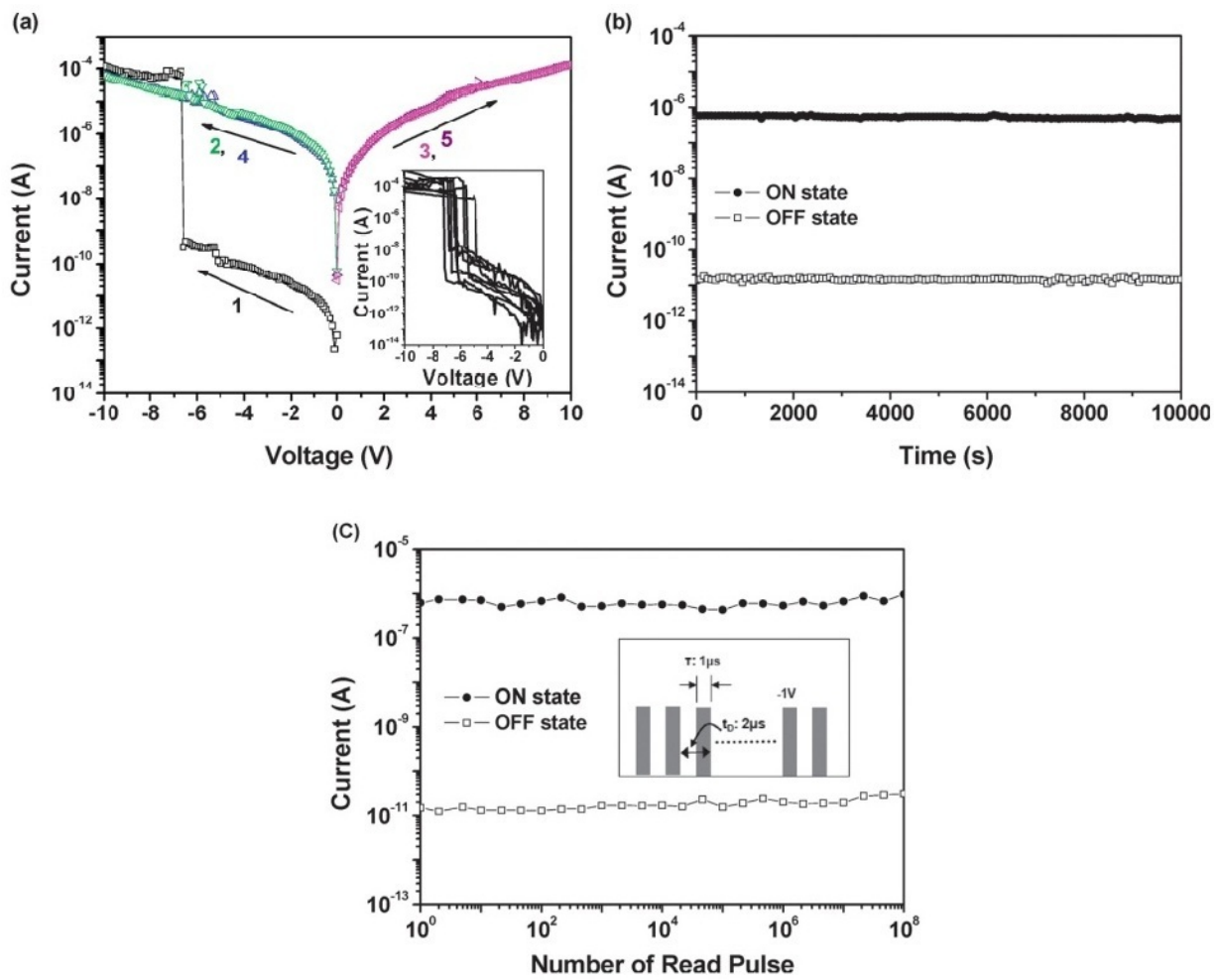
Figure 15. (a) I–V characteristics of 7 wt% GO composite device. The inset shows the switching behavior in different memory cells. (b) Retention time test. (c) Stimulus effect of read pulses. (Yu et al., 2012)
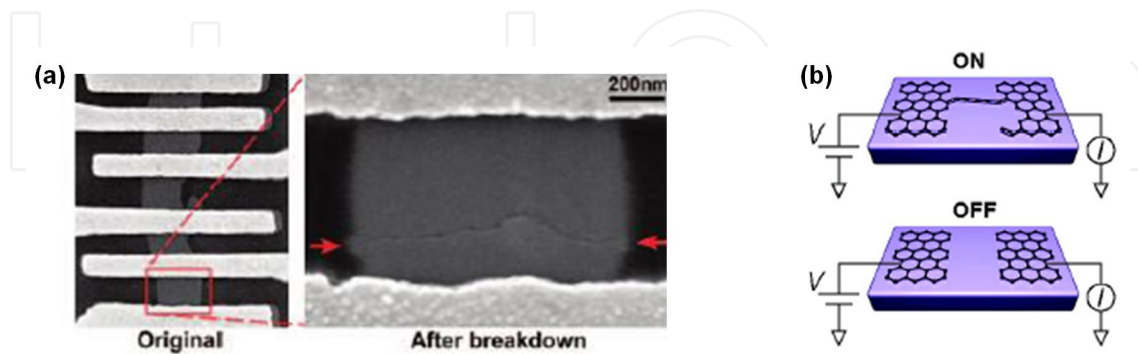

Figure 16. (a) SEM image of the device before (left panel) and after breakdown (right panel). The arrows indicate the edges of the nanoscale gap. (b) Proposed schematic atomic configurations in the ON and OFF states. (Standley et al., 2008)
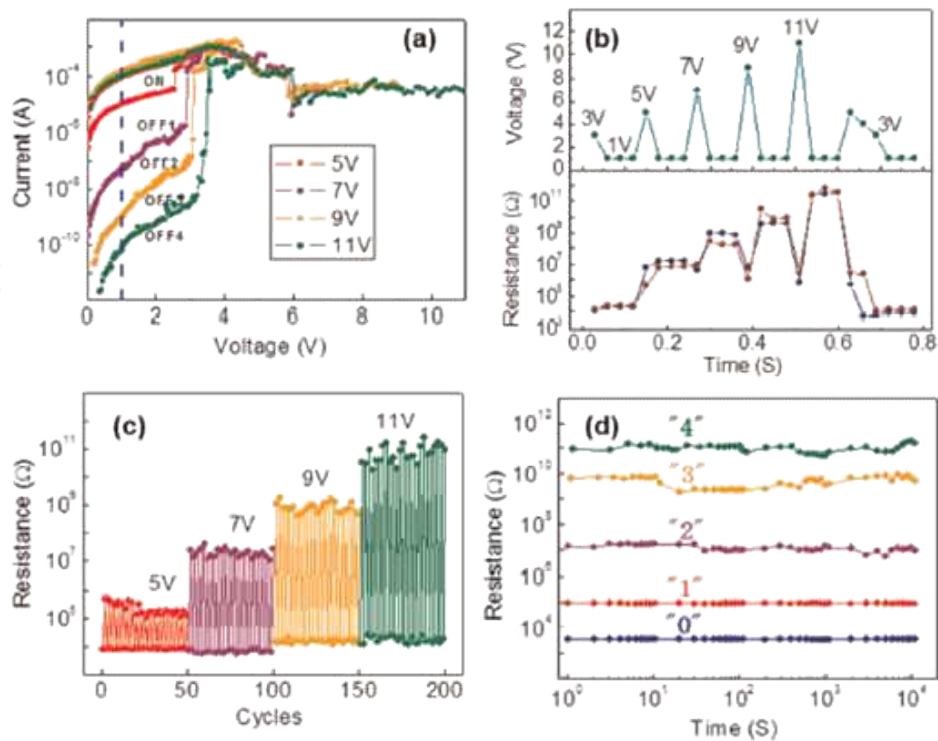
Figure 17. Multilevel resistive switching properties of graphene/SiO$_2$ nanogap structures. (a) Typical I–V characteristics of a device with a width of 1 µm, length of 0.4 µm, and thickness of 2.3 nm. The vertical line cut at 1 V indicates five resistance states. By sweeping the reset voltage from 0 to 5 V, the OFF1 state (red) was established. The subsequent reset voltages sweep up to higher voltage of 7 V (purple), 9 V (orange), and even higher to 11 V (olive) from 0 V, and lower conduction states of OFF2, OFF3, and OFF4 were achieved subsequently. (b) Top: series of bias pulses with different magnitudes of 3, 5, 7, 9, and 11 V, corresponding to the sweep voltages in (a) with three reading pulses of 1 V after each programming pulse was applied. Bottom: resistance changes corresponding to the each voltage pulse in the top panel. (c) Cycled switching of the device under various reset voltages. (d) Retention time of more than 10^4 s for each conduction state tested by a continuous 1 V pulse. (He et al., 2012)

5. Summary and prospect

Resistive random access memory based on the resistive switching effect induced by electrical stimulus has inspired scientific and commercial interests due to its high operation speed, high scalability, and multibit storage potential. The reading of resistance states is nondestructive, and the memory devices can be operated without transistors in every cell, thus making a cross-bar structure feasible. Although a large variety of solid-state materials have been found to exhibit the resistive switching effect, GO is a very promising material for RRAM applications since due to an ultrathin thickness (~1 nm) and its unique physical–chemical properties. Both GO and GO-polymer hybrid exhibit good memory performances, such as high ON/OFF ratio and long retention time. The resistive switching of GO is always related to defect migration, such as metal ions and oxygen vacancies, whereas the switching of GO-polymer hybrid is considered to be attributed to charge transfer reaction between GO sheets and polymer molecules. Since both high switching speed and good retention could be

simultaneously achieved in GO-polymer hybrid RRAM device, such memory device is expected to overcome the "voltage–time dilemma" (i.e., one could not realize high write/erase speed and long retention time simultaneously in pure electronic mechanism-based RRAM cells). Pure electronic mechanisms in RRAM cells postulate the trapping and detrapping of electron in immobile traps as the reason for the resistance changes, also known as Simmons & Verderber model. While in GO-polymer hybrid systems, the electron transfer occurs between graphene sheets and functional molecules covalently or non-covalently bonded to graphene, which may avoid the "voltage–time dilemma".

However, to meet the requirements of future memory applications, GO-based resistance memories should overcome several hurdles. Firstly, the size and chemical composition of GO sheets must be controllable, for example, the type, number and distribution of oxygen functional groups attached to both sides of graphene sheets. Secondly, the resistive switching mechanism of GO is still not clear. For metal/GO/metal sandwiches, although the formation/rupture of metal filaments is considered to be responsible for the resistive switching, the filament growth and inhibition kinetics remains ambiguous. As to the switching of GO-polymer hybrid, no direct evidences have been provided to support the charge transfer hypothesis so far. Thirdly, it is a real challenge to improve the thermal stability of GO and GO-polymer hybrid since memory devices may work at elevated temperature.

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