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Chapter 11

Design of Multi Gb/s Monolithically Integrated Photodiodes and Multi-Stage Transimpedance Amplifiers in Thin-Film SOI CMOS Technology

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Additional information is available at the end of the chapter

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1. Introduction

The development of new integrated high-speed Si receivers is requested for short distance optical data link and emerging optical storage (OS) systems, notably for the Gb/s Ethernet standard [1] - [8] and Blue DVD (Blu-Ray, HDDVD) [3], [4], [9]. As requirements on bandwidth, gain, power consumption as well as low read-out noise and cost are quite severe, an optimal design strategy of a monolithically integrated solution, i.e. with on-chip photodetector and transimpedance amplifier (TIA), is required.

In optical communication, however, non integrated detectors are usually employed [2] - [8] since the particular indirect energy band properties of Silicon make this semiconductor not very efficient for optical reception at 850nm wavelength. As Si is the most widely used and low cost semiconductor material in electronics and due to the availability of low-cost 850nm transmitters, there is yet a great interest and challenge to integrate such receivers. 1 to 10 Gb/s, high sensitivity and low complexity, low-cost silicon photodetectors for the monolithic integration of optical receivers for short distance applications at 850nm are really an issue as the Si absorption thickness required for high-speed (low transit time and low capacitance) favors thin-film technologies for which the responsivity is low. Some solutions exist but at the price of more costly and complex fabrication processes [10-16]. At the system level, owing to its low dark current (pA range) [17], low capacitor (10fF) for the photodetector [1] and possibility to integrate this detector with high-performance low-capacitance transistors, global thin-film SOI monolithically integrated photoreceivers have

potentially higher gain and lower noise performances which in turn, as we will show here, can increase the IC-sensitivity and alleviate this requirement on the photodetector itself. Furthermore only SOI photodiodes have so far achieved bandwidth compatible with the 10Gb/s specification and even higher data rate among the "easy to integrate" Si photodetectors [1], [15], [16] and [18].

In the blue and UV wavelengths, these diodes achieve a high responsivity [17] and then combine all the advantages of high speed, low dark current and finally high sensitivity [1]. This makes SOI receivers the best candidate for blue DVD applications and future optical storage generation. This also suggests that blue wavelength for multi Gb/s short reach optical communication could be used in a near future under the condition that the recent progresses in blue emitting sources make them available [17, 19].

We present here a top-down design methodology, fully validated by Eldo circuit simulations [20] and experimental measurements, which allows to predict and optimize, starting from the speed requirements and the technological parameters, the architecture and performances of the receiver. Our approach generalizes the one proposed in [21] to all inversion regimes. In addition our design strategy is based on the $\frac{gm}{id}$ methodology [22] and allows one to optimize the diode and the transimpedance in a simultaneous way. Thanks to this modeling and the low capacitance of thin-film integrated SOI photodiodes, we have optimized various monolithic optical front-end suitable for 1 to 10 Gb/s short distance communication or Blue DVD applications that show the potentials of $0.13\mu m$ Partially-Depleted (PD) SOI CMOS implementation in terms of gain, sensitivity, power consumption, area and noise.

In section 2 (Optical Receivers Basics), the simple resistor system is first presented as well as its limitations. The transimpedance amplifier is then introduced and its basic theory and concepts such as transimpedance gain, bandwidth and stability are derived. Important parameters to compare transimpedance amplifiers are also discussed as well as architectures most often used in the high speed communication area. Then in section "Design of Multistage Transimpedance Amplifiers", we present our top-down methodology to design transimpedance amplifiers in the case where the voltage gain of the voltage amplifier used in the TIA is independent of the feedback resistor R_f. This is usually the case when the TIA bandwidth is not too close to the transistors frequency limit f_t of a given technology and leads to a multi-stage approach. Our design procedure is then applied to the design of a 3 stages 1GHz bandwidth transimpedance amplifier in a 0.13 μm PD-SOI CMOS technology. Finally, in section "Single stage Transimpedance Amplifier Modeling", we present a top-down methodology to design transimpedance amplifiers when the voltage gain depends on R_f. This is the case for very high-speed single-stage transimpedance amplifiers. Our design procedure is then applied to the design of a single stage 10GHz bandwidth transimpedance amplifier in a 0.13 μm PD-SOI CMOS technology and to the design of a 1GHz bandwidth single stage TIA in a 0.5 μm FD-SOI CMOS technology.

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2. Optical Receivers Basics

2.1 The simple Resistor Optical Receiver

The optical receiver is a key element in the optical link. It performs the optical to electrical conversion. The receiver consists of a photodetector followed by a preamplifier and eventually one or more post-amplifiers. The performance of an optical receiver is mainly determined by the preamplifier - photodiode combination. In high-speed communication links, the two most important specifications are speed and sensitivity. In many cases, the speed is fixed by the application, while the sensitivity has to be maximized. The ultimate limitation is noise. The main noise sources are the photodiode and the preamplifier. In a good design, the latter contribution is minimal. Little noise is added when no active components are used in the preamplifier. This is the case for the simplest preamplifier possible presented in fig. 1a: a simple resistor R_L that performs both the current - voltage conversion and the preamplification. In this figure, the simple receiver is followed by a buffering amplifier with gain A. Its major drawback is the limited maximal achievable bandwidth when low noise is important. For an input current i_{ph}, the output voltage of the simple optical receiver of fig. 1 a) is given by:

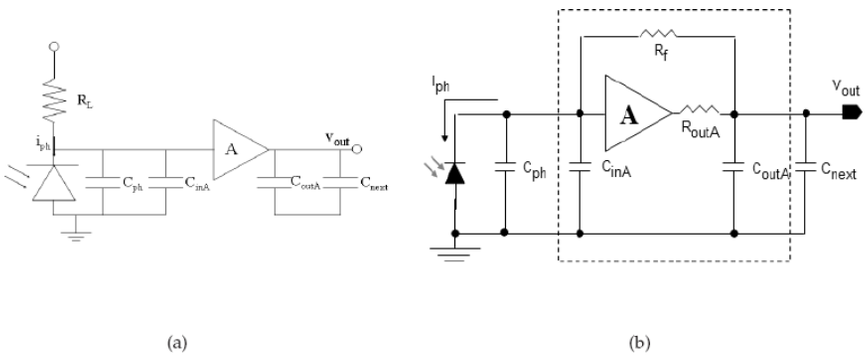

Figure 1. a) Simple photodiode-resistor receiver, followed by a voltage amplifier. b) Transimpedance Amplifier.

$$v_{out} = R_L \,.i_{ph} \,.\left(\frac{1}{1 + s.R_L \,.(C_{ph} + C_{inA})}\right).A \tag{1}$$

in which C_{ph} is the total photodiode capacitance and C_{inA} is the input capacitance of the voltage amplifier. The bandwidth of this simple receiver is thus given by:

$$BW_{Rdiode} = \frac{1}{R_L \,.(C_{ph} + C_{inA})} \tag{2}$$

The bandwidth is limited by C_{ph} which is often much bigger than C_{inA} and the transimpedance-gain R_L of the very first stage. As a result, the required bandwidth constrains the max-

imal transimpedance-gain R_L and accordingly the achievable sensitivity of this receiver. Indeed, the equivalent input noise current spectral density of this front-end is given by [21]:

$$\overline{di_{eq,R}^2}(w) = \frac{4.kT}{R_L} + \frac{|1 + s.R_L.(C_{ph} + C_{inA})|^2}{R_L^2}.Svg_{Amp}^2 \tag{3}$$

in which the first term is due to the resistor and the second term to the voltage amplifier. The noise of the latter is concentrated in the equivalent spectral density voltage source at the gate of the input transistor, Svg_{Amp}. As the noise is inversely proportional to R_L, low-noise operation implies that the pole is located at a relatively low frequency. This receiver is therefore not suitable for high speed communication applications. To achieve high speed in combination with a large resistor, the latter is used as a feedback resistor with an inverting voltage amplifier. The resulting structure is a transimpedance amplifier.

2.2 The Transimpedance Amplifier

The transimpedance amplifier (TIA) (fig. 1b) is the most widely used preamplifier for high-speed optical receivers. It is based on an inverting voltage amplifier with open-loop gain A and a feedback resistor R_f to convert and amplify the input current i_{ph} from a photodiode to an output voltage v_{out}. The transimpedance amplifier is a circuit with shunt-shunt feedback. As a general rule, this reduces both the amplifier input and output impedances by the loop-gain of the amplifier [23]. In turn, this reduction of input impedance allows one for improving the sensitivity and speed trade-off, we faced in the simple resistor amplifier. In this section, various important aspects of transimpedance amplifiers are analyzed.

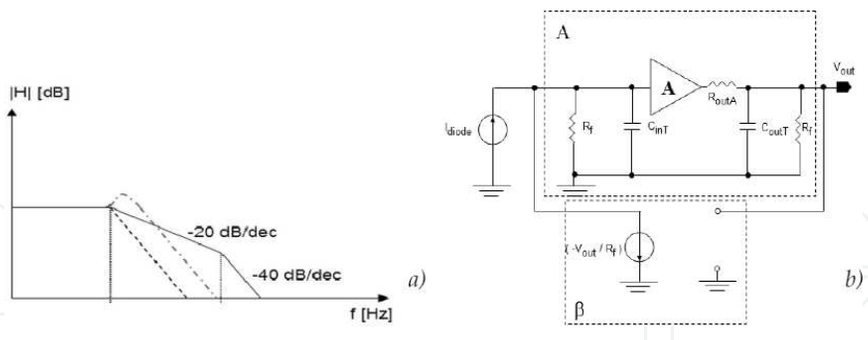

Figure 2. a) Frequency response shape for 2 distant (⁇, close (peaking) (-⁇, and complex conjugate(- -) poles and b) Transimpedance Amplifier divided in direct and feedback paths.

2.2.1 Bandwidth of the Transimpedance Amplifier

To analyze the TIA frequency behavior, the most important capacitors have been included in fig. 1b. The total input capacitance of the circuit C_{inT} consists of the photodiode capacitance C_{ph}, eventually with its associated parasitics, and the voltage amplifier input capacitance C_{inA}. The output capacitance C_{outT} is the sum of the amplifier output capacitance C_{outA}

http://dx.doi.org/ 10.5772/50531

and the input capacitance of the subsequent stage, C_{next}. The closed-loop transimpedance-gain is given by:

$$Z_{cl}\frac{v_{out}}{i_{ph}}=\frac{\frac{A}{A+1}.R_f-\frac{R_{outA}}{A+1}}{1+s.\left(\frac{(R_f+R_{outA}).C_{inT}}{A+1}+\frac{R_{outA}.C_{outT}}{A+1}\right)+s^2.\frac{R_f.C_{inT}.R_{outA}.C_{outA}}{A+1}} \tag{4}$$

For a well designed voltage amplifier with sufficiently large gain A and small output impedance R_{out} this can be simplified to:

$$Z_{cl}\simeq\frac{R_f}{1+s.\left(\frac{R_f.C_{inT}}{A}+\frac{R_{outA}.C_{outA}}{A}\right)+s^2.\frac{R_f.C_{inT}.R_{outA}.C_{outA}}{A}} \tag{5}$$

This compares well with the simplified transfer function of a system with two well separated real poles p_1 and p_2, which is given by [24]:

$$T_2\simeq\frac{T_o}{1+\frac{s}{p_1}+\frac{s^2}{p_1.p_2}} \tag{6}$$

The TIA dominant pole p_1 can theoretically be situated either at the input or at the output node. In between those two extreme cases, both poles approach each other and give rise to a complex conjugated pole pair. This intermediate poles placement is best avoided as it results in a bump in the frequency response with overshoot and long settling times of the transients [24] (see also fig. 2a).

In the case of high speed circuits where the diode capacitance C_{ph} usually dominates the other capacitances and where we try to have the resistance R_f value as high as possible to increase the transimpedance-gain, the dominant pole is usually located at the input node and the transimpedance bandwidth is then given by:

$$BW_{trans}\simeq\frac{A}{R_f.C_{inT}} \tag{7}$$

Comparing this bandwidth with that given by the simple resistor amplifier one (eq. 2), we see an improvement by a factor A of the transimpedance-gain-bandwidth product of the transimpedance amplifier. This means that for a given bandwidth, a TIA will have a transimpedance gain increased by A compared to the simple resistor amplifier. To be stable the gain A has however to be constrained, as we will see below.

2.2.2 Stability of the Transimpedance Amplifier

As the transimpedance amplifier contains a feedback loop, its stability has to be assured. To analyze this problem, the shunt-shunt feedback amplifier is presented by its equivalent circuit of fig. 2b [23]. From this figure, the open-loop gain and the feedback factor are easily derived:

$$T_{openLoop} \simeq -A.R_f \cdot \frac{1}{1+s.R_f.C_{inT}} \cdot \frac{1}{1+s.R_{outA}.C_{outT}} \beta = -\frac{1}{R_f} \tag{8}$$

The loop gain, which is an important factor in the amplifier stability analysis is given by:

$$T_{loop} = T_{openLoop}.\beta \simeq A.\frac{1}{1+s.R_f.C_{inT}} \cdot \frac{1}{1+s.R_{outA}.C_{outT}} \tag{9}$$

To obtain a stable system, the non-dominant pole of the amplifier loop gain has to be sufficiently higher than the 0 dB crossing frequency, which is given (the dominant pole is assumed at the input node) by:

$$w_{T_{loop},0dB} \simeq \frac{A}{R_f.C_{inT}} \tag{10}$$

The latter is equal to the TIA closed-loop bandwidth (Eq. 7). Actually, the equivalence of these two equations demonstrates that a TIA behaves as a voltage amplifier in unity-gain feedback configuration. The stability analysis of both structures is therefore identical [21]. To achieve a reasonable phase-margin, non-dominant poles have to be sufficiently higher than the receiver bandwidth. This implies for the second pole in this structure [24]:

$$\frac{1}{R_{outA}.C_{outT}} \geq X_A \cdot \frac{A}{R_f.C_{inT}} \tag{11}$$

where X_A is a factor ranging from 2 to 3 depending on the required phase margin [25]. In general, some extra poles may be present on the internal nodes of the voltage amplifier. These must obviously also be considered during the design and be placed at sufficiently high frequencies to guarantee stability. These requirements ultimately limit the maximal achievable transimpedance-gain and bandwidth.

To summarize, the transimpedance amplifier allows one, owing to its feedback mechanism, to increase the frequency of the dominant pole to a value that is A times higher that the one we would have with a simple resistor. However, by increasing the gain A, the dominant pole approaches the second pole. In order to avoid stability problems, we have to limit the gain A such that the dominant pole stays around 3 times smaller that the second pole (the factor 3 corresponds to the classical 60° phase margin condition in open loop configuration).

http://dx.doi.org/ 10.5772/50531

2.3 Comparison of Transimpedance Amplifiers

In analogy with the gain-bandwidth product used for an amplifier, the transimpedance-gain (R_f) - bandwidth (BW_{trans}) product or ZBW has been proposed as the parameter that measures both the speed and the sensitivity performance of the transimpedance amplifier [21]:

$$ZBW \simeq Rf\,.BW_{trans} \simeq \frac{A}{C_{inT}} \tag{12}$$

In a given device, ZBW is a constant. This tells us that, to some extent, transimpedance gain can simply be traded for bandwidth and vice-versa by tuning the feedback resistor. This substitution is only limited by stability considerations. The maximal achievable bandwidth has to be a factor smaller than the first non-dominant pole of the receiver to maintain sufficient phase-margin. This factor of merit also emphasizes the need in critical high speed applications for photodiodes integrated on chip along with the receivers which can reduce the photodiode capacitance drastically (by a factor up to ten times) by removing the bonding capacitor. SOI has here an advantage over other Si integrated technologies for high speed applications (e.g. 10 GBps) because both the photodiode and the amplifier will have smaller capacitances, and also because SOI photodiodes themselves can achieve such high transit time frequencies [1].

2.4 Architecture of Transimpedance Amplifiers

Transimpedance amplifier may differ by the kind of voltage amplifiers they use. In the high-speed communications field, two amplifier architectures are mostly used: the single transistor voltage amplifier (STVA) and the CMOS inverter used as an amplifier. A three stages TIA version of both cases is shown in fig. 3a and b. The inverter case has the advantage of auto biasing (the current depends on the gate voltage and the size of the P and NMOS transistor) and then requires no additional bias circuit. The inverter based amplifier has, however, less design flexibility as the gate voltages of the PMOS and NMOS transistors are equal, on the contrary to the case of the SVTA circuit. In very high speed applications, in order to improve crosstalk immunity, differential versions of the transimpedances are also employed and then differential pairs or two single inverters with a dummy branch can be used [26], [27] and [7].

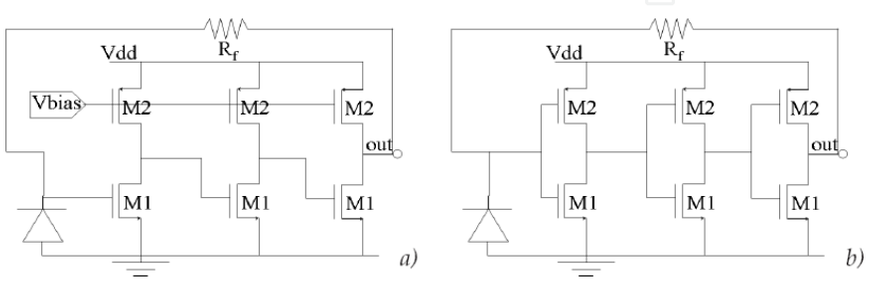

Figure 3. Schematic view of a 3 stages a) SVTA and b) CMOS inverter TIA.

One can distinguish different type of TIAs by their number of stages. Typical designs use either a single-stage or multi-stage approach. It can be shown [21] and will be further developed that applications requesting a high bandwidth compared to the technology's f_t are limited to single-stage amplifiers as there is no room for placing the extra poles that are inevitably introduced by the multiple-stage designs. However, for frequencies at least 20 to 30 times lower than f_t, a multi-stage design is the way to go.

3. Design of Multistage Transimpedance Amplifiers

3.1 Optimizing the number of stages of STVA transimpedance amplifiers

We will now describe our methodology to optimize the stages number N that maximizes the voltage gain in transimpedance amplifiers based on N identical STVA amplifiers. It is based on the $\frac{gm}{id}$ methodology and generalizes to all regimes of inversion the methodology of Ingels [21] that was developed for strong inversion (when we can assume that $C_{gs} = \frac{2}{3} \cdot C_{ox}$). Extension to the CMOS Inverter or the differential pair TIA is quite straightforward. The gain of a single SVTA stage is given by:

$$A_{Nsi} = \frac{gm_1}{gout} = \left(\frac{gm}{Id}\right) 1.V_{ea}.L_{eq} \tag{13}$$

where V_{ea} is the Early voltage by μm of length and L_{eq} is an equivalent length in μm. In the case of the amplifier of figure 3a, we have:

$$L_{eq} = \frac{L_1.L_2}{L_1 + L_2} \tag{14}$$

The whole gain of the amplifier is then:

$$A_{Ns} = A_{Ns_i}^N \tag{15}$$

For the single stage amplifier, with the dominant pole at the input and only one non-dominant pole at the output, the condition of stability was given by eq. 11. In the case of a multi-stages amplifier, we now have a multiple pole roll-off. To achieve same phase margin with a N pole roll-off than with a single pole, we must now place each of these N poles at a frequency $X_N.X_A$ higher than the dominant pole frequency. X_N is given by [21]:

$$\arctan\left(\frac{1}{X_A}\right) = N.\arctan\left(\frac{1}{X_N.X_A}\right) \tag{16}$$

http://dx.doi.org/ 10.5772/50531

As X_A has to be larger than 2 to 3, X_N is approximately equal to N while:

$$\tan(x) \simeq x \quad x \ll 1 \tag{17}$$

As a result, the ith stage bandwidth of the N-stages voltage amplifier used in a TIA has to be at least (the drain capacitance of transistor M2, C_{d_2} has been neglected here. This will be addressed latter):

$$BW_{Ns_i} = \frac{g_{out_i}}{C_{d_{1,i}} + C_{gs_{1,i+1}}} \geq X_N . X_A . BW_{trans} \tag{18}$$

By multiplying both sides of this equation by the gain of 1 stage, A_{Ns_i}, and isolating the gain on the right side, we obtain that to be stable the gain of 1 stage has to be lower than:

$$A_{Ns_i} \leq \frac{GBW_{NS_i}}{X_N . X_A . BW_{trans}} \tag{19}$$

GBW_{Ns_i} is the gain-bandwidth product of an individual stage i:

$$GBW_{NS_i} = A_{Ns_i} . BW_{Ns_i} = \frac{gm_{1,i}}{C_{d_{1,i}} + C_{gs_{1,i+1}}} \tag{20}$$

By introducing:

$$ft = \frac{gm_1}{2\pi C_{gs_1}} = \frac{\frac{gm}{Id_1} i_{dn1}}{2\pi C_{gso_1} L_1^2} = \frac{f_1\left(\left(\frac{gm}{Id}\right)_1\right)}{L_1^2} \tag{21}$$

$$X_C \simeq \frac{C_{d_1}}{C_{gs_1}} = \frac{C_{ox}.l_{ov} + C_{xjo}.X_j + C_{dgo_1}.L_1}{C_{gso_1} L_1} = f_2((\frac{gm}{Id})_1, L_1) \tag{22}$$

where the parameter f_t in function of the normalized drain current, i_{dn}, or of the parameter gm/Id, is a technological curve for a given length which tends towards a maximum in strong inversion. X_C is also a technological curve which depends on the transistor inversion degree and is minimum in strong inversion. We can then rewrite GBW_{Ns_i} and the stability condition on the maximum value of the gain as a function of a technological curve *vs*. the inversion degree of the transistor:

$$GBW_{NS_i} = \frac{2.\pi . f_t}{1 + X_C} \tag{23}$$

$$A_{N\,s_i} \leq \frac{2.\pi.f_t}{(1+X_C).X_N.X_A.BW_{trans}} \tag{24}$$

This last equation combined with the equation of the gain A_{Ns_i} (eq. 13) allows us to write the following condition on $\left(\frac{gm}{Id}\right)_1$ for a given BW_{trans}, a given N, and a given X_A:

$$\left(\frac{gm}{Id}\right)_1 \leq \frac{2.\pi.f_t}{(1+X_C).X_N.X_A.BW_{trans}.V_{ea}.L_{eqi}} = f_{Nstab}\left(\left(\frac{gm}{id}\right)_1\right) \tag{25}$$

This implicit equation of $\left(\frac{gm}{Id}\right)_1$ can be solved recursively. We start with a minimum value of $\left(\frac{gm}{Id}\right)_1$, imposed when the gate to source voltage is at is maximum value, i.e. Vdd, compute f_{Nstab} for this $\left(\frac{gm}{Id}\right)_1$ and then compare the two values. If $\left(\frac{gm}{Id}\right)_1$ is lower than f_{Nstab}, we then increase $\left(\frac{gm}{Id}\right)_1$, compute a new f_{Nstab} and compare and iterate while $\left(\frac{gm}{Id}\right)_1$ stays lower than f_{Nstab} or while $\left(\frac{gm}{Id}\right)_1$ is lower than the maximum $\left(\frac{gm}{Id}\right)_1$ available in the technology. In this last case the gain will not be limited by the stability but by the feasibility.

The method is illustrated graphically in fig. 4. As the f_{Nstab} vs. $\left(\frac{gm}{Id}\right)_1$ curves are shifted down by increasing N, the optimal value of $\left(\frac{gm}{Id}\right)_1$, i.e. $\left(\frac{gm}{Id}\right)_{1_{\max}}$, related to the maximum voltage gain decreases with the number of stages. The gain of each single stage is then decreased (eq. 13), while the overall gain can still increase as we add more stages (eq. 15). We see that in term of voltage gain, an optimal value of stages N_{opt} exists. In fig. 4a, we can see that for a bandwidth of 1GHz in a typical 0.13μm PD-SOI technology, eq. 25 features a solution in terms of $\left(\frac{gm}{Id}\right)_{1_{\max}}$ for N greater than 1 owing to the sufficient value of the ratio f_t over $f_{t_{trans}}$ (This ratio is not constant over the $\left(\frac{gm}{Id}\right)_1$ range but is around 130 for its maximum value ($f_{t_{max}}/f_{t_{trans}}$)). Therefore, the curve of $\left(\frac{gm}{Id}\right)_{1_{\max}}$ vs. N can be calculated (fig. 5 (a)). The total voltage gain, A_{Ns}, vs. N and the optimal number of stages, N_{opt}, can be deduced from there (fig. 5 (b)). In the case of fig. 5 (b), N_{opt} is equal to 9. In the case of fig. 4b, if we increase the transimpedance bandwidth specification to 10 GHz and then work at $f_{t_{max}}/f_{t_{trans}}$ ratio of about 10, eq. 25 has no solution for N greater than 1 and N_{opt} is then equal to 1 (To have stable solutions for N greater than 1 would require in fact to have $\left(\frac{gm}{Id}\right)_1$ lower than its minimum value).

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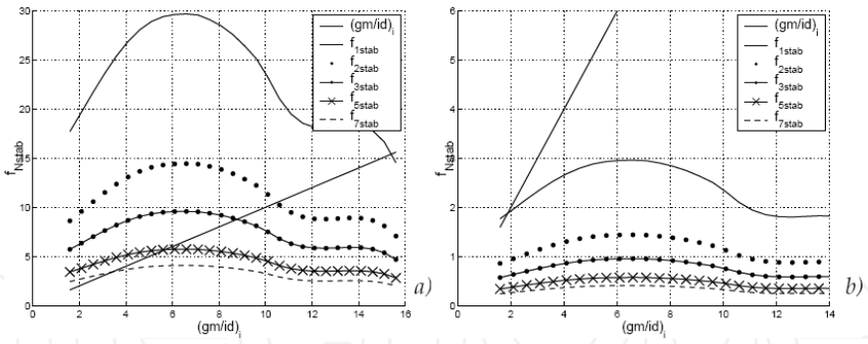

Figure 4 {a) f_{Nstab} vs.$\left(\frac{gm}{Id}\right)_1$ (eq. 25) for BW_{trans}=2.π.1GHz, X_A=3 and ST 0.13μm PD-SOI technology. While the $\left(\frac{gm}{Id}\right)_1$ curve is below the f_{Nstab} curve, the system is stable. The optimal $\left(\frac{gm}{Id}\right)_1$ that is related to the maximum voltage gain is at the intersection of these two curves. As the f_{Nstab} curves are shifted down by increasing N, the optimal value of $\left(\frac{gm}{Id}\right)_1$ decreases with the number of stages. b) same but for BW_{trans}=2.π.10GHz. As the f_{Nstab} curves have been shifted down by a factor of 10 due to the 10 times higher transimpedance bandwidth compared to a), increasing N is not possible any more and only a single stage transimpedance with low $\left(\frac{gm}{Id}\right)_1$ can fulfill the stability requirements.

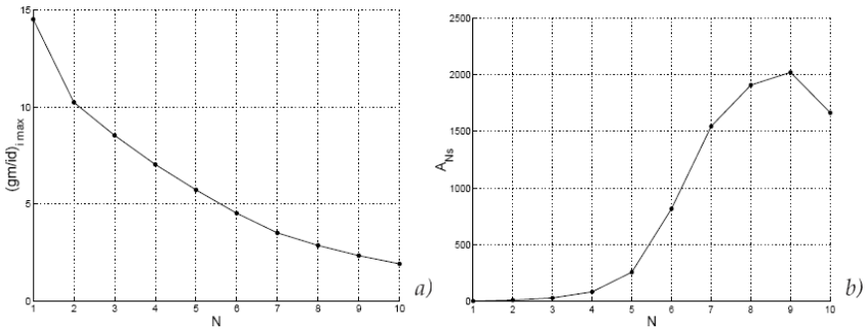

Figure 5. a) Evolution of $\left(\frac{gm}{Id}\right)_{1_{max}}$ and b) total amplifier voltage gain A_{Ns} (b) vs. N for BW_{trans}=2.π.1GHz, X_A=3 and ST 0.13μm PD-SOI technology.

3.2 Current mirror impact on optimal stages number and gain

We have neglected so far the current mirror drain capacitance, C_{d_2}, in the calculation of the output pole as it gave us useful indications on the maximal gain vs. the number of stages for a given transimpedance bandwidth without having to choose neither W1 nor W2. However, C_{d_2} can lead to significant and unacceptable loss in phase margin. As the drain currents of M1 and M2 are the same, we can relate W2 to W1 by:

$$W2 = \frac{i_{dn1}}{i_{dn2}} \cdot \frac{L\ 2}{L\ 1} . W1 \tag{26}$$

and then introduce a factor X_{C2} independent of W1 and W2 to add to Xc:

$$X_{C2} \simeq \frac{C_{d_2}}{C_{gs_1}} = \frac{C_{gdo_2}.L_2 + C_{ox}.l_{ov} + C_{xjo}.X_j}{C_{gso_1}L_1}.\frac{i_{dn1}}{i_{dn2}}.\frac{L_2}{L_1}$$
$$X_{C2} = f\left(\left(\frac{gm}{Id}\right)_1, \left(\frac{gm}{Id}\right)_2, L_1, L_2\right) \tag{27}$$

As L1 and L2 are usually kept to their minimum value in order to minimize capacitances and area and to maximize speed performances, the maximum value of $\left(\frac{gm}{Id}\right)_1$ has now a dependency on $\left(\frac{gm}{Id}\right)_2$ due to the term X_{C2}:

$$\left(\frac{gm}{Id}\right)_1 \leq \frac{2.\pi.f_t}{(1 + X_C + X_{C2}).X_N.X_A.BW_{trans}.V_{ea}.L_{eq_i}} = f^*_{Nstab}\left(\left(\frac{gm}{Id}\right)_1, \left(\frac{gm}{Id}\right)_2\right) \tag{28}$$

The selection of $\left(\frac{gm}{Id}\right)_2$ results in a trade-off between dynamic range and other performances. To keep W2 small compared to W1, and then keep negligible the effect of the degradation of X_{C2} on $\left(\frac{gm}{Id}\right)_{1_{max}}$, and thus on the gain and on R_f, we see that we need i_{dn2} to be large compared to i_{dn1}. This implies to have $\left(\frac{gm}{Id}\right)_1$ larger than $\left(\frac{gm}{Id}\right)_2$ and bias the mirror in strong inversion. However, this reduces the dynamic range by increasing the saturation voltage of the mirror Vds_{sat_2}. In strong inversion, the latter can be approximated by:

$$Vds_{sat_2} = \frac{2}{\left(\frac{gm}{Id}\right)_2} \tag{29}$$

Once $\left(\frac{gm}{Id}\right)_2$ has been chosen, we can deduce $\left(\frac{gm}{Id}\right)_{1_{max}}$ and the maximum number of stages from the maximum voltage gain as done earlier. As can be seen on fig. 6, the optimal number of stages for the gain is now reduced from 9 to 3 when taking into account the correction due to the capacitance of the mirror. Indeed, $\left(\frac{gm}{Id}\right)_{1_{max}}$ now decreases more rapidly with N as, for a fixed $\left(\frac{gm}{Id}\right)_2$, X_{C2} increases with N due to the decrease of the ratio i_{dn1}/i_{dn2} with $\left(\frac{gm}{Id}\right)_1$. This indicates that the mirror has a more detrimental effect when increasing the number of stages, which can be observed when comparing the values of $\left(\frac{gm}{Id}\right)_{1_{max}}$ *vs*. N on fig. 6c) and fig. 5b). These values are nearly identical until N=3. This indicates that, as long as its size is kept small because of a good $\left(\frac{gm}{Id}\right)$ ratio, the mirror has a relatively small influence while for N greater than 3, the capacitance of the mirror dominates the output capacitance and totally degrades the

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performances. Once the number of stages has been chosen, we still have to choose W1. This can be done by optimizing noise, area and power consumption.

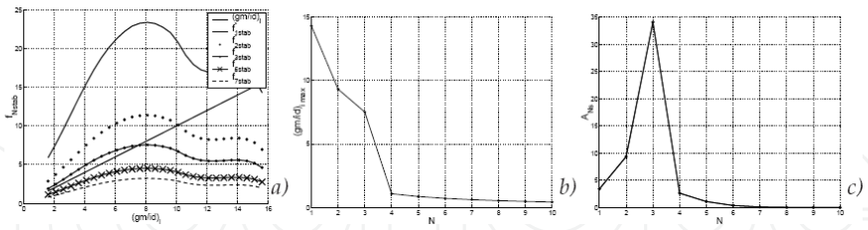

Figure 6. a) f^*_{Nstab} vs. $\left(\frac{gm}{Id}\right)_{i}1$ (eq. 28), b) evolution of $\left(\frac{gm}{Id}\right)_{1_{max}}$, and c) total amplifier voltage gain A_{Ns} vs. N. BW_{trans}=2.π.1GHz, X_A=3, $\left(\frac{gm}{Id}\right)_2$=2.5 V^{-1}, and ST 0.13μm PD-SOI technology.

3.3 Noise

To analyze the TIA noise performance, we have to consider its major noise sources which are the feedback resistor, R_f, thermal noise, modeled by the voltage noise source, $Sv^2_{R_f}$ and the voltage amplifier noise. The latter is concentrated in the voltage noise source at the gate of the input transistor of the amplifier (gate of M1 of the first stage), Svg^2_{Amp} . The power spectral density of the feedback noise source is given by:

$$Sv^2_{R_f}(f)=4kT.R_f \tag{30}$$

For the amplifier power spectral density referred to its input, in a first approximation, we can only take into account the noise of the first stage, as, from stage to stage, the relative importance of the noise of each subsequent stage is approximatively divided by the gain of each preceding stage. Svg^2_{Amp} is then given by:

$$Svg^2_{Amp}(f) \simeq Svg_1^2 + 2.\left(\frac{\left(\frac{gm}{Id}\right)_2}{\left(\frac{gm}{Id}\right)_1}\right)^2.Svg_2^2 \tag{31}$$

where Svg_1^2 and Svg_2^2 are the power spectral densities of the equivalent voltage noise sources at the gate of first stage transistors M1 and M2 respectively. A factor 2 was introduced for Svg_2^2 terms, as we assumed that M2 was biased by an identical mirror transistor. In transimpedance design where the TIA bandwidth is usually high compared to the corner frequency, i.e. the frequency at which the 1/f noise of the transistors becomes negligible in comparison with the thermal noise, we can neglect the 1/f terms in Svg_i^2 and express:

$$Svg_i^2(f) \simeq Svg_{1_{th}}^2 = \frac{4kT}{gm_i}.n.\alpha\alpha = \frac{2}{3+\left(\left(\frac{gm}{id}\right)_i.n.U_t\right)^2} \tag{32}$$

where the parameter α has the well known 2/3 value in strong inversion and 1/2 in weak inversion [28]. We then derive:

$$Svg_{Amp}^2(f) \simeq \frac{4kT}{gm_1}.n.\alpha_1.\left(1+2.\frac{\left(\frac{gm}{Id}\right)_2}{\left(\frac{gm}{Id}\right)_1}.\frac{\alpha_2}{\alpha_1}\right) = \frac{4kT}{gm_{eq}}.\alpha_1 \tag{33}$$

The total TIA output noise power spectral density is finally given by:

$$Sv_{out}^2(f) \simeq \frac{Sv_{R_f}^2 + \left|1=s.R_f.C_{inT}\right|^2.Svg_{Amp}^2}{\left|1+s.\frac{R_f.C_{inT}}{A_{Ns}}\right|^2.\left|1+s.R_{outA}.C_{outT}\right|^{2.N}} \tag{34}$$

To compare with the noise of the simple resistor system (eq. 3), we can calculate the equivalent input referred current noise power spectral density of the transimpedance amplifier:

$$Si_{in}^2(f) \simeq \frac{4kT}{R_f} + \frac{\left|1+s.R_f.C_{iNT}\right|^2}{R_f^2}.Svg_{Amp}^2 \tag{35}$$

As R_f is A (the voltage gain) times higher than R_L for same bandwidth and same input capacitance, the TIA noise power is reduced by about a factor A. The shape of Svg_{out}^2 vs. f is plotted in fig. 7a. At low frequencies, the noise is usually dominated by the resistor noise ($R_f >> \frac{1}{gm_1}$):

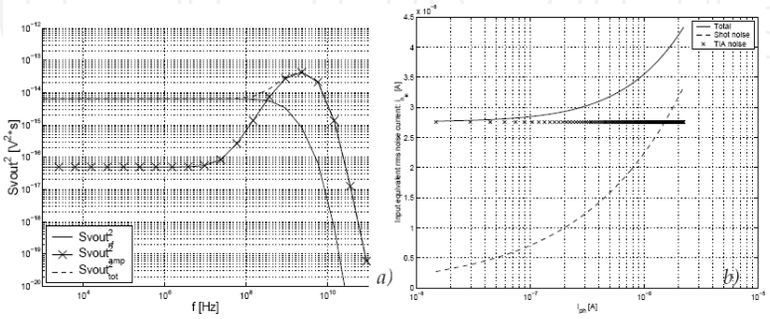

Figure 7. a) $Sv_{out}^2(f)$ vs. f for W1=1μm. b) i_{ph} for W1=4μm. BW_{trans}=2.π.1GHz, X_A=3, $\left(\frac{gm}{Id}\right)_2$=2.5 V^{-1} and ST 0.13μm PD-SOI technology.

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$$Sv_{out}^2(f) \simeq Sv_{out_{Rf}}^2(f) \simeq \frac{Sv_{R_f}^2}{|1+s.\frac{R_f.C_{inT}}{A_{Ns}}|^2.|1+s.R_{outA}.C_{outA}|^{2.N}} \tag{36}$$

However, at medium frequency in the bandwidth of the transimpedance, the amplifier contribution to the noise $Sv_{out_{amp}}^2$ which is:

$$Sv_{out_{Amp}}^2(f) \simeq \frac{|1+s.R_f.C_{inT}|^2.Svg_{Amp}^2}{|1+s.\frac{R_f.C_{inT}}{A_{Ns}}|^2.|1+s.R_{outA}.C_{outT}|^{2.N}} \tag{37}$$

exhibits a zero at the frequency $\frac{1}{2.\pi.R_f.C_{in}}$ which raises it to a maximum plateau value where $Sv_{out_{amp}}^2$ is increased by a factor A_{Ns}^2 compared to its low frequency value in the frequency range between the TIA and amplifier bandwidth. The RMS value of the output noise is given by:

$$v_{n_{out,TIA}} \simeq \sqrt{\int_0^\infty Sv_{out}^2(f)df} \tag{38}$$

To simplify the calculations, as was done in [21], the complete integral is approximated by the sum of three components. They are, respectively:

- the integral of the noise of the feedback resistor, which we can approximate by:

$$v_{n_{out,R_f}}^2 \simeq \int_0^\infty \frac{4kT.R_f}{|1+\frac{jw}{BW_{trans}}|^2}.df \tag{39}$$

Since:

$$\int_0^\infty \frac{1}{1+(\frac{2.\pi}{BW_{trans}}.f)^2}.df = ft_{trans}.[\arctan(\frac{w}{ft_{trans}})]_0^\infty = \frac{\pi}{2}.ft_{trans} \tag{40}$$

we have:

$$v^2_{n_{out,R_f}} \simeq 4kT.R_f.\frac{\pi}{2}ft_{trans} = \frac{kT}{C_{inT}}.A_{Ns} \tag{41}$$

• the integral of the noise of the amplifier up to the transimpedance amplifier bandwidth, which can be approximated by:

$$v^2_{n_{out,Amp1}} \simeq \int_0^{ft_{trans}} |1 + jw.R_f.C_{inT}|^2.Svg^2_{Amp}.df = Svg^2_{Amp}.(ft_{trans} + \frac{ft^3_{trans}}{3}.(2.\pi)^2.R^2_f.C^2_{inT}) \tag{42}$$

This can be rewritten as:

$$v^2_{n_{out,Amp1}} \simeq \frac{kT}{C_{inT}}.\frac{A_{Ns}}{gm_{eq}.R_f}.\alpha_1.\frac{2}{\pi}\left(1 + \frac{A^2_{Ns}}{6.\pi}\right) \tag{43}$$

• the integral of the amplifier noise from the transimpedance amplifier bandwidth up to infinity, which we can approximated by:

$$v^2_{n_{out,Amp2}} \simeq \int_{ft_{trans}}^{\infty} \frac{A^2_{Ns}.Svg^2_{Amp}}{|1 + \frac{jw}{BW_{NS_i}}|^{2.N}}.df \tag{44}$$

Since [29]:

$$\int_0^{\infty} \frac{1}{(1 + (\frac{2.\pi}{BW_{N_{S_i}}}.f)^2)^N}.dw = \frac{2.N-3}{2.N-2}.\int_0^{\infty} \frac{1}{(1 + (\frac{f}{ft_{Ns_i}})^2)^{N-1}}.df \tag{45}$$

by defining:

$$a_n = \prod_{k=2}^{N} \frac{2k-3}{2k-2\,\mathrm{a}} \tag{46}$$

we have:

$$v^2_{n_{out,amp2}} \simeq A^2_{Ns}.Svg^2_{Amp}.\left(a_n\frac{\pi}{2}ft_{N_{S_i}} - ft_{trans}\right) = \frac{kT}{C_{inT}}.\frac{A^3_{Ns}}{gm_{eq}.R_f}.\alpha_1\left(a_n.X_N.X_A - \frac{2}{\pi}\right) \tag{47}$$

Finally, the TIA RMS value of the output noise is given by:

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$$
\begin{aligned}
v_{n_{out,TIA}} &= \sqrt{v_{n_{out,R_f}}^2 + v_{n_{out,amp1}}^2 + v_{n_{out,amp2}}^2} \\
&= \sqrt{\frac{kT}{C_{inT}}.A_{Ns}\left[1 + \frac{\alpha_1}{gm_{eq}.R_f}.\left(\frac{2}{\pi} + A_{Ns}^2\left(a_n.X_N.X_A - \frac{2}{\pi}.\left(1 - \frac{1}{6.\pi}\right)\right)\right)\right]} \\
&= \sqrt{\frac{kT}{C_{eq}}.[1 + f_{amp}]}
\end{aligned}
\tag{48}
$$

The $\frac{kT}{C_{eq}}$ dependency of the noise is usual and conform to the theory of system in feedback loop. To reduce the amplifier contribution (f_{amp}) to the output noise, we see that we need a value of gm_{eq} (and then of gm_1) as well as a value of R_f as high as possible. The RMS value of the equivalent input noise current reduces with R_f and is given by:

$$
i_{n_{in,TIA}} = \frac{v_{n_{out,TIA}}}{R_f} \tag{49}
$$

It can be easily verify that for same bandwidth and same input capacitance, the input noise current reduces by about a factor $\sqrt{A_{Ns}}$. This confirms that the input noise power of the transimpedance amplifier is reduced by about a factor A_{Ns} compared to the simple resistor system. Additional noise sources arise from the photodiode dark current I_{dark}, the dark current shot noise, $in_{in,dark}$ and the photocurrent shot noise itself $in_{in,ph}$. The latter is inherent to the mechanism of photodetection and set the ultimate detection threshold of the ideal detector. We have:

$$
i_{n_{in,ph}} = \sqrt{2.q.I_{ph}.\frac{\pi}{2} f t_{trans}} i_{n_{in,dark}} = \sqrt{2.q.I_{dark}.\frac{\pi}{2} f t_{trans}} \tag{50}
$$

I_{dark} can be calculated from [17] and is, for a typical SOI diode with a total length and width of 50µm, smaller than 10^{-12}A. From eq. 50), this yields a dark current shot noise of around 10^{-11} A for a transition frequency of 1GHz. Both are usually negligible when compared to the other sources of noise. The total input noise is given by:

$$
i_{n_{ic}} = \sqrt{i^2 + i^2 + i^2} \tag{51}
$$

As illustrated in fig. 7b, the transimpedance readout noise usually dominates at low input current, while at high input current it is the photocurrent shot noise that dominates.

3.4 BER, sensitivity and dynamic range

In order to achieve a given BER (Bit Error Rate), i_{ph} must be at least a factor Q times larger than the RMS value of the input noise. For a typical BER of 10^{-12}, Q must be equal to 7.

By definition, the sensitivity, S, is equal to the minimum input power to achieve a given BER. Since i_{ph}=$R.P_{in}$, the sensitivity is given by:

$$S = \frac{7.i_{n_{in}}}{R} \tag{52}$$

where R is the responsivity of the photodiode. It can be calculated with the model developed in [17]. To ensure that the receiver can achieve the required BER, we must have:

$$S \leq P_{in_{\max}} \tag{53}$$

where $P_{in_{max}}$ is the maximum input power before saturation of the receiver (due to its dynamic range limitation). In the dark, the current flowing through R_f is negligible and the output voltage is about equal to the gate voltage of M1. When a photocurrent i_{ph} crosses R_f, the maximum reachable output voltage is Vdd, the supply voltage, minus the saturation voltage of the transistor M2, Vd_{sat_2}. We can derive the maximum photocurrent and from there the maximum input power before saturation of the receiver:

$$I_{ph_{\max}} = \frac{Vdd - Vd_{sat_2} - Vg_1}{Rf} P_{in_{\max}} = \frac{I_{ph_{\max}}}{R} \tag{54}$$

3.5. Power consumption

The power consumption of the TIA is equal to the power consumption of the N stages plus the power consumption of the biasing branch:

$$P_{tot} = (N+1).Vdd.Id = (N+1).Vdd.\frac{W1}{L1}.i_{dn1} \tag{55}$$

For a given W1, the power consumption increases with N due to the increased number of stages but also due to the increase of power consumption per stage related to the decrease of $\left(\frac{gm}{Id}\right)_1$ and the related increase of i_{dn1} with N for for a given transition frequency. Once N and the related $\left(\frac{gm}{Id}\right)_1$ have been chosen, the power consumption linearly increases with W1.

3.6 Diode capacitance Optimization

The diode capacitance C_{ph} must be accounted for when optimizing the detector. As discussed in [1], C_{ph} is proportional to the diode area, A_d, which is fixed by the diameter D of the optical fiber that carries the light signal, and inversely proportional to the length L_i of the intrinsic zone. To decrease this capacitance, we could increase L_i. However this increases the

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transit time of the carriers in the diode and thus decreases its cut-off frequency $f_{c_{tr}}$ [1]. We will then fix the value of L_i such that $f_{c_{tr}} > ft_{trans}$ where ft_{trans} is the desired cut-off frequency of the receiver. Note that as $f_{c_{tr}}$ depends on the bias of the diode [1], which is equal to the gate voltage of the input transistor, M1, of the amplifier, L_i and C_{ph} depend on $\left(\frac{gm}{Id}\right)_1$. The choice of L_i fixes the capacitance C_{ph} and the number of finger, m, of the diode, and influences C_{in}. As the amplifier gain is chosen to fulfill the stability requirements, the value of R_f is then adapted in order to maintain the RC frequency of the dominant pole.

3.7 Design of a 1GHz, 3 stages SVTA Transimpedance Amplifier in 0.13 μm PD-SOI CMOS technology

We will now apply the design methodology presented above to the design of a 1GHz, 3-stages SVTA transimpedance amplifier in a typical 0.13 μm PD-SOI CMOS technology. The model has been implemented using Matlab. We assume that the photodiode has a total length and width of 50µm, which is typical. We first have to choose a value for $\left(\frac{gm}{Id}\right)_2$ based on Matlab results of fig. 8. As explained above, by increasing $\left(\frac{gm}{Id}\right)_2$, the ratio of $\frac{W_2}{W_1}$ increases, and X_{C_2} increases compared to X_C. As a result, the maximum value of $\left(\frac{gm}{Id}\right)_1$ that we can choose to ensure stability also decreases. While the ratio of $\frac{W_2}{W_1}$ remains sufficiently small with regard to 1, the output voltage swing can be increased significantly by increasing $\left(\frac{gm}{Id}\right)_2$, while the other performances are only slightly degraded. This can be useful to ensure proper dynamic range margin and reliability against statistical variations on V_{th}. However, the ratio of $\frac{W_2}{W_1}$ vs. $\left(\frac{gm}{Id}\right)_2$ has a very sharp transition around 3.1 and all the performances, even the dynamic range (as $\left(\frac{gm}{Id}\right)_1$ collapses), are greatly degraded after this transition. The mirror suddenly becomes too big compared to M1. A $\left(\frac{gm}{Id}\right)_2$ of 2-2.5 seems to achieve a reasonable trade-off.

Once we have chosen the value of $\left(\frac{gm}{Id}\right)_2$, the value of $\left(\frac{gm}{Id}\right)_1$ is determined by eq. (28). We still have to determine the value of W1 based on model results of fig. 9. If we increase W1, the bias current increases as $\left(\frac{gm}{Id}\right)_1$ and then i_{dn1} are constant. As the bias current increases and $\left(\frac{gm}{Id}\right)_2$ and then i_{dn2} are constant, W2 also increases with W1. Since W1 and W2 are increased, the input capacitance is increased and then R_f must decrease accordingly, in order to keep the transition frequency at the required value of 1GHz. Note that while the output

capacitance is also increased by the increase of W1 and W2, the output pole stays at the same frequency as the output impedance is automatically reduced accordingly by the increase of the bias current. The stability requirement (eq. 18) is thus satisfied. Larger transistors are intrinsically less noisy as gm is increased (see eq. 32). As a result, the TIA noise is reduced when W1 and W2 are increased. This leads to a better receptor sensitivity. A W1 of 4 μm seems to be a good trade-off. Note that the output dynamic range is constant with W1 as it is only a function of $\left(\frac{gm}{Id}\right)_1$ and $\left(\frac{gm}{Id}\right)_2$. Thus the input dynamic range and the maximum input power increase with W1 because R_f is decreased. However, in any case, S is well below $P_{in_{max}}$ and the required sensitivity is then achieved. A very good sensitivity of approximately 1μW is achieved at a wavelength of 405 nm. This demonstrates the potential of SOI thin-film photodiodes for blue DVD and short-distance optical applications. The bias current is about 200μA which leads to a power consumption of:

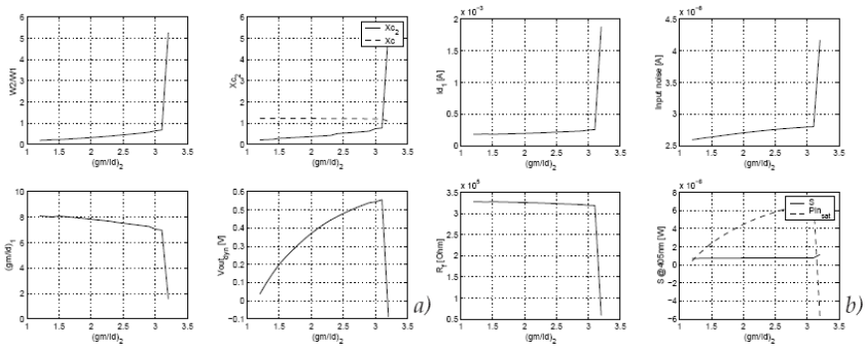

Figure 8. a) Performance of TIA vs. $\left(\frac{gm}{Id}\right)_2$ b) idem for W1=4μm. BW_{trans}=2.π.1GHz, X_A=3 and ST 0.13μm PD-SOI technology.

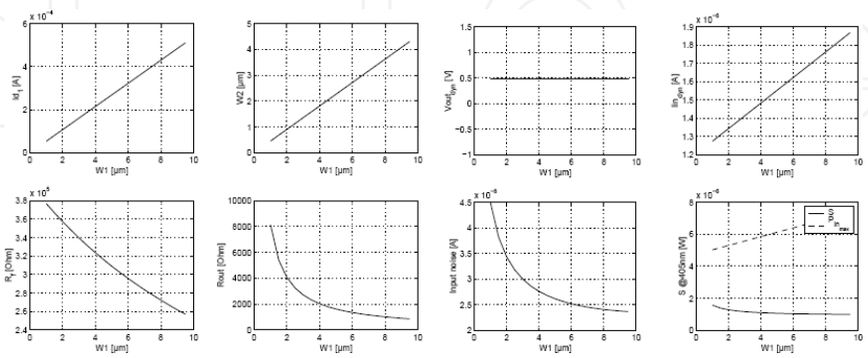

Figure 9. Performance of TIA vs. W1. BW_{trans}=2.π.1GHz, X_A=3 and ST 0.13μm PD-SOI technology.

$$P_{tot} = 4 \times 1.2V \times 20\mu A = 960\mu W \tag{56}$$

http://dx.doi.org/ 10.5772/50531

	$\frac{gm}{Id}$	W [μm]	L [μm]
M1	7.5	4	0.13
M2	2.5	1.8	0.13
Id1	R_f	Zcl	A_{3s}
214.8μA	332.8 kΩ	323.6 kΩ	35
$i_{n_{in,TIA}}$	S@405nm	P_{tot}	$Vout_{dyn}$
27.5 nA	1.1μW	1mW	0.48V
L_i	C_{ph}	Idark	m
3.4 μm	13.6fF	3×10^{-13} A	13

Table 1. Model Results for 1GHz 3 stages TIA design in a 0.13μm SOI CMOS technology

Modeled performances are in table 1. Numerical simulations of the designed circuit have then be carried out using Eldo and a BSIMSOI model fitted for ST transistors. Both values of transimpedance gain given by Matlab and by Eldo are very close from each other and around 330 kΩ (fig. 10a). However, the BSIMSOI model used in Eldo is slightly different from that we have used in the Matlab design. In the latter, we have indeed used technological curves (f_t, transistor capacitances, transconductance, output conductances...) vs. $\frac{gm}{id}$ which were extracted from ST transistors measurements done at UCL. The main differences are slightly higher drain capacitances and higher Early voltages for the BSIMSOI model. The slightly higher drain capacitance lowers the frequency of the non-dominant poles. It also decreases the frequency of the dominant pole, but in this case this effect was more than balanced by the increase of V_{ea}, which results in an increase in A_{Ns} and in the TIA bandwidth up to 2.5GHz. This reduces the phase margin of the TIA compared to Matlab and leads to a peaking of around 2.5dB in the transfer function given by Eldo. In order to increase the phase margin and reduce the peaking, we can increase the value of R_f in the Eldo simulation. By increasing R_f up to 700kΩ, the peaking is reduced to a value below 0.1dB, the TIA bandwidth reduces to 1.2 GHz, while the TIA transimpedance gain is increased by 2.1.

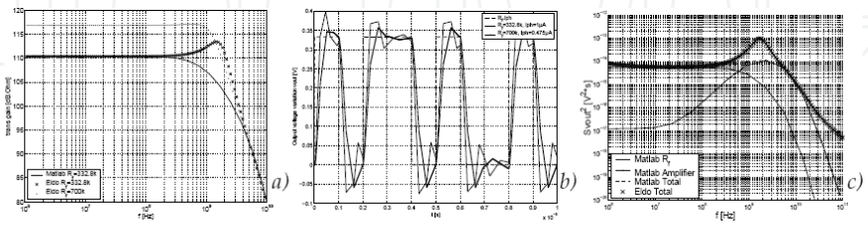

Figure 10. a) Comparison of transimpedance gain in dBΩ vs. frequency given by our model implemented with Matlab and by Eldo numerical simulations. b) TIA output voltage variation, v_{out}, to 1ns width photocurrent pulses given by Eldo transient numerical simulations. The input photocurrent, i_{ph} multiplied by the TIA gain is also given as reference signal. c) TIA output noise spectral power density, Svg^2_{out} , *vs.* frequency given by our model implemented with Matlab and by Eldo numerical simulations. The noise contribution from R_f and from the amplifier to the total spectral density are given for the Matlab results. R_f=332.800k Ω.

We then performed transient simulation of the transimpedance circuit (fig. 10b) for both R_f values. The variation of the output voltage, v_{out} to the 1ns width photocurrent pulses confirms that in a simulation point of view, both circuits (identical amplifier, but different R_f values) are suitable for 1 GBps applications. Compared to the circuit with R_f=700k Ω, that with R_f=332.8k Ω has steeper response (as its bandwidth is higher) but higher overshooting that requires a longer time to vanish (as its phase margin is lower). The multistage amplifier voltage gain A_{Ns} that fixes the TIA bandwidth and phase margin, hence its stability, depends on V_{ea}^{N} . This Early voltage is difficult to model carefully, especially in deep sub-micron process, as it can quite vary statistically with fabrication process and short channel effects. It is therefore a critical issue in the design of multistage amplifier TIA. In order to handle it, a sufficient phase margin has to be taken into account. In our case, the phase margin seems sufficient despite the increase of V_{ea} by about a factor 2. The possibility to tune the feedback resistor in the design is another very interesting and efficient solution. This can be achieved by using a transistor to implement R_f and by tuning its gate voltage.

Noise simulations were also performed with Eldo. Eldo spectral power density of output noise voltage are close to Matlab results (fig. 10c). Below 200kHz, both Matlab and Eldo total power densities are identical and are dominated by the feedback resistance contribution. Above, the high frequency peak values are related to the low voltage amplifier power densities multiplied by the voltage gain of the amplifier. The higher peak in Eldo is then explained by the higher voltage gain compared to Matlab. The equivalent RMS value of the input integrated noise given by Eldo is 41.5nA for R_f=332.8k Ω. This is a little higher than the 27.5nA predicted with Matlab due to the peak. For the Eldo simulations with R_f=700k Ω, this noise reduces to 19.1nA. As can be expected, by increasing R_f, the input noise and sensitivity performance of the receiver are improved.

3.8 Design methodology Summary

To summarize, in our multistage top-down design methodology, we first determine the optimal number of stages (which is greater than 1 when the TIA bandwidth is not too close to the transistors frequency limit f_t of a given technology) to optimize the voltage gain of the amplifier and hence R_f and the transimpedance gain. This maximum voltage gain was shown to be limited by stability considerations and to impose a value on $\left(\frac{gm}{Id}\right)_1$. The choice of $\left(\frac{gm}{Id}\right)_2$ results from a trade-off between dynamic range and other performances, while W1 is chosen to compromise power consumption vs. noise and sensitivity.

4. Single-stage Transimpedance Amplifier Modeling

In this section we will focus on the design of a high-speed transimpedance receiver. The term "high-speed" is in fact here related to technology and means that we have to design at a ratio ($f_{t_{max}}/ft_{trans}$)) close to ten or less. In a 0.13μm SOI CMOS technology as used here, it corre-

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sponds to 10GBps application. As just discussed in the section 3.1, for this kind of applications, the optimal number of stages is 1. This is simply due to the fact that there is no room to place extra poles in the feedback loop to achieve stability. In fig. 4b, we can also see that the $\left(\frac{gm}{Id}\right)_{1_{\max}}$ that we will choose to maximize the gain is low. Combined with the small lengths of the transistors, this will lead to very low achievable voltage gains. If we optimize the design for low voltage gain and high bandwidth, the value of the feedback resistor, R_f, will be low and comparable with the value of the output impedance of the amplifier. In this case the voltage gain will become dependent on R_f. A typical solution to this problem is to use an output buffer. In our case, however, this has to be rejected as it would add an extra pole in the feedback loop. We thus have to accordingly adapt our design scheme to take into account the voltage gain dependency on R_f. In the text, we will call this new case of figure the degenerated case compared to the previous one that we will refer as the non-degenerated case.

4.1 Design Methodology of single-stage Transimpedance Amplifier

The schematic view of the single stage transimpedance is presented in fig. 11a. As previously, to simplify the analysis of this shunt-shunt feedback circuit, we can rewrite its small signal schematic in its canonical form [25] (fig. 11b). The amplifier is presented as a controlled current source with an output impedance to take account of R_f in the expression of the voltage gain Ao (fig. 11b). The input capacitance, C_{in}, consists of the amplifier input capacitance, C_{g1}, and the photodiode capacitance, C_{ph}. The transimpedance gain in closed loop, Z_{cl} is then:

$$Z_{el} = \frac{-R_f}{\frac{(1 + R_f C_{in} s).\left(1 + \frac{C_{out} s}{g_{out} + gf}\right)}{Ao} + 1} \tag{57}$$

As previously, assuming that the dominant pole is that of the input, the bandwidth of the transimpedance is given by:

$$BW_{trans} = 2\pi . f t_{trans} = \frac{Ao}{R_f C_{in}} \tag{58}$$

Dynamic range (eq. 54) and power consumption expressions (eq. 55) are not changed compared to the non-degenerated case, while voltage gain Ao and non dominant output pole, which is also the bandwidth of the amplifier, BW_{1s} now depend on R_f or its inverse g_f:

$$Ao = \frac{gm_1}{g_{out} + gt} BW_{1s} = 2\pi . f t_{1s} = \frac{g_{out} + gf}{C_{out}} \tag{59}$$

By making these substitutions, however, noise analysis stays essentially the same. The total output noise power spectral density of the transimpedance (eq. 34), is now given by:

$$Sv_{out}^2(f) \simeq \frac{Sv_{R_f}^2 + |1 = s.R_f.C_{inT}|^2 .Svg_{Amp}^2}{|1 + s.\frac{R_f.C_{inT}}{A_{Ns}}|^2 .|1 + s.R_{outA}.C_{outT}|^{2.N}} \tag{60}$$

where $Sv_{R_f}^2$ and Svg_{Amp}^2 are still given by eq. (30) and eq. (33). The RMS value of the noise is still obtained by integration of Svg_{out}^2 (eq. 38). Again the integral can be approximated by the sum of three fragments (see eq. 41, 42, 47 and eq. 48) from which, only the expression of the amplifier high frequency noise has to be modified accordingly. Eq. (47) now becomes:

$$v^2 \simeq Ao^2.Svg^2.\left(\frac{\pi}{2} f t_{1s} - f t_{trans}\right) \tag{61}$$

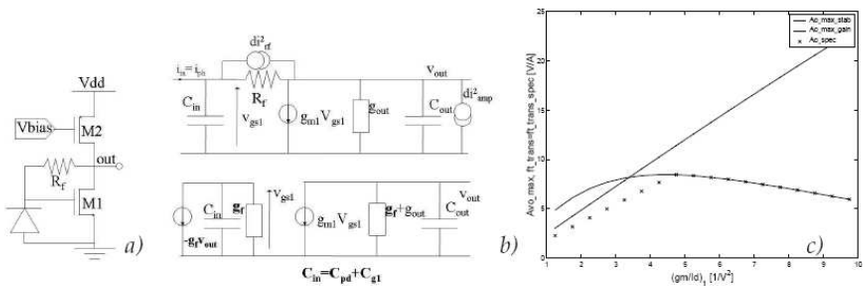

Figure 11. a) Photodiode and its transimpedance. b) Small signal diagram of the photodiode and the transimpedance. Above, with noise sources . Below, equivalent diagram in its canonical feedback form. c) $Ao_{max_{stab}}$, $Ao_{max_{gain}}$ et Ao_{spec} in function of $\left(\frac{gm}{Id}\right)_1$ for ft_{trans}=0.5GHz and k=0.75, 0.5μm FD-SOI technology.

Even though the gain and the non-dominant pole now both depend on the value of R_f, the dependence of one compensating the other, the condition of stability can be rewritten as a condition on a maximum gain $Ao_{max_{stab}}$ exactly as in the non-degenerated case:

$$Ao \leq \frac{ft}{(X_c + X_{c2}).X_A.f t_{trans}} = Ao_{\max\ stab} \tag{62}$$

Again, we see that, for a given bandwidth and a given phase margin, i.e. for a given X_A, the maximal achievable amplifier gain dictated by stability conditions is imposed by technology and inversion degree but is independent of R_f. It is this gain, which is maximum near strong inversion (f_t is decreasing, X_C is increasing and X_{C2} is decreasing with $\left(\frac{gm}{Id}\right)_1$) (figure 11c), that we would like to choose in order to optimize the performances of the circuit. However,

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as the gain depends on R_f, we cannot directly specify a value of $\left(\frac{gm}{Id}\right)_1$ as it was done in eq. (28) for the non-degenerated case. Moreover, nothing now guarantees that this maximum gain is achievable. Indeed, the gain given by eq. (59) can be rewritten:

$$Ao = \frac{\left(\frac{gm}{Id}\right)1 \cdot Id_1}{\frac{Id_1}{V_{ea}L_{eq}} + gf} (63) \tag{63}$$

where g_f is unknown and linked to the gain by eq. (58). As we will now see, for a fixed gain Ao_{spec}, one can derive the input transistor width, W1, from its length, *L1*, its $\frac{gm}{id}$ and specification on the bandwidth. From these considerations we can derive the maximum gain achievable against $\left(\frac{gm}{Id}\right)_1$. Indeed, fixing Ao equal to Ao_{spec}, we find by eq. (58) a condition on the R_fC_{in} product to satisfy the temporal specification:

$$R_f C_{in} = \frac{Ao_{spec}}{BW_{trans}} (64) \tag{64}$$

By injecting this equation in the expression of the gain eq. (63), we find:

$$Ao_{spec} = \frac{\left(\frac{gm}{Id}\right)1 \cdot i_{dn_1} \cdot \frac{W1}{L\ 1}}{\frac{i_{dn_1}W_1}{V_{ea}L_{eq}L_1} + \frac{BW_{trans}(C_{ph} + C_{g1o}.W1.L\ 1)}{Ao_{spec}}} (65) \tag{65}$$

We can write:

$$W1 = \frac{C_{ph}.BW_T}{\left(\frac{gm}{Id}\right)1\frac{1}{L\ 1} - C_{g1o}BW_T.L\ 1 - Ao_{spec}\frac{1}{L\ 1.V_{ea;}L_{eq}}} \tag{66}$$

where C_{g1o} is equal to the input capacitor of the amplifier, C_{g1}, divided by W1 and L1 and is related to $\left(\frac{gm}{Id}\right)_1$. In order to keep W1 positive and finite, we need that the denominator of this expression stay strictly positive. This gives the maximum achievable gain, which is an increasing function of $\left(\frac{gm}{Id}\right)_1$ (see fig. 11c):

$$Ao_{\max_{gain}} = V_{ea}.L_{eq}[(\frac{gm}{Id})1 - BW_T.CL_{g1o}.L1^2] \tag{67}$$

Finally, we choose to satisfy the constraints and to optimize the performances of the circuit:

$$Ao_{spec} = \min(kc.Ao_{\max_{gain'}} Ao_{\max_{stab}}) \tag{68}$$

where kc is a proportionality factor strictly smaller than 1 according to eq. (67). fig. 11c shows the evolution of the gain in function of the $\left(\frac{gm}{Id}\right)_1$ for kc=0.75. The maximum reachable gain will then be close to the intersection of the two gain characteristics.

4.2 Design of a 10GHz single stage TIA in a 0.13μm PD-SOI CMOS technology

We now apply the design methodology presented in subsection 4.1 to the design of a 10GHz, single stage SVTA transimpedance amplifier in a typical 0.13μm PD-SOI CMOS technology. The model has been implemented using Matlab. Again we used a typical photodiode with a total length and width of 50µm. We first have to choose a value for $\left(\frac{gm}{Id}\right)_2$ based on Matlab results of fig. 12. As explained above, by increasing $\left(\frac{gm}{Id}\right)_2$, the ratio of $\frac{W_2}{W_1}$ increases as well as the ratio of the drain capacitance of M2 to the gate to source capacitance of M1, X_{C_2}, compared to X_C (the $\frac{C_{d_1}}{C_{gs1}}$ ratio) for a given $\left(\frac{gm}{Id}\right)_1$. Then the maximum value of $Ao_{max_{stab}}$ that we can choose to ensure stability also decreases. As a result, Ao_{spec} decreases. As we are working at the technology frequency limit, the stability limitations prevail over the feasibility (which is by the way independent on $\left(\frac{gm}{Id}\right)_2$). This reduction of Ao_{spec} induces a reduction of W1 (see eq. 66) and then of Id1 and C_{in}. The reduction of C_{in} is however not sufficient to compensate the decrease of the value of R_f due to the reduction of Ao_{spec} (eq. 64). Noise and then sensitivity performances are also degraded when increasing $\left(\frac{gm}{Id}\right)_2$. The noise in the mirror then increases (see eq. 33). However, in order to have acceptable dynamic range, a $\left(\frac{gm}{Id}\right)_2$ larger than 2 V^{-1} is required. Increasing $\left(\frac{gm}{Id}\right)_2$ is also beneficial for power consumption. Finally a $\left(\frac{gm}{Id}\right)_2$ of 2.5 V^{-1} seems to be a good trade-off in between all these considerations for a $\left(\frac{gm}{Id}\right)_1$ of 5 V^{-1}.

However, we also have to determine the value of $\left(\frac{gm}{Id}\right)_1$. This can be done using model results of fig. 13. Again, the maximum gain is mainly dominated by $Ao_{max_{stab}}$. The curve is a non-mono-

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tonic one as f_t and X_{C2} (as the ratio of W2/W1) mainly decrease, while X_C decreases with $\left(\frac{gm}{Id}\right)_1$. The curve presents then a flat maximum between $\left(\frac{gm}{Id}\right)_1$ =4.5 to 6.5 V^{-1}, which corresponds to a minimum in W1 and a maximum in R_f (eq. 58). The current Id1 strongly decreases with $\left(\frac{gm}{Id}\right)_1$ up to these values as both i_{dn1} and W1 decrease. When further increasing $\left(\frac{gm}{Id}\right)_1$, Id1 keeps decreasing but more slowly, as i_{dn1} still decreases but W1 now increases. The input noise also presents a minimum value of around 1.5μA that is mainly related to the maximum value of R_f and, then, a minimum in sensitivity in the range of $\left(\frac{gm}{Id}\right)_1$ of 4 to 5 V^{-1}.

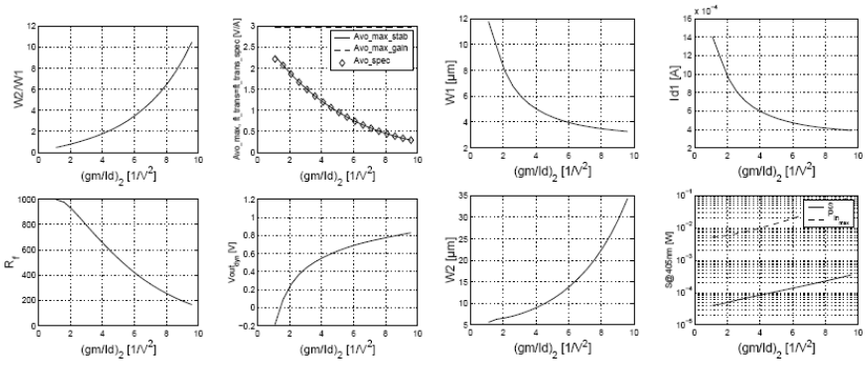

Figure 12. Performance of TIA vs. $\left(\frac{gm}{Id}\right)_2$ ft_{trans}=10GHz, $\left(\frac{gm}{Id}\right)_1$ = 5 V^{-1}, k=0.75, X_A=3, A_d=2500μm², 0.13μm PD-SOI CMOS technology, Vdd=1.2V.

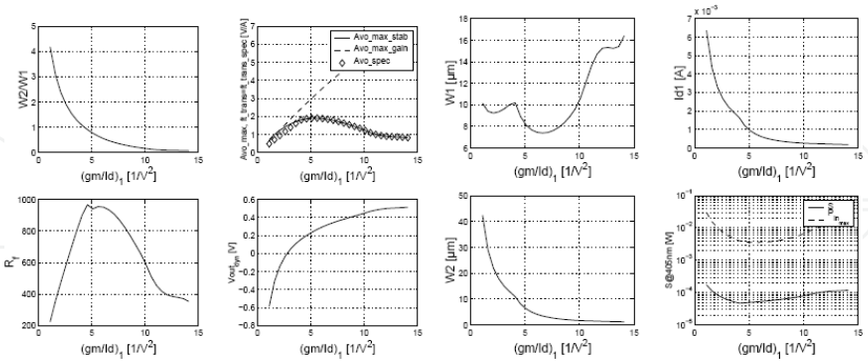

Figure 13. Performance of TIA vs. $\left(\frac{gm}{Id}\right)_1$ for ft_{trans}=10GHz, $\left(\frac{gm}{Id}\right)_2$ = 2 V^{-1}, kc=0.75, X_A=3, A_d=2500μm², 0.13 μm PD-SOI CMOS technology, Vdd=1.2V.

Note that the small decrease in R_f around $\left(\frac{gm}{Id}\right)_1$ =4.5 V^{-1}, while Ao_{spec} still increases is due to the fact that C_{ph} is increased (and then also C_{in}) by a decrease in L_i in order to maintain the

transit time in the diode despite the reduction of *Vg1* due to the increase of $\left(\frac{gm}{Id}\right)_1$. The dynamic range increases as Vds_{sat1} decreases with $\left(\frac{gm}{Id}\right)_1$ and calls for a high value of $\left(\frac{gm}{Id}\right)_1$. A $\left(\frac{gm}{Id}\right)_1$ of 5 to 6 V^{-1} seems a good trade off. Finally, in this range, results shows that it is better in terms of performances (R_f, noise, ...) to take a higher value of $\left(\frac{gm}{Id}\right)_1$ in order to gain on dynamic range margin and then to be able to further decrease the value of $\left(\frac{gm}{Id}\right)_2$. We then take a $\left(\frac{gm}{Id}\right)_1$ of 6 V^{-1} and a $\left(\frac{gm}{Id}\right)_2$ of 2 V^{-1}. Modeled performances are summarized in table 2.

	$\frac{gm}{Id}$	**W** $[\mu m]$	**L** $[\mu m]$
M1	6	7.5	0.13
M2	2	4.3	0.13
Id1	R_f	Zcl	Ao
$643\mu A$	952Ω	623Ω	1.9
$i_{n_{in,TIA}}$	S@405nm	P_{tot}	$Vout_{dyn}$
$1.75\mu A$	$50\mu W$	1.543mW	0.29V
L_i	C_{ph}	Idark	m
$1.6\ \mu m$	25.4fF	8×10^{-13} A	26

Table 2. Model results for 10GHz single stage TIA design in a 0.13μm SOI CMOS technology

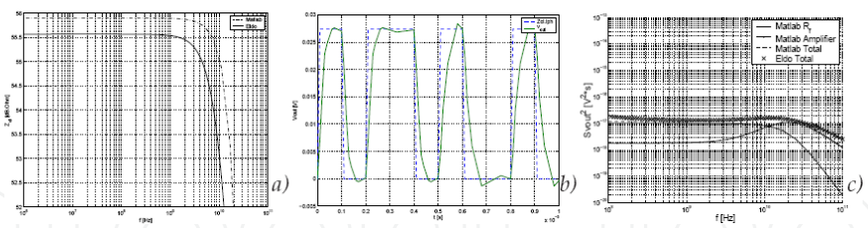

Figure 14. a) Transimpedance gain in dBΩ vs. frequency. b) Transimpedance output voltage variation, v_{out}, to 0.1ns width photocurrent pulses given by Eldo transient numerical simulations. The input photocurrent, i_{ph} multiplied by the TIA gain is also given as reference signal. c) TIA output noise spectral power density, Svg^2_{out}, *vs*. frequency given by our model implemented with Matlab and by Eldo numerical simulations. The noise contribution from R_f and from the amplifier to the total spectral density are given for the Matlab results.

Numerical simulations of the designed circuit have then be carried out using Eldo and a BSIMSOI model fitted for the ST transistors. The simulated transimpedance gain is around 600 Ω, while the transimpedance bandwidth is 10 GHz (fig. 14a). We then performed transient simulation of the transimpedance circuit (fig. 14b). The variation of the output voltage, v_{out} related to the 0.1ns width photocurrent pulses confirms that in a simulation point of view, the designed circuit is suitable for 10 Gb/s applications. Noise simulations were also

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performed with Eldo. Eldo spectral power density of output noise voltage is in very good agreement with Matlab results (fig. 14c). Below a few GHz, the total power densities are dominated by the feedback resistance contribution. Above, the high frequency peak values are related to the low voltage amplifier power densities multiplied by the voltage gain of the amplifier. The equivalent RMS value of the input noise integrated up to 10^{13} Hz given by Eldo is 1.76µA which is in perfect agreement with the 1.75µA predicted with Matlab.

4.3. Design of a 1GHz single stage TIA in a 0.5μm SOI CMOS technology and scaling perspectives

In order to compare technologies and draw some conclusions on scaling, we have applied the Matlab model to the design of a 1GHz single stage transimpedance in a fully depleted 0.5 μm SOI CMOS technology [30]. Again we are working at the technology frequency limit here such that the stability limitation prevails compared to the feasibility. The evolution of the performances with $\left(\frac{gm}{Id}\right)_1$ and $\left(\frac{gm}{Id}\right)_2$ in their principles are very similar to those of the previous design and will not be explained here again. As expected, the most suitable $\left(\frac{gm}{Id}\right)_1$ is near that enabling the maximum gain. Modeled performances are summarized in table 2. When comparing 0.13 and 0.5 μm technologies for the design of 1GHz TIA (see table 1 and table 3), we first notice that the use of a more advanced technology has allowed to use 3 stages instead of one owing to a better f_t. This allows for a real increase in performance of the transimpedance (transimpedance gain Z_{cl} increased by more than 16 times, sensitivity improved by 7.5 times). The total transimpedance area should not increase since the use of more stages should be compensated by a reduction of the length of the transistors while the width is about the same. The power consumption is however increased in the 0.13μm technology by a factor of 4. The higher bias current is mainly due to a much higher $\frac{W}{L}_1$ ratio and the higher number of stages while these are however partially compensated by the decrease of Vdd. The power consumption can even be reduced by 4 in the 0.13μm design by reducing W1 by 4 and then be equal to the 0.5μm design. In this case R_f but also the input noise will increase leading to a slightly reduced sensitivity of 1.56µW (see fig. 9) but still more than 5 times better than the sensitivity of the 0.5μm design. The use of 0.13μm technology also allows for an increase of the photodiode performance (smaller capacitance and higher photosensitive to total area ratio owing to the reduction of the size of the P+ and N+ areas).

In a similar way, the uses of very advanced technology nodes with improved f_T, such as the 22nm CMOS one with typical f_T of about 400 to 500GHz (improved by about a factor 4 compared to that of a 0.13μm technology), could allow for improving the sensitivity of the receiver at 10GHz by allowing for a multi-stage approach and a further reduction of C_{ph}. Also a single stage 40Gb/s could be attempted. A SOI integrated PIN photodiode with an intrinsic length reduced to below 1μm could fulfill such requirements in terms of transit time cutoff frequency, but with an increased capacitance [1]. This, coupled with the reduced intrinic voltage gain of the single stage amplifier related to the reduced early voltage of ultra short transistor, might result in too low R_f and sensitivity values. To compensate a reduced photo-

diode total surface but with no reduction of input power (i.e. relying on progress at the emitter side: better focused optical signal, higher power density emission at the source,...) might be necessary.

	$\frac{gm}{Id}$	W [μm]	L [μm]
M1	5	3.5	0.5
M2	1.5	2	0.5
Id1	R_f	Zcl	Ao
52.1μA	24315Ω	19644Ω	4.2
$i_{n_{in,TIA}}$	S@405nm	P_{tot}	$Vout_{dyn}$
160 nA	8μW	229.25μW	0.51V
L_i	C_{ph}	Idark	m
3.6 μm	24fF	1×10^{-13} A	10

Table 3. Model Results for 1GHz single stage TIA design in a 0.5μm SOI CMOS technology

4.4 Design methodology Summary

To summarize our single-stage top-down design methodology, we have shown that, as the voltage gain is now dependent on R_f, the maximum voltage gain is limited, on one hand, by stability considerations (which usually prevail in weak or moderate inversion regime), and on a second hand, by feasibility considerations (which usually prevail in strong inversion) and that this results on a constraint on W1. The choice of $\left(\frac{gm}{Id}\right)_2$ results from a trade-off between dynamic range and power consumption vs. voltage gain, R_f, noise and then sensitivity performance. The choice of $\left(\frac{gm}{Id}\right)_1$ results on a trade-off between dynamic range, which is maximum towards the weak inversion, and the other performances, which are maximum near the maximum gain (resulting of the stability and feasibility curves) in moderate inversion.

5. TIA experimental characterization

A single-stage 10GHz SVTA Amplifier was realized in the ST 0.13μm SOI CMOS technology. It is co-integrated with a PIN photodiode and a 50Ω output buffer for the RF measurements (fig. 15a). The latter has a 3mA bias current, a 0.79 voltage gain and a 1μA equivalent input noise. Modeled and simulated receiver bandwidths were 10GHz, both before and after insertion of the output buffer. TIA modeled performances are presented in table 4. These expected performances are not as good as those reported in table 2. This is mainly because, in the actual design, we imposed a transit time frequency of the photodiode 1.5 times higher (i.e. 15 GHz) than the bandwidth of the TIA itself in order to make sure to measure the TIA cutoff frequency. This in turn imposed a smaller intrinsic length to the photodiode and a

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higher diode capacitance. The $\frac{gm}{id}$'s taken for the actual design are also a little bit more conservative, leading to larger value of the widths of M1 and M2 and then to a larger amplifier input capacitance. The total input capacitance is then larger in the implemented design, R_f and Z_{cl} are decreased which in turn also reduces the noise performances of the TIA.

	$\frac{gm}{Id}$	W [μm]	L [μm]
M1 M2	5 2.5	12.2 12.2	0.13 0.13
Id1	R_f	Zcl	Ao
1.45 mA	364Ω	215Ω	1.5
$i_{n_{in,TIA}}$	S@405nm	P_{tot}	$Vout_{dyn}$
2.9μA	nc	nc	0.35V
L_i	C_{ph}	Idark	m
0.8 μm	42fF	nc	43

Table 4. Model results for the realized 10GHz single stage TIA design in a 0.13µ*m* SOI CMOS technology

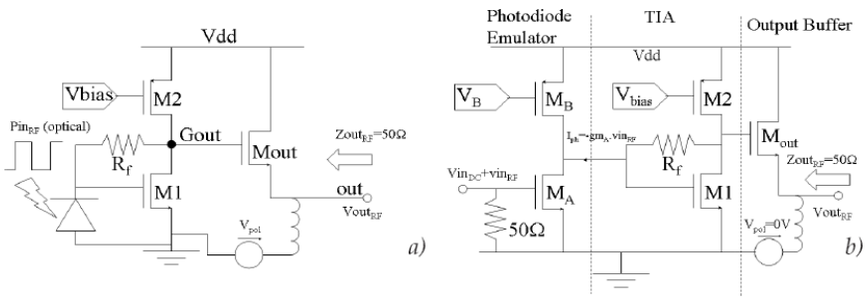

Figure 15. Schematic of the fabricated TIA and its output buffer a) with the co-integrated PIN photodiode and b) with the photodiode emulator used for the S parameter measurements

A DC transimpedance gain of 212Ω was measured which is in very good agreement with the 214Ω gain predicted by the model. For the AC measurements, we used a modulated 1mW 830 nm laser. The remaining available optical power at the fiber output after modulation and fiber coupling losses was less than 0.01mW which is far below the sensitivity of our receiver and made these measurements impossible. One solution could be to use a femtosecond pulsed laser either at 850nm or 425nm by frequency doubling for example. Because we expected the problem of sensitivity with opto-electrical measurements, we had also designed a "photodiode emulator". The latter was a single transistor voltage amplifier with its output connected at the input of the transimpedance (fig. 15b). The output capacitance of this amplifier was designed to be very similar to that of the PIN diode while its output impedance was kept sufficiently larger than R_f in order to have an equivalent input TIA pole as close as possible to the real case. By varying the gate voltage of the input transistor of this

diode emulator, an equivalent photocurrent is created at the TIA input. This allows for the electrical characterization of the TIA bandwidth. A photograph of the chip is shown in Fig 16a. S parameters measurements were done in the 40MHz-40GHz band. These measurements were obtained after a calibration to remove the impedance effect of the RF probes and cables used to connect the device to the spectrum analyzer.

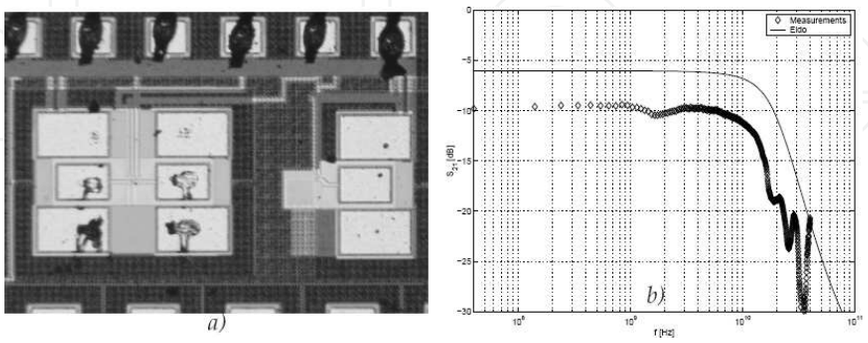

Figure 16. a) Photograph of the TIA chip. On the left: the TIA with the output buffer and the photodiode emulator used for the S parameter measurements. On the right: TIA with the PIN photodiode and the output buffer. b) Measured and Eldo-simulated curves of S_{21}*vs*. frequency. Vdd=1.2V. Vin_{DC}=0.35V. V_B=0.3V. V_{bias}=0.35V.

The bandwidth of the TIA is characterized by the S_{21} parameter which is equal to $gm_a.Z_{cl}.A_{vout}$. It is dominated in the frequency band of interest by the transimpedance poles. A_{vout} is the gain of the output buffer which is a little less than one (-1.8dB) in the bandwidth of interest. Measured curve of S_{21} *vs*. frequency is compared to the Eldo simulated curve in fig. 16b. Both are very similar and have a bandwidth slightly exceeding 10GHz. The few dB difference between the low frequency plateau of S_{21} is related to a small difference in bias currents. The measured current consumption (equal to $2xId_B+2xId_2+Id_{out}$) is equal to 5mA while the simulated one is equal to 6mA. This confirms experimentally the ability of 0.13 µm CMOS SOI technology for 10Gb/s transimpedance circuits.

6. Conclusions

In this chapter the design of the transimpedance amplifier, which is the most used receiver front-end for high speed optical applications, has been investigated.

In the Optical Receivers Basics section, the simple resistor system was first presented as well as its limitations. The transimpedance amplifier was then introduced and its basic theory and concepts such as transimpedance gain, bandwidth and stability were derived. Important figures of merit to compare transimpedance amplifiers were also discussed as well as some architectures most often used in the high speed communication area.

Then in the Design of Multistage Transimpedance Amplifiers section, we have presented our top-down methodology to design transimpedance amplifiers in the case where the voltage gain of the voltage amplifier used in the transimpedance amplifier is independent of the

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feedback resistor R_f. We have shown that this happens when the bandwidth of the transimpedance amplifier is not too close to the transistors frequency limit f_t of a given technology and leads to multi-stages approach. Our systematic design procedure was then applied to the design of a 3-stages 1GHz bandwidth transimpedance amplifier in a 0.13 μm PD-SOI CMOS technology. It has allowed us to determine the optimal number of stages (3) to optimize the voltage gain of the amplifier and hence R_f and the transimpedance gain. This maximum voltage gain was shown to be limited by stability considerations. Model Results were validated by Eldo numerical simulations.

Finally, in the Single-stage Transimpedance Amplifier Modeling section, we have presented a top-down methodology to design transimpedance amplifiers when the voltage gain is dependent on R_f. This is the case for very high speed single stage transimpedance amplifiers. In this case we showed that the maximum voltage gain was limited, on one hand, by stability considerations (which usually prevail in weak or moderate inversion regime), and on a second hand, by feasibility considerations (which usually prevail in strong inversion). Our design procedure was applied to the design of a single-stage 10GHz bandwidth transimpedance amplifier in a 0.13 μm PD-SOI CMOS technology and to the design of a 1GHz bandwidth single-stage transimpedance amplifier in a 0.5 μm FD-SOI CMOS technology. Model Results were validated by Eldo numerical simulations and measurements.

Model results for the 3-stage 1GHz bandwidth transimpedance amplifier in a 0.13 μm PD-SOI CMOS technology showed that C_{in} was very low owing to 1) very good AC performances of thin-film SOI photodiodes (the monolithic integration which avoid bonding capacitor is possible due to the availability of thin-film SOI diodes with 1GHz bandwidth and the very low capacitance of the SOI PIN photodiodes themselves) and 2) the low capacitances of MOS transistors in SOI technology. This fact combined with the high technology $\frac{f_t}{BW_{trans}}$ ratio which has enabled the multi-stages approach, has allowed for chosing a very high feedback resistor and then to achieve very high transimpedance gain and low noise operation and this with a very low power consumption. Coupled with the very good responsivity at 405nm (0.25 A/W) and the very low dark current (DC performances) of the thin-film SOI photodiodes, a record sensitivity of 1μW (with a BER of 10^{-12}) is projected. This shows the adequacy of 0.13 μm PD-SOI CMOS technology for Blue-DVD applications where the todays specifications are to be able to read input optical power of a few μW [9] but at a 4 times lower bandwidth (250MHz). Coupled with the low responsivity of the thin-film SOI photodiodes at 850nm (0.005A/W), a sensitivity of 50μW or -13dBm is still achieved which is considered as an adequate sensitivity receiver for optical communications and comparable to CMOS realization reported in the literature using non integrated diodes with a 90 time better responsivity [31]. This shows the potential interest of this technology for monolithically integrated 1Gb/s optical communication receivers at 850nm or even to realize a blue DVD player which is compatible with the previous red standard.

The design of a 1GHz bandwidth single-stage transimpedance amplifier in a 0.5 μm FD-SOI CMOS technology has allowed us to draw conclusions on the evolution of the performances vs. the CMOS technology scaling down, when compared to the previous design. We first no-

tice that the use of a more advanced technology has allowed us to use 3 stages instead of one owing to its better f_t for same TIA bandwidth. This has naturally allowed a real increase of the performances of the transimpedance: transimpedance gain Z_{cl} by more than 16 times, sensitivity improved by 7.5 times, but at a 4 times higher power consumption in the 0.13μm technology. At same power consumption the receiver sensitivity in the 0.13μm technology, if slightly reduced, still remains more than 5 times better than the sensitivity of the 0.5μm design.

Ref.	[32]	[33]	[5]	[6]
Technology	InAlAs/InGaAs	0.2μm SiGe	23 GHz Si Bipolar	35 GHz, 0.3μm Si Bip.
Bitrate [Gb/s]	10 (7.3GHz)	10 (9GHz)	10 (7.8 GHz)	10 (10.5 GHz)
TIA Gain [Ω]	460	$R_f = 500$	710 ($R_f = 735$)	$R_f = 800$
receiver Total Gain [Ω]		1.5k		1k
C_{ph} **[pF]**			0.1	0.15
ZBW [ThzΩ]	3		5	6
Power [mW]		300	143	450
Dynamic Range		15μA-1mA	11-900μA	16μA-2mA
Input noise [μA RMS]		1	2	3
Power Supply [V]		3	6.5	8.5
Comments		LP	tunable LP	CP (+3GHz BW)
Ref.	[26]	[27]	[7]	this work
CMOS Technology	0.18μm Bulk	0.12μm Bulk	0.18μm Bulk	0.13μm PD-SOI
Bitrate [Gb/s]	10 (6GHz)	10	10 (7.6GHz)	10 (10GHz)
TIA Gain [Ω]			430	623($R_f = 952$)
receiver Total Gain [Ω]		1.5k	22400	
C_{ph} **[pF]**			0.15	0.025
ZBW [ThzΩ]			3.27	6.23
Power [mW]	88	10	210	1.55
Dynamic Range	2.5μA-2.5mA		50-500μA	12-465μA
S@850nm [dBm]		-13.1	-12	1.35 (-13@405nm)
Input noise [μA RMS]			7.3	1.74
Power Supply [V]	2.2	1	1.8	1.2
Comments	LP	wirebonded GaAs photodiode,LP	photodiode (Oepic) R=0.85A/W,LP	thin-film SOI PIN diode (R=0.005A/W)

Table 5. Overview of 10 Gb/s Transimpedance receivers in the literature. LP and CP stand respectively for inductive and capacitive peaking techniques

Concerning the design of a single stage 10GHz bandwidth transimpedance amplifier in a 0.13 μm PD-SOI CMOS technology, the low C_{in}, due as previously to the monolithic SOI integration, has enabled us to achieve the highest feedback resistor and one of the highest gain and then the highest transimpedance gain-bandwidth product ZBW (see table 5), as we are achieving one of the highest bandwidth reported for 10Gb/s (theoretically a bandwidth of about 3/4 the data rate is sufficient so that 10 GHz could be related to 13Gb/s operation)). This is achieved without using inductive (LP) or capacitive (CP) peaking techniques which allows to increase ZBW (or the bandwidth for same R_f) but at the expense of chip area (inductors or capacitors to integrate), design complexity, need for tuning... Noise performances are also very good, especially compared to other CMOS designs. The power consumption of the TIA preamplifier (not the complete receiver) is one of the best achieved so far. However, coupled with the low responsivity of thin-film SOI photodiodes at 850nm, a sensitivity of 1.35mW or +1.3dBm is achieved for this monolithically integrated receiver for 10Gb/s optical communications at 850nm. At 405nm on the other hand, the same receiver achieves a high

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sensitivity of -13dBm. In order to increase the sensitivity at 850nm wavelength however, we can try to increase the diode responsivity. Promising solutions such as the use of SOI CMOS compatible GeOI photodiodes have been discussed in [1]. We can also try to further decrease the transimpedance noise by increasing R_f. With a single-stage approach at a bandwidth of 7.5GHz, our model predicts a 850nm sensitivity of -1.25dBm. Combining this with an avalanche gain of 4 that has been demonstrated with thin-film SOI PIN diodes at 10 Gb/s [18], adequate sensitivity of at least -7dbm [8] should be achieved at 10Gb/s. To further improve the sensitivity, we think that the best solution is to attempt a multistage approach so that the voltage gain (and hence ZBW) could be improved. By reducing the bandwidth to about 7.5GHz and using inductive or capacitive peaking if necessary this could be achieved. If not, the uses of very advanced technologies with improved f_t, such as 22nm CMOS ones with f_t of about 400 to 500GHz (improved by about a factor 4 compared to that of a 0.13μm technology), could allow for improving the sensitivity of the receiver at 10GHz by allowing for a multi-stage approach and a further reduction of C_{ph}. Finally, in such technologies higher data rate could be attempted, e.g. a single stage 40Gb/s. A SOI integrated PIN photodiode with a shorter intrinsic length could fulfill such requirements in terms of transit time cutoff frequency [1], but with an increased capacitance value. This, coupled with the reduced intrinic voltage gain of the single stage amplifier related to the reduced early voltage of ultra short transistor, might result in too low R_f and sensitivity values. To compensate a reduced photodiode total surface but with no reduction of input power (i.e. relying on progress at the emitter side) might be necessary.

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References

[1] Afzalian, Aryan, & Flandre, Denis. (2011). Design of Thin-Film Lateral SOI PIN Photodiodes with up to Tens of GHz Bandwidth, Advances in Photodiodes, Gian Franco Dalla Betta (Ed.). ISBN: 978-953-307-163-3, InTech, 153-172.

[2] Schneider, K., & Zimmermann, H. (July 2006). "Three-stage burst-mode transimpedance amplifier in deep-sub-μm CMOS technology",. *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 53(No. 7), 1458-1467.

[3] Hermans, C., & Steyaert, M. (July 2006). "A high-speed 850-nm optical receiver front-end in 0.18- μm CMOS". *IEEE J. Solid-State Circuits*, Vol. 41(No.7), 1606-1614.

[4] Zimmermann, H. (2000). "Integrated Silicon Opto-electronics". Springer, Berlin.

[5] Neuhauser, M., M. Rein, H., & Wernz, H. (Jan. 1996). "Low-noise, high-gain Si-bipolar preamplifiers for 10 Gb/s optical-fiber links-design and realization". *IEEE J. Solid-State Circuits*, Vol. 31, 24-29.

[6] Ohhata, K., Masuda, T., Imai, K., Takeyari, R., & Washio, K. (Jan. 1999). "A wide-dynamic range, high-Transimpedance Si bipolar preamplifier IC for 10-Gb/s optical fiber links". *IEEE J. Solid-State Circuits*, vol. 34(No. 1), 18-24.

[7] Chen, W.-Z., Cheng, Y.-L., & Lin, D.-S. (June 2005). "A 1.8-V 10-Gb/s fully integrated CMOS optical receiver analog front-end". *IEEE J. Solid-State Circuits*, Vol. 40(No. 6), 1388-1396.

[8] Kromer, C., Sialm, G., Berger, C., Morf, T., Schmatz, M.L., Ellinger, F., Erni, D., Bona, G.-L., & Jackel, H. (Dec. 2005). "A 100-mW 4/spl times/10 Gb/s transceiver in 80-nm CMOS for high-density optical interconnects". *IEEE J. Solid-State Circuits*, Vol. 40(No. 12), 2667-2679.

[9] Hobenbild, M., Seegebecht, P., Pless, H., & Einbrodt, W. (17-18 Nov. 2003). "High-speed photodiodes with reduced dark current and enhanced responsivity in the blue/uv spectra". *EDMO 2003*, pp60-65.

[10] Y. Liu, M., Chen, E., & Y. Chou, S. (1994). "140 GHz metal-semiconductor-metal photodetectors on silicon-on-insulator substrates with a scaled active layer". *Appl. Phys. Letters*, Volume 65(Issue 7), 887-888.

[11] Ghioni, M. (July 1996). "A VLSI-Compatible High-Speed Silicon Photodetector for Optical Data Link Applications". *IEEE Trans. On Electron Devices*, Vol 43(No. 7), 1054-1060.

[12] Ho, J.Y.L., & Wong, K.S. (1996). "High-Speed and high-sensitivity silicon-on-insulator metal-semiconductor-metal photodetector with trench structure". *Appl. Phys. Letters*, Volume 69(Issue 1), 16-18.

[13] F. Levine, B., D. Wynn, J., P. Klemens, F., & Sarusi, G. (1995). "1Gb/s Si high quantum efficiency monolithically integrable $\lambda = 0.88\mu m$ detector". *Appl. Phys. Letters*, Volume 66(Issue 22), 2984-2986.

[14] Csutak, S.M., Dakshina-Murthy, S., & Campbell, J.C. (May 2002). "CMOS-compatible planar silicon waveguide-grating-coupler photodetectors fabricated on silicon-on-insulator (SOI) substrates". *IEEE Journal of Quantum Electronics*, Volume 38(Issue 5), 477-480.

[15] Emsley, M.K., Dosunmu, O., Unlu, M.S., Muller, P., & Leblebici, Y. (Sept. 16-18). "Realization of High-Efficiency 10 GHz Bandwidth Silicon Photodetector Arrays for Fully Integrated Optical Data Communication Interfaces". *Proc. of ESSDERC 2003 Conference*, Estoril, Portugal, 47-50.

[16] Dehlinger, G., Koester, S.J., Schaub, J.D., Chu, J.O., Ouyang, Q.C., & Grill, A. (Nov. 2004). "High-speed Germanium-on-SOI lateral PIN photodiodes". *IEEE Photonics Technology Letters*, Volume 16(Issue 11), 2547-2549.

[17] Afzalian, A., & Flandre, D. (June 2005). "Physical Modeling and Design of Thin-Film SOI Lateral PIN Photodiodes". *IEEE Trans. on Electron Devices*, Vol. 52(No. 6), 1116-1122.

[18] Yang, B., Schaub, J.D., Csutak, S.M., Rogers, D.L., & Campbell, J.C. (May 2003). "10-Gb/s all-silicon optical receiver". *IEEE Photonics Technology Letters*, Volume 15(Issue 5), 745-747.

[19] Bhatnagar, A., Latif, S., Debaes, C., & Miller, D.A.B. (Sept. 2004). "Pump-probe measurements of CMOS detector rise time in the blue". *IEEE Journal of Lightwave Technology*, Volume 22(Issue 9), 2213-2217.

[20] http://www.mentor.com/products/ic_nanometer_de-sign/custom_design_simulation/eldo/.

[21] Ingels, M., & Steyaert, M. (2004). "Integrated CMOS Circuits For Optical Communications". Springer.

[22] Silveira, F., Flandre, D., & Jespers, P.G.A. ((1996)). "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a Silicon-on-Insulator micropower OTA". *IEEE Journal of Solid-State Circuits*, 31, 1314-1319.

[23] Gray, P., & Meyer, R. (1984). "Analysis and Design of Analog Integrated Circuits". John Wiley & Sons.

[24] Laker, K., & Sansen, W. (1994). "Design of Analog Integrated Circuits and Systems". McGraw-Hill, Inc.

[25] Schubert, T., & Kim, E. ((1996)). "Active And Non-Linear Electronics". Wiley.

[26] Tao, R., & Berroth, M. (16-18 Sept. 2003). "A 10Gb/s fully differential CMOS transimpedance preamplifier". *Proceedings of the 29th 2003 European Solid-State Circuits Conference, ESSCIRC '03*, 549-552.

[27] Guckenberger, D., Schaub, J.D., Kucharski, D., & Kornegay, K.T. (12-14 June 2005). "1V, 10mW, 10Gb/s CMOS optical receiver front-end". *Digest of IEEE 2005 Radio Frequency integrated Circuits (RFIC) Symposium*, 309-312.

[28] Enz, C., Krummenacher, F., & Vittoz, E. (1995). "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications". *Analog Integrated Circuits and Signal Processing*, vol. 8, 83-114.

[29] Spiegel, M. (1974). "Mathematical Handbook of Formulas and Tables". McGraw-Hill Inc., New York.

[30] http://www.emmarin.ch/.

[31] M. Csutak, S. (Dec. 2001). "Optical receivers and photodetectors in 130nm CMOS technology". *PH.D thesis*, University of Texas at Austin.

[32] Chien, F.T., & Chan, Y.J. (May 1998). "Transimpedance amplifiers fabricated with In/sub 0.52/Al/sub 0.48/As/In/sub 0.47/As doped-channel heterostructures". *Electronics Letters*, vol. 34(no. 11), 1142-1143.

[33] Maxim, A. (17-19 June 2004). "A 10Gb/s SiGe transimpedance amplifier using a pseudo-differential input stage and a modified Cherry-Hooper amplifier". *Symposium on VLSI Circuits 2004*, 404-407.