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Hardware Implementation of a Real-Time Image Data Compression for Satellite Remote Sensing

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1. Introduction

The image data compression is very important to reduce the image data volume and data rate for the satellite remote sensing. The chapter describes how the image data compression hardware is implemented and uses the FORMOSAT-5 Remote Sensing Instrument (RSI) as an example. The FORMOSAT-5 is an optical remote sensing satellite with 2 meters Panchromatic (PAN) image resolution and 4 meters Multi-Spectrum (MS) image resolution, which is under development by the National Space Organization (NSPO) in Taiwan. The payload consists of one PAN band with 12,000 pixels and four MS bands with 6,000 pixels in the remote sensing instrument. The image data compression method complies with the Consultative Committee for Space Data Systems (CCSDS) standard CCSDS 122.0-B-1 (2005). The compression ratio is 1.5 for lossless compression, 3.75 or 7.5 for lossy compression. The Xilinx Virtex-5QV FPGA, XQR5VFX130 is used to achieve near real time compression. Parallel and concurrent handling strategies are used to achieve high-performance computing in the process.

2. Image compression methodology

The CCSDS Recommended Standard for Image Data Compression is intended to be suitable for spacecraft usage. The algorithm complexity is sufficiently low for hardware implement and memory buffer requirement. It can support strip-based input format for push broom imaging. The compressor consists of two functional blocks, Discrete Wavelet Transfer (DWT) and Bit Plane Encoder (BPE). The image compression methodology is described in the following sections.

2.1 Discrete wavelet transform

The CCSDS Recommendation supports two choices of DWT: an integer DWT (IDWT) and a floating point DWT (FDWT). The integer DWT requires only integer arithmetic, is capable of providing lossless compression, and has lower implementation complexity, but lower compression ratio. The floating point DWT provides improved compression effectiveness, but requires floating point calculations and cannot provide lossless compression.

The DWT stage performs three levels of two-dimensional (2-d) wavelet decomposition and generates 10 subbands as illustrated in Fig. 1. The low pass IDWT is as Equation (1) and the high pass IDWT is as Equation (2). The low pass FDWT is as Equation (3) and the high pass FWDT is as Equation (4), j=0, 1,…11999 for PAN band, j=0,1,…5999 for MS bands in FORMOSAT-5 case.

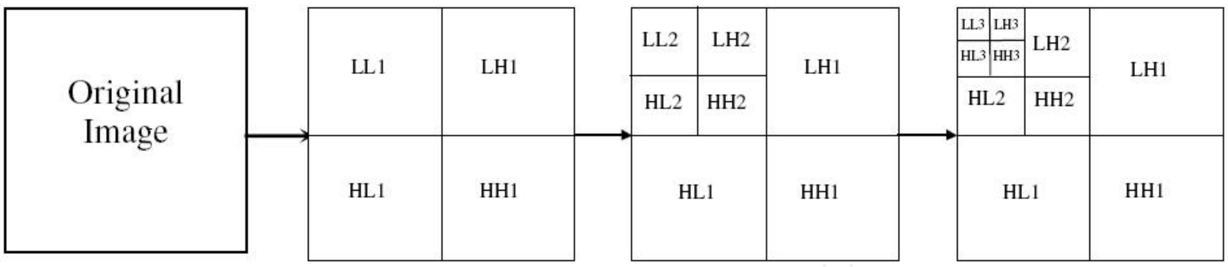


Fig. 1. Three-Level 2-d DWT Decomposition of an Image

$$C_j = \frac{1}{64}x_{2j-4} - \frac{1}{8}x_{2j-2} + \frac{1}{4}x_{2j-1} + \frac{23}{32}x_{2j} + \frac{1}{4}x_{2j+1} - \frac{1}{8}x_{2j+2} + \frac{1}{64}x_{2j+4} \tag{1}$$

$$D_j = \frac{1}{16}x_{2j-2} - \frac{9}{16}x_{2j} + x_{2j+1} - \frac{9}{16}x_{2j+2} + \frac{1}{16}x_{2j+4} \tag{2}$$

$$C_j = \sum_{n=-4}^{4} h_n X_{2j+1+n}\,; \qquad j = 0,1,\ldots,11999 \tag{3}$$

$$D_j = \sum_{n=-3}^{3} g_n X_{2j+1+n}\,; \qquad j = 0,1,\ldots,11999 \tag{4}$$

For FDWT, the coefficients in the equation (3) and (4) are listed in Table 1. The coefficients used in the FORMOSAT-5 are a little different from those defined in the CCSDS 122.0-B-1. Just 24 bits, not 32 bits, are used for these coefficients in the FORMOSAT-5 to save FPGA multiplexer resource.

	FDWT Coefficients defined in CCSDS			FDWT Coefficients used in FORMOSAT-5	
i	Low Pass Filter, h_i	High Pass Filter, g_i		Low Pass Filter, h_i	High Pass Filter, g_i
0	0.852698679009	- 0.788485616406		0.852698564529	- 0.788485646247
±1	0.377402855613	0.418092273222		0.377402901649	0.418092250823
±2	- 0.110624404418	0.040689417609		- 0.110624432563	0.040689468383
±3	- 0.023849465020	- 0.064538882629		- 0.023849487304	- 0.064538883647
±4	0.037828455507			0.037828445434	

Table 1. Coefficients of floating point DWT

2.2 Bit plane encoder

After DWT processing, the Bit Plane Encoder handles DWT coefficient for data compression. The Bit Plane Encoder encodes a segment of images from most significant bit (MSB) to least significant bit (LST). The BPE encoding uses less bits to express image data to achieve compression ratio. In CCSDS 122.0-B-1, the maximum number of bytes in the compressed segment can be defined to limit the data volume. The quality limit can be defined to constraint the amount of DWT coefficient information to be encoded.

The BPE performs DC and AC data encryption as the flow shown in Fig.2. In DC part data encryption, AC part maximum value of each block will be computed. Then, a scheme should be used to determine how many bits for "DC_MAX_Depth" and "AC_MAX_Depth" in this segment. In addition, the DC and AC optimized encryption type and value of W/8 blocks should be determined. Finally, the DC part data and W/8 AC_MAX data will be encrypted and the bit stream is transmitted to next stage. W is the pixel size per image line, e.g. W is 12,000 for PAN image and W is 6,000 for MS image in FORMOSAT-5.

In AC part data encryption, it consists of 5 stages. Data encryption and bit-out proceed block by block in each stage. The entropy coding scheme is used by data encryption. The stage 0 is for processing DC 3rd part data. The stage 1 is for processing Parent part coefficients in each block. The stage 2 is for processing Children part coefficients in each block. The stage 3 is for processing Grand-Children part coefficients in each block. The stage 4 is just concatenated stage 1, stage2 and stage 3 left data. After adding segment header, the compressed image data are finished.

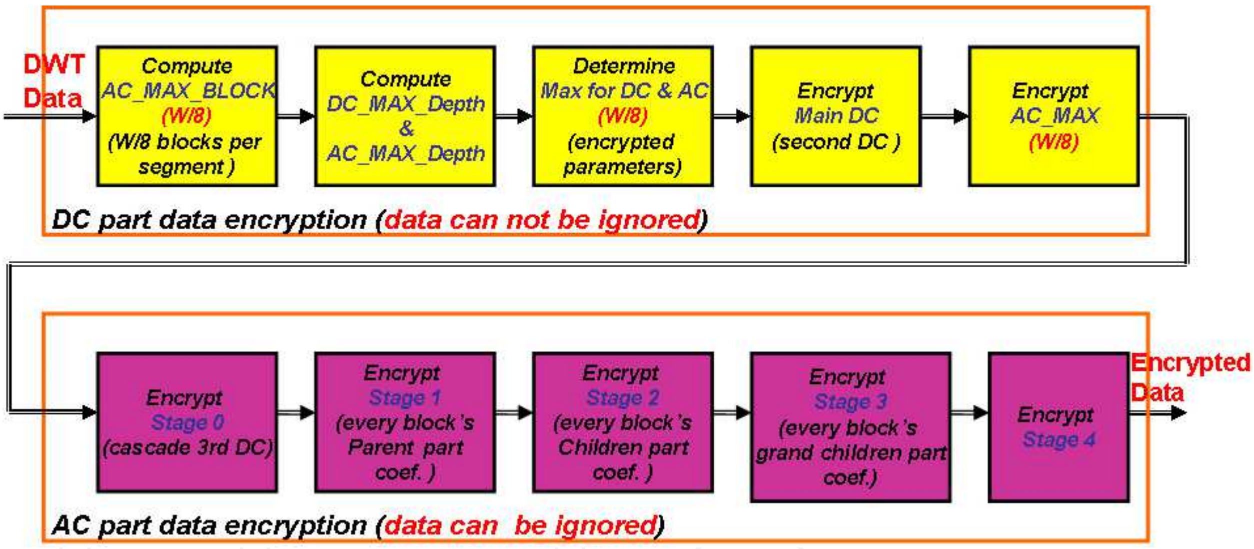

DWT Data
Compute AC_MAX_BLOCK (W/8) (W/8 blocks per segment)
Compute DC_MAX_Depth & AC_MAX_Depth
Determine Max for DC & AC (W/8) (encrypted parameters)
Encrypt Main DC (second DC)
Encrypt AC_MAX (W/8)
DC part data encryption (data can not be ignored)
Encrypt Stage 0 (cascade 3rd DC)
Encrypt Stage 1 (every block 's Parent part coef.)
Encrypt Stage 2 (every block 's Children part coef.)
Encrypt Stage 3 (every block 's grand children part coef.)
Encrypt Stage 4
Encrypted Data
AC part data encryption (data can be ignored)

Fig. 2. BPE Encoding Flow

3. Hardware implementation

3.1 Architecture description

The image flow of the Remote Sensing Instrument in the FORMOSAT-5 is shown in Fig. 3. Behind the telescope, there is one CMOS sensor module inside the Focal Panel Assembly (FPA) to take the images. The CMOS sensor module can be accessed by two FPA electronics. The output data stream is sent to the Image Data Pre-processing (IDP) module in the RSI EU for data re-ordering. Then the resultant data are sent to the Image Data Compression (IDC) module for data compression. The compressed data with format header are stored in the Mass Memory (MM) modules under the control of the Memory Controller (MC) module. While the satellite flies above the ground station, the image files can be retrieved and transmitted to the ground station.

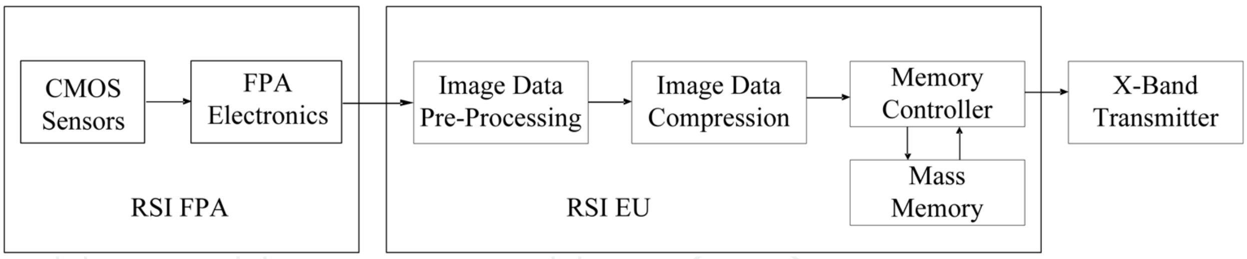


Fig. 3. Image Flow of Remote Sensing Instrument

3.2 Design and implementation

The image data input interfaces between each functional module are shown in the Fig. 4. The serial image data from FPA are re-ordered in the IDP to make the image data output in correct pixel order. Then the image data are transferred to IDC in parallel on 12-bit data bus with lower transmission clock rate. One channel of PAN data and four channels of MS data are compressed individually in the IDC. The compressed PAN and MS data are stored individually in image files under the control of MC module.

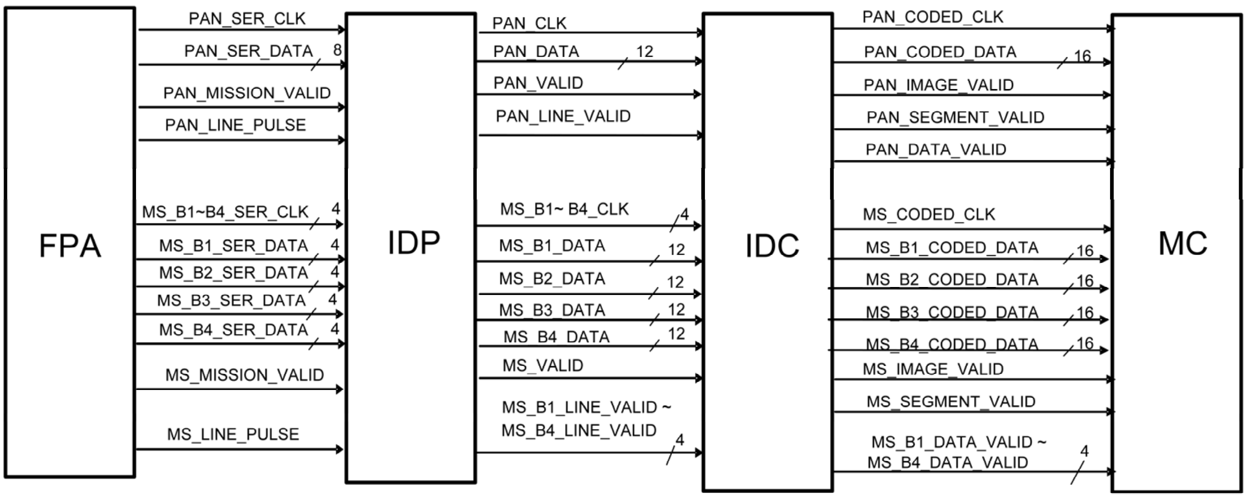


Fig. 4. Image Data Signal Interfaces between Functional Modules

3.3 Hardware design

The image data rate between each stage is shown in Fig. 5. The PAN sensors output are divided into 8 channels with 80Mbps rate individually to accommodate the high data rate. The channel rate for each MS band is 40Mbps. The parallel handling architecture can increase the image data handling speed.

The PAN and MS image data compression boards are shown in Fig. 6 a) & b). The architecture block diagram of the PAN channel in IDC is illustrated in Fig. 7. The MS channels are similar. The space grade Xilinx FPGA, XQR5VFX130, is used for image compression processing. The major characteristics of the XQR5VFX130 are 130,000 logic cells, 298 blocks of 36K bits RAM, 320 enhanced DSP slices,700Krad total dose, and etc. The PROM part for FPGA programming is XQR17V16, which has 16Mbits memory size with 50krad total dose capability. One XQR5VFX130 FPGA is used for PAN data compression.

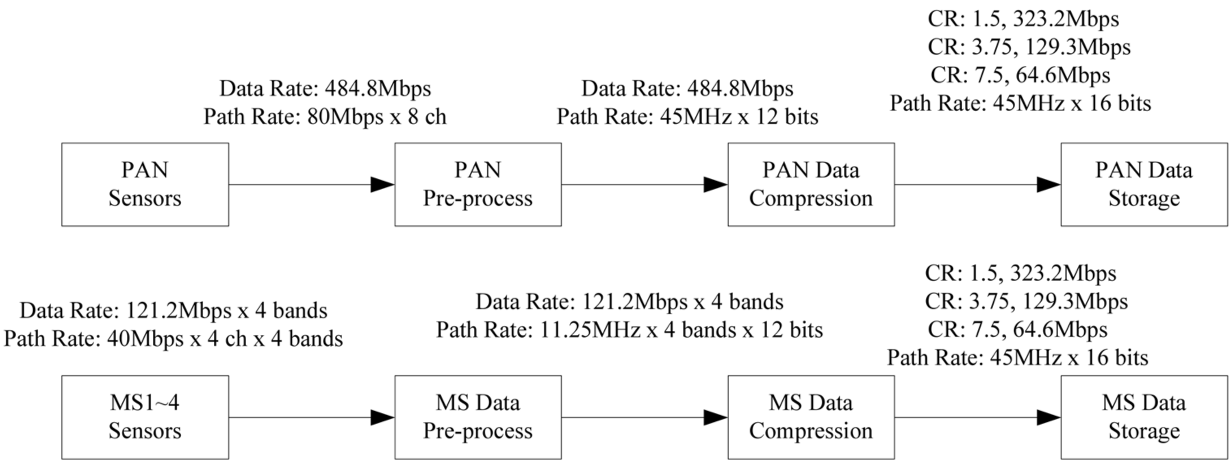


Fig. 5. Image Data Rate between each stage

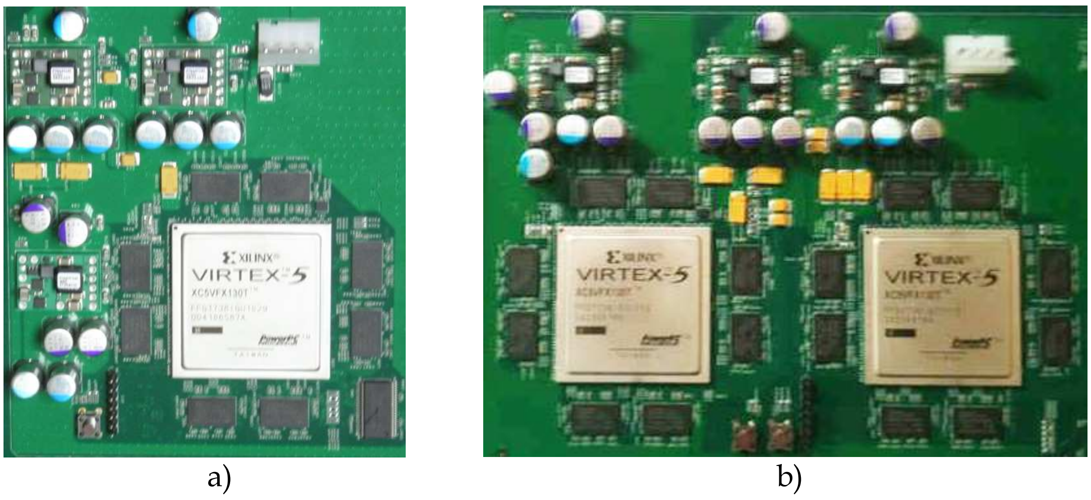

a) b)

Fig. 6. a) PAN Compression Circuit Board; b) MS Compression Circuit Board

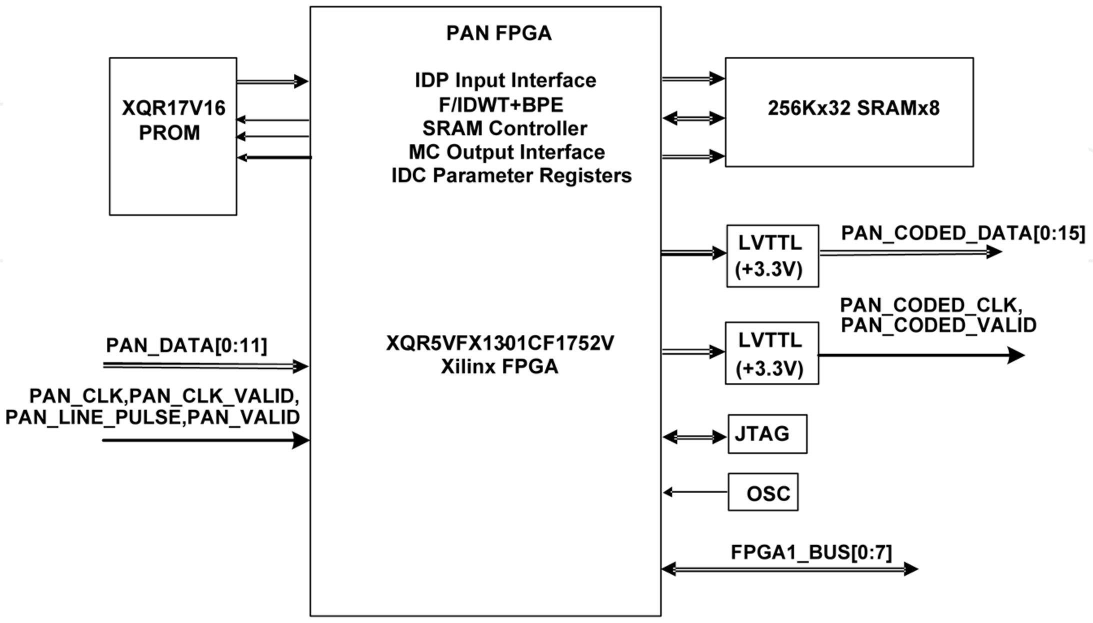


Fig. 7. Architecture Block Diagram of the PAN Channel in IDC

Two XQR5VFX130 FPGAs are used for four MS data compression. The external memories, 24 chips of 256K x 32 SRAM, are used as data buffer during compression process.

3.4 DWT process

The DWT flows at three levels are illustrated in Fig. 8a, 8b and 8c. The RAM memory banks are used for buffer storage. In the first level, the LL1, LH1, HL1 and HH1 are generated. Then, the LL1 is transmitted to level 2 DWT process to generate LL2, LH2, HL2 and HH2. The LL2 is transmitted to level 3 DWT process to generate LL3, LH3, HL3 and HH3. The LL3 contains the most information of the original image. These subbands are stored in the temporary buffers for BPE process.

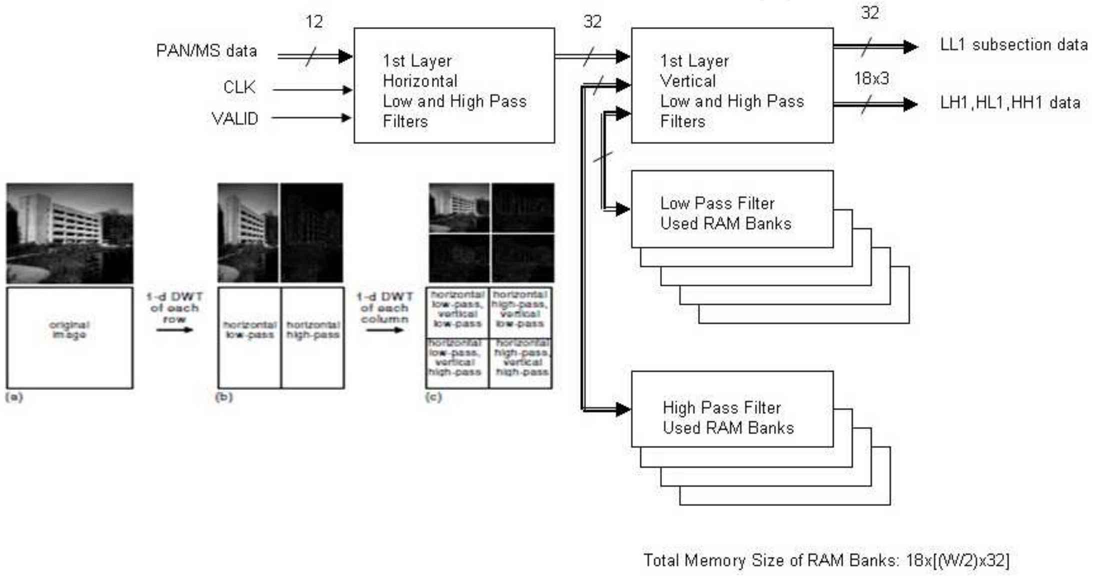

PAN/MS data
CLK
VALID
12
1st Layer Horizontal Low and High Pass Filters
32
1st Layer Vertical Low and High Pass Filters
32
18x3
LL1 subsection data
LH1,HL1,HH1 data
Low Pass Filter Used RAM Banks
High Pass Filter Used RAM Banks
original image
1-d DWT of each row
horizontal low-pass
horizontal high-pass
1-d DWT of each column
horizontal low-pass, vertical low-pass
horizontal high-pass, vertical low-pass
horizontal low-pass, vertical high-pass
horizontal high-pass, vertical high-pass
(a)
(b)
(c)
Total Memory Size of RAM Banks: 18x[(W/2)x32]

Fig. 8a. DWT Flow (1)

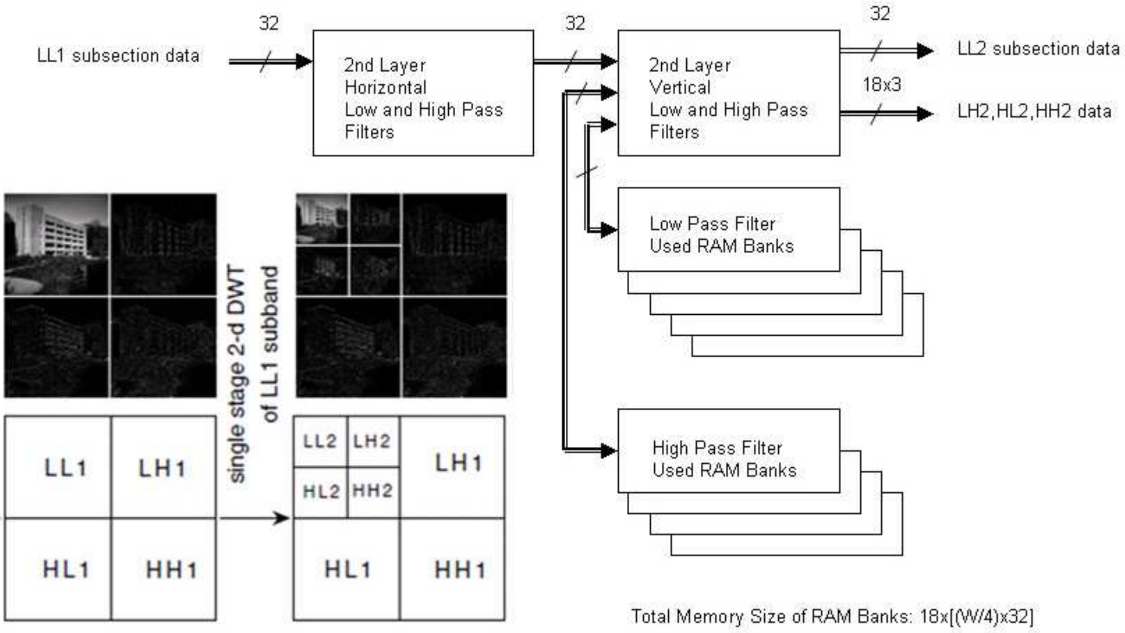

LL1 subsection data
32
2nd Layer Horizontal Low and High Pass Filters
32
2nd Layer Vertical Low and High Pass Filters
32
18x3
LL2 subsection data
LH2,HL2,HH2 data
Low Pass Filter Used RAM Banks
High Pass Filter Used RAM Banks
single stage 2-d DWT of LL1 subband
LL1
LH1
HL1
HH1
LL2
LH2
HL2
HH2
LH1
HL1
HH1
Total Memory Size of RAM Banks: 18x[(W/4)x32]

Fig. 8b. DWT Flow (2)

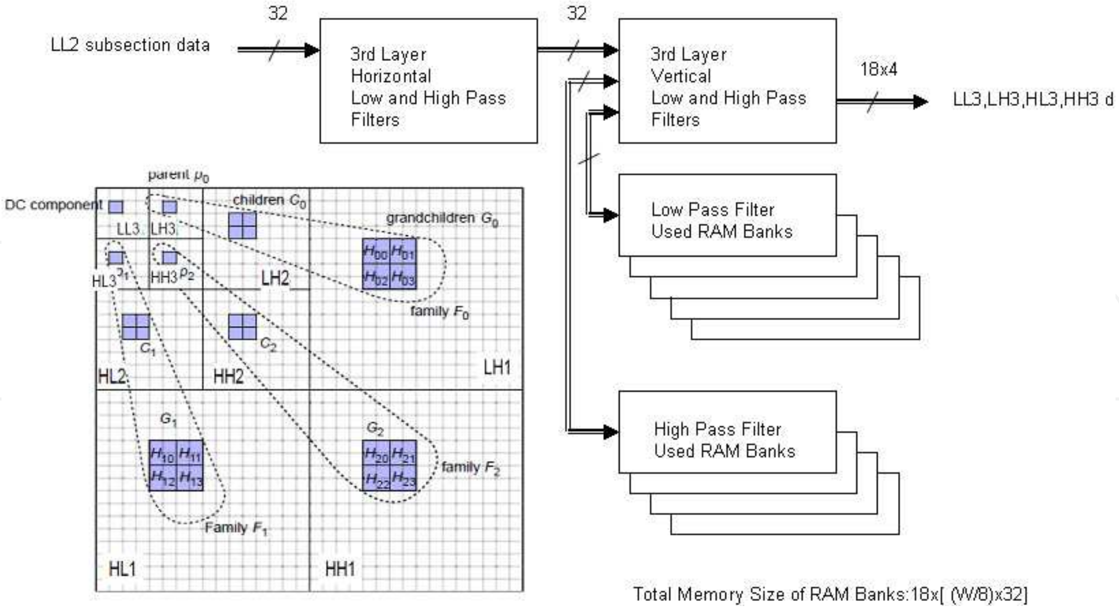


Fig. 8c. DWT Flow (3)

3.5 BPE process

The BPE module is the actual unit to perform data compression. When DWT acknowledges that one section data is completed and saved in the buffer, BPE retrieves the wavelet domain data from buffer and uses different compression scheme for different DWT sub-section data. According to various compression ratio requirements, BPE performs data truncation or appends zero fill bits. After necessary header information is added, the compressed data is sent to mass memory word by word for storage.

The compression data format is listed in Table 2. Within a segment, BitDepthDC is defined as the bit number of the maximum value in all DC coefficients. BitDepthAC is defined as the bit number of the maximum value in all AC coefficients. The amount of quantization q' of DC coefficients is determined by the dynamic range of the AC and DC coefficients in a segment in Table 3. DC quantization factor q is defined as q= max(q', BitShift(LL3)). The value of q indicates the number of least significant bits in each DC coefficient that are not encoded in the quantized DC coefficient values. The number of bits needed to represent each quantized DC efficient, N = max {BitDepthDC – q, 1}. For example, one segment has BitDepthDC=16 and BitDepthAC=4. According to Table 3, the DC quantization amount

Segment Header
Initial coding of DC coefficients
Coded AC coefficient bit depths
Coded bit plane b=BitDepthAC-1
Coded bit plane b=BitDepthAC-2
…………
Coded bit plane b=0

Table 2. Compression Data Format

DC and AC dynamic range	q' value	Remark
$BitDepthDC \le 3$	q' = 0	DC dynamic range is very small; no quantization is performed
$BitDepthDC - (1 + \lfloor BitDepthAC / 2 \rfloor) \le 1$ $and\ BitDepthDC > 3$	q' = BitDepthDC-3	DC dynamic range is close to half the AC dynamic range
$BitDepthDC - (1 + \lfloor BitDepthAC / 2 \rfloor) > 10$ $and\ BitDepthDC > 3$	q' = BitDepthDC-10	DC dynamic range is much higher than half the AC dynamic range
Otherwise	q' $= 1 + \lfloor BitDepthAC / 2 \rfloor$	DC dynamic range is moderately higher than half the AC dynamic range

Table 3. DC Coefficient Quantization

q' = 16 -10 = 6. Then, DC quantization factor q is 6 and N = 16 - 6 =10. So, each DC coefficient bit(15) ~ bit(6) are encoded using coding quantization method, and bit(5) ~ bit(4) will just concatenated immediately at the end of the coded quantized DC coefficients of the segment, finally bit(3) ~ bit(0) are encoded at AC stage0 phase. The detailed coding algorithm is described in CCSDS 122.0-B-1 (2005).

The AC part data have the major portion of image (63/64), so AC part data coding dominates the whole compression performance. The CCSDS adopts bit plane encoding concept, that is, the most important bits of each AC subsection part data is encoded first, then less important bits, until specified segment byte limit size is achieved or bit 0 of each data segment is encoded. Even, it is needed to append zero bits to achieve segment byte limited size.

In order to have good compression efficiency, the CCSDS standard specifies AC Parent, Children, and Grand Children data to proceed entropy symbol mapping scheme. The basic concept of entropy coding is to use smaller bit pattern to represent more frequently repeated bit pattern.

In the CCSDS standard, a "gaggle" consists of a set of 16 consecutive blocks within a segment. There are two running phases in our design to use entropy coding scheme to represent the final coding result, pre-running phase and normal running phase. The pre-running phase is designed to get 2-bits、3-bits、and 4-bits entropy value for each gaggle on each bit-plane. The normal running phase is to use entropy table to map the final coding bits string. The detailed coding algorithm is described in CCSDS 122.0-B-1 (2005). The IDC implementation block diagram is shown in Fig. 9.

3.6 FPGA design optimization

Some design skills are used to save the limited multiplier and memory resources in the FPGA chip. In the Equation (1) and (2), nine multipliers for Low Pass Filter and seven multipliers for High Pass Filter are needed. Totally 3 x 2 x (9+7) = 96 multipliers are needed for 3 layers, horizontal and vertical, low pass and high pass filter. By using the multiplexers, adders and timing sharing algorithm in our IDC design as in Fig. 10 and 11, three multipliers for Low Pass Filter and two multipliers for High Pass Filter are needed. In other words, totally 3 x 2 x (3+2) = 30 multipliers are needed for 3 layers 2 dimension FDWT architecture, i.e. 66 multipliers are reduced.

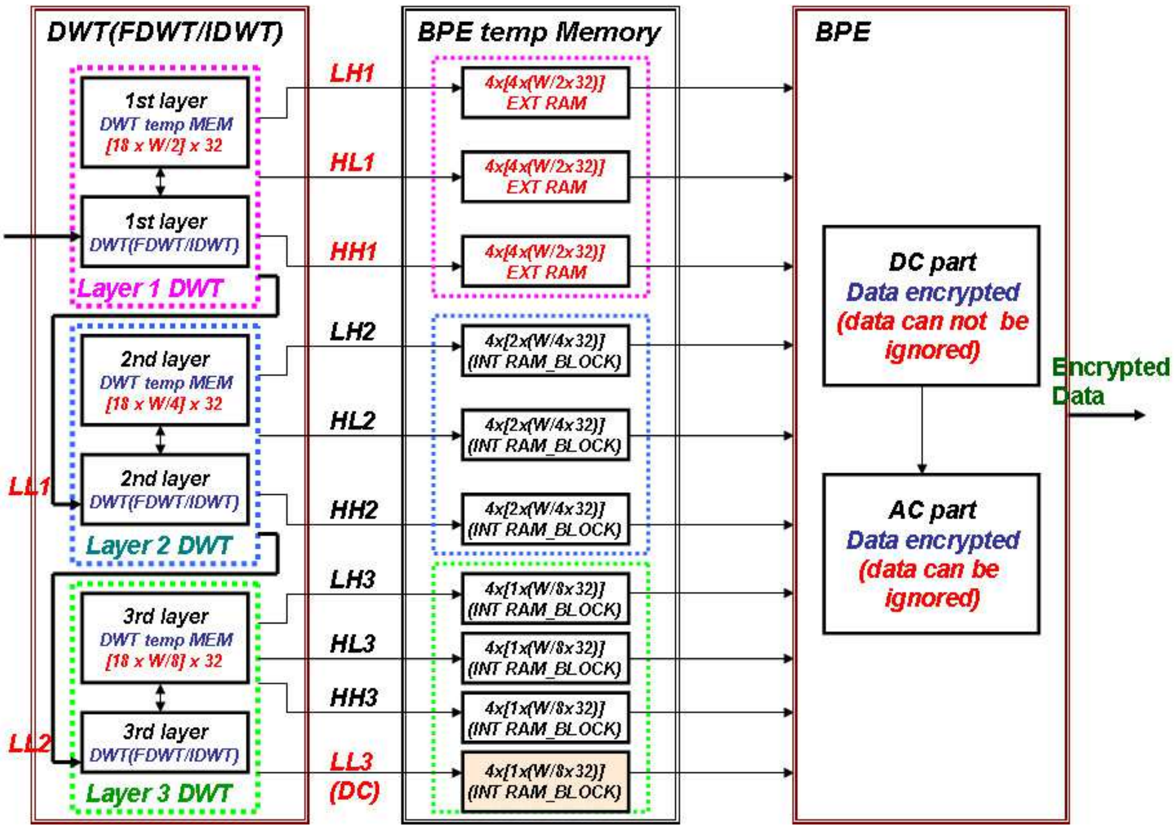


Fig. 9. IDC Implementation Block Diagram

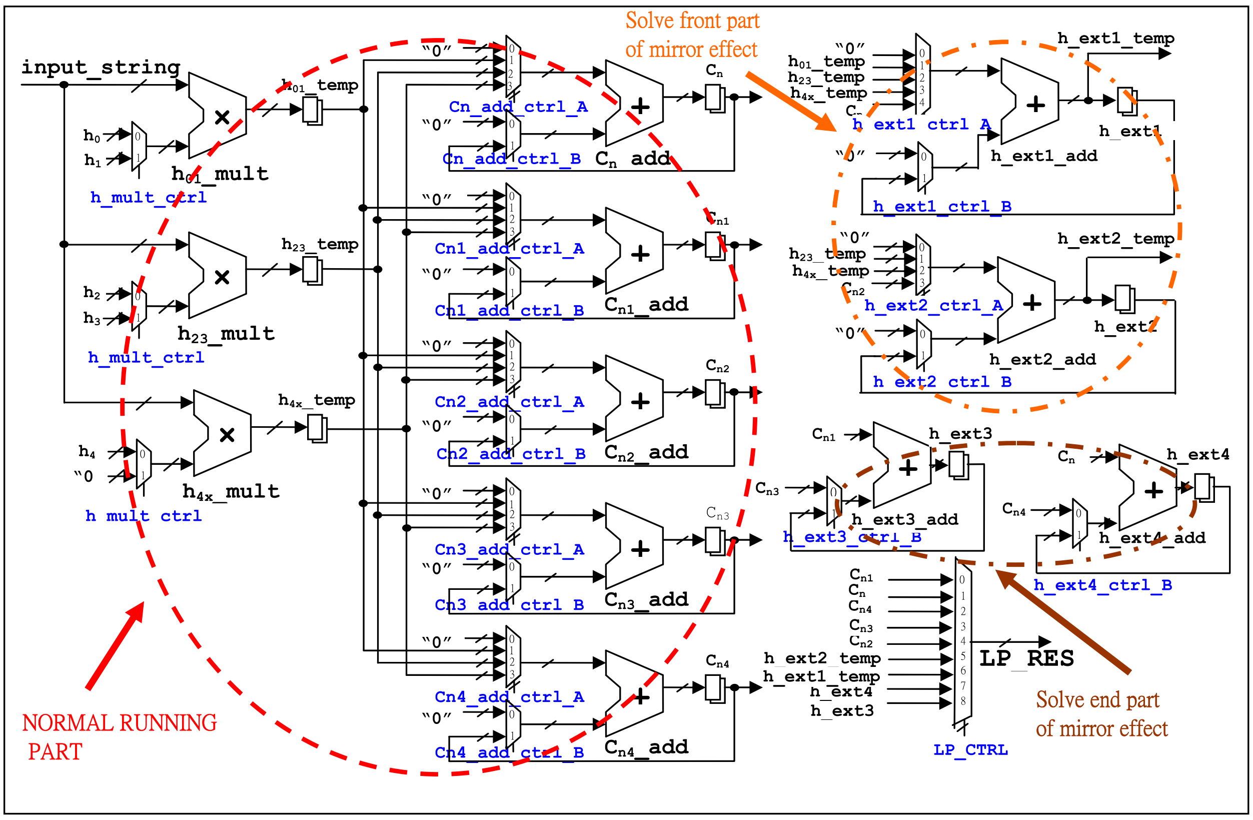


Fig. 10. Approach of 9 Taps Low Pass Filter in IDC

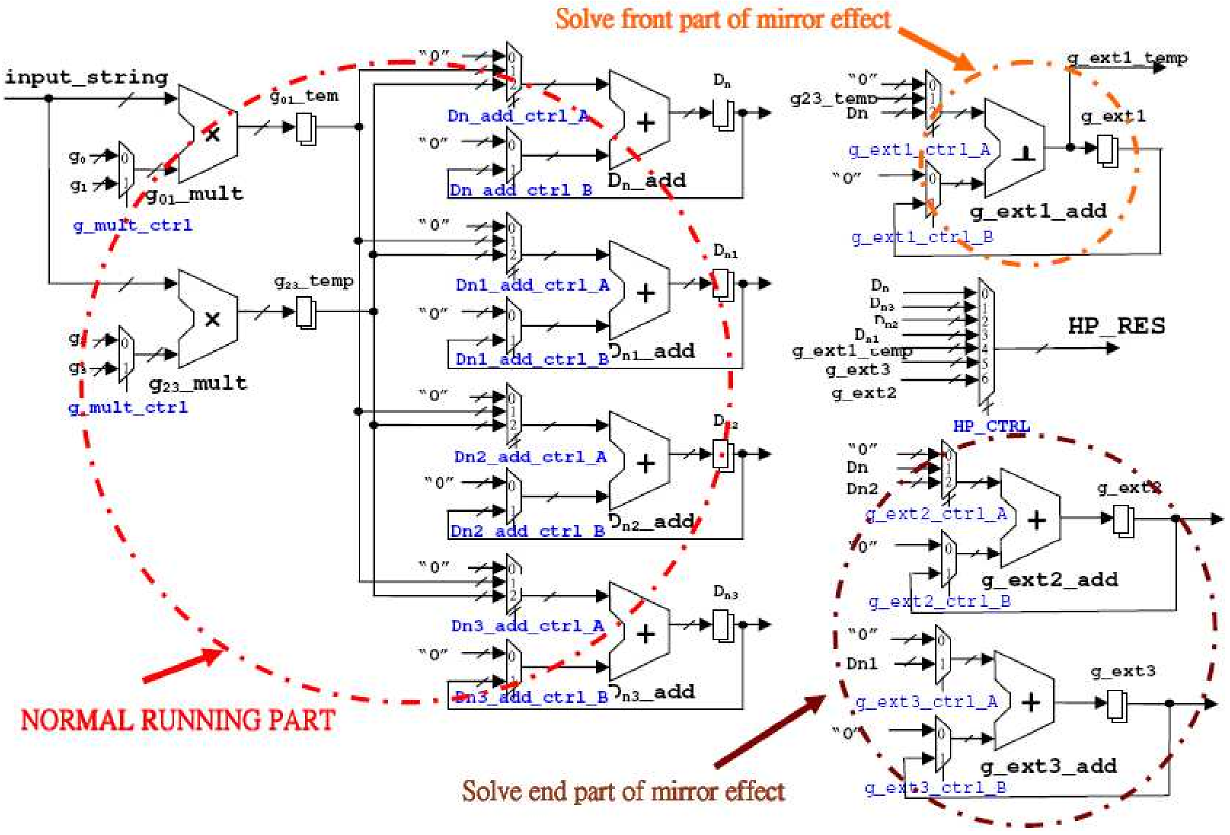


Fig. 11. Approach of 7 Taps High Pass Filter in IDC

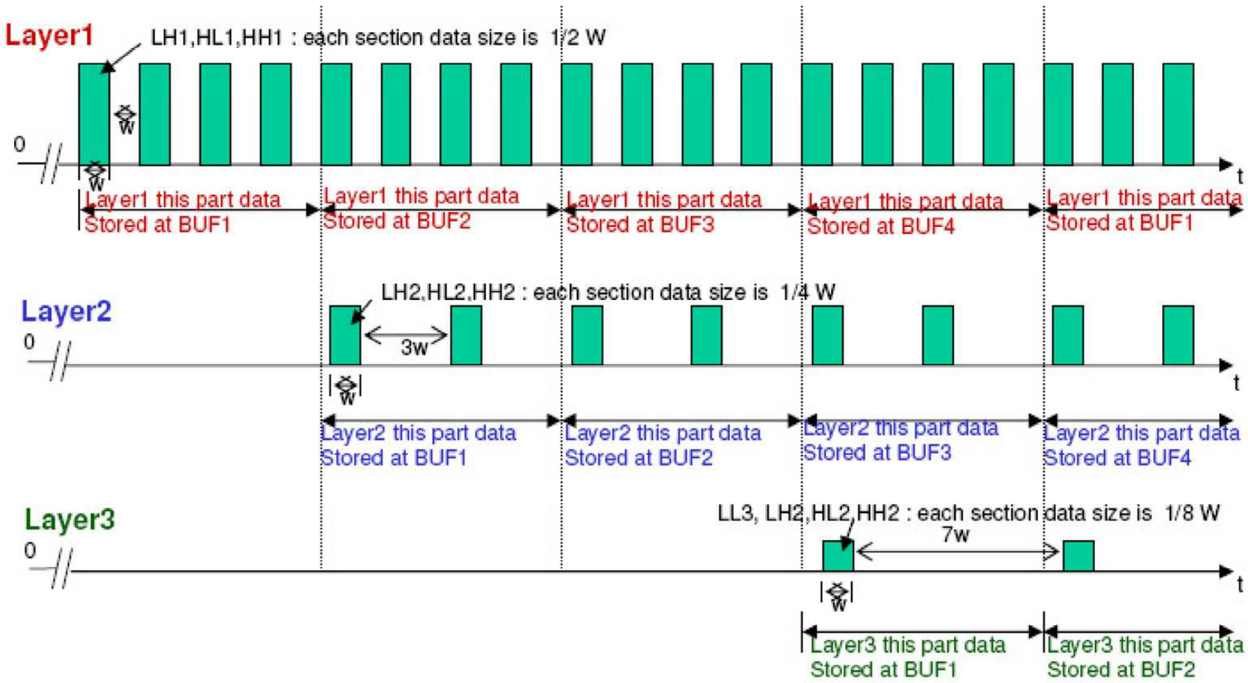

Layer1
LH1,HL1,HH1 : each section data size is 1/2 W
W
0
t
Layer1 this part data Stored at BUF1
Layer1 this part data Stored at BUF2
Layer1 this part data Stored at BUF3
Layer1 this part data Stored at BUF4
Layer1 this part data Stored at BUF1
Layer2
LH2,HL2,HH2 : each section data size is 1/4 W
3W
W
0
t
Layer2 this part data Stored at BUF1
Layer2 this part data Stored at BUF2
Layer2 this part data Stored at BUF3
Layer2 this part data Stored at BUF4
Layer3
LL3, LH2,HL2,HH2 : each section data size is 1/8 W
7w
W
0
t
Layer3 this part data Stored at BUF1
Layer3 this part data Stored at BUF2

Fig. 12. DWT Timing Relation between Three Layers

The timing relation chart of DWT three layers is shown in Fig. 12. The "W" is the original source image width (pixels/line) which is 12000 for PAN and 6000 for MS in FROMOSAT-5.

The source clock is 45 MHz for PAN and 11.25 MHz for MS. In the Layer1, LH1, HL1 and HH1 data are generated every two source clocks with data size W/2 words. In the Layer2, LH2, HL2 and HH2 data are generated every four source clocks with data size W/4 words. In the Layer 3, LL3, LH3, HL3, HH3 data are generated every 8 source clocks with data size W/8 words. The data in different layers are generated interleavely to achieve high throughput for real time data processing.

The buffer size to handle the image compression is Width * Length for frame-based method. But for the strip-based method, just fixed buffer size, Width * 138, is needed. For 8 minutes FORMOSAT-5 PAN imaging data, the buffer size for frame-based will be 200,000 times of buffer size for strip-based. So, it is very important to use strip-based method to save memory size, cost, and handling time in satellite application, even for ground image handling. The total required memory can be reduced as shown in Table 4. It can save the cost and reduce the power consumption used by memory chips.

	CCSDS 120.1-G-1	FORMOSAT-5 Approach
Low Pass Filter	[2 x (**9** x W/2n)] x 32 bits	[2 x (**5** x W/2n)] x 32 bits
High Pass Filter	[2 x (**7** x W/2n)] x 32 bits	[2 x (**4** x W/2n)] x 32 bits

Where : W is pixels per line (12000); n is layer number (1~3)

Table 4. Memory Size in FDWT Implementation

The Xilinx Virtex-5QV FPGA static power is 2.49761 watts estimated by Xilinx XPower Analyzer tool. Since the throughput is 40.4 Msamples/sec for PAN, the power consumption of the compression FPGA is about 0.06 Watt/Msamples/sec. The total power consumption of the PAN compression board is about 5 watts, including SRAM and IO circuit, i.e. equivalent to 0.124 Watt/Msamples/sec.

There are some benefits to use space grade FPGA chip than ASIC. The space grade FPGA has good anti-radiation capability. The line pixel number and clock rate can be reconfigured. There are some comparisons of data compression chips in Table 5.

Model Features	FORMOSAT-5 RSI EU IDC	CAMBR DWT+BPE IC [Winterrowd 2009]	ANALOG DEVICES ADV202
Chip Type	Xilinx Space Grade FPGA	ASIC	ASIC
Compression Algorithm	CCSDS 122.0	CCSDS 122.0	JPEG2000
Line Width (Pixels)	12000	8192	4096
Bits Per Pixel	12	16	8, 10, 12, 14, 16
Input Data Rate	480Mbps	320Mbps	780Mbps
Radiation(Total Dose, Si)	700K	>=50K	Commercial
Power Consumption (Watt/Msamples/sec)	0.06	0.17	0.05

Table 5. Data Compression Chip Comparison

4. Image quality verification

The 12-bit test images in the CCSDS official website have been tested and similar results are gotten as in the CCSDS report. In order to consider more practical case, one North Vancouver image taken by FORMOSAT-2 satellite on 2009/12/9 is adopted. The compression ratios are set 1.5, 3.75 and 7.5. The Peak Signal to Noise Ratio (PSNR) is used as the performance index.

$$PSNR \equiv 20\log_{10}\frac{2^{B}-1}{\sqrt{MSE}}(dB), \tag{5}$$

where B denotes the bit depth and the Mean Squared Error (MSE) is given by

$$MSE = \frac{1}{w \cdot h}\sum_{i=1}^{w}\sum_{j=1}^{h}\left(x_{i,j} - \hat{x}_{i,j}\right)^{2} \tag{6}$$

where $x_{i,j}$ is the pixel of the original image, $\hat{x}_{i,j}$ is the pixel of the decoded image, w is the width of image and h is the height of image.

In our verification, one 8-lines strip-based segment is adopted with 1500 blocks for PAN and 375 blocks for MS. The average PSNR is calculated by Matlab® software. The test results are listed in the Table 6.

Compression Ratio	Image / Methods	Panchro-matic Band	Red Band	Green Band	Blue Band	Infrared Band
CR=1.5	IDWT	Lossless	Lossless	Lossless	Lossless	73.1
	FDWT	51.1	51.1	51.1	51.1	51
CR=3.75	IDWT	47.3	47.8	44.3	45.3	41.1
	FDWT	47.7	48	45	45.8	41.7
CR=7.5	IDWT	43.1	41.8	37.6	38.1	38.5
	FDWT	43.6	42.2	38	38.5	35.1

* IDWT: Integer Discrete Wavelet Transform FDWT: Floating Point Discrete Wavelet Transform

Table 6. Image PSNR under Various Compressions

When the IDWT is used with compression ratio 1.5, the PSNR is very large to indicate near lossless compression, except the infrared band. When the FDWT is used with compression ratio 7.5, the PSNR may drop to 35dB which is worse than average PSNR 56.77dB using six 12-bit CCSDS test images. This is mainly because North Vancouver image shown in Fig. 13 is much more complicated than the standard CCSDS test images.

To use the satellite image as data input to real compression hardware, a set of simulated Focal Plane Assembly (FPA) is under development as illustrated in Fig. 14. The satellite image taken by FORMOSAT-2 is expanded from 8 bits to 12 bits per image pixel by adding random value of 4 least significant bits to simulate FORMOSAT-5 image. The test image can be downloaded from the personal computer to the image sensors simulator which is to replace the real image sensor array in the FPA. Then the test image can be transmitted out by the FPA simulator like real push broom image data. The test image will be compressed by hardware, then decompressed by software to check the hardware compression performance to simulated satellite image.

To have a quick check on hardware function, a test image with 1024 pixels x 1024 pixels size and 12 bits resolution has been downloaded to a prototype board. The test image is compressed by hardware, and then decompressed by software. These two images are shown

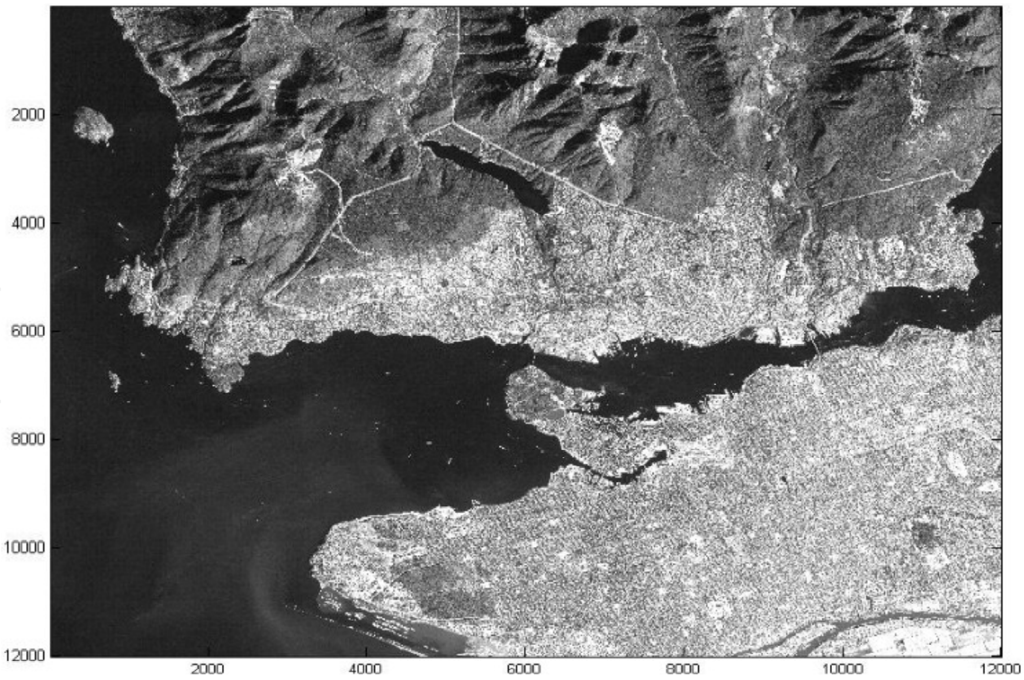


Fig. 13. North Vancouver Image Taken by FORMOSAT-2 satellite

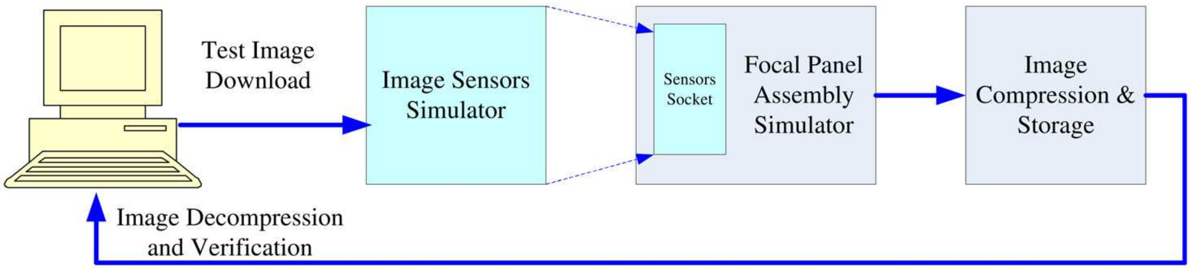
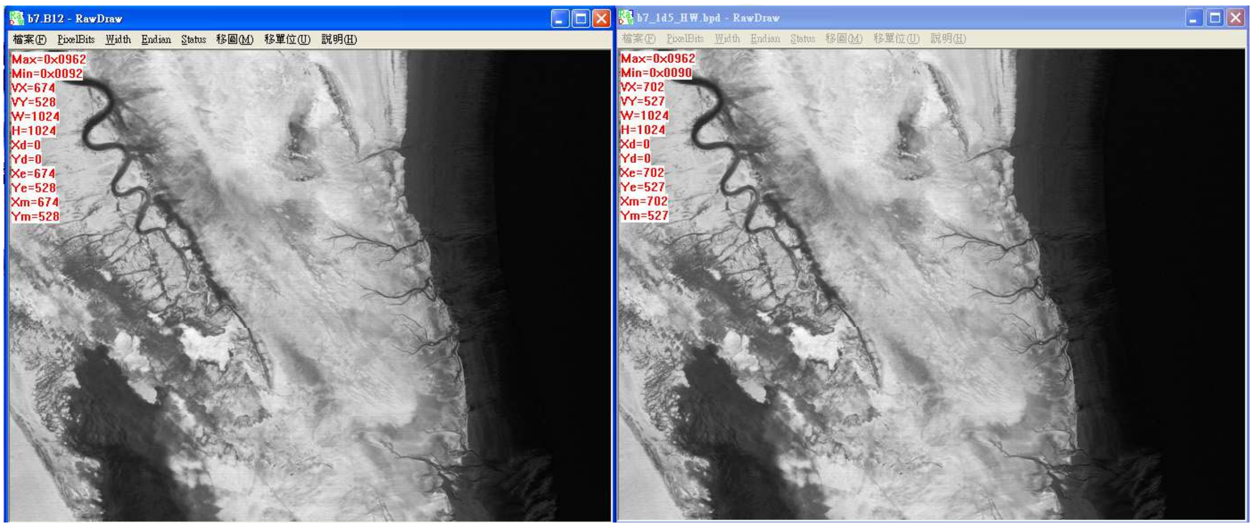


Fig. 14. Architecture of Image Compression Verification on Hardware

in Fig. 15. The PSNR is 82.8dB for compression ratio 1.5, 56.9dB for compression ratio 3.75, and 49.2dB for compression ratio 7.5.


b7.B12 - RawDraw
檔案(F) PixelBits Width Endian Status 移圖(M) 移單位(U) 說明(H)
b7_1d5_HW.bpd - RawDraw
檔案(F) PixelBits Width Endian Status 移圖(M) 移單位(U) 說明(H)

Max=0x0962
Min=0x0092
VX=674
VY=528
W=1024
H=1024
Xd=0
Yd=0
Xe=674
Ye=528
Xm=674
Ym=528

Max=0x0962
Min=0x0090
VX=702
VY=527
W=1024
H=1024
Xd=0
Yd=0
Xe=702
Ye=527
Xm=702
Ym=527

Fig. 15. Test Image before Compression (left) and Test Image after Decompression (right)

5. Conclusion

In this chapter there has been described the implementation of CCSDS recommended image data compression. The parallel processing, time sharing and computation via pure hardware in FPGA chip can achieve high-performance computing. The image data compression module based on FPGA has been developing to provide enough compression ratios with required image quality for FORMOSAT-5 mission. The performance has been verified by standard CCSDS 122.0 test images and FORMOSAT-2 images. The technology can be used on similar image data compression application in space. The compression throughput can be promoted following the improvement on the FPGA technology. The main advantage of this technique is that it allows real time image compression by efficient hardware implementation with low power consumption. This makes it especially suitable for satellite remote sensing.

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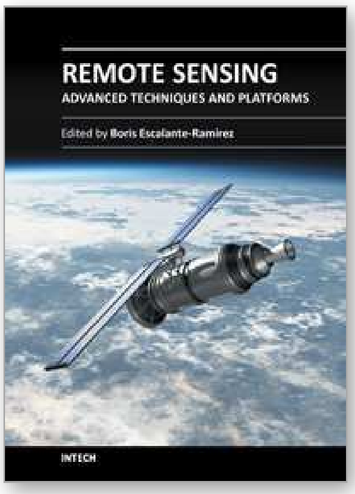
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