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Integration of Electrografted Layers for the Metallization of Deep Through Silicon Vias

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1. Introduction

After many years as a hypothetical possibility, 3D integrated circuits (3D IC) stacking has emerged as a potential key enabler for maintaining semiconductor performance trends. Implementing 3D, however, will almost certainly require development of through-silicon vias (TSVs), which in the past few years have been elevated by the semiconductor industry to the status of a crucial mainstream technology.

TSVs sit at the foundation of the 3D-IC revolution and are a key enabler for extending semiconductor integration trends into a new phase. Integrated device manufacturers and fabless design houses need small, high-density, fine-pitch vias for improved signal integrity and Si real-estate savings. They need them now, and cannot wait for very thin wafer processing and handling technologies to become mainstream – TSVs must cope with current mainstream wafer thickness.

Deep TSVs with aspect ratio (AR) greater than 15:1 elegantly fulfill both requirements. But they cannot be manufactured with acceptable yield/cost using traditional dry processes for liner, barrier and seed deposition. Chemical and physical vapor deposition (CVD, PVD) techniques show basic shortcomings and impose high capital investments, holding back the industry-wide adoption of 3D-IC solutions. Beyond that, physical limitations of PVD and CVD techniques prevent reaching a good step coverage of the deposited layers inside the vias (step coverage is defined by the ratio between thickness deposited on top vs. bottom of the vias), which is required to perform void-free gap filling of electroplated copper.

Electrografting (eG) and chemical grafting (cG) (Bureau et al., 1999; Palacin et al., 2004; Pinson & Podvorica, 2005; Voccia et al., 2006; Belanger & Pinson, 2011) are two fundamental molecular engineering technologies, delivering high-quality films for high-AR (HAR) TSVs (Suhr et al., 2008). The term “grafting” indicates the formation of strong chemical bonds at the molecular level between the underlying layer’s extreme surface (e.g., silicon) and the film being grown from the surface out (e.g., the isolation liner).

This nanotechnology solution generates surface-initiated conformal films which are thin, continuous, adherent and uniform. They are wet-process techniques, operated in standard plating tools, which have proven their efficiency to deposit ultra-thin (< 10nm) seed layers on PVD (Haumesser et al., 2003, 2004; Raynal et al., 2006) or atomic layer deposition (ALD) (Shih et al., 2004; Shue, 2006) diffusion barriers for interconnect back end of line (BEOL) applications.

1.1 Electrografting (eG) and chemical grafting (cG) mechanisms

Electrografting is based on surface chemistry formulations and processes. It is applied to conductive and semiconductive surfaces, and enables self-oriented growth of thin coatings of various materials, initiated by in-situ chemical reactions between specific precursor molecules and the surface. Contrary to electrodeposition which requires a potential supply throughout deposition to fuel the redox processes, electrografting is an electro-initiated process which requires a charged electrode only for the grafting step, but not for the thickening. As eG is mainly (but not only) a cathodic process, it can generally be applied to various metallic and semiconducting surfaces without any concern over oxide formation.

Electrografting of vinylic polymers onto conducting surfaces has historically been achieved via a direct electron transfer from the cathode to the electro-active monomers in solution. In this approach, eG occurs when vinylic monomers such as acrylonitrile (AN), methacrylonitrile (MAN), vinylpyridine (VP), and methyl methacrylate (MMA), all members of the family of electron-deficient alkenes, are submitted to reductive electrolysis, with a classical three-electrode setup in an anhydrous organic medium (Deniau et al., 1992a). Strictly anhydrous conditions are required here because the resulting radical-anion, together with the anions that allow the propagation of the growing grafted polymer chains, are highly sensitive to proton sources.

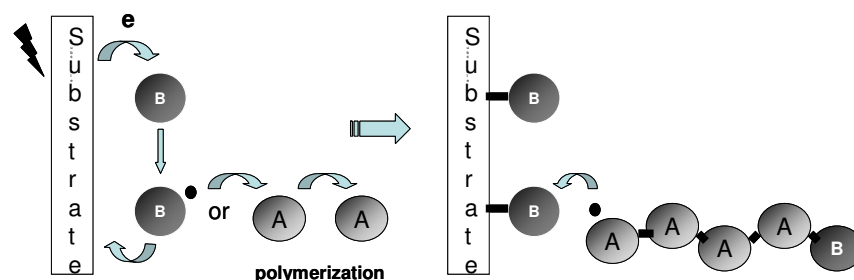


Fig. 1. Schematic representation of radical polymerization electrografting process.

Radical polymerization does not suffer the same drawback and is easily performed in protic conditions (Deniau et al., 2006). Mechanisms of radical polymerization (Tessier et al., 2009) presented in fig. 1 show that polymer electrografting is an electro-induced grafting process followed by a purely chemical propagation step. The first electro-induced step is crucial to form the chemical bond between the polymer and the surface. A specific organic precursor (B) is used both to form a first primer grafted layer and to initiate the polymerization of the vinyl monomer (A) in solution. The termination step of the polymerization leads to the grafting of macromolecular chains ($-\text{[A-A-A]}_n\text{-B}$) onto the first primer grafted layer.

Chemical grafting is based on the same fundamental mechanisms as electrografting, and is used on any surface (including non-conductive surfaces), electron being replaced by a reducing agent (Mevelléc et al., 2007).

1.2 Benefits of electrografting (eG)

Electrodeposition has been known for years for coating conducting surfaces with metals. Electroplating (Kanani, 2005; Schlesinger & Paunovic, 2010) is currently the most widely used method for coating surfaces in many industries (automotive, petrochemical, aerospace) including printed circuit boards, vias and copper interconnections for electronics.

Starting in the 80's with the electrochemical reduction of acrylonitrile on a metallic cathode (Lecayon et al., 1982), electrografting is a relatively new technique, with two major differences compared to electrodeposition: (I) eG being an electro-initiated process, i.e. a process in which Faradaic electrochemical reactions are coupled to a range of non-Faradaic chemical reactions, current densities applied for thickening are lower than the current densities required by electrodeposition techniques; and (II) the initial charge transfer to the first monomers leads to the formation of a direct covalent bond between some surface atoms and carbon atoms of the polymeric backbone.

Lower current densities applied are a benefit of electrografting technology when applied to resistive underlying layers, coatings being more uniform and less sensitive to the ohmic drop involved by underlying layer resistivity (Gonzalez et al., 2006; Mevellec, 2010).

Direct covalent bonds achieved between coatings and surfaces involve highly adherent electrografted films, via very strong substrate-molecules links, studied by quantum chemistry simulations (Bureau et al., 1996). Experimental evidence of those covalent bonds is not an easy task, and has been demonstrated by XPS analysis technique. As reported in (Deniau et al., 1992b), XPS measurements on very thin eG films exhibit a low-energy shoulder in the C1s signal. This peak cannot be observed for thicker films because it is buried under the strong C1s signals arising from the grafted polymer itself. The corresponding binding energy (283.6 eV) was later attributed to the carbon-nickel bond that links the polymer chain to the Ni electrode (Bureau et al., 1994).

2. Complete metallization of high aspect ratio (HAR) TSVs using electrografting

Aspect ratio is defined by the ratio between the diameter of the via and its depth, and a ratio greater than 10:1 defines the HAR TSVs category. Producing these vertical connections is achieved by: drill a blind hole through the silicon wafer, deposit a uniform liner layer of dielectric material to electrically isolate the via, deposit a barrier layer to prevent copper from diffusing into silicon, and then completely fill the via with electro-chemically deposited (ECD) copper. Chemical mechanical polishing (CMP) and wafer-thinning steps conclude the sequence.

2.1 Comparison between dry and wet TSVs metallization scheme

While the process flow to metallize TSVs is relatively simple, the industry's conventional approach to bringing it into volume production is, in essence, a patchwork of dry process equipment and consumables, such as plasma-enhanced CVD (PE-CVD), ionized PVD (iPVD), and ALD, which were originally designed for dual-damascene applications. One of the main benefits of electrografting is its large reduction in cost of ownership per wafer with respect to conventional dry approaches (Lerner, 2008; Truzzi & Lerner, 2009).

Comparison between dry and wet TSVs metallization scheme is presented in fig. 2. Two schemes are available for electrografting : (1) the deposition of the full stack "wet isolation/ NiB barrier/ Cu seed layer", followed by Cu filling using typical acidic Cu fill chemistry; (2) the deposition of "wet isolation / NiB barrier" followed by Cu filling using a new TSV-grade Cu fill chemistry. Path (2) is preferred because it requires only three steps (instead of four), which involves less cost and higher throughput.

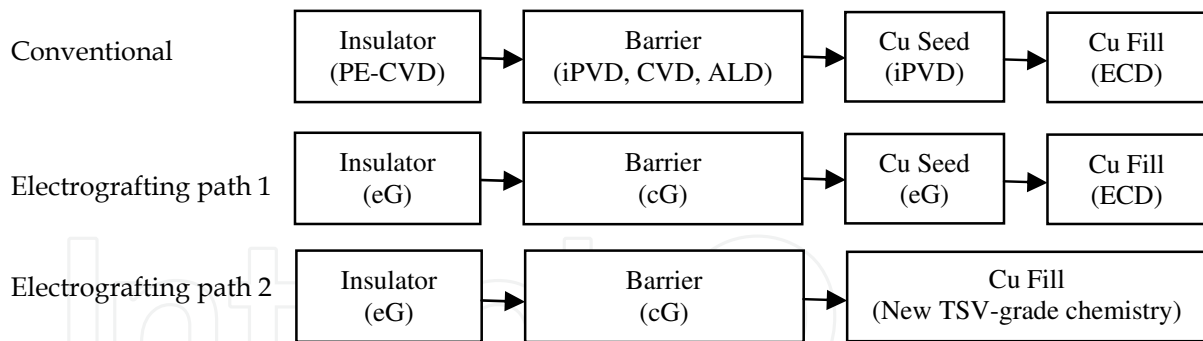


Fig. 2. Comparison between dry and wet (electrografting) TSVs metallization scheme.

2.1.1 Description of electrografting path 1 for TSVs metallization

A polymer layer is directly grafted onto the silicon surface, yielding a highly conformal and adherent coating. This first grafted layer acts as an insulating layer (fig. 3a) as well as an adhesion promoter for the subsequent barrier layer deposition, performed by chemical grafting (cG).

Chemical grafting is based on the same fundamental mechanisms as electrografting, and is used on non-conductive surfaces. Specific chemical groups have been chosen to strongly bond the barrier activator with the polymer. This improves adhesion between the barrier and the polymer through a chemical grafting step - it creates a chain of chemical bonds from the substrate to the barrier. The barrier film (fig. 3b) consists of a NiB alloy. Activation of the electrografted insulating layer is carried out at ambient temperature using a metallic catalyst.

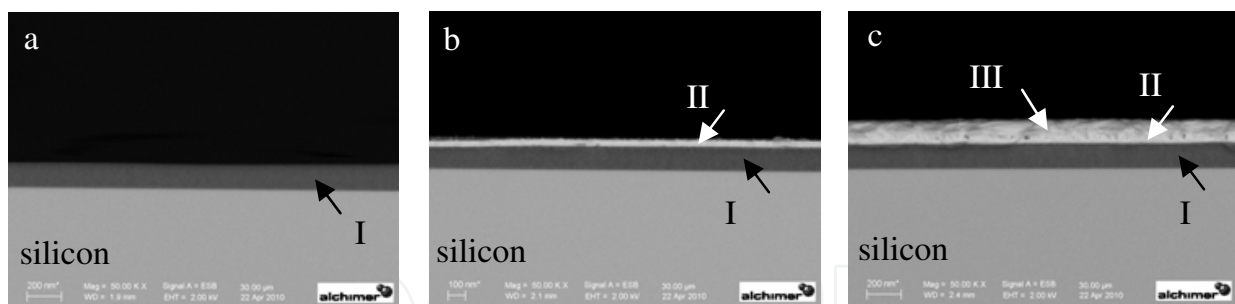


Fig. 3. SEM cross sections of wet insulator (I), NiB barrier (II) and Cu seed layer (III) electrografted on top of silicon surface.

A bath containing specific organics and copper is used to deposit a Cu seed layer (fig. 3c) on the NiB barrier by means of the same electrografting technique. An electrochemical process is applied to provide a conformal and continuous Cu seed layer directly on the NiB barrier.

Both NiB barrier and Cu seed layer can also be deposited on top of dry dielectrics, as for example SiO₂, SiC, SiOC or SiN. SEM cross-sections of barrier and Cu seed deposited on top of SiO₂ are reported in fig. 4.

The electrografted copper seed is also directly applicable to various dry-deposited diffusion barriers, without any adhesion promoter in between (Ledain et al., 2008; Raynal et al., 2009).

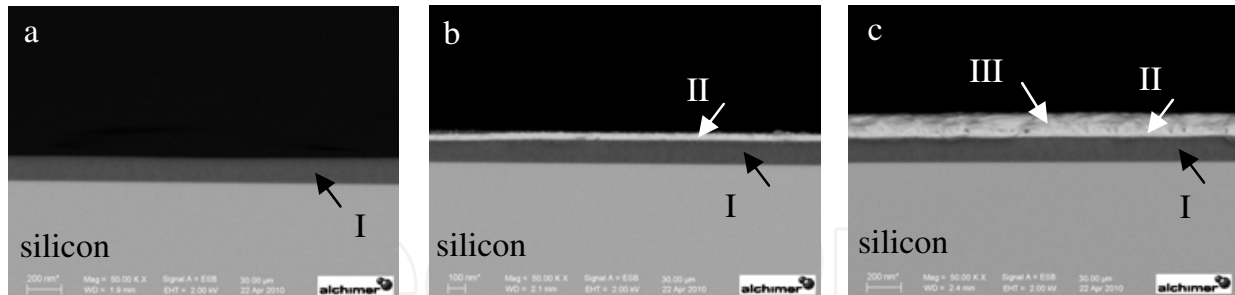


Fig. 4. SEM cross sections of NiB barrier (II) and Cu seed layer (III) electrografted on top of SiO_2 (I) surface.

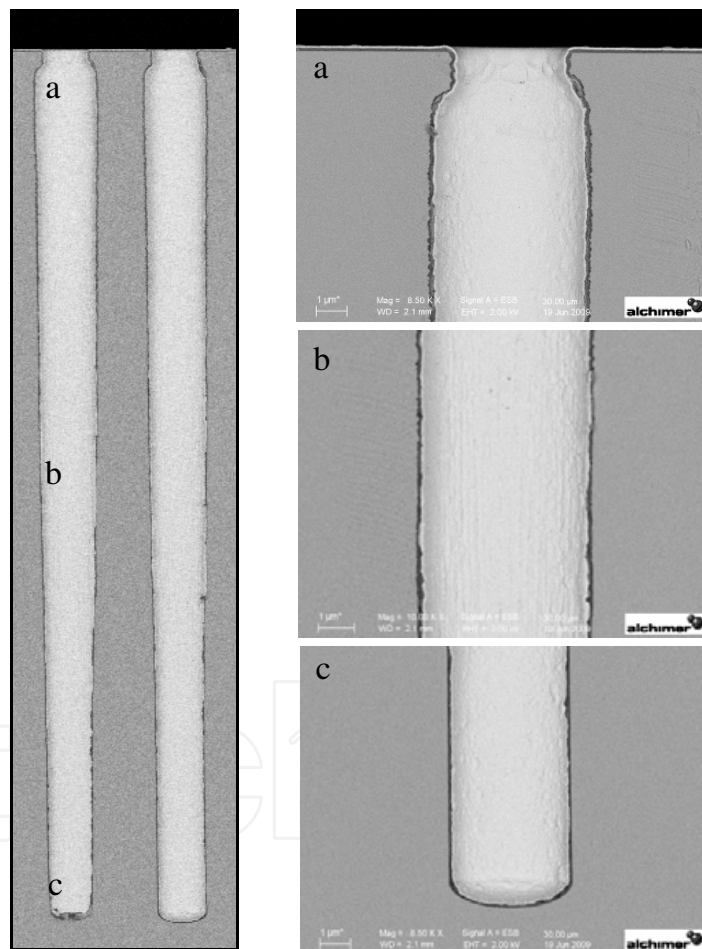


Fig. 5. SEM cross sections of high aspect ratio via (AR 18:1, $4\mu\text{m} \times 72\mu\text{m}$) coated with electrografted layers; (a) top of via, (b) via middle, (c) via bottom.

Electrografting and chemical grafting formulations and processes fulfill all standard wafer fab requirements and safety guidelines and have been developed and specifically tailored for TSV diameters ranging from 1 to $200\mu\text{m}$, covering a depth/diameter AR range from 2:1 to 20:1 (fig. 5). Higher ARs are possible.

Electrografted and chemical grafted layers, activated from the surface, are not sensitive to its topography, and fit perfectly well with the highly scalloped TSVs sidewalls induced by Bosch etching process (fig. 6).

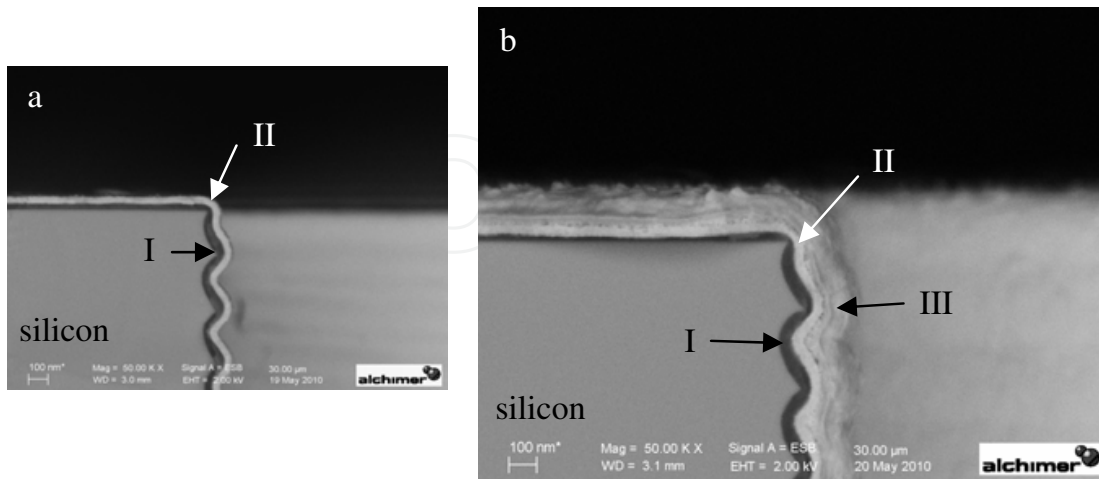


Fig. 6. SEM cross sections of wet insulator (I), NiB barrier (II) and Cu seed layer (III) on top of scalloped silicon surface.

Wet TSVs metallization process is scalable up to 12inch wafers, as illustrated in fig. 7 with three 12inch wafers stopped at different steps of the metallization process.

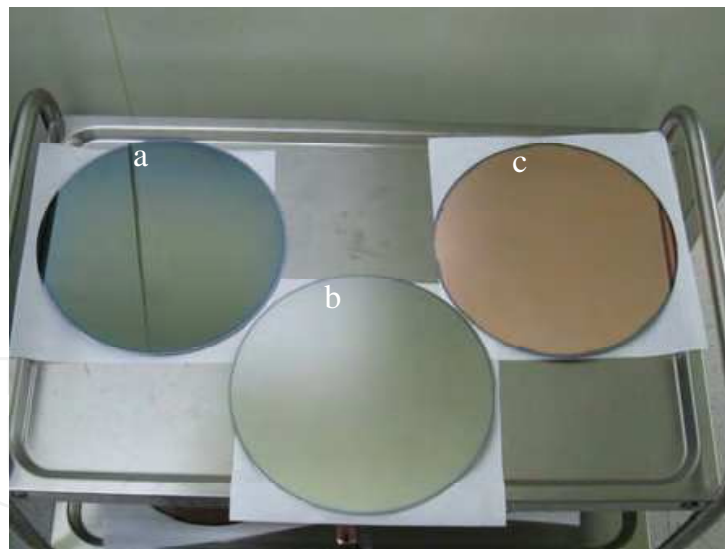


Fig. 7. Top view of 12inch wafers with various layers electrografted on them; (a) wet insulator; (b) wet insulator / NiB barrier; (c) wet insulator / NiB barrier / Cu seed layer.

2.1.2 Description of electrografting path 2 for TSVs metallization

Wet insulator and NiB barrier deposition remains exactly the same as in path 1.

Filling narrow, deep vias without voids is not an easy task. Most commercially available chemistries encounter problems due to the sheet resistance (R_s) of the underlying layer, and this is the reason why Cu-seed layers are required. However, because of the extremely poor

step coverage of dry-process barriers and seed layers (< 10%), sheet resistance values at the bottom of the via are very high, making it difficult to initiate the filling process.

Via filling completion directly from the barrier requires barrier layers with low resistivity values, and copper plating chemistries with low sensitivity to ohmic drop. NiB barrier has been selected because of its barrier properties (see section 2.2.2.), and because Ni-based barrier films present much lower resistivity values than conventional dry barriers (fig. 8). Indeed, NiB chemical grafting barrier formulations have been optimized to reduce the resistivity value below $25\mu\Omega\cdot\text{cm}$; this value makes it possible to eliminate Cu seed layers, and sets the stage for direct fill of TSVs from the barrier layer, further simplifying the TSV process sequence.

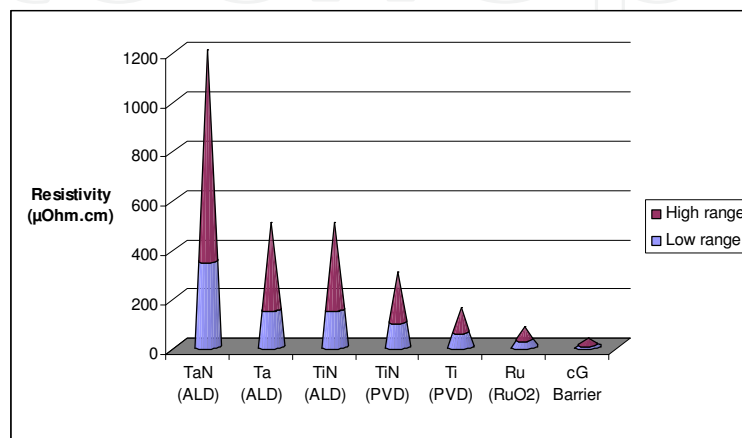


Fig. 8. Resistivity range of conventional dry barriers, compared with chemically grafted (cG) NiB barrier.

Today, a new mildly basic TSV plating chemistry is available to fill the vias (Truzzi, 2010) based on the same nanotechnology concept described in this paper. This TSV-grade chemistry is not sensitive to the sheet resistance of the underlying layer, and can be applied over R_s values up to $50 \Omega/\text{sq}$. It is fully compatible with industry standard wet-process tools and, in contrast with ECD solutions, it does not attack or degrade the underlying layer.

Some examples of copper filling in various TSV dimensions, achieved directly from the NiB barrier, are presented in fig. 9. The new TSV-grade Cu fill chemistry has been used in all cases. Fig. 9a shows an example of copper filling achieved in different TSV dimensions at the same time, which demonstrates the wide process window of this new TSV-grade chemistry regarding vias size.

2.2 Properties of electrografted wet insulator layer, NiB barrier layer, Cu seed layer and new TSV-grade Cu fill chemistry

Film thickness can be controlled to any value from 40 to 400 nm with maximum non-uniformity of 5% within wafer (300mm). This provides a step coverage value (bottom/top thickness ratio) up to 90% for liner and metal layers. As a reference, typical dry-process barrier step coverage values are lower than 10% for 10:1 aspect ratio TSVs. Adhesion of all layers was measured using a 16-squares scribe tape test method: all layers successfully passed the test. Film properties of each layer, as well as reliability test results, are discussed in detail in (Truzzi et al., 2009; Raynal et al., 2010). Selected basic film properties are summarized in table 1.

Parameter	Value	Unit	Notes
Wet insulator			
CTE	30	ppm/°C	
Dielectric constant	3		SiO ₂ = 4.2
Breakdown Voltage	28	MV/cm	SiO ₂ = 10
Capacitance Density	0.13	fF/μm ²	
Leakage current	15	nA/cm ²	SiO ₂ = 10-20
Surface Finish	1.6	Nm	SiO ₂ = 2
Substrate resistivity	< 200	Ohm.cm	
Young Modulus	3.4	Gpa	SiO ₂ = 107
Stress @ 200nm	10	Mpa	SiO ₂ = 100
Moisture Absorption	< 1%		168hrs @ 90%RH
TGA (1hr/temp. point)	450	°C	<4% mass loss
Contact angle	50%		
Chemical purity (at%)	S,F,Ca,Na,K : 0 Cl : 0.2 Organic polymer : 99.8		
NiB barrier			
Resistivity	25	μOhm.cm	TiN = 100-250
Rs uniformity	5	%	
Barrier property	Equivalent to TiN after 400 °C 2 hours		
Cu penetration after 400°C 2 hours	42	% barrier thickness	TaN/Ta = 54
Hardness	14.3	GPa	TiN = 25
Stress	200	MPa	TaN = 1500 TiN = -750
Cu seed layer			
Resistivity	1.8	μOhm.cm	ECD-Cu = 1.8
Rs uniformity	5	%	
Grain size	110	Nm	ECD-Cu = 100
Stress	50	MPa	
ECD gap-fill compatibility	No voids		
New TSV-grade Cu fill			
Resistivity	1.8	μOhm.cm	ECD-Cu = 1.8
Rs uniformity	5	%	
Chemical purity	Cl : 100x less than baseline plating chemistries C : 10x less than baseline plating chemistries S : equivalent to baseline plating chemistries		
Stress	50	MPa	
Copper gap-fill	No voids		

Table 1. Selected film properties of electrografted wet isolation, NiB barrier, Cu seed layer and new TSV-grade Cu fill, compared with industry baseline.

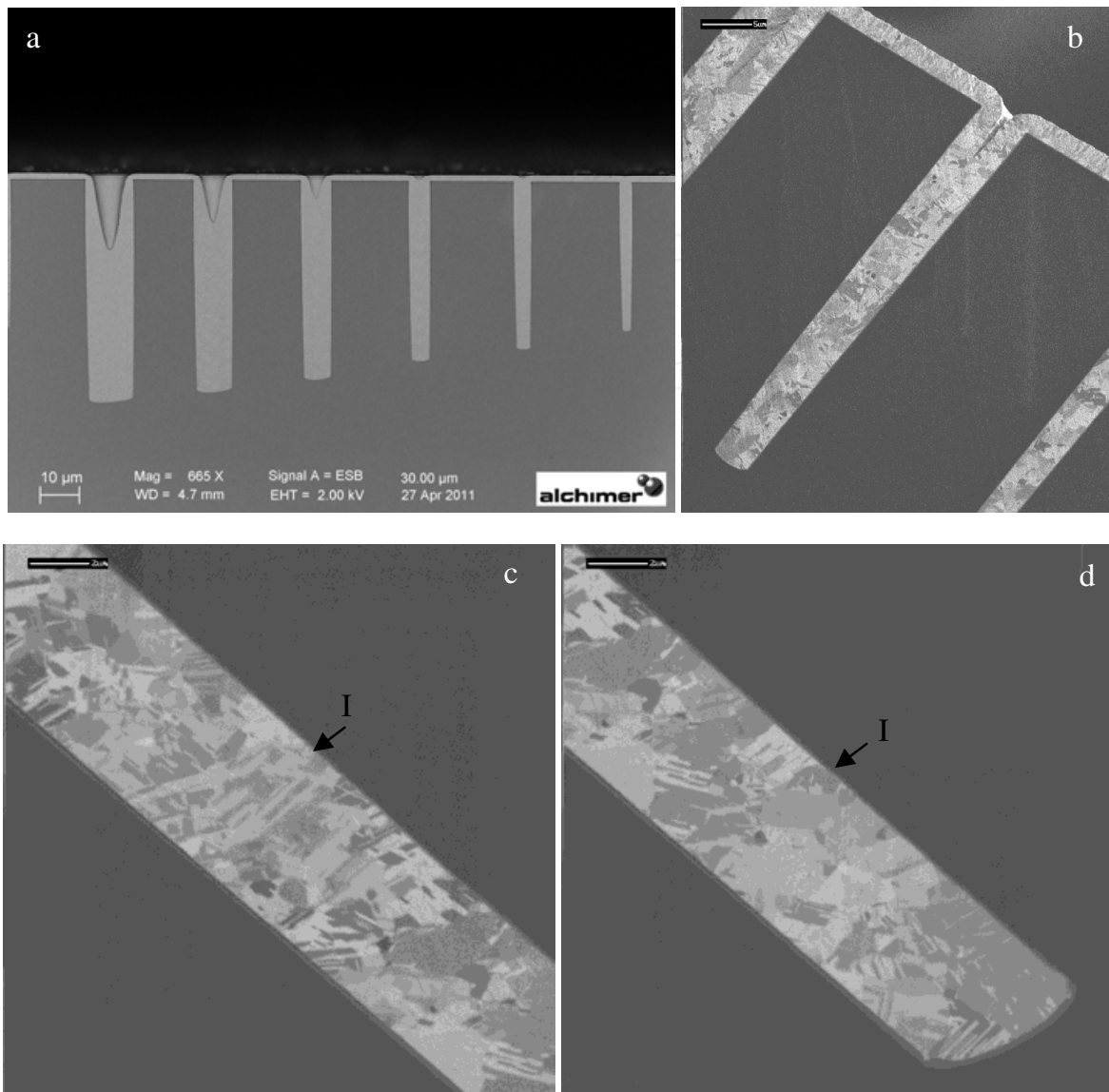


Fig. 9. SEM cross sections of copper filling achieved with the new TSV-grade Cu fill chemistry, directly from NiB barrier; (a) filling of various TSV dimensions (via diameter $3.5\mu\text{m}$ to $12\mu\text{m}$, AR 4.5:1 to 11:1); (b) filling of TSVs $5\mu\text{m} \times 50\mu\text{m}$ (AR 10:1); (c) middle depth of filled TSVs $5\mu\text{m} \times 50\mu\text{m}$, showing wet insulator layer (I); (d) via bottom of filled TSVs $5\mu\text{m} \times 50\mu\text{m}$, showing wet insulator layer (I).

2.2.1 Properties of wet insulator

Electrical properties of wet insulator have been characterized using conventional mercury probe analysis tool. Fig. 10 presents a typical $C(V)$ curve recorded with the stack wet insulator / Si p-doped. Dielectric constant calculated from this curve is 3. Breakdown voltage, leakage current and capacitance density have been measured from $I(V)$ curves performed with the same mercury probe analysis method.

Thickness of the wet insulator is measured by ellipsometry. Examples of typical $n=f(\lambda)$ and $k=f(\lambda)$ curves recorded with wet insulator are presented in fig. 11. According to $n=f(\lambda)$ curve, refractory index is measured in the range 1.7-1.8nm.

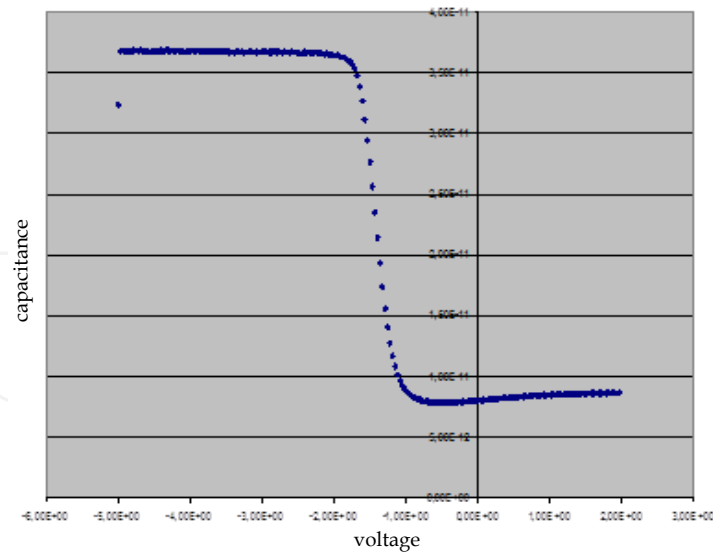


Fig. 10. Typical C(V) curve of the stack wet insulator / Si p-doped.

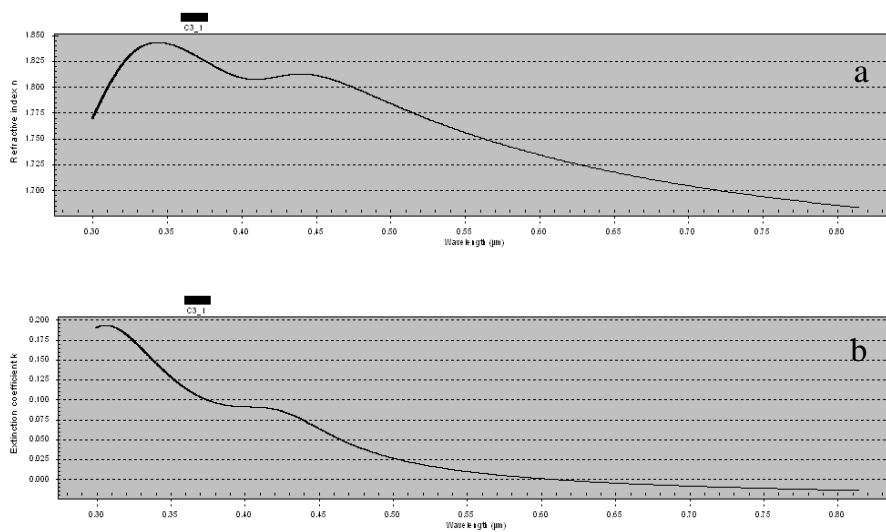


Fig. 11. Typical (a) $n=f(\lambda)$ and (b) $k=f(\lambda)$ curves recorded with wet insulator.

CTE (coefficient of thermal expansion) of the wet insulator is measured using an ellipsometer linked to a heater. As presented in fig. 12, a CTE of 30ppm/°C is measured for wet insulator, 30ppm/°C being the mean value obtained on four different samples. On each sample, CTE was measured after one cycle of sample warm and cool.

Wet insulator being a polymer, T_g value can be deduced from CTE curves (Fryer et al., 2001). Indeed, wet insulator thickness evolution vs. temperature being linear from 50°C to 200°C, this means that no microstructural reorganization is observed in this range of temperatures, and T_g value of the wet insulator is higher than 200°C.

Reduced modulus has been measured using nanoindentation analysis technique, with a maximum force applied of 5000 nN and a maximum indenting depth of 35 nm. Typical curve of force vs. penetration depth is presented in fig. 13a, Young modulus characterization being achieved during the loading of the indenter inside the wet insulator. Young modulus measurement of 4.05 GPa is the mean value of 15 measurements (fig. 13b).

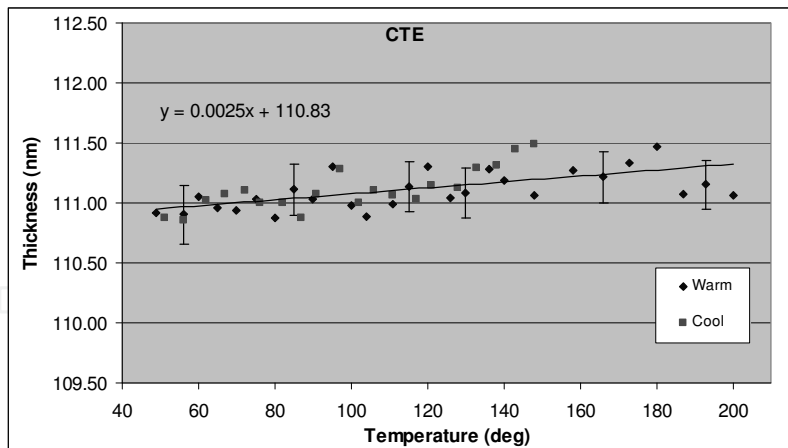


Fig. 12. Coefficient of thermal expansion (CTE) measured with wet insulator.

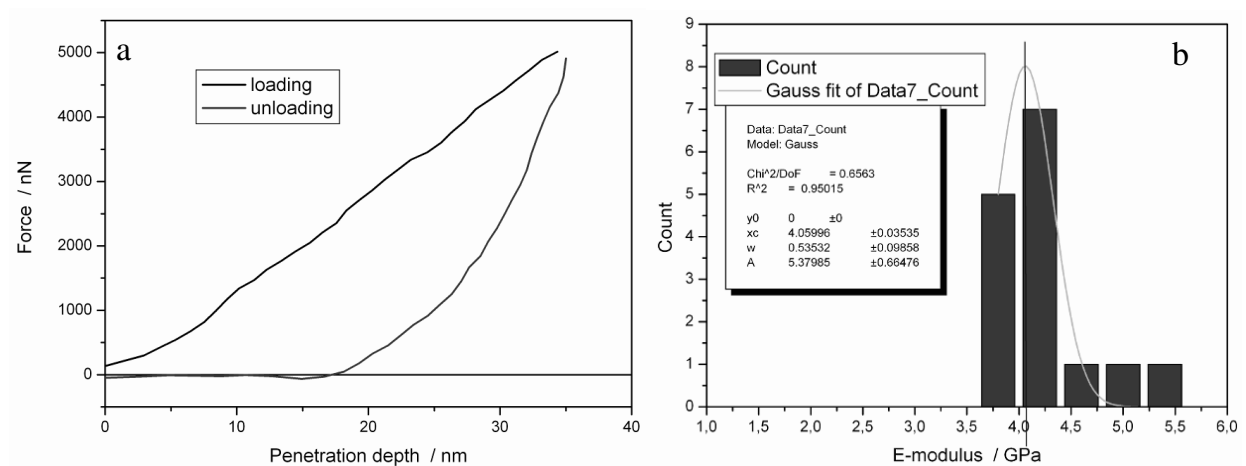


Fig. 13. (a) Typical curve of force vs. penetration depth recorded by nanoindentation analysis of wet insulator; (b) values obtained on 15 measurements.

Thermo-Gravimetry Analysis (TGA) has been performed to check the stability of the wet insulator under thermal stress. Experimental conditions are the following: anneal is achieved under nitrogen atmosphere, for a duration of one hour at each selected temperature. Range of analysis is 300°C - 500°C, with a step of 50°C between each experiment. Fig. 14 shows that less than 1% of mass loss is measured after 350°C applied during one hour to the wet insulator, and less than 4% after 450°C applied during one hour.

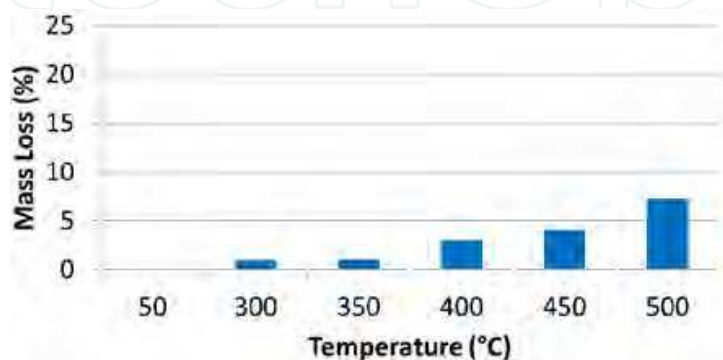


Fig. 14. Mass loss of the wet insulator as a function of temperature (1h / temp. point).

2.2.2 Properties of NiB barrier

Barrier property is measured by TOF-SIMS depth profile, after anneal of the complete stack (wet insulator / NiB barrier / copper) to 400°C during 2 hours under forming gas. Analysis is performed starting from the front side (copper) of the sample, or from the backside (silicon) of it. In the case of a start from the back side, a mechanical polishing and grinding of the sample is first performed to reduce silicon bulk thickness.

Examples of TOF-SIMS depth profiles are shown in fig. 15, x axis being representative of sample depth and y axis being proportional to compound quantity. Barrier property is quantified by the difference between NiB barrier and copper signals. The better is the barrier property, the higher is this difference.

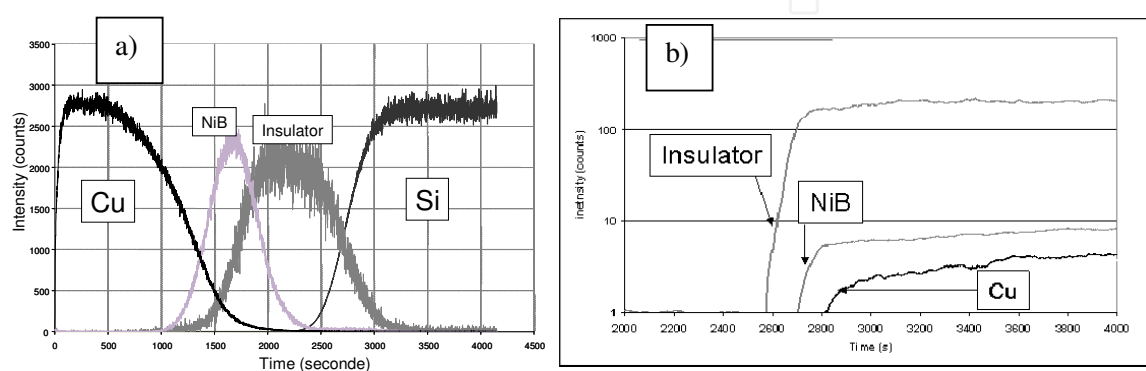


Fig. 15. ToF-SIMS depth Profile of Cu layer (100nm) on top of NiB barrier (40nm) and wet insulator (200 nm) after anneal to 400°C during 2 hours using (a) front side and (b) back side analysis.

As shown in fig. 15b, diffusion of Cu atoms occurred only into the NiB barrier layer. Cu atoms are effectively blocked by this layer, which prevents diffusion into the wet insulator and the silicon substrate. NiB film acts as a very efficient copper diffusion barrier, and a proven surface for subsequent Cu deposition.

Porosity of the barrier has been checked using a method based on the chemical attack of SiO₂ by Hydrofluoric Acid (HF) solutions. The stack PE-CVD SiO₂ / NiB barrier (200nm / 50nm) has been deposited on top of a Silicon substrate, the whole stack being dipped into HF 1% during 5 minutes. After this chemical treatment, if some porosity is present into the NiB barrier, than HF is going to diffuse in it, and attack the underlying layer SiO₂. Fig. 16 demonstrates that no attack of the underlying layer SiO₂ is observed after dipping in HF, and therefore NiB barrier is not porous.

2.2.3 Properties of Cu seed layer

A bath containing specific organics and copper is employed to deposit a Cu seed layer on NiB barrier by means of the same electrografting technique. The electrografted copper seed is also directly applicable to various dry-deposited diffusion barriers, without any adhesion promoter in between. Table 2 summarizes the dry diffusion barriers that have been successfully tested with the eG Cu seed layer technology. No instance of incompatibility between a diffusion barrier and eG Cu seed has been reported so far.

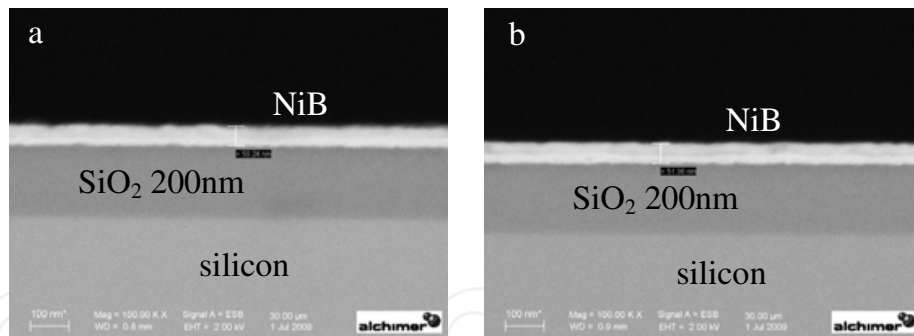


Fig. 16. Demonstration of the non porosity of NiB barrier by dipping the stack SiO₂ / NiB in HF 1%; (a) before HF dip and (b) after HF dip.

	Ta	TaN	Ti	TiN	TiW
ALD				Yes	
CVD				Yes	
PVD	Yes	Yes	Yes	Yes	Yes

Table 2. Compatibility of dry diffusion barriers with electrografting technology.

An example of electrografted copper seed deposited in 5µm x 50µm (AR 10:1) TSVs coated with CVD TiN is presented in fig. 17. Step coverage (step coverage is defined by the ratio between thickness deposited on top vs. bottom of the vias) of eG copper seed deposited inside those TSVs is close to 90%.

Copper grain size of eG copper seed deposited on top of dry barriers had been previously characterized in (Raynal et al., 2009). These measurements were re-visited in the case of eG copper seed deposited on top of cG barrier, with similar results obtained by XRD, EBSD and self anneal rate. One example of EBSD measurement is shown in fig. 18.

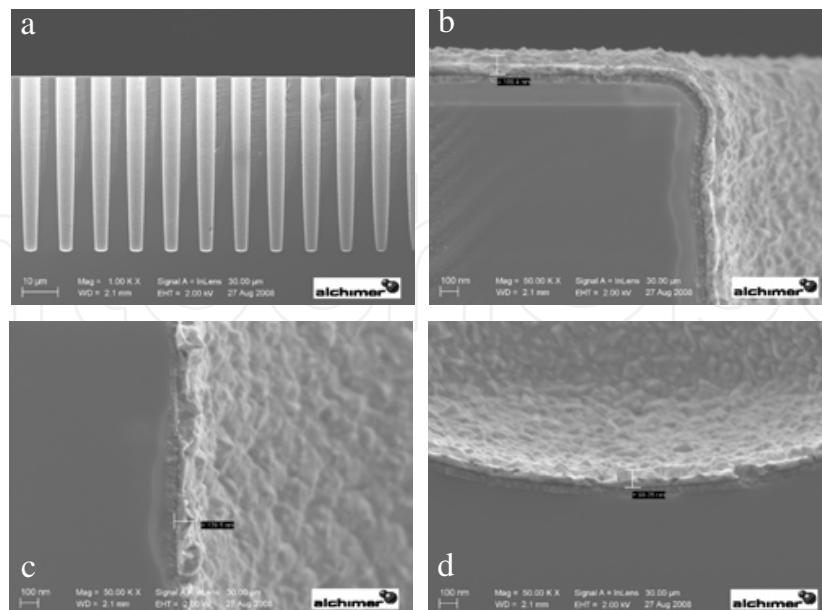


Fig. 17. SEM cross sections of eG copper seed deposited in 5µm x 50µm (AR 10:1) TSVs coated with CVD TiN: (a) overview; (b) via top (109nm of eG copper); (c) sidewalls (129nm of eG copper); (d) via bottom (98nm of eG copper).

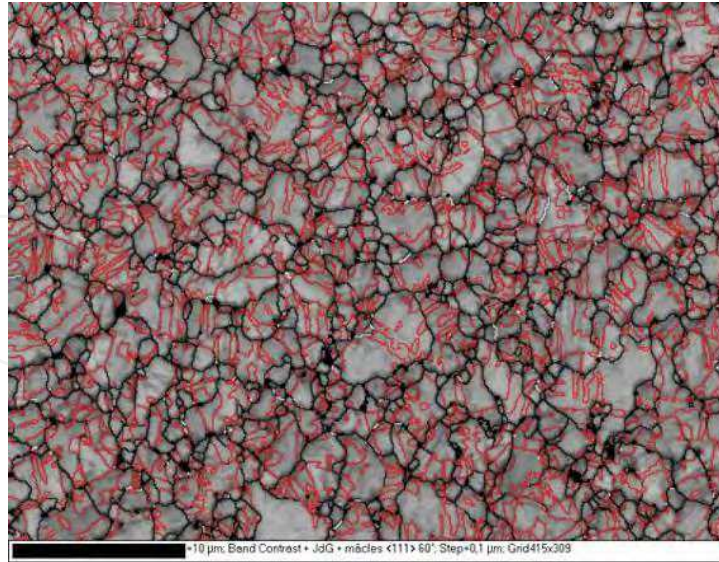


Fig. 18. EBSD picture of eG copper seed layer deposited on top of NiB barrier.

Several studies of PVD copper microstructure have been performed in the past, especially when PVD Cu is deposited on top of PVD Ta. In this case, a strong (111) texture of the copper is reported in the literature, linked to the heteroepitaxial growth of Cu on (002) orientation of Ta. This heteroepitaxial relationship is observed between Cu and Ta, but not with TiN barriers (Wong et al., 1998).

Copper microstructure has been compared between PVD copper deposited on top of TiN barrier and eG copper seed deposited on top of NiB barrier. In both cases, weak (111) orientation of the copper layer is measured.

A summary of eG copper resistivity evolution vs. layer thickness is presented in fig 19. The trend reported in fig. 19 is similar to PVD copper layers (Barnat & Lu, 2001), copper resistivity below 100nm thick being impacted by grain boundary and surface scattering.

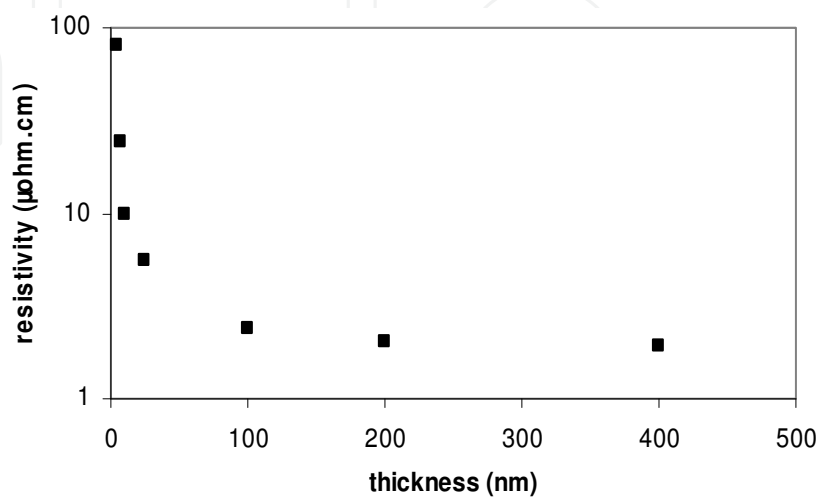


Fig. 19. eG copper resistivity vs. layer thickness.

Thermal treatments need to be done to decrease copper layer resistivity and to reach the value of $1.8\mu\Omega\cdot\text{cm}$ for layers thicker than 100nm. This phenomenon is related to grain size growth during annealing, which can be observed by XRD or EBSD analysis techniques.

Successful Cu gap fillings have been demonstrated, starting from eG copper seed, in a wide range of TSV dimensions. Those results have been achieved with conventional acidic plating chemistries. SEM cross-sections presented in fig. 20 show some examples of void-free gap fillings, starting from eG copper layers with a step coverage between 60% and 90%, in the case of both $20\mu\text{m} \times 75\mu\text{m}$ and $50\mu\text{m} \times 100\mu\text{m}$ TSVs.

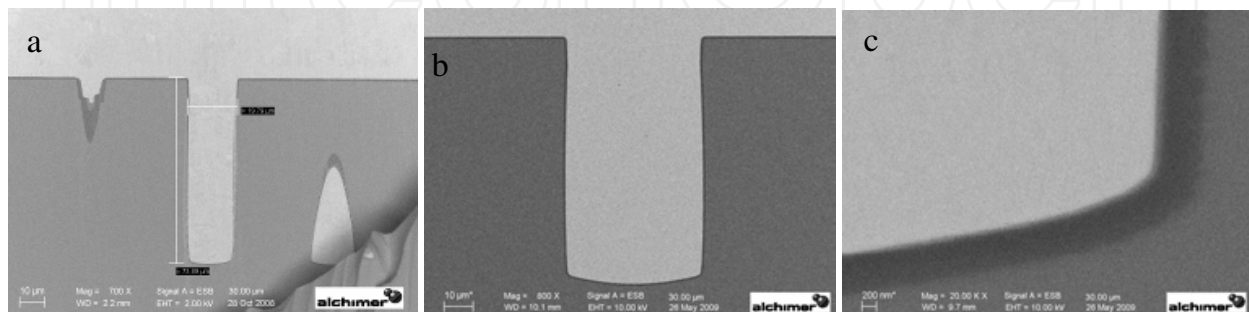


Fig. 20. SEM cross sections of TSVs filled with conventional acidic plating solutions, starting from eG copper seed: (a) $20\mu\text{m} \times 75\mu\text{m}$ TSVs; (b) $50\mu\text{m} \times 100\mu\text{m}$ TSVs; (c) via bottom zoomed $50\mu\text{m} \times 100\mu\text{m}$ TSVs.

2.2.4 Properties of the new TSV-grade Cu fill chemistry

This new TSV-grade chemistry is dedicated to the copper filling of TSV structures. It is less aggressive than conventional acidic chemistries, involving no degradation of the underlying layer, and less sensitive to the ohmic drop, which allows to fill directly on top of the NiB barrier. Its formulation is simpler, which involves a better process control, and a lower contamination of the copper deposited.

Contamination in the copper bulk has been compared by TOF-SIMS depth profiles, between this new TSV-grade chemistry (New fill) and a conventional acidic plating chemistry for TSV applications (Baseline). TOF-SIMS depth profiles are presented in fig. 21, x axis being representative of sample depth and y axis being proportional to compound quantity. Fig. 21 shows an order-of-magnitude reduction in carbon contamination and a two orders-of-magnitude reduction in chlorine contamination for the new TSV-grade copper fill compared to conventional plating chemistries. Those trends remain similar before and after copper anneal to 250°C under forming gas.

Copper grain size has been compared between new TSV-grade and conventional plating chemistries for copper $1\mu\text{m}$ thick (fig. 22), using EBSD analysis technique. Grain size is higher in the case of new TSV-grade chemistry, and more uniform compared to conventional acidic plating. Stress observed by EBSD in grain boundary mode (fig. 22e & 22f) is lower with the new TSV-grade Cu fill (stress being proportional to red lines density).

Cristalline orientation is also extracted from EBSD analysis. As observed in fig. 23, copper deposited with the new fill chemistry is more (111) oriented than baseline chemistry.

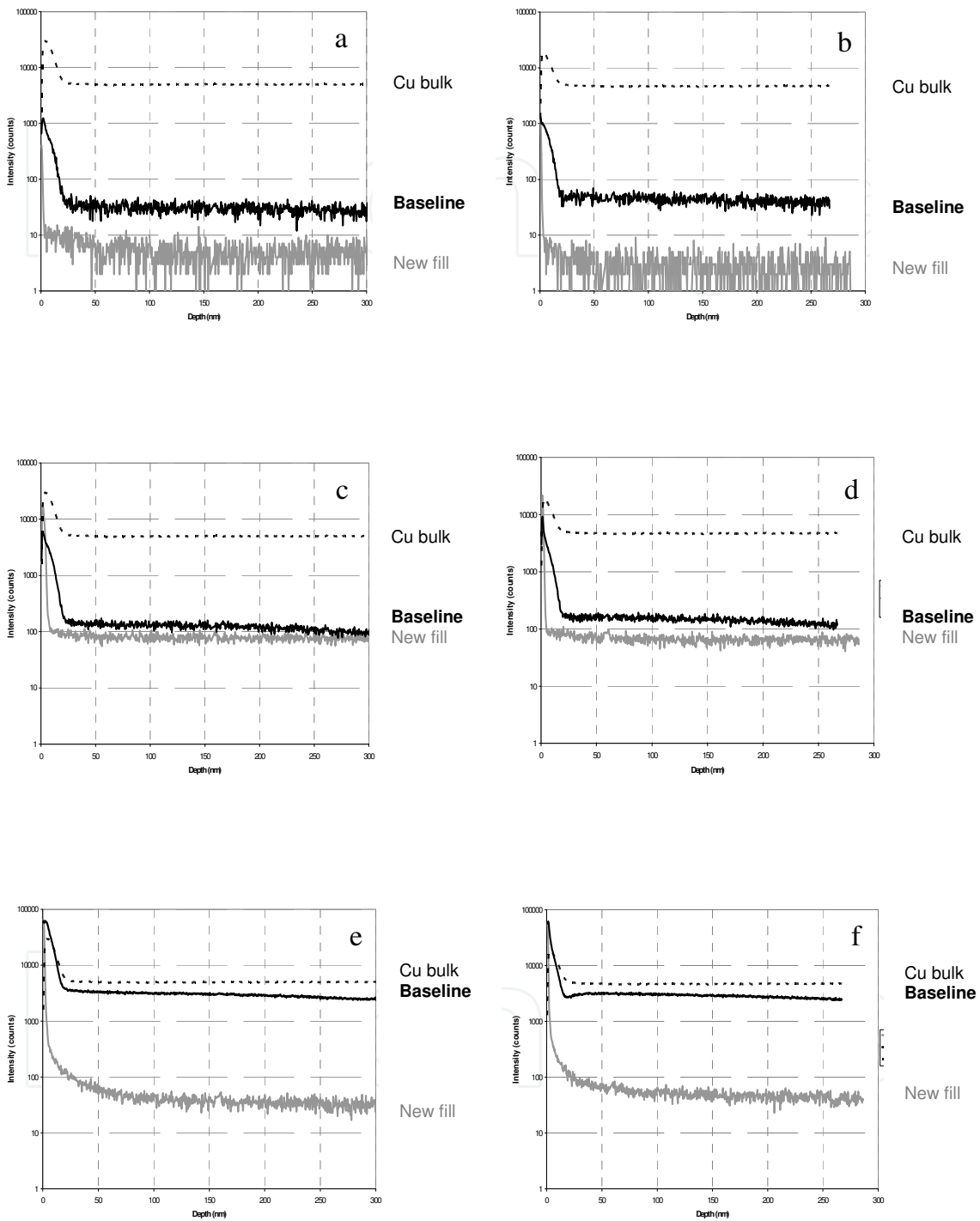


Fig. 21. TOF-SIMS depth profiles of conventional acidic plating (Baseline) vs. new TSV-grade Cu fill (New fill) chemistry: (a) Carbon as deposited; (b) Carbon after anneal 250°C; (c) Sulfur as deposited; (d) Sulfur after anneal 250°C; (e) Chlorine as deposited; (f) Chlorine after anneal 250°C.

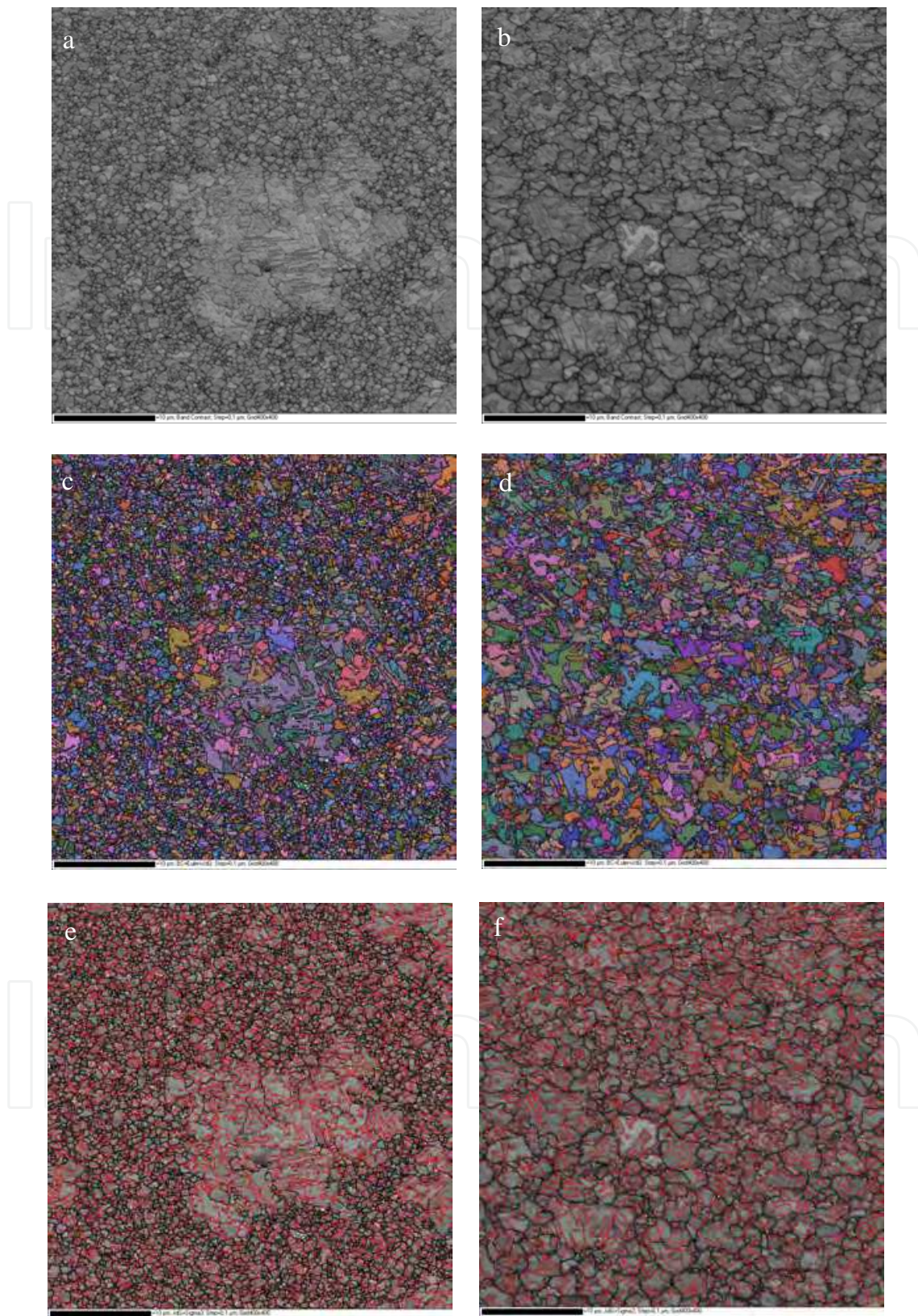


Fig. 22. EBSD top views of (a) conventional plating and (b) new TSV-grade Cu fill in Band Contrast mode; (c) conventional plating and (d) new TSV-grade Cu fill in Euler Angle mode; (e) conventional plating and (f) new TSV-grade Cu fill in Grain Boundary mode.

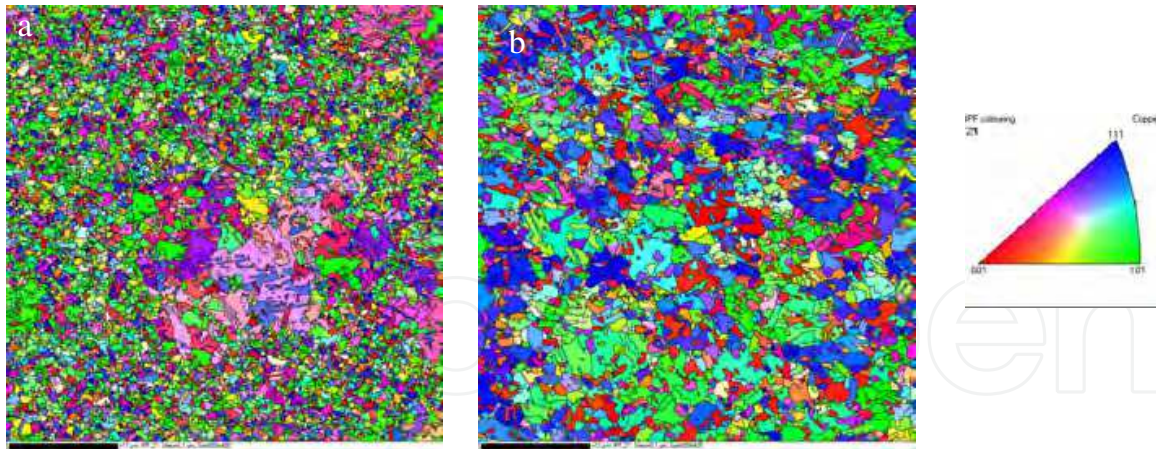


Fig. 23. EBSD top views of (a) baseline plating and (b) new TSV-grade Cu fill in grain orientation mode.

2.3 Wet process TSV - Reliability

2.3.1 Thermo-mechanical considerations of the stack

As reported in table 1, Young modulus (elasticity module) of the wet insulator is measured below 5GPa, which is much lower than the value obtained with SiO₂ (107 GPa, see table 1). This low value of Young modulus represents an obvious advantage in the use of electrografted layers, related to the mechanical properties of the metallized via. Indeed, thermally-induced stress in bulk silicon is proportional to the square of TSV radius and elasticity module (Lu et al., 2010). Silicon stress is reduced by 30x (97%) when used with the wet insulator. This comes on top of the via size reduction induced by smaller radius, as enabled by electrografting (see 2.4 section).

2.3.2 Reliability tests

Specific test vehicles, with typical TSV design rules, were used to assess the reliability of an integrated stack of electrografting and chemical grafting layers filled with the new TSV-grade Cu fill chemistry. Those tests included temperature cycling (1000 cycles from -55°C to 125°C), moisture sensitivity levels, high-temperature storage, thermal shock, and solder heat resistance (Truzzi, 2010). All samples passed the reliability tests. Fig. 24 shows a SEM cross-section and top view of filled structures after 1000 thermal cycles. Table 3 presents an overview of thermal cycles performed with various stacks.

Additionally, electrografting layers have been integrated into test vehicles and exposed to autoclave (AC) and high-temperature storage (HTS) reliability testing. The autoclave test was conducted for 96 hours at 121°C, 100% relative humidity and 2 bar absolute pressure. High-temperature storage was performed for 20 hours at 205°C. Both tests showed positive results with no significant difference in film performance before and after the tests (Reed et al., 2010).

2.4 Design considerations

For a given TSV depth, this nanotechnology approach allows to manufacture smaller vias, thereby unlocking the possibility to design small, fine-pitch TSVs for demanding via-middle applications such as memory-on-logic for mobile computing. From the signal integrity

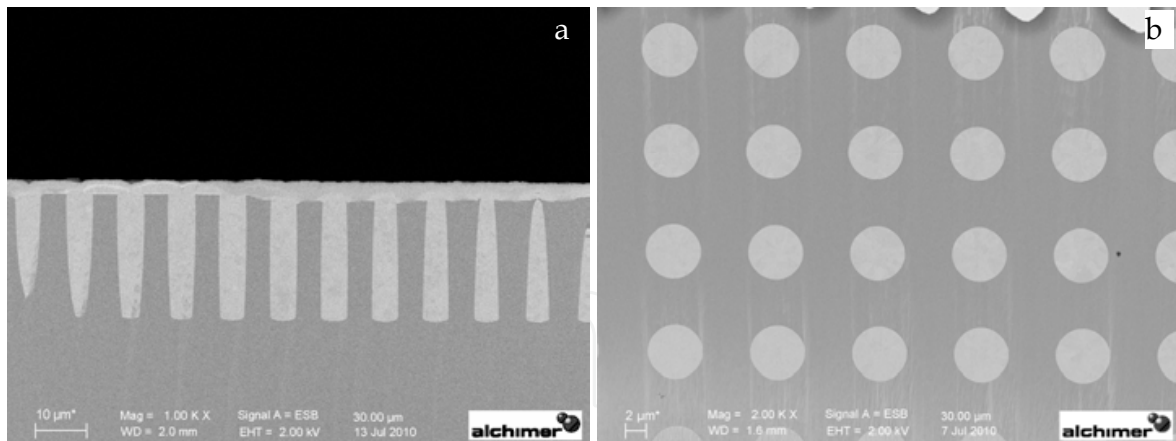


Fig. 24. $5\mu\text{m} \times 25\mu\text{m}$ TSVs coated with wet insulator and NiB barrier, filled with the new TSV-grade Cu fill, and exposed to 1000 thermal cycles from -55°C to 125°C : (a) SEM cross-section and (b) SEM top view after copper polishing.

Via size	Insulator	Barrier	Copper seed	Fill	Conditions	Result
50x100 μm	Dry SiO ₂	Dry TiN	eG Cu seed	Acidic plating	10 cycles from 30°C to 300°C. Ramp up 54°C/min → plateau 300°C 5min → ramp down 33°C/min → plateau 30°C 5min	PASS
50x100 μm	Dry SiO ₂	Dry TiN	eG Cu seed	Acidic plating	1000 cycles from -55°C to 125°C . Ramp up 36°C/min → plateau 125°C 15min → ramp down 36°C/min → plateau -55°C 5min	PASS
5x25 μm	Dry SiO ₂	Dry TaN/Ta	eG Cu seed	Acidic plating	1000 cycles from -55°C to 125°C . Ramp up 36°C/min → plateau 125°C 15min → ramp down 36°C/min → plateau -55°C 5min	PASS
5x25 μm	eG wet insulator	cG NiB	-	New TSV-grade	1000 cycles from -55°C to 125°C . Ramp up 36°C/min → plateau 125°C 15min → ramp down 36°C/min → plateau -55°C 5min	PASS
7x25 μm	eG wet insulator	cG NiB	-	New TSV-grade	1000 cycles from -55°C to 125°C . Ramp up 36°C/min → plateau 125°C 15min → ramp down 36°C/min → plateau -55°C 5min	PASS
10x30 μm	eG wet insulator	cG NiB	-	New TSV-grade	1000 cycles from -55°C to 125°C . Ramp up 36°C/min → plateau 125°C 15min → ramp down 36°C/min → plateau -55°C 5min	PASS

Table 3. Overview of thermal cycles performed with various stacks.

standpoint, as shown in (Truzzi & Lerner, 2009), HAR TSVs with a diameter ranging from 1 to $5\mu\text{m}$ and a depth ranging from 25 to 100 μm show smaller self-capacitance and less cross-talk than larger TSVs with similar depth (Weerasekera, 2008). Fig. 25 shows how one single large TSV exhibits a worse transmission behavior than nine small properly positioned TSVs, with ground vias correctly shielding signal lines. As for the impact of TSVs on Si real estate, the area needed for vias decreases exponentially with decreasing diameter (fig. 26). In order to illustrate this point, we can consider the assumptions listed in table 4.

Fig. 26 shows an exponential dependency of Si cost on via diameter for constant depth value: savings grow exponentially with increasing aspect ratio. In other words, a technology enabling a 3X improvement in aspect ratio allows a 8X increase in the number of TSVs per given area.

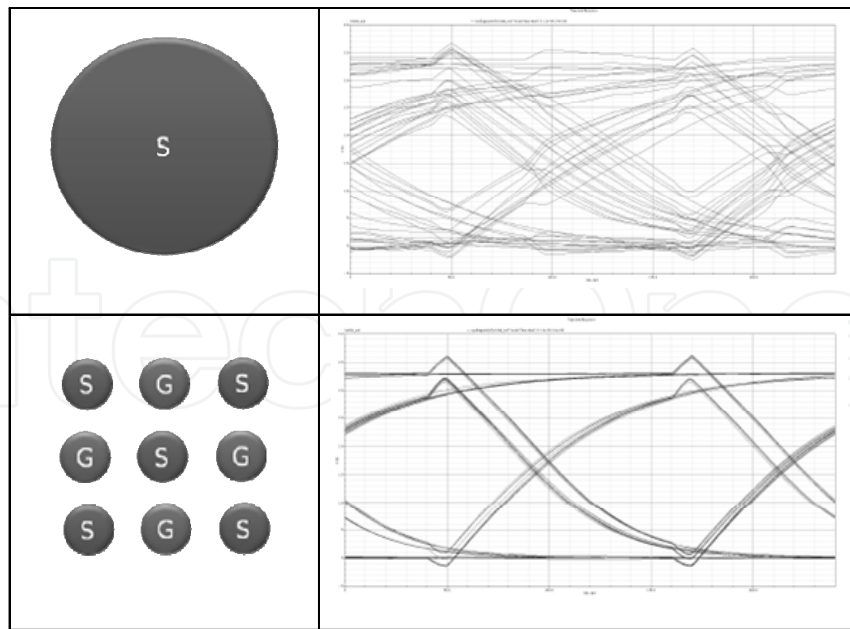


Fig. 25. Eye diagram comparison between one large single TSV and nine small, correctly designed vias.

Die	10 x 10	Mm
die area	100	mm ²
# TSVs	10000	
TSV density	100	TSV/mm ²
TSV depth	50	μm
Keep out area	2.5X diameter	

Table 4. Si area penalty model.

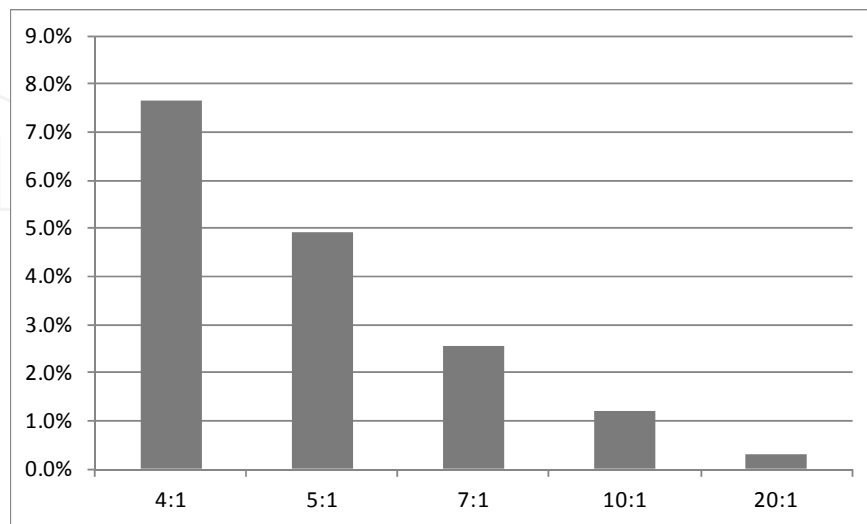


Fig. 26. Si area penalty for TSVs as a function of aspect-ratio, keeping a constant depth value of 50μm.

2.5 Bath analysis and manufacturing

The electrografting nanotechnology described in this paper is ready to be used in a production environment. The electrochemical baths are highly stable, shelf life of all the chemistries being more than 3 months.

After preparation of the chemical baths, monitoring and replenishment of the solutions can be easily carried out using conventional analytical methods, such as pH measurement or UV-visible spectrophotometry. Table 5 summarizes analytical methods available for each bath.

Fig. 27 presents the characterization of the eG copper seed solution during a marathon performed with 900 8inch wafers, using a replenishment of 1ml/h. Process performance (adhesion, copper resistivity, step coverage in TSVs, uniformity within wafer ...) remained stable during the entire marathon.

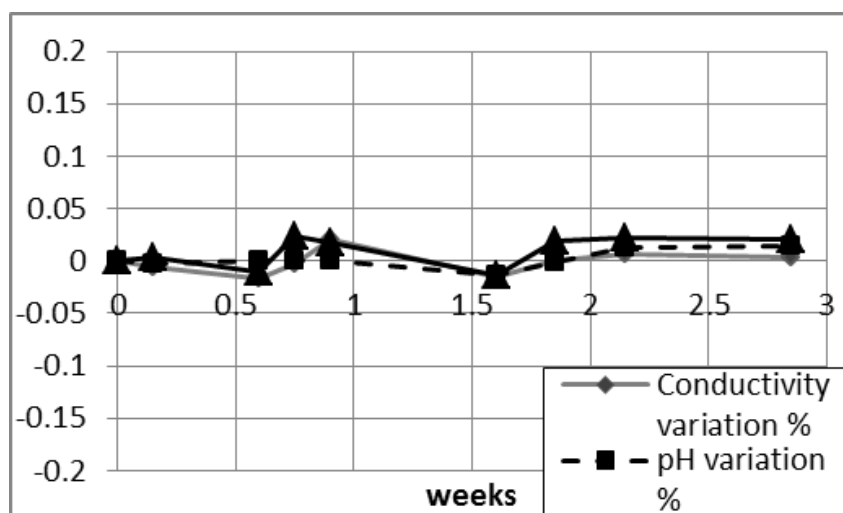


Fig. 27. eG Cu seed bath evolution during a marathon performed with 900 8inch wafers.

	UV-visible	Titration	pH	CVS
Wet insulator	■			
NiB barrier	■	■	■	
eG Cu seed	■	■	■	
New TSV-grade Cu fill	■	■	■	■

Table 5. Analytical methods required for each wet process TSV bath.

3. Conclusion

Electrografting nanotechnology has been optimized for highly conformal growth of TSV films. Complete metallization of high aspect ratio vias is available with this technique, from insulation (by electrografted wet insulator) to copper gap filling using a new TSV-grade Cu fill chemistry.

This technology is fully compatible with standard semiconductor plating tools, enabling a large reduction in cost-of-ownership per wafer compared to dry process approaches (Lerner, 2008), while also providing stable and well-monitored chemical baths.

Film properties meet or exceed current TSV requirements, and chemical formulations are production-ready. TSVs manufactured using electrografting can be very narrow and have aspect ratios up to 20:1, thus broadening the 3D-IC design space and offering a process solution that can be extended for at least several generations into the future.

4. Acknowledgment

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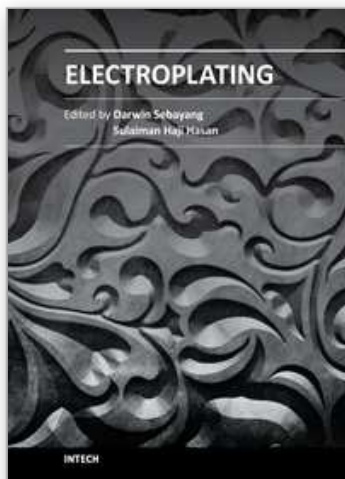
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