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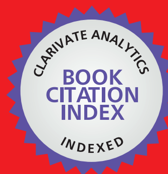


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# Nanowires: Promising Candidates for Electrostatic Control in Future Nanoelectronic Devices

Dura Julien[1,2], Martinie Sébastien[2], Munteanu Daniela[2], Triozon François[1], Barraud Sylvain[1], Niquet Yann-Michel[3] and Autran Jean-Luc[2]

*[1]CEA-LETI MINATEC and [3]CEA-UJF, Institute for Nanosciences and Cryogenics (INAC), Grenoble, [2]IM2NP-CNRS, UMR CNRS 6242, Marseille, [1,2,3]France*

## 1. Introduction

The microelectronics activity regroups the study, design, and manufacturing of very small electronic components. These devices are essentially based on interconnected transistors, sort of "switches" which allow controlling the electric current, and are made of semiconductor materials. Depending on the voltage applied to its "gate" electrode, a transistor is in ON state (high current) or OFF state (smallest possible current and low power consumption). Since the invention of the first transistor in 1948, technological progress allowed miniaturizing drastically electronic circuits, and the industry grew fast up to now. For example, the first microprocessor of INTEL (the "4004") contained 2300 transistors while the Pentium 4 in the early 2000's got 55 millions of transistors and the dual core more than 150 millions. To have a clear idea on the fast growing of this industry, in the 60's and 70's, the number of transistors in integrated circuits was doubled every year. Since the 80's, the standard rule is a factor 2 every 18 months. This evolution is more known as the "Moore's law". Of course, such an industry implies several companies. Microelectronics is become very competitive in performances as well as for economical aspects. The price of 1 million of transistor was 75000 € in 1973, while it was of 6 cents in 2000 then 0.5 cent in 2005. The common objective in microelectronics is so to go ahead with the improvement of transistor in all aspects (electronic performances and economical).

To follow this endless race, the well-known concept of downscaling is required consisting in continuously shrinking the geometrical dimensions of the transistor. However, for small device length, the electrostatics of the device is affected, which degrades the control of the electric current. So, to keep the performances under control, the device architectures have evolved by, for example, improving the gate (controlling electrode) or using thin-film transistor. This article focuses on MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistor) made on silicon, since it is the technology used since decades for microprocessors. The main part of the MOSFET is its semiconducting "channel" coupled to conducting "source" and "drain" regions, and surrounded by one or several gate electrodes

which control the current through the channel. The gate is separated from the channel by a thin insulating oxide. Figure 1 shows transmission electron microscopy (TEM) images of several MOSFET architectures (a) and schematics of these devices and of their potential for channel length reduction (b).

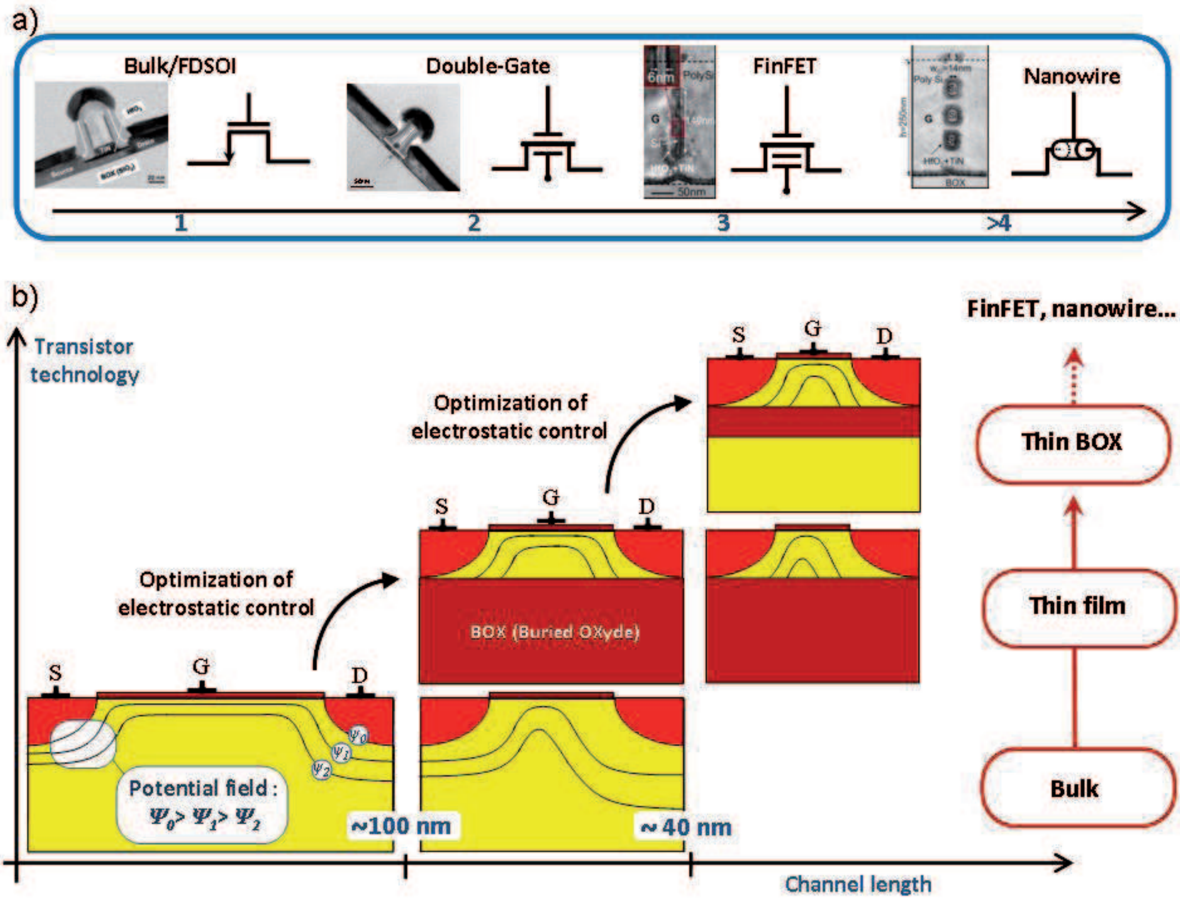


Fig. 1. a) Different MOSFET architectures observed by TEM (Fully-Depleted Silicon on Insulator FDSOI (Barral & al., 2007a), Double Gate (Barral & al., 2007b), finFET (Dupre & al., 2008) and stacked nanowires (Dupre & al., 2008)); b) schematics of the downscaling concept.

The essential parameter used to analyse the electrostatic behaviour (so to compare MOSFET architectures) is the natural length λ (Collinge, 2007). It represents the perturbation induced by the transistor source and drain junctions on the gate control. Numerical simulations establish that a device is relatively free of electrostatic perturbations if λ has a value smaller than 5–10 times the gate length.

$$\lambda = \sqrt{\frac{\varepsilon_{si}.t_{si}.t_{ox}}{N.\varepsilon_{ox}}} \quad (1)$$

where $\varepsilon_{si}$ and $\varepsilon_{ox}$ are the silicon and oxide permittivity, $t_{si}$ and $t_{ox}$ the silicon and oxide thickness and N represents the number of gates of the architecture. Thus, for a given value of silicon thickness and oxide ($t_{si}$=10 nm and $t_{ox}$=1.5 nm) the corresponding minimum length for the bulk, thin BOX FDSOI, and nanowire are 20 nm, 15 nm and 10 nm respectively. That is why ITRS recommends nanowires for technology node sub-22nm (International

Technology Roadmap of Semiconductor [ITRS], 2009) and regarding the advanced processing technologies, the literature provides a wide range of devices based on nanowires, stacked (Dupre & al., 2008), twin (Hwi Cho & al., 2007) or single Ω-FET nanowires (Tachi & al., 2009). In the following, a complete study of the electrostatics of nanowire MOSFETs is performed including all the ultimate physical phenomena which can occur in future electronic devices.

## 2. The electronic structure of silicon nanowires

Standard silicon layers used in microelectronics are crystallographic. Silicon atoms are disposed in a periodical lattice similar to the diamond structure: each atom is tetrahedrally bonded to its four neighbours (see figure 2). The cubic unit cell parameter $a_0$ equals 5.43 Å, corresponding to an interatomic distance of 2.34 Å. Ideal silicon nanowires are thus periodic along their axis, and the length $L$ of their unit cell depends on the crystallographic orientation:

- $L=a_0$ for <100> oriented nanowires,
- $L=a_0/\sqrt{2}$ for <110> oriented nanowires,
- $L=a_0\sqrt{3}$ for <111> oriented nanowires.

The orientation and diameter of the nanowire determines its electronic structure, from which result its electrical and optical properties. In the following of this work, we will consider cylindrical nanowires oriented along the <100> axis, as the one represented in figure 2.

The electronic structure of bulk silicon is expressed by the dispersion relations $E_n(k)$, which give the energy of an electron wavefunction with wavevector $k$ in band $n$. A schematic of low energy electrons in the conduction band is shown in figure 3. It represents the iso-energy surfaces in the first Brillouin zone (wavevector space). For conduction bands, we can count six energy minima, named the six "Δ valleys" of bulk silicon. Each valley is characterized by an effective mass $m_l$ along its orientation axis and $m_t$ along its transverse directions. The longitudinal mass is $m_l$ equal to $0.919m_0$ and $m_t$ is equal to $0.196m_0$ where $m_0$ is the free electron mass.

In the following, we consider transport along the x-axis. So, projecting bulk valleys on the nanowire axis (x for the transport, y and z for the perpendicular direction), we can define two different valleys of the nanowire characterized by a conduction and a confinement masses. The valleys 1 and 2 of the figure 3 correspond to the longitudinal valley while the valleys 3, 4, 5 and 6 refer to the transverse valley. The table 1 gives the corresponding masses of the two nanowire valleys. The confinement mass of the transverse valleys is approximated by a "cylindrical mass", which preserves cylindrical symmetry in the calculations.

| | Conduction mass | Confinement mass |
|---|---|---|
| Longitudinal valley | $m_l$ | $m_t$ |
| Transverse valley | $m_t$ | $2.m_l.m_t / (m_l + m_t)$ |

Table 1. Definition of the longitudinal and the transverse masses for the <100> oriented nanowire.

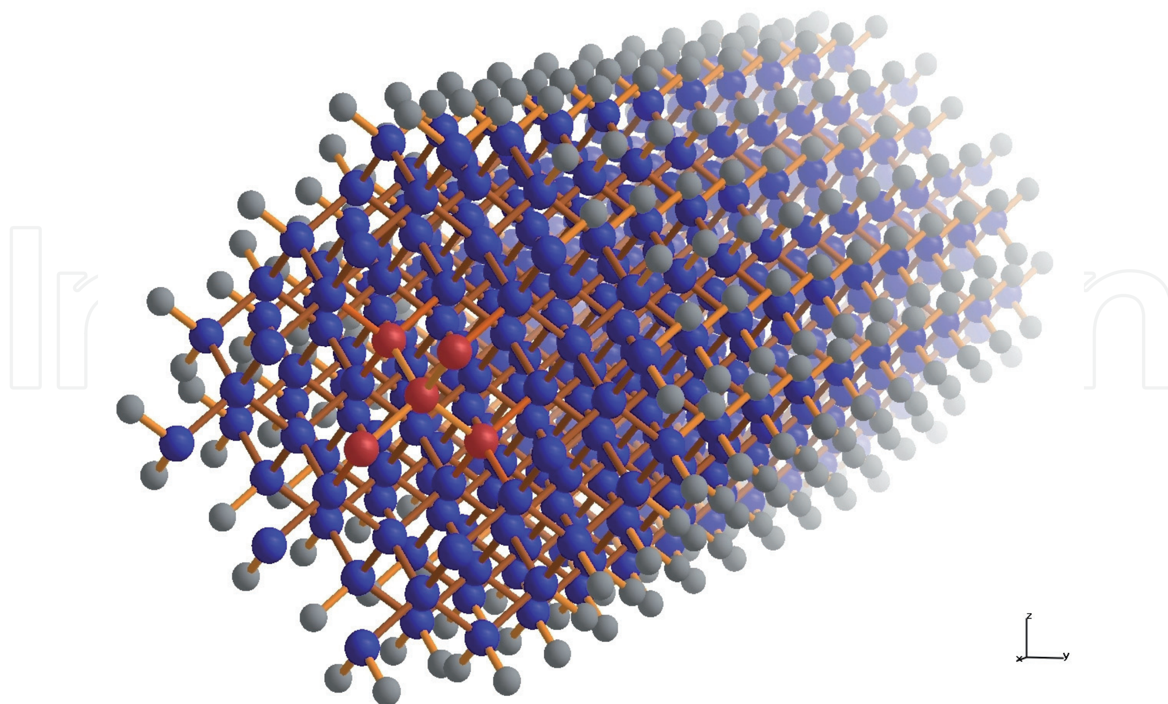

Fig. 2. Atomistic representation of a <100>-oriented nanowire. Blue: silicon atoms, grey: hydrogen atoms (necessary to passivate the surface in the tight-binding model), red: highlight of the tetrahedral structure of silicon. The nanowire is 1.5nm thick and 5nm long.

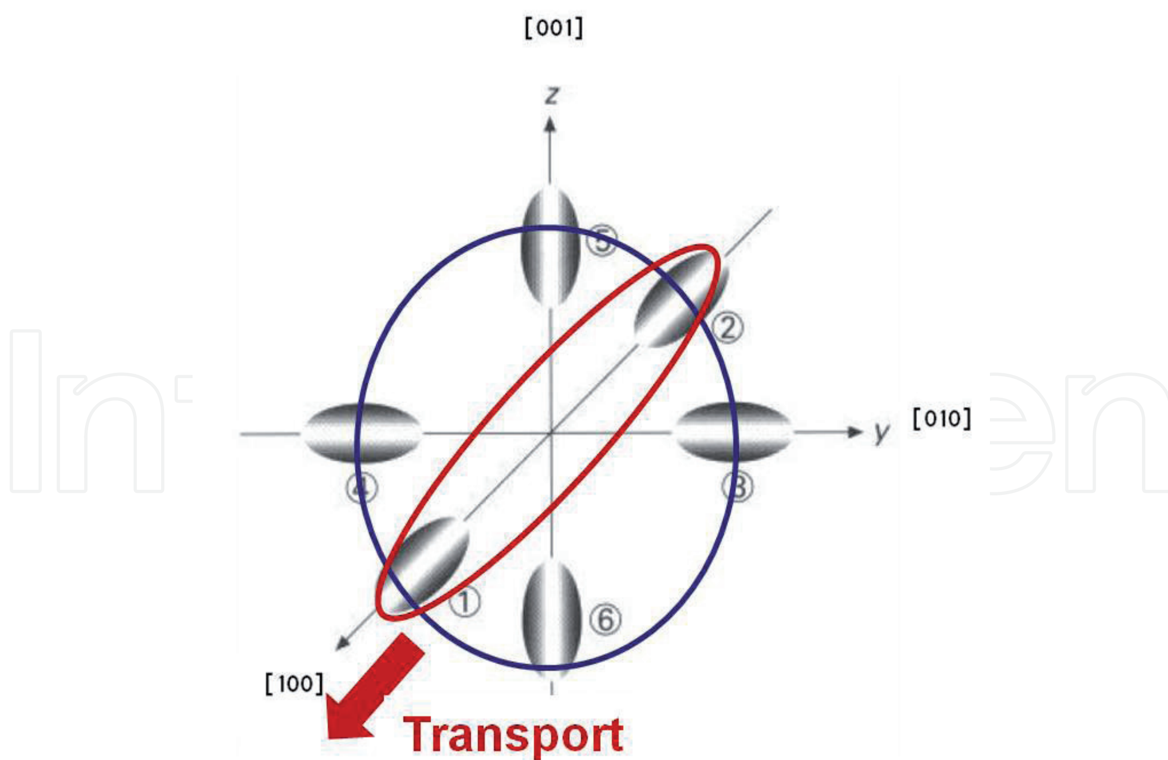


Fig. 3. Iso-energy surfaces of the conduction band of bulk silicon in wavevector space, and definition of longitudinal and transverse valleys for transport along a <100>-oriented nanowire.

This effective mass approach is only valid for thick nanowires (diameter > 5 nm) and low electron energy (a few tenths eV). The band structure of silicon is described more accurately by atomistic models, which allow modelling thinner nanowires. A tight-binding model is used here. It consists in developing the wavefunctions on an atomic orbital basis set. The $sp^3$ model developed by (Niquet & al., 2000) is used here and in previous studies (see section 3.4). This model is fitted on first principles calculations based on the density functional theory (DFT) and so-called "GW" corrections for the bandgap. It contains one *s* orbital and three *p* orbitals per silicon atom and describes accurately electron (conduction band) and hole (valence band) dispersion relations. When studying nanostructures, the surface is passivated with hydrogen atoms (see figure 2). This model choice is due to the lack of a convenient tight-binding model for the $Si/SiO_2$ interface. Passivation avoids unrealistic surface states and should not modify much the electronic structure of the nanowire. The tight-binding calculations are performed with the code TB_Sim (TBSIM, 2011), which solves the Schrödinger equation in nanostructures containing up to $10^7$ atoms (Niquet & al., 2006). For thin nanowires (diameter < 5 nm), the obtained electronic structure differs from the effective mass calculation (see section 3.4). TB_Sim also allows Poisson-Schrödinger calculations, which give the repartition of the charge density in the nanowire under the influence of the gate voltage. Again, corrections of the effective mass approach are needed for thin nanowires.

## 3. Modelling of the electrostatics in MOSFETs based on nanowires

### 3.1 Definition of the threshold voltage

As said previously, the MOSFET transistor is defined by two states (ON or OFF) depending on the voltage applied at the gate. In fact, this polarization creates an electric field in the active region of the transistor which makes carriers concentrate near the interface with the oxide. Increasing the gate voltage, conduction bands start to fill with carriers from lower energy bands to higher energy bands up to saturation. In this regime, the semiconductor is then analog to a metal and forms a conduction layer between contacts (source and drain) of the transistor. Commonly, the threshold voltage is so defined as the frontier of the two states of the transistor and represents its capacity to switch from one state to the other. It is essentially dependent on the electrostatic characteristics. That is why, it is necessary to fully describe the potential $\psi$ everywhere in the device active region. For this purpose, the Poisson equation, given here in cylindrical coordinates, is solved:

$$\frac{d^2\psi}{dr^2}+\frac{1}{r}.\frac{d\psi}{dr}=\frac{q}{\varepsilon_{Si}}(N_A+n) \tag{2}$$

where $N_A$ is the channel doping, n is the electron density, $\varepsilon_{Si}$ the silicon permittivity, and q the elementary charge. Note that *n* depends on $\psi$ via the Fermi-Dirac occupation of electronic states.

Two approaches can be used to obtain the solution of such an equation. The first one is the double integration solving (Jimenez & al., 2004; Yu & al., 2007); however the solution is not totally analytical which is not convenient in our case. The second approach is to make an assumption on the potential description along the nanowire radius. In the following, we assume a parabolic potential along the radius of the nanowire cross-section described as:

$$\psi(r,x) = \beta_1 + \beta_2.r + \beta_3.r^2 \tag{3}$$

where the parabolic terms $\beta_i$ are x-dependent functions.

To define these terms, the general expression of the potential (eq. 3) is injected in boundary conditions specific to nanowires (eq. 4): the potential at the position r=D/2 is equal to the potential at the position r=–D/2 (symmetry condition) and is defined as the surface potential $\psi_s$:

$$\psi(D/2, x) = \psi(-D/2, x) = \psi_s(x) \tag{4}$$

Equation (3) becomes:

$$\psi(r,x) = \psi_s(x) - \beta_3.\frac{D^2}{4} + \beta_3.r^2 \tag{5}$$

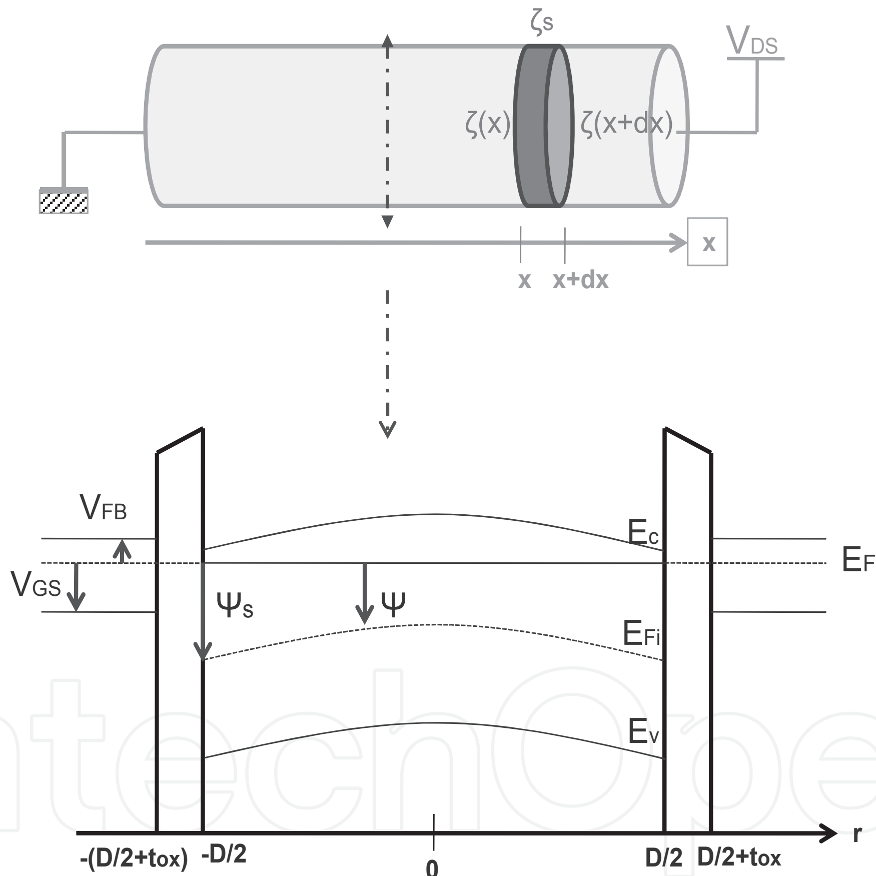


Fig. 4. (a) Schematics of a nanowire device (for a better view the gate oxide and material are not shown), indicating the specific area used in the Gauss law. (b) Band diagram along a vertical cut-line in the nanowire.

The term $\beta_3$ is found by including (5) into the Poisson equation (2) and integrating along the nanowire radius from 0 to D/2:

$$\beta = \beta_3 = \frac{q.N_A}{4\varepsilon_{Si}} + \frac{Q_{i,lin}}{\varepsilon_{Si}.D} \tag{6}$$

where $Q_{i,lin}$ is the charge integrated along the nanowire radius and $\psi_s$ is the surface potential.

It is important to note that the parabolic assumption is valid at threshold, but could lose its validity in other operation regimes (for example in the strong inversion regime). Figure 4(a) shows the schematics of the nanowire with the longitudinal polarization ($V_{DS}$) along the x-axis (transport). Figure 4(b) shows the band diagram along a transverse cutline in the nanowire for an applied gate voltage $V_{GS}$. The potentials are defined with respect to the intrinsic Fermi level as illustrated in figure 4(b).

The starting point of the threshold voltage modelling is the boundary condition at the $Si/SiO_2$ interface:

$$V_{GS} - V_{FB} = \frac{\varepsilon_{Si}}{C_{ox}}.\zeta_S + \psi_S + \phi_F \tag{7}$$

where $V_{FB}$ is the flat-band voltage, $\zeta_S$ is the electric field at the interface, $\phi_F$ is the Fermi potential and $C_{ox}$ is the oxide capacitance in cylindrical coordinates expressed in (Dura & al., 2010).

In our case, we consider the threshold voltage defined as the gate voltage for which the inversion charge reaches its threshold value fixed to (Munteanu & al., 2005):

$$Q_{ith,lin} = \frac{kT}{q}.C_{ox} \tag{8}$$

where $k$ is the Boltzmann constant and $T$ is the temperature. Under this condition, the surface potential reaches its threshold value, called $\psi_{s,th}$. The threshold voltage is then obtained as:

$$V_{th} = V_{FB} + \frac{\varepsilon_{Si}}{C_{ox}}.\beta.D + \psi_{s,th} + \phi_F \tag{9}$$

with

$$\beta = \frac{q.N_A}{4\varepsilon_{Si}} + \frac{kT}{q}\frac{C_{ox}}{\varepsilon_{Si}.D} \tag{10}$$

In equation (9), only the surface potential is unknown and has to be modeled taking into account the physical phenomena specific to nanowire MOSFETs described below: quantum confinement, short channel effect, and band structure effect.

### 3.2 Quantum mechanical confinement (QE)

In silicon nanostructures such as nanowires, the wavefunctions related to the different valleys are modified and kinetic energy is quantized along the confinement directions, leading to a set of energy subbands for each valley. Previous works highlight the necessity to consider quantum confinement in the transport modelling of planar architectures (Munteanu & al., 2005), for which the confinement is one-dimensional. For nanowire

devices, quantum confinement is two-dimensional (leading to a 1D electronic gas) and its impact is expected to be stronger (Autran & al., 2005). Figure 5 shows the wavefunction in the first five subbands for the longitudinal valley and for two different nanowire diameters (5 and 10nm). These wavefunctions are calculated using an effective mass Schrödinger-Poisson solver (TBSIM, 2011). The associated energy represents the difference between each energy subband and the first subband level.

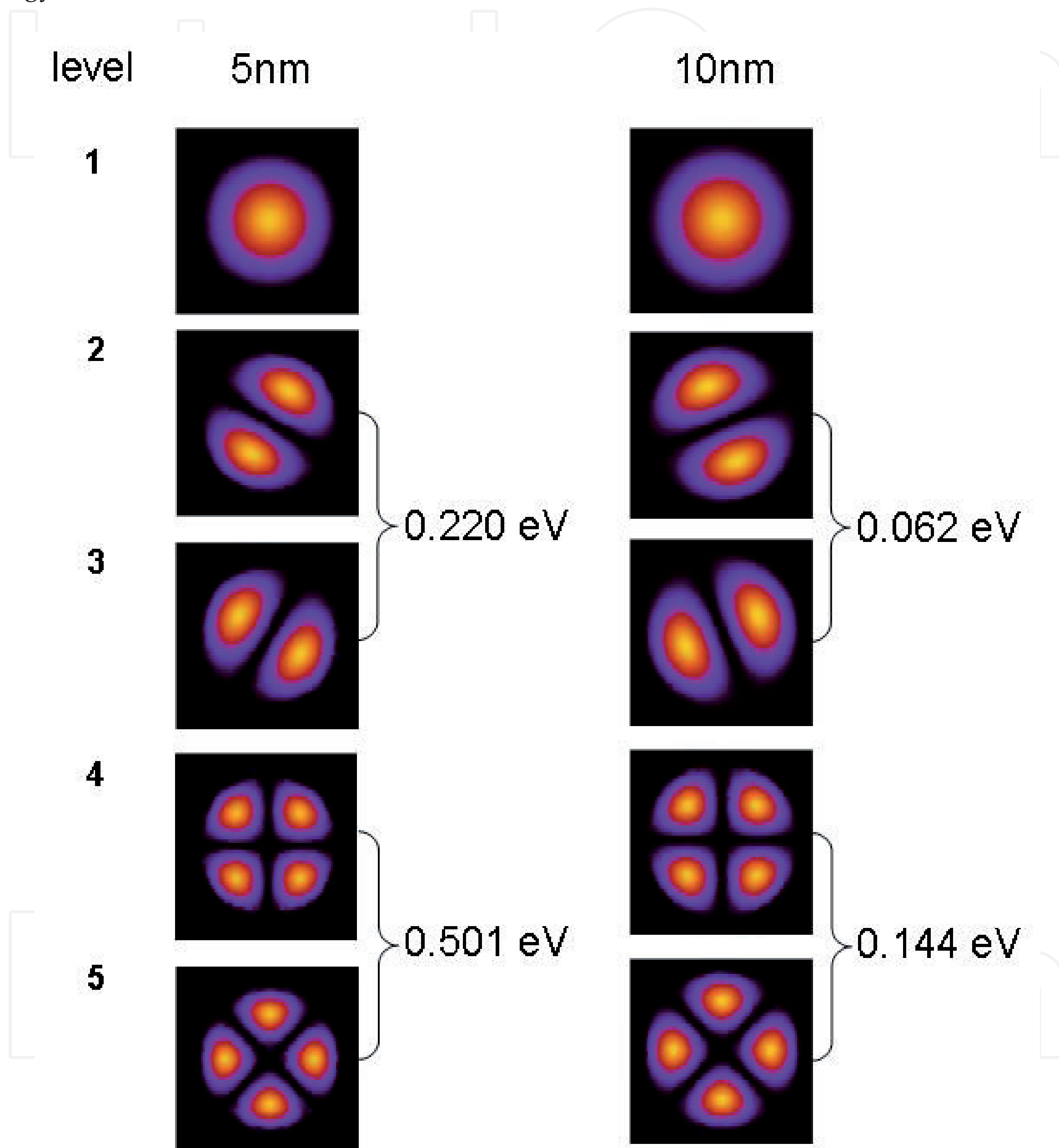


Fig. 5. Square modulus of the wavefunction for the five first levels in the longitudinal valley of a 5 and 10nm nanowire diameter. Energy increase of each subband with respect to the first level.

To extract numerically the impact of the diameter on the quantization of carriers, the same calculation has been done for the tranverse valley and for different nanowire diameters. We can note that for low diameters, the quantized levels are higher. So, regarding the targeted MOSFET downscaling to a few nanometers, quantum-mechanical effects have to be

included in the previous analytical model of threshold voltage in order to assess their impact up to circuit performances.

For this purpose, the 1D quantum charge integrated along the radius $Q_{i,lin}$ has to be used:

$$Q_{i,lin} = \sum_j \sum_i n(E_c, i, j) \tag{11}$$

with

$$n(E_c, i, j) = 2 \int_{E_c}^{+\infty} \rho_{1D}(E, E_c).f(E).dE \tag{12}$$

where the factor 2 accounts for the number of equivalent valleys, *j* is the valley index, *i* is the subband index, $Ec = E^i_j$ is the subband bottom energy, $\rho_{1D}(E,E_c)$ is the 1D density-of-states of the subband, and $f(E)$ is the Fermi-Dirac distribution function:

$$\rho_{1D}(E, E_c) = \frac{1}{\pi}.\left(\frac{2.mj}{\hbar^2}\right)^{1/2}.\frac{1}{\sqrt{E - E_c}} \tag{13}$$

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT}\right)} \tag{14}$$

where $m_j$ is the 1D density-of-states effective mass in valley *j* and $E_F$ is the Fermi level. The general expression of the charge is then:

$$Q_{i,lin} = q \sum_j \sum_i \left(\frac{1}{\pi}.g(j).\sqrt{\frac{2m_j}{\hbar^2}}\right).\sqrt{\frac{kT}{q}}.\int_0^{\infty} \frac{r^{-0.5}}{1 + e^{r - \frac{q}{kT}\left(E^i_j - \frac{Eg}{2} - \psi_S\right)}}.dr \tag{15}$$

Under non-degenerate condition (valid at threshold), the Fermi-Dirac distribution can be approximated by a simple exponential (corresponding to the Boltzmann distribution). The expression of the charge becomes (Autran & al., 2004):

$$Q_{i,lin} \approx Q^*.e^{\frac{q.\psi_S}{kT}} \tag{16}$$

with

$$Q^* = q \sum_j \sum_i \left(\frac{1}{\pi}.g(j).\sqrt{\frac{2m_j}{\hbar^2}}\right).\sqrt{\frac{kT}{q}}.\sqrt{\pi}.e^{-\frac{q}{kT}(E^i_j + \frac{Eg}{2})} \tag{17}$$

where Eg is the silicon bandgap, and g(j) is the degeneracy of the valley j (equal to 2 for each valley). The charge is then obtained by a sum over the different silicon valleys (index j) and a sum over all quantized levels (index i) of each valley (in practice limited to 5). The quantum energy levels are needed in (17) and have to be calculated analytically. For a

cylindrical cross-section of the nanowire, the analytical expressions of the transversal (index t) and longitudinal (index l) quantum energy levels are given by (Baccarani, 2008):

$$\begin{aligned} E_t^i &= E_{1,2}^i = \frac{(\alpha.\hbar.i)^2}{4.q.(D/2)^2}.(\frac{1}{m_t}+\frac{1}{m_l}) \\ E_l^i &= E_3^i = \frac{(\alpha.\hbar.i)^2}{2.q.(D/2)^2}.\frac{1}{m_t} \end{aligned} \quad (18)$$

where α is a numerical parameter (Baccarani, 2008). We can note a good agreement between (18) with α=2.1 and a self-consistent cylindrical 1D Schrödinger-Poisson solver (ATLAS, 2010) for the first energy level (transversal and longitudinal) (Dura & al., 2010).

From equation (16), the surface potential at threshold voltage is given by:

$$\psi_{s,th} = \frac{kT}{q}.\ln(\frac{Q_{ith,lin}}{Q^*}) \quad (19)$$

with $Q_{ith,lin}$ the inversion charge at threshold defined by (8).

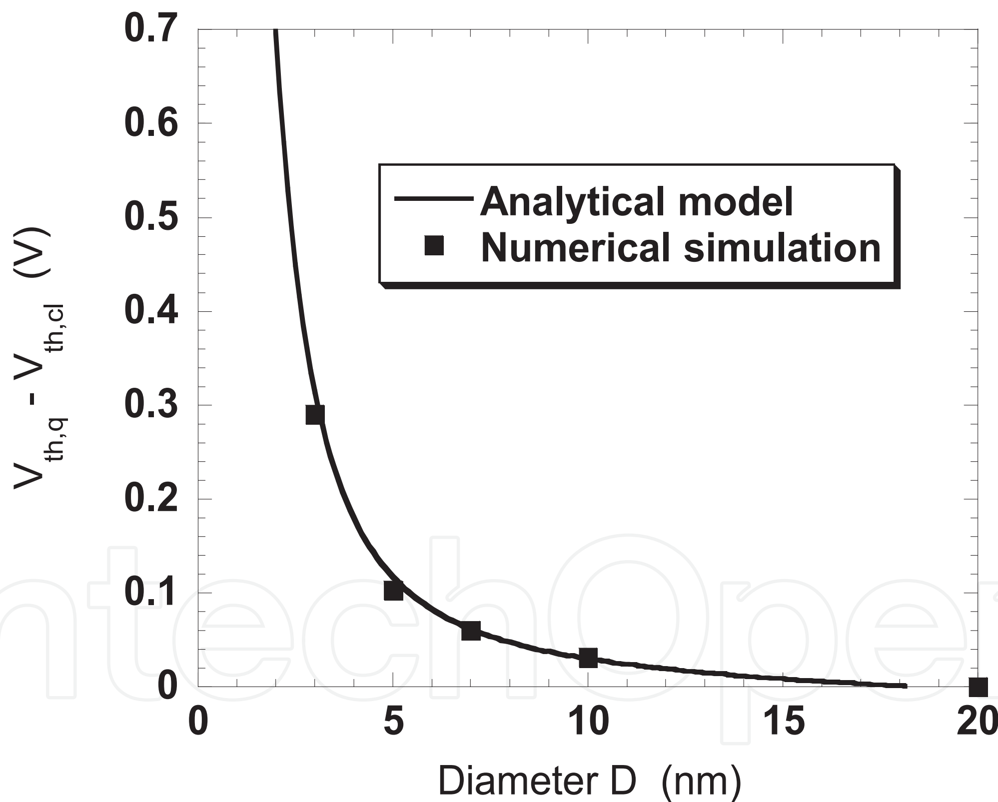


Fig. 6. Threshold voltage shift between quantum (Vth,q) and classical (Vth,cl) approaches versus nanowire diameter in long channel transistors. Comparison between the analytical model and data obtained from Schrödinger-Poisson numerical solving (ATLAS, 2010).

Including this expression in (9), the quantum threshold voltage for long channel transistor is easily obtained. Figure 6 plots the difference between quantum and classical threshold voltage versus the nanowire diameter; as expected, this difference increases when reducing the nanowire diameter, due to a stronger quantization of carrier energy when the nanowire

diameter is reduced. Figure 6 also shows a very good agreement between the analytical model and data obtained by a Schrödinger-Poisson numerical solving (ATLAS, 2010).

### 3.3 Short-Channel Effect (SCE)

As said in the introduction, the downscaling of transistor is required. That is why the gate length is continuously reduced. However, from a certain dimension, the transistor junctions (source and drain) have an impact on the electrostatic control of the device. Previously 1D (only the gate voltage), it becomes 2D because gate and drain polarizations compete to control the device. And this strongly affects the device characteristics. Thus, MOSFET architectures are considered to be impacted by the short channel effect when the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction. The main result is the modification of the threshold voltage (or the loss of electrostatic control) due to the shortening of the channel length. It is attributed to two phenomena: SCE (Short Channel Effect) and DIBL (Drain Induced Barrier Lowering). The first one is coming from the superposition of the depletion-layer widths of the source and drain junction. The second phenomenon is a secondary effect on the charge sharing due to higher drain voltage. Nanowire transistors being expected for ultimate technology node, consideration of short channel effect is required in a realistic modeling of this architecture.

To fully describe 2D electrostatic effects (SCE and DIBL) in short channel devices, we propose a full analytical model describing the threshold voltage impacted by SCE and DIBL. The x-dependence (transport direction) of the surface potential has to be know. Applying the Gauss law on a nanowire slice as illustrated in figure 4(a), the following equation is obtained (Munteanu & al., 2005):

$$-\zeta(x).\pi.\frac{D^2}{4}+\zeta(x+dx).\pi.\frac{D^2}{4}-\zeta_S(x).\pi.D.dx=-\frac{q.N_A.\pi.D^2}{4.\varepsilon_{Si}} \quad (20)$$

where $\zeta$ is the electric field expressed by:

$$\zeta(x)=-\eta.\frac{d\psi_S(x)}{dx} \quad (21)$$

$\eta$ is a fitting parameter which models the lateral electric field variation (Banna & al., 1995). It depends on the channel doping, the channel length, the nanowire diameter and the polarization. An empirical formula for $\eta$, obtained from numerical simulations, will be presented below to include these both effect. Introducing (21) in (20), we find a second order equation for the surface potential:

$$\frac{d^2\psi_s}{dx^2}-4\frac{C_{ox}}{\eta.\varepsilon_{Si}.D}.\psi_s=\frac{2}{\eta.\varepsilon_{Si}.D}[q.N_A.\frac{D}{2}-2C_{ox}(V_{GS}-V_{FB}-\phi_F)] \quad (22)$$

The solution of this equation is given by (Munteanu & al., 2005):

$$\psi_s=K_1.e^{\gamma.x}+K_2.e^{-\gamma.x}-\frac{K_3}{\gamma^2}$$
$$\gamma=\sqrt{\frac{4.C_{ox}}{\eta.\varepsilon_{Si}.D}} \quad (23)$$

where $K_1$, $K_2$ and $K_3$ are functions resulting from the Poisson equation solving:

$$K_1 = \frac{(1 - e^{-\gamma.L_c}).(V_b + K_3/\gamma^2) + V_{DS}}{2.sh(\gamma.L_c)} \quad (24)$$

$$K_2 = -\frac{(1 - e^{+\gamma.L_c}).(V_b + K_3/\gamma^2) + V_{DS}}{2.sh(\gamma.L_c)} \quad (25)$$

$$K_3 = \frac{2}{\eta.\varepsilon_{Si}.D}[q.N_A.\frac{D}{2} - 2C_{ox}(V_{GS} - V_{FB} - \phi_F)] \quad (26)$$

where $V_b$ is the built-in potential depending on the channel doping $N_A$, the source/drain doping $N_{SD}$ and the intrinsic carrier density $n_i$ as:

$$V_b = \frac{kT}{q}.\ln\left(\frac{N_A.N_{SD}}{n_i^2}\right) \quad (27)$$

The position where the surface potential is minimum $x_{min}$ and the value of $\psi_S$ ($\psi_{s,min}$) at the position $x_{min}$ are obtained by forcing the first derivative of equation (23) to be equal to zero (Munteanu & al., 2005):

$$x_{\min} = \frac{1}{2.\gamma}.\ln(\left|\frac{K_2}{K_1}\right|) \quad (28)$$

$$\psi_s = \psi_{s,\min} = 2\sqrt{K_1.K_2} - K_3/\gamma^2 \quad (29)$$

We assume that the transistor switches on when $\psi_{s,min} = \psi_{s,th}$. By inserting this expression in the general expression of the threshold voltage (9), we obtain:

$$V_{th} = V_{FB} + \frac{\varepsilon_{Si}}{C_{ox}}.\beta.D + \phi_F - K_3/\gamma^2 + 2\sqrt{K_1.K_2} \quad (30)$$

We can, by analogy to (Suzuki & al., 1996), distinguish two different terms. The first one (independent from the channel length) refers to the long-channel threshold voltage $V_{th,long}$; the second term, which tends to zero for long channel length, represents the threshold voltage roll-off and describes the impact of SCE/DIBL:

$$V_{th,long} = V_{FB} + \frac{\varepsilon_{Si}}{C_{ox}}.\beta.D + \phi_F - K_3/\gamma^2 \quad (31)$$

$$\Delta V_{th} = -2\sqrt{K_1.K_2} \quad (32)$$

where the variation of the threshold voltage is defined as:

$$\Delta V_{th} = V_{th} - V_{th,long} \tag{33}$$

At threshold, $V_{GS}=V_{th}$ in (26) and, considering (33), $K_3$ will depend on $\Delta V_{th}$. Moreover $K_1$ and $K_2$ depend on $K_3$, they will also depend on $\Delta V_{th}$. Then, developing (33) leads to a second order equation of $\Delta V_{th}$ as:

$$A.\Delta V_{th}^2 + B.\Delta V_{th} + C = 0 \tag{34}$$

with

$$\begin{cases} A = sh(\gamma.L_C)^2 + 2.[1 - ch(\gamma.L_C)] \\ B = 2.[1 - ch(\gamma.L_C)].[2.H_4 + V_{DS}] \\ C = 2.H_4.[1 - ch(\gamma.L_C)].[H_4 + V_{DS}] + V_{DS}^2 \\ D = V_b - V_{th,long} + V_{FB} + \phi_F \end{cases} \tag{35}$$

Finally, the threshold voltage roll-off is the solution of (34) given by:

$$\Delta V_{th} = \frac{-B + \sqrt{B^2 - 4.A.C}}{2.A} \tag{36}$$

We can note that to find this term, we have to take into account the long-channel threshold voltage (see coefficient D in eq.35) which includes the dependence on the quantum confinement. Consequently, this model includes both the impact of quantum confinement on the long channel and the threshold voltage roll-off. The most common model (such as references (Banna & al., 1995; Suzuki & al., 1996)) does not include the effect of quantum confinement on the evolution of the short channel effect in analytical modeling which becomes dominant in nanoscale device such as nanowire (this aspect will be detailed later in paragraph 4).

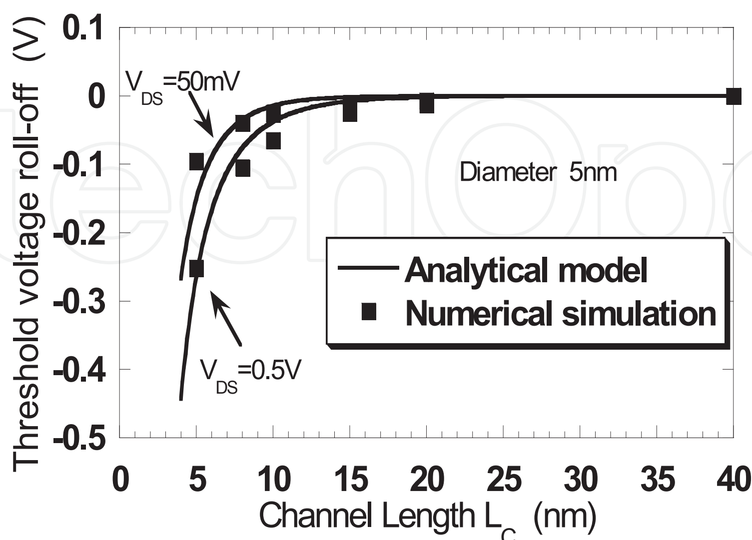


Fig. 7. Threshold voltage roll-off versus channel length for low ($V_{DS}$=50mV) and high (0.7V) drain voltage obtained by the analytical model and TCAD simulations for a 5 nm nanowire diameter; $t_{ox}$=1 nm.

The threshold voltage roll-off is represented in figure 7 for nanowire diameters of 5 nm (calculated in the classical case, i.e. without quantum confinement). TCAD numerical simulations have been done for a cylindrical structure using a drift-diffusion model in order to obtain drain current characteristics as a function of the gate voltage. The threshold voltage is extracted from these current-voltage characteristics using the classical constant current method. The threshold voltage data extracted from TCAD simulations for different diameters have been used to derive an empirical expression of the parameter $\eta$ including the dependence on the channel length, nanowire diameter and drain to source voltage:

$$\eta = \frac{D}{f_0 + D} + V_{DS} \cdot \left[ f_1 . L_C + f_2 . L_C{}^2 \right] \tag{37}$$

where $f_0$, $f_1$ and $f_2$ are constant fitting parameters, calibrated on numerical simulations. Equation (37) is valid for a wide range of nanowire diameter (down to 2 nm) and channel lengths (down to channel length equal to the nanowire diameter). The results in figure 7 show a good agreement between the analytical model and threshold voltage data obtained from TCAD simulations.

### 3.4 Band Structure Effect (BSE)

Advanced atomistic numerical simulations (Neophytou & al., 2008; Niquet & al., 2000, 2006; Sarrazin & al., 2009; Nehari & al., 2006) have shown that a strong reduction of the silicon thickness impacts the material properties by modifying the band structure. Indeed, the dimensions targeted in ultra-scaled devices are those of a few tens atomic layers (several nanometers). At these dimensions, the electronic properties differ from the calculations shown in section 3.2 and based on the bulk effective masses. In (Sarrazin & al., 2009), atomistic tight-binding (TB) Schrödinger-Poisson simulations have been performed for the case of [001] oriented silicon nanowire in order to highlight the variation of the band structure with the nanowire diameter. The code TB_Sim (TBSIM, 2011) has been used with a $sp^3$ tight-binding model (Niquet & al., 2000). Figure 8 shows the valence and the conduction bands for Si nanowire width of 2nm and 10nm. We can note that when thinning the silicon film the minimum of the conduction band is increased and the general shape of bands becomes smoother (Sarrazin & al., 2009). However, the bandgap increase is smaller than the effective mass result of section 2.4.

In order to include these modifications in the previous threshold voltage modelling, analytical expressions of parameters affected by the band structure effect (band gap and effective masses) are proposed here. Diameter-dependent analytical functions (fitted on numerical simulations as illustrated in figure 9) are found for the bandgap and effective masses (inspired from (Niquet & al., 2000):

$$E_g = E_{g,bulk} + \frac{K_1}{D^2 + A_1 . D + B_1} \tag{37}$$

$$m_{t(l)} = m_{t(l),bulk} + \frac{K_2}{D^2 + A_2 . D + B_2} \tag{38}$$

where A, B and K are fitting constants.

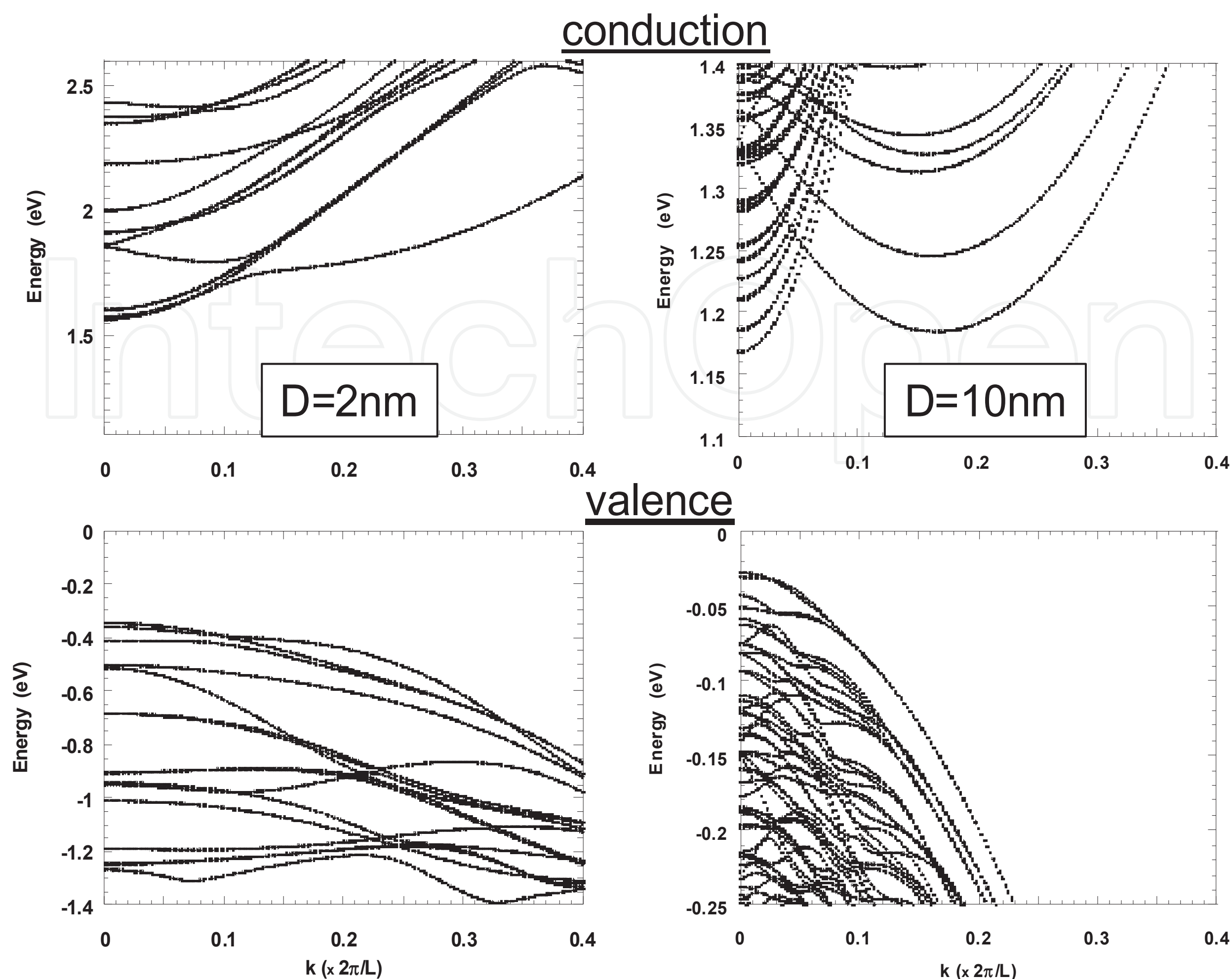


Fig. 8. Silicon nanowire band structure obtained with a tight-binding Schrödinger-Poisson solver (TBSIM, 2011) for two different diameters (2 and 10 nm). Up: Conduction band; down: Valence band.

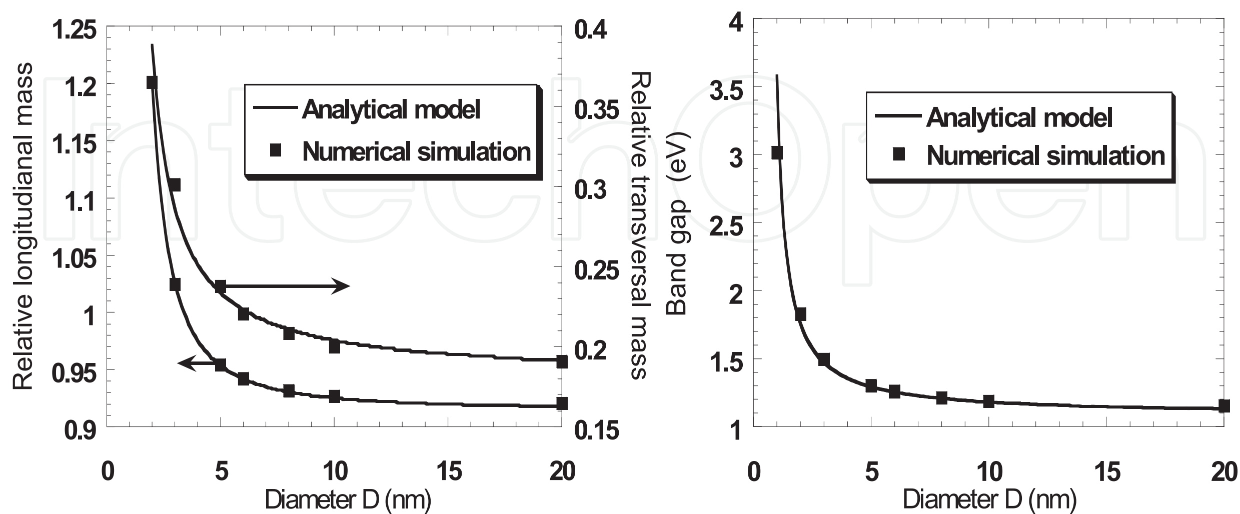


Fig. 9. Variation of the silicon band gap (a) and relative longitudinal and transversal masses (b) with respect to the silicon nanowire diameter. Comparison with atomistic simulations obtained in (Sarrazin & al., 2009).

## 4. Results and discussion

We have just presented the modeling of all the physical phenomena which affect the electrostatics of nanowire MOSFETs. In this part, the impact of each mechanism is assessed at different levels of interest: threshold voltage, drain current and small-circuits performance.

### 4.1 Impact on the threshold voltage

#### 4.1.1 Long-channel transistors

Figure 10 shows the long-channel threshold voltage increase due to quantum confinement, without BSE (i.e., considering bulk value for the band gap and the conduction masses) and with BSE (i.e., considering equations (37) and (38)). The analytical model has been compared to both numerical simulations (Sarrazin & al., 2009) and experimental data (Suk & al., 2007).

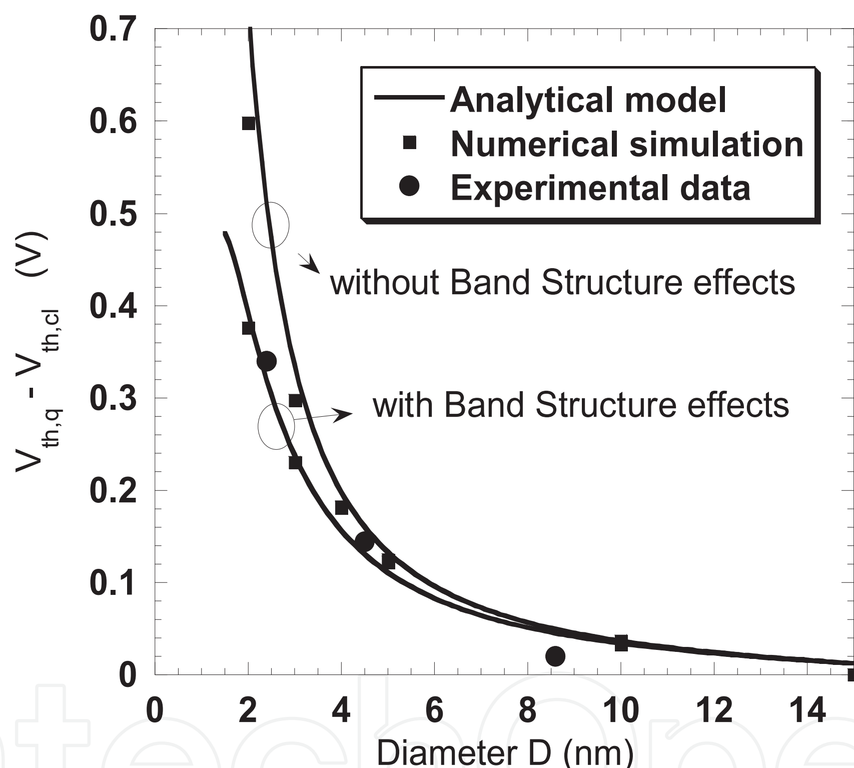


Fig. 10. Difference between quantum ($V_{th,q}$) and classical threshold voltage ($V_{th,cl}$) with and without BSE versus nanowire diameter (long channel transistors). Comparison between the analytical model, atomistic simulations (Sarrazin & al., 2009) and experimental data (Suk & al. 2007).

We can note that the band structure effects tend to limit the impact of the quantum confinement on the threshold voltage of the nanowire. This is coherent with equation (18). Increasing the effective masses, the quantum energy levels are lowered and the energy quantization decreases; then the quantum threshold voltage is lower. Figure 10 highlights the importance of considering BSE especially for thin film where the difference between threshold voltage with BSE and threshold voltage without BSE increases when reducing the nanowire diameter.

### 4.1.2 Short-channel transistors

In the following, we investigate the impact of the quantum confinement on SCE, then the impact of BSE on SCE. As stated previously, the threshold voltage roll-off depends on quantum confinement through the long-channel threshold voltage which includes quantum confinement effects.

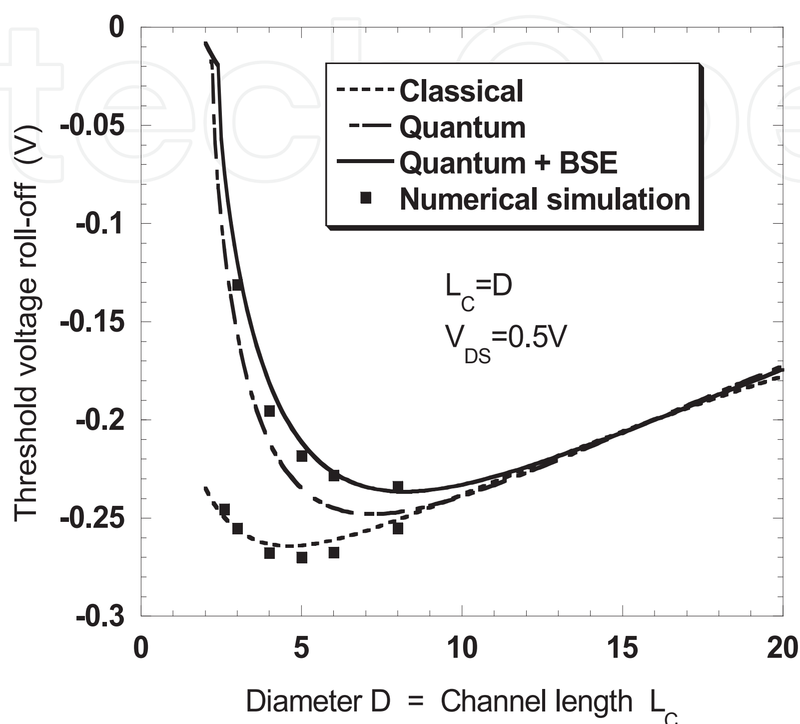


Fig. 11. Impact of band structure variations on SCE. Threshold voltage roll-off versus nanowire diameter for a channel length equal to the nanowire diameter. Comparison with data extracted from numerical simulations using a cylindrical Schrödinger-Poisson solver (Munteanu & Autran, 2003).

Figure 11 shows the impact of quantum effect and BSE on SCE as a function of the nanowire diameter. The curves plot the threshold voltage roll-off for a channel length equal to the nanowire diameter for the three approaches: classical (i.e., without quantum confinement and BSE), quantum without BSE, and quantum with BSE. Quantum threshold voltage obtained using the analytical model is validated in Fig. 11 with numerical simulation data obtained with a cylindrical Schrödinger-Poisson solver (Munteanu & Autran, 2003; Zervos & Feiner, 2004). We can note that the quantum confinement tends to limit SCE. This is due to the enhanced electrostatics control of the active area due to carrier energy quantization. As expected, the difference between quantum and classical approaches increases when reducing the nanowire diameter (due to the increase of energy quantum level for thinner films). When considering quantum confinement, the carrier energy is higher than for classical approach. That is why it is less affected by the longitudinal source to drain electric field, which generally strongly impacts the transistors performances at these channel length values. Moreover, figure 11 shows that BSE tend to amplify the impact of quantum effects on SCE: the threshold voltage roll-off is reduced when considering quantum confinement with BSE compared to the case when only quantum confinement is considered. For long channels, the threshold voltage decrease when considering BSE was due to the increase of

the effective masses which lowered the quantized levels. In the case of short channels, the reduction of SCE when BSE are taken into account is the consequence of the band gap increase. A wider band gap means a higher energetic barrier, leading to a better electrostatics control which is less impacted by source-channel and drain-channel junctions when reducing the nanowire channel length. Moreover, we can note that below a certain diameter (depending on the modeling approach), the diameter thinning has a stronger impact on the threshold voltage roll-off than the channel length reduction. For the same channel length to diameter ratio, the threshold voltage roll-off is higher for D=5 nm than for D=2 nm. Indeed, for ultra-thin films, the quantization of carrier energy is very strong and the carrier concentration is mainly controlled by quantum confinement. In the case of D=2 nm, the strong electrostatic control due to the ultra-thin diameter completely overcomes the increase of SCE expected for these ultra-short channel lengths.

### 4.2 Impact on the injection velocity

Another parameter affected by the BSE is the thermal velocity which depends on masses along the transport direction. Indeed, in our case, for a transport along the (001) direction, the expression of thermal velocity is:

$$v_{th} = \sqrt{\frac{2.kT}{\pi.m_t}} \tag{39}$$

Figure 12 (Dura & al., 2011) shows the thermal velocity evolution with respect to the nanowire diameter. We can note a non-negligible reduction for ultra-thin nanowires up to a 20% decrease for D = 2 nm.

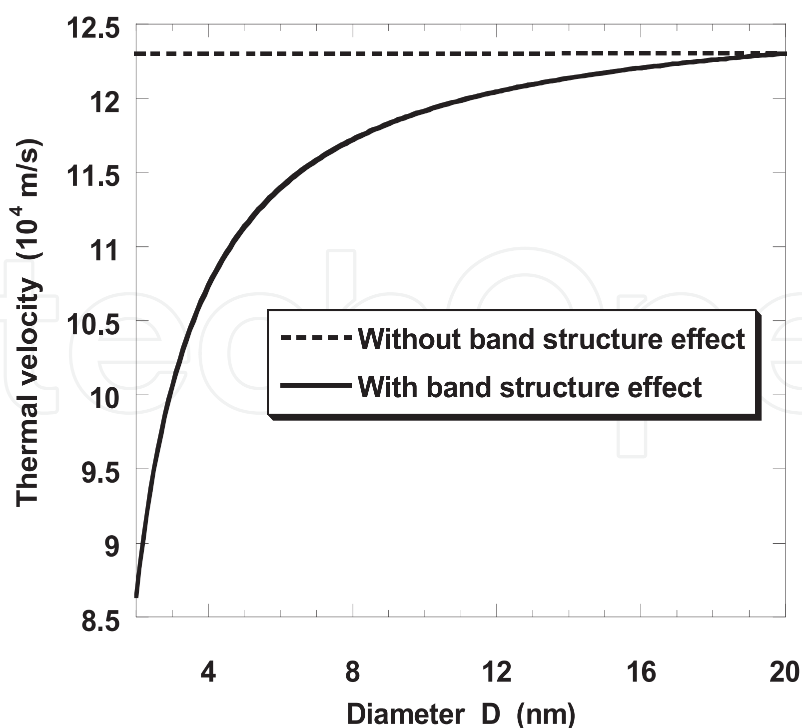


Fig. 12. Impact of the band structure effect on the thermal velocity with respect to the silicon nanowire diameter.

### 4.3 Impact on ballistic drain current of nanowire MOSFET

In previous works, we have demonstrated the analytical model of drain current in GAA nanowire MOSFETs in the ballistic transport regime (without interactions). We remind that this ballistic drain current is derived from the flux method initiated by McKelvey *et al* (McKelevey & al., 1961), doing a balance in the active region between the different carrier fluxes. In the degenerate case, the ballistic drain current is given by the following expression:

$$I_D = \pi.D.C_{ox}.(V_{GS} - V_t).\frac{\Im_0(\eta_F)}{\Im_{-1/2}(\eta_F)}.v_{th}.\left(\frac{1-\frac{\Im_0(\eta_F - \frac{q.V_{DS}}{kT})}{\Im_0(\eta_F)}}{1+\frac{\Im_{-1/2}(\eta_F - \frac{q.V_{DS}}{kT})}{\Im_{-1/2}(\eta_F)}}\right) \quad (40)$$

where D is the nanowire diameter, $v_{th}$ is the thermal velocity discussed above, $V_{GS}$ is the drain to source voltage, $V_{DS}$ is the drain to source voltage, $C_{ox}$ is the oxide capacitance, $\eta_F$ is the Fermi level, $\Im_0$ and $\Im_{-1/2}$ are the Fermi integral of order 0 and -1/2 respectively and $V_t$ is the threshold voltage modeled above.

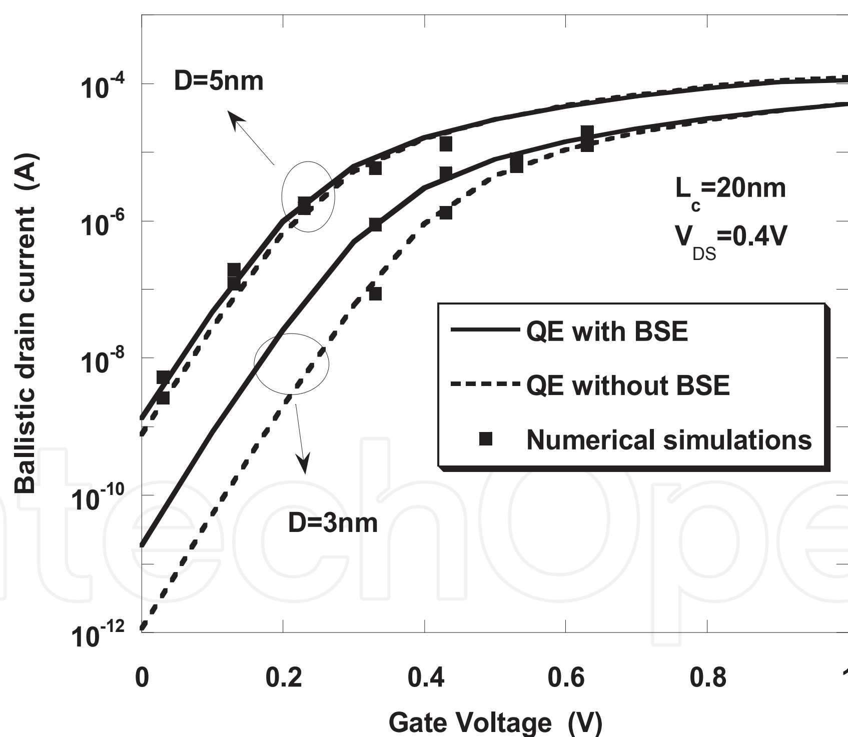


Fig. 13. Impact of the band structure effect on the ballistic drain current. Comparison with numerical simulations (deterministic Wigner equation solving (Barraud & al., 2009)).

Figure 13 shows the result at the device level for a long channel transistor and for two different nanowire diameters (3 and 5nm) (Dura & al., 2011). The ballistic drain current model is compared to numerical simulations based on a deterministic Wigner equation solver (Barraud & al., 2009). We can note a strong impact of BSE on the current in the sub-

threshold regime for 3nm-diameter due to the $V_t$ variation while the ON-state current stays almost unchanged. From this graph, we can highlight the necessity to take into account the correction due to bands variations in the modeling if we expect to provide predictive devices performances. Indeed, at 3nm, the off-state current is increased by more than one decade when BSE is considered.

### 4.4 Impact on performances of small circuits based on nanowire MOSFETs

After implementation in a Verilog-A environment, the model presented above has been used to simulate a CMOS inverter and then a complete 11 stages-ring oscillator. In order to build-up the CMOS inverter a p-type nanowire MOSFET is considered symmetrically to the n-type transistor in the inverter setup. The impact of BSE can be addressed at the circuit level through the study of the commutation characteristics of the inverter or the oscillation frequency of a ring oscillator.

Figure 14 shows the input/output characteristics of the inverter for the classical case (i.e., without QE), with quantum effects (QE) and with band structure effects (QE+BSE). We can note that the inverter characteristic is more abrupt when considering only QE. Similarly to the results obtained for the threshold voltage, BSE tends to limit the impact of quantum confinement by smoothing the CMOS inverter switch.

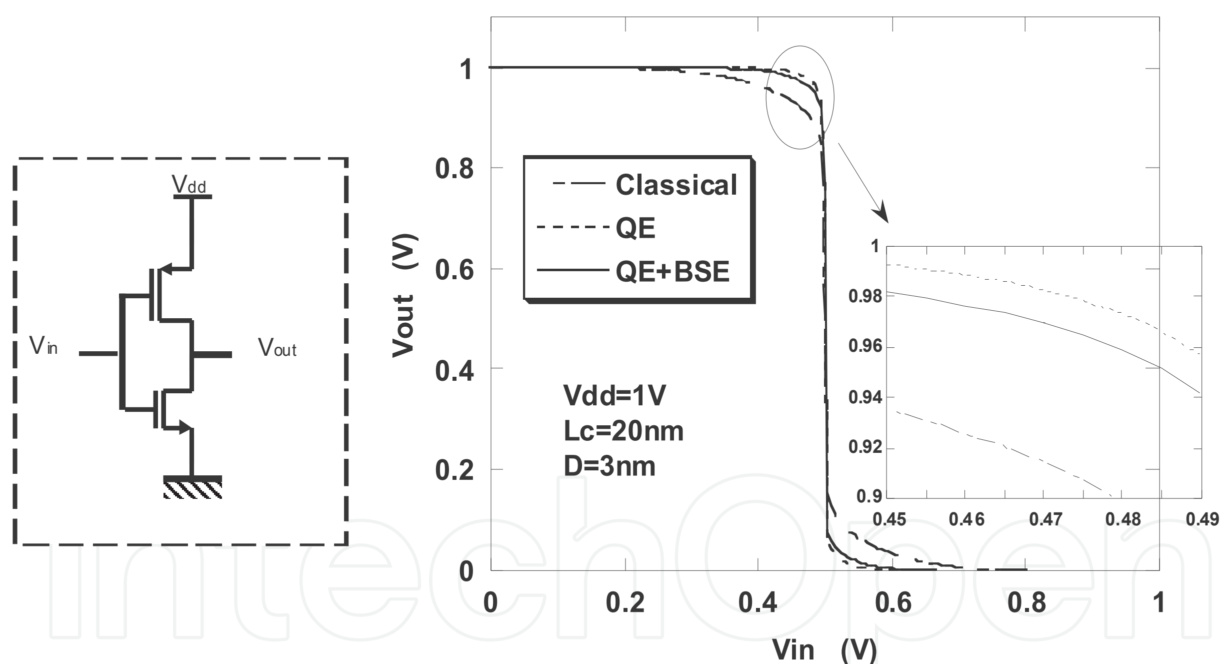


Fig. 14. Impact of BSE on the inverter characteristic. Comparison between classical (i.e, without QE), quantum (QE) and low dimensions effects (QE+BSE).

Regarding the ring oscillator, the results seem opposite to the inverter case. The better performances are for the classical case and introducing quantum confinement reduces the oscillation frequency. This is due to the fact that the ring-oscillator frequency is directly proportional to the ON-state current in strong inversion regime Vdd=1.5V (far from the threshold voltage). QE increases $V_{th}$ and consequently reduces the current. The injection velocity also impacts directly the current and then the oscillation frequency is affected. The result is a reduction of the oscillation frequency when BSE are taken into account.

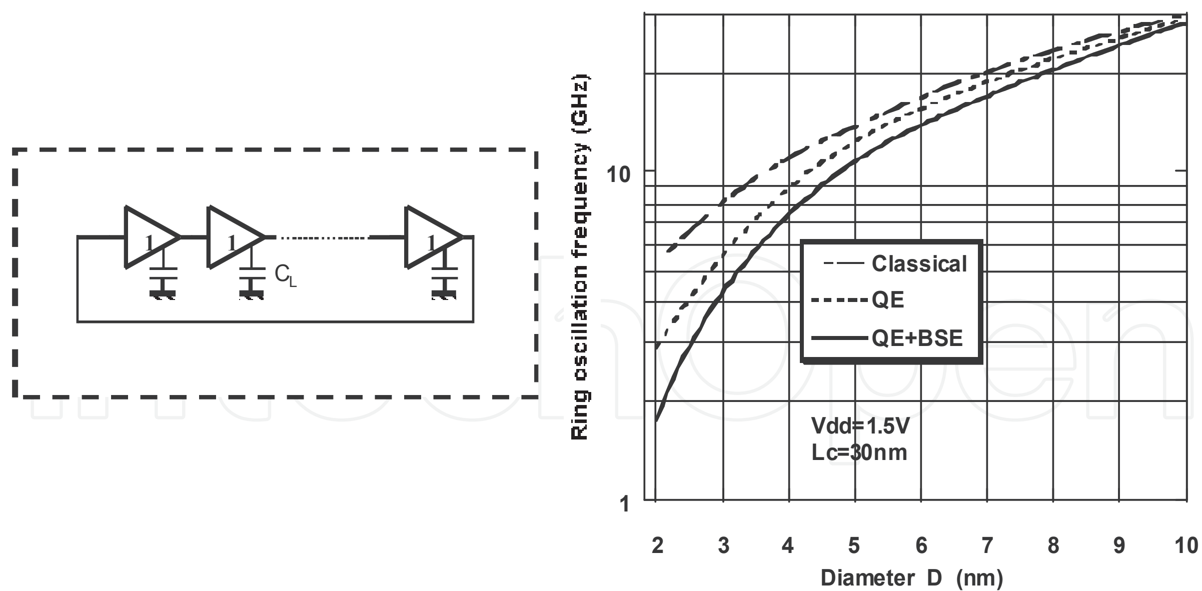


Fig. 15. Impact of BSE on the ring oscillator frequency versus the nanowire diameter. Comparison between classical, quantum (QE) and low dimensions effects (QE+BSE).

## 5. Conclusion

In this chapter, the potential of silicon nanowires for microelectronics applications was evaluated. Regarding the evolution of transistor architectures, they appear as the best configuration for the gate control of the device. The particular shape with a surrounding gate provides an ideal electrostatic control to immunize transistors against perturbations generated by the scaling down of dimensions. In this work, we have developed a complete model of the electrostatic of transistors based on nanowires. The physical phenomena affecting the electrostatics was considered: short-channel effects due to the channel length reduction or the quantum mechanical effects due to the diameter thinning. Moreover, ultimate mechanisms as the modification of the band shape of silicon material is studied based on advanced simulations (essentially tight-binding Schrodinger-Poisson solving). All this physics (thanks to analytical model development) is transposed to higher simulation levels as characteristics of transistor or small-circuit performances. Following this idea, we have seen the impact of short-channel, quantum or band structure effect on the threshold voltage. For ultra-thin nanowires, we highlighted the necessity to consider all these phenomena to be as close as possible to experimental data. Then, a study of their impact on transport was performed with the analysis of ballistic drain current of single transistor and performances of inverters or ring oscillators. In all cases, the evaluation of performances is inaccurate if quantum or band structure effects are not considered. For example, one decade and a half of difference on OFF-state current or a reduction of factor 2 or 3 on the oscillation frequency show the importance of the electrostatics (and so a realistic modeling) if we envisage nanowires as the future technological solution in microelectronics.

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