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Impedance Matching in VLSI Systems

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1. Introduction

The continuous scaling process into submicrometric dimensions of silicon based devices has allowed the integration of a large number of systems in a single chip. Besides, the operating frequencies of such systems are higher and a large amount of information can be processed in a short period of time. On the other hand, while the core frequencies are increasing, higher data rates for off-chip interconnections become necessary, for example a processor that communicates with the memory in order to process information. Unfortunately, at high rates the signal wave length is comparable with the physical length of the interconnections, because of this, parasitic and transmission line effects have to be taken into account. As a consequence, the transmitted signal integrity is degraded resulting in communication errors (Thierauf S., 2004), (Brooks D., 2003).

It has been shown that, for modern off-chip communication systems, current mode signaling offers several advantages over voltage-mode at high data rates (Juan, 2007), but they need to be matched in impedance to the interconnection line. However, impedance matching requires termination resistors. Moreover, due to the large number of input/output circuits in a single chip, terminations have to be placed on-chip (Fan Y. & Smith J., 2003) so that the PCB area is not increased. One of the most important transmission line effects that degrades signal integrity in these signaling schemes is reflection loss. In this case, signal reflections traveling trough the line are present in either driver to receiver or receiver to driver directions. Unfortunately, it is difficult to achieve perfect matching of impedances due to the large process variations in the fabrication of interconnection lines and the different traces between them (Ramachandran N. et. al., 2003). Also, temperature variations and external effects are present inside and outside the chip. As a conclusion, impedance matching techniques must be developed in order to automatically adapt the impedance variations of the line.

In this chapter systems for on-die automatic impedance matching for off-chip signaling are described. In order to perform the automatic matching operation an algorithm that integrates the sign of the impedance matching error and the sign of the coupling branch current is implemented. The advantage of this algorithm is that it works without interfering with the driver operation. Computer simulations of layout extractions are presented. Also, a system of knowlegde- based impedance matching which avoids the calculation of a complex mathematical model is presented.

2. Signaling schemes

Electrical signaling schemes, which have become one of the most important topics in digital design and a hot topic in research, are the techniques used in the transmission of digital signals from one place to another through an interconnection (Dally & Poulton, 1998). Typical medias for the transmitted signals are on-chip, PCB and backplane interconnections as well as cable lines.

Electrical signaling schemes are classified into voltage mode and current mode signaling schemes depending on the signal carriers of the data through the interconnection. Besides, signaling schemes are also grouped into single ended, fully differential, pseudo differential and incremental signaling (Juan, 2007). In this section electrical signaling schemes are presented and the advantages of current mode over voltage mode are enlisted.

2.1 Voltage mode signaling

In Fig. 1 the model for a voltage mode signaling scheme is shown where the line driver is represented by a voltage source V_{DD} that corresponds to the value of the voltage swing. The resistance R_S represents the output impedance of the driver and the transitions between logic states is achieved by changing the position of the switch. Thus, these logic states, namely 1 and 0, are represented by two supply voltage levels. The circuit drives the output signal through the transmission line with characteristic impedance Z_O to the far end of it where a CMOS inverter compares the received voltage against a voltage reference derived from the power supply. Finally the voltage source V_N represents the power supply noise generated between the transmitter and the receiver at both ends of the line which, in fact, deteriorates the signal integrity at the far end.

An important property in voltage mode signaling is that due to the large swing of the signal the noise margins are also large. Even so, special care must be taken in the design of such circuits because of the swing dependent noise sources that are added to the data signals.

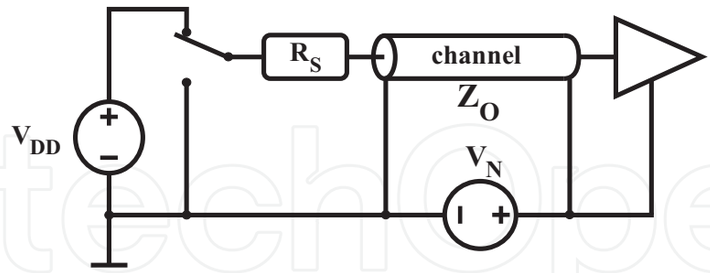


Fig. 1. Voltage mode signaling modeling.

Some realizations of circuits for voltage mode signaling are presented in (Ramachandran N. et. al., 2003),(Dehon et. al., 1993),(Deutschmann B. & Ostermann T., 2003), (Svensson C. & Yuan J., 1991), (Choy C. S. et. al., 1997), (Shin S. K. et. al., 2005) and (Balatsos A., 1998). The simplest voltage mode signaling circuit is shown in Fig. 2. It consists of an inverter stage at the near end of the channel where each transistor acts as a switch that directs the output node to the respective rail voltage (V_{DD} through M_1 and V_{SS} through M_2). Also, it is important to say that at any time one transistor of the circuit is inactive while the other is active. As a consequence the signal transmitted through the channel is the voltage at the output V_O of the

inverter and can be computed with equation (1)for rising edge signal and (2) for falling edge, (Juan, 2007).

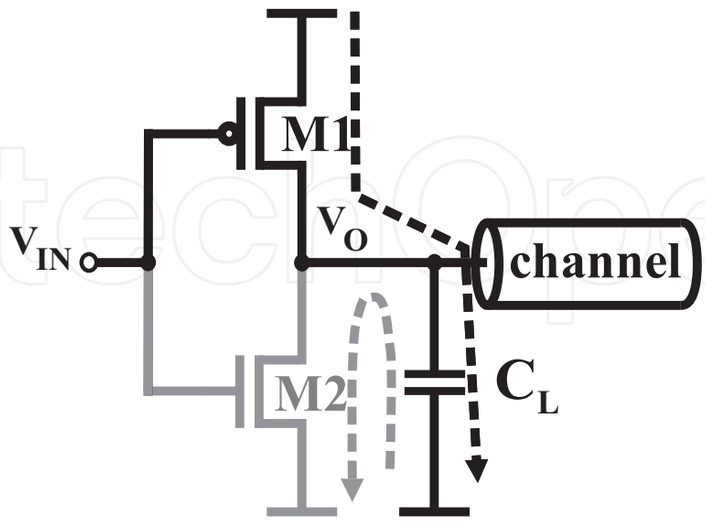


Fig. 2. Voltage mode signaling typical circuit.

$$C_L \frac{dv_o(t)}{dt} + \frac{v_o(t) - V_{DD}}{R_p} - C_L V_{OL}\delta(t) = 0 \tag{1}$$

$$C_L \frac{dv_o(t)}{dt} + \frac{v_o(t)}{R_n} - C_L V_{OH}\delta(t) = 0 \tag{2}$$

In equations (1) and (2) the constants R_n and R_p are the resistances of the NMOS and PMOS transistor channels when they are biased in the triode region. C_L is the load capacitance of the driver, V_{OL} and V_{OH} are the voltages that represent the logic states 0 and 1. Finally, the products $C_L V_{OL}\delta(t)$ and $C_L V_{OH}\delta(t)$ are the contribution of the initial voltage for the processes of charging and discharging respectively.

The power consumption for voltage mode signaling systems is shown in equation (3), where κ is the switching activity coefficient. It is clear that the dependence with the frequency represents a disadvantage for high frequency applications.

$$P \approx \kappa C_C V_{DD}^2 f \tag{3}$$

In the following subsections advantages and limitations of various voltage mode signalling schemes, such as single ended, fully differential, pseudo differential and incremental, are presented. This classification is obtained from (Juan, 2007).

2.1.1 Single ended signaling

In single ended signaling, only one conductor per channel is needed to carry the signal to the receiver side of the system. As shown in Fig. 3(a), the signal arriving to the far end of the line contains both the transmitted one and a noise component that is generated by the devices

that are near to the conductor. This signal is compared against a reference signal V_{REF} that is generated locally in the receiver.

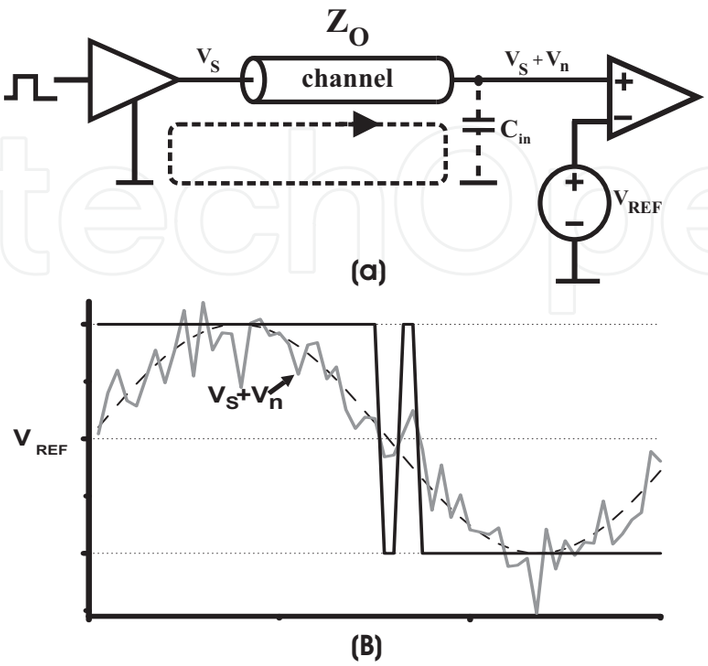


Fig. 3. (a) Single ended signaling in voltage mode; (b) input output voltage examples

In Fig. 3(b) the input and output voltage examples for a single ended voltage mode link are shown. Due to the single ended characteristic of the system the noise can not be rejected by the comparator and, in consequence, the output presents unwanted error symbols. That is why such systems are susceptible to coupled noise. In addition, in Fig. 3(a) the dotted line shows the path of the signal in the interconnection which goes from the driver to the receiver through the line and returns usually through the ground planes. The capacitor C_{in} is the input impedance of the comparator. This path represents a large area loop that results in high level electromagnetic emissions that affect devices located close to the channel.

2.1.2 Fully differential signaling

The fully differential signaling for voltage mode links is shown in Fig. 4. The main difference compared with the single ended scheme is that it uses two interconnections to carry the signal to the far end of the line. Another important characteristic is that conductors are so close to each other that the induced noise tends to be the same in each one. As a consequence the signals that are present at the line far ends are the transmitted positive voltage V_S^+ plus the induced potential V_n, i.e. $V_S^+ + V_n$ and, in the same way, the signal in the other polarity is $V_S^- + V_n$. At the receiver side the determination of the symbol is done by means of the voltage comparator configured in a differential way, because of this, the noise component is cancelled. As a conclusion, it can be said that fully differential configuration for signaling provides excellent common mode noise immunity.

By analyzing Fig. 4 the signals that charge the input capacitors C_{in+} and C_{in-} are the time varying differential currents that flow in opposite ways in each conductor. These currents

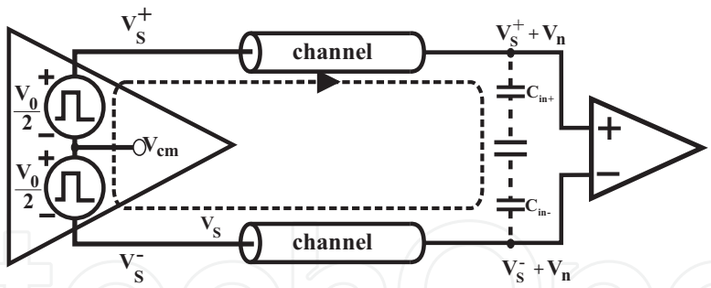


Fig. 4. Fully differential voltage mode signaling

form the closed loop shown with the dashed line in the Fig. 4. Compared with the one in single ended, the area occupied by this loop is small due to the proximity of the conductors. As a consequence, the electromagnetic coupling with other channels is small. Finally, the most important shortcoming of the differential signaling systems is the occupied area by the two lines.

2.1.3 Pseudo differential signaling

The pseudo differential signaling for voltage mode links is shown in Fig. 5, it is, in essence, a combination of the single ended and the differential signaling systems. In the pseudo differential scheme a single conductor is used as a reference for a group of signal paths. A common number for this group is four. As in fully differential signaling, the physical lines running from the transmitter to the receiver are so close between them that the induced noise V_{ni} is considered the same in all of them. In consequence, if differential comparators are considered as receivers then noise components can be eliminated.

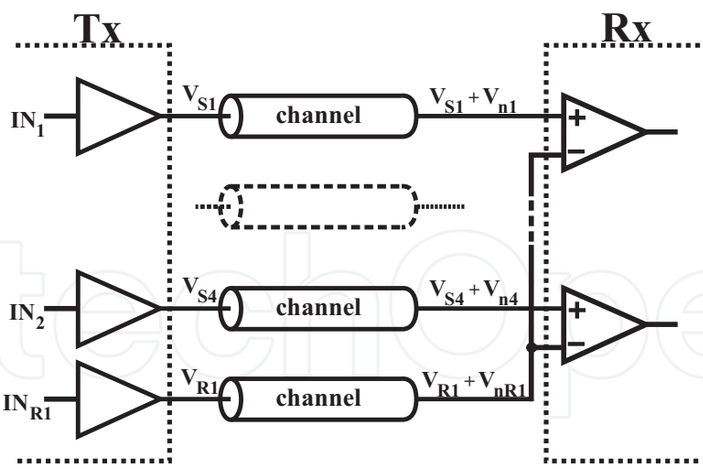


Fig. 5. Pseudo differential voltage mode signaling

It is clear that the main advantage of pseudo differential links is the reduced number of conductors that it needs. Unfortunately, the use of a single conductor as a reference signal also represents a drawback, because the area for the signal loops is increased. As a consequence, the channel inductance is larger compared to that in the fully differential approach. A solution for this drawback is presented in (Carusone A. et. al., 2001), where an incremental signaling approach with high signal integrity is presented.

2.2 Current mode signaling

A model for a current mode signaling system is shown in Fig. 6. In this case the line driver is represented by a current source I_S and the couple of switches that direct the current trough the line. At the far end of the link a resistor R_L is connected between the reference and signal lines and its purpose is not only to match the transmission line impedance but also to convert the current into voltage. This voltage is then changed to digital by the differential-mode comparator at the receiver side.

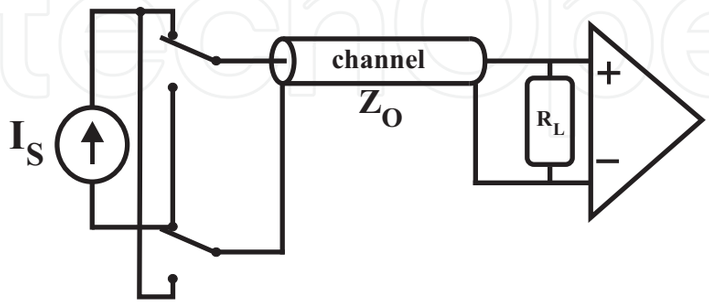


Fig. 6. Current mode signaling modeling.

In current mode signaling systems the symbols are represented by branch current signals. For the case of Fig. 6 when switches are in the upper side a current I_S flows through the line from transmitter to receiver and, in the ideal case, through the load resistor. In this case a voltage $V_L = I_S * R_L$ is present at the input of the comparator. In the opposite case, when switches are in the lower side, the current flows from receiver to driver, then the voltage drop is $V_L = -I_S * R_L$. In consequence, the total voltage swing at the far end of the link is $V_{sw} = 2 * I_S * R_L$.

One of the most basic drivers for current mode signaling systems is shown in Fig. 7 where the current I_S is directed to one branch or to the other just by switching the transistors M_1 and M_2. The control of this action is achieved by the digital data to be transmitted Dat and $\overline{Dat}$. The resistances R are implemented to match the characteristic impedance Z_0 of the channel.

One of the most important advantages of current mode signaling is that the information is represented by branch currents and, due to the low impedance characteristic of the transmission media, the voltage swing for these systems is small even though the current signals are big. As a consequence, circuits can operate with a low voltage supply and current swings are not affected by the variations on the supply voltages (as opposed to voltage mode signaling). From the argument of swing invariance to supply changes, it can be concluded that current mode signaling has superior signal integrity compared with the voltage mode one.

An important issue in signaling systems is the propagation delay and is directly related to the rising and falling time of the signal. For a capacitive node, the rising(falling) time is shown in (4), (Juan, 2007), where I is the average current charging and discharging the node, C_n is the node capacitance and ΔV_n is the node voltage swing.

$$\Delta t = \frac{C_n \Delta V_n}{I} \tag{4}$$

From equation (4) it can be inferred that if a small Δt is needed then the voltage swing ΔV_n must be minimized or the charging/discharging current must be big. Then, from equation

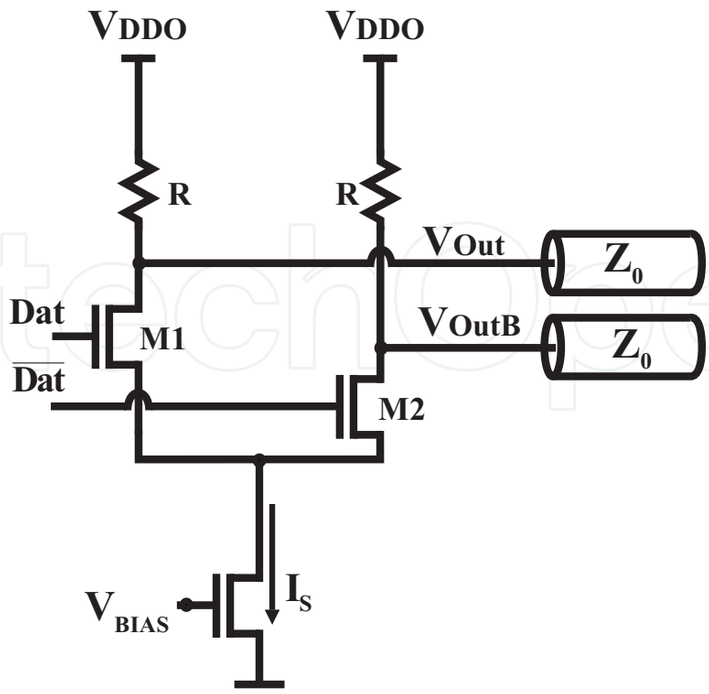


Fig. 7. Current mode signaling circuit.

(4),it can be concluded that current mode signalling systems have small propagation delay which make them suitable for high speed environments.

An important topic regarding electronic systems is power consumption. In particular, it is essential for signaling systems because they tend to consume big quantities of power. The power consumption in current mode circuits can be calculated by using equation (5), where it can be seen that there is not a dependence with frequency. Moreover, has only static power consumption which represents a benefit in high frequency applications.

$$P \approx I * V_{DD} \tag{5}$$

In the following subsections two of the most important realizations for current mode signaling are presented. They are called unipolar and bipolar current mode signalling.

2.2.1 Unipolar current mode signaling

The symbol codification in unipolar current mode signaling (UCMS) is shown in Fig. 8, where a logical 1 is represented by the current I_1 and the logical 0 is represented by the absence of current. In this system the transmitter offset current is represented by I_{X0} and the possible values for the symbol are represented by the black area (it is clear that a zero current is easy to implement, that is why the black area corresponding to the symbol 0 is small). The receiver offset I_{r0} and sensitivity I_{rs} are also sketched in the scheme, they are near the reference current I_R.

In Fig. 9 the unipolar current mode signaling system is depicted. The UCMS block represents the driver which is, in this case, the one shown in Fig. 7. As stated before, the driver sinks a current I from one line each time, i. e. there is no signal flowing in both conductors at the

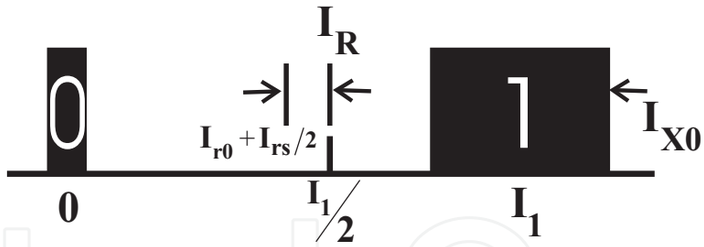


Fig. 8. Symbols in unipolar current mode signaling.

same time. At the far end of the lines, termination resistors R_T are placed in order to generate a differential voltage at the input of the receiver. This voltage is given by the difference between the positive and the negative inputs of the comparator as shown in equation (6).

$$\Delta V_{in} = |V_{in}^{+} - V_{in}^{-}| = |V_{DD} - R_T I - V_{DD}| = R_T I \tag{6}$$

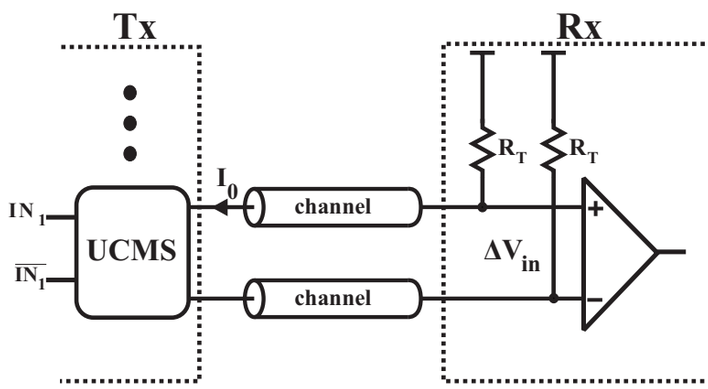


Fig. 9. Unipolar current mode signaling system.

As stated before, the variations in the voltage supply and in the ground sources do not have effect in the current flowing through the channel. Furthermore, due to the differential configuration at the receiver side, the common mode noise is eliminated. The disadvantage in unipolar signalling is that electromagnetic emission exists because only one conductor is carrying the current each time.

2.2.2 Bipolar current mode signaling

The symbol codification in bipolar current mode signaling is presented in Fig. 10. In this case the logical 1 is represented, as in unipolar signaling, by the current I_1. The difference is that the logical 0 is represented by the current $-I_1$.

By comparing Fig. 10 with Fig. 8 it can be appreciated that the allowed area for the logical 1 offset at the receiver has decreased. The reason for this is that the area of the offset for the logical 0 has to be increased because the current that represents it is now different from zero. The receiver offset I_{r0} and sensitivity I_{rs} are also sketched in the scheme, they are near the reference current I_R which is centered in zero amperes in bipolar signaling.

An example of bipolar current mode signaling systems is depicted in Fig. 11. It can be seen in the figure that current flows always in both interconnections but in opposite directions, as

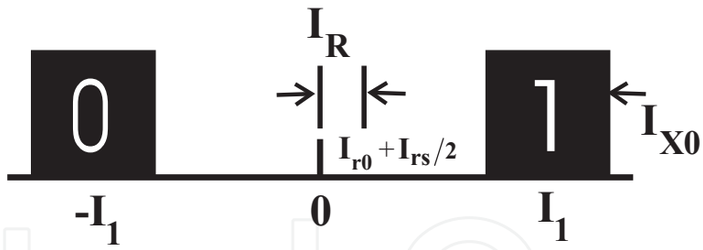


Fig. 10. Symbols in bipolar current mode signaling.

stated before in this section. This property allows these systems to have a low electromagnetic emission because field components are cancelled due to the opposite directions of the current. Another characteristic of bipolar signaling is that the load resistance R_T is placed between the interconnections in such a way that current signals generate a voltage which is compared by the differential mode comparator at the receiver.

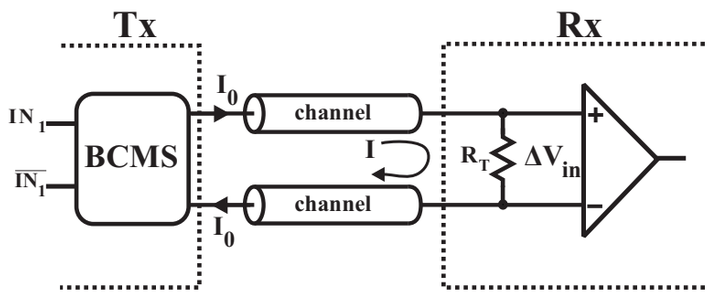


Fig. 11. Bipolar current mode signaling system.

Bipolar current mode signalling systems are also called low voltage differential signalling (LVDS) and a typical driver is shown in Fig. 12 where the both switches direct the signal to the corresponding conductor according to the data input IN_1. A disadvantage of LVDS links is that both switches current mode sources are implemented with transistors. Then, there are four transistors between the supply voltage and the ground, which is not so desirable in low supply voltage applications. Also common mode feedback circuits are needed increasing the driver size in a considerably amount.

When a N-bit parallel link is needed, a group of N bipolar current mode drivers are put together in a special array. This array is called current mode incremental signaling and specific details on this approach are presented in (Wang T. & Yuan F., 2007).

2.3 Specifications for signaling standards

The specifications for the signaling standards are essential in communication because they establish the voltage levels so that the driver and receiver agree with the logic high and low conditions.

An illustration of the specifications for digital signaling is shown in Fig. 13. The voltages V_H and V_L are the expected voltage levels for the logic values 1 and 0 respectively. In the transmitter side, the driver's goal is to have a high logic level that goes above a minimum voltage level, i.e. $V_{0H} \leq V_H$ and at the receiver side the accepted voltages must go above V_{IH}. Then the noise margin for the high logic level can be written as $NM_H = V_{0H} - V_{IH}$. In a similar way, the noise margin for a logic low is $NM_L = V_{IL} - V_{OL}$.

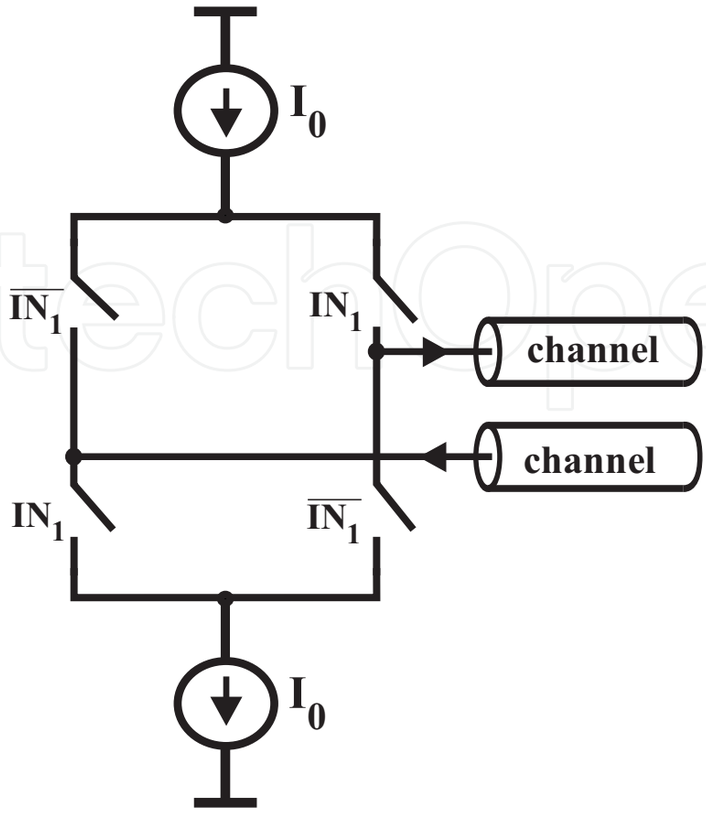


Fig. 12. Low voltage differential signaling driver.

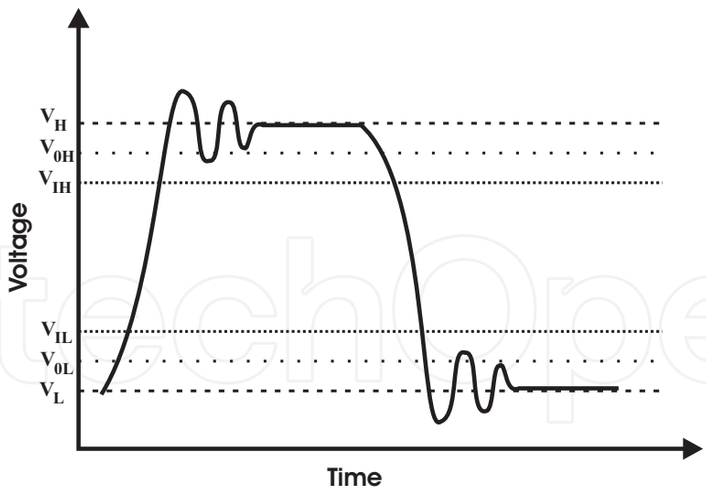


Fig. 13. Specifications for digital signaling.

In table 1 voltage specifications for some common standards are enlisted (Young B., 2001). Although some of them are current mode, the values are presented in voltage which represent the drop on the termination resistors. Another important issue is that the standards are in order from the lowest to the highest speed that can be achieved, then higher speeds are

Stan dard	V_{DDQ}	V_{0L}		V_{0H}		Termi nation	Driver
		Min	Max	Min	Max		
TTL	$5 \pm 10\%$		0.4	2.4		None	PP
LVTTL	$3.3 \pm 10\%$		0.4	2.4		None	PP
GTL			0.4			R_{system} [1]	OD
HSTL	1.5 ± 0.1		0.4	$V_{DDQ} - 0.4$			PP
ECL	$-5.2 \mp 5\%$	-1.810	-1.620	-1.025	-0.880	$50\Omega(-2V)$	CM
PECL	$5 \pm 5\%$	3.190	3.380	3.975	4.120	50Ω	CM
LVPECL	$3.3 \pm 5\%$	1.490	1.680	2.275	2.420	50Ω	CM
LVDS		0.925			1.474	50Ω	CM

Table 1. Driver specifications for signaling standards

accomplished by systems with terminations, reduced voltage swings and with differential configuration.

3. Impedance matching techniques

As stated in previous sections, impedance matching techniques must be implemented in order to reduce return losses. It has been also shown that the fastest signaling standards implement termination resistors in order to match the interconnection impedance. Four of the most common termination techniques are shown in Fig. 14, (Brooks D., 2003). The first technique is the parallel termination (Fig. 14(a)) where a single resistor is connected either to ground or to V_{DD} and its value is equal to the characteristic impedance of the line. Although this is one of the most used methods, its disadvantage is that the current is always flowing through it, thus increasing the power consumption of the system.

The second termination technique is shown in Fig. 14(b), it is called Thevenin termination and consists of a couple of resistors, one connected to ground and the other to V_{DD}. The advantage of this scheme is that it provides pull up and pull down functions improving noise margins in some cases. The drawback of this system is that it is not easy to find the optimum values of the resistors in order to match the characteristic impedance of the line. The third technique is the AC termination and is depicted in Fig. 14(c). It is composed by a series connection of a resistor and a capacitor. Here the capacitance blocks the DC signals in order to reduce the power consumption but distortion can appear when high speed links are considered. Finally the series termination scheme is presented in Fig. 14(d). This is one of the most often used techniques, specially in voltage mode drivers.

Unfortunately the techniques presented in Fig. 14 are implemented with fixed devices and process, temperature and voltage supply variations are not taken into account for the design of such systems. In the following subsections some techniques are presented in which variable terminators are implemented to automatically adapt the impedance of the transmission line.

3.1 Automatic impedance matching control techniques

An important issue in automatic impedance matching is the control technique used in the adaptation process. It takes the reference signal which indicates the desired value of the impedance and the signal that represents the actual value of the impedance and process them in order to have the same value. The output of the circuit sets the value of the impedance that matches the interconnection.

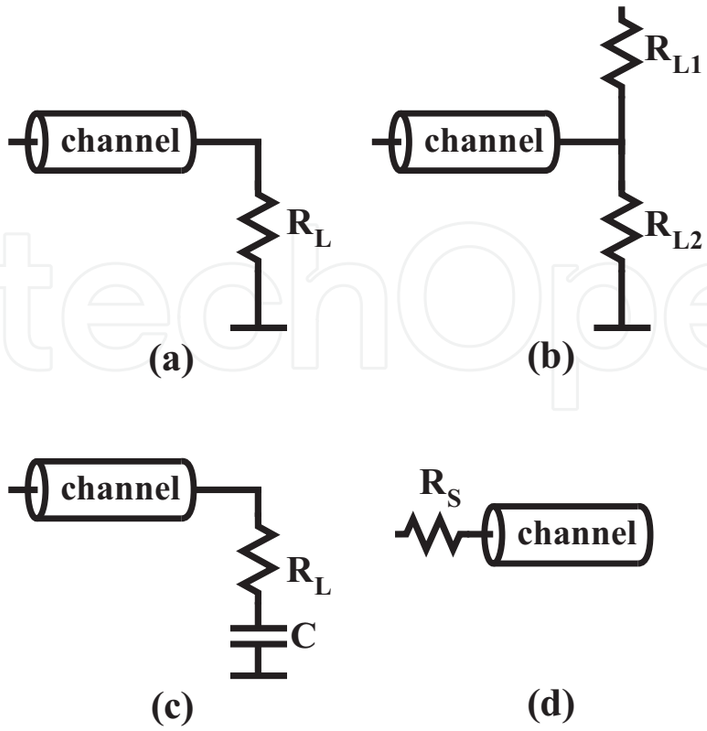


Fig. 14. Termination techniques. (a) Parallel, (b) thevenin, (c) AC and (d) Series.

One of the most common technique used to control the impedance in signaling systems is the one shown in Fig. 15. This technique represents the concept for the circuits presented in (Dehon et. al., 1993), (Koo K. et. al., 2001), (Koo K. et. al., 2006) and (Muljono H. et. al., 2003). It has in essence three stages, the first is a clocked comparator that decides if the impedance value is higher or lower than the reference one. The second stage is a counter which can be either binary or thermometer coded and its input is an $Up/\overline{Dn}$ signal that comes from the comparator. The last stage is a digital register that is used to hold the value of the counter when the matching condition of the impedance is fulfilled. The digital outputs of the register are used to control arrays of transistors in a pull up or pull down connection. The drawback of this technique is that switching noise in the supply lines can be generated due to the turning on and the turning off of the transistor array.

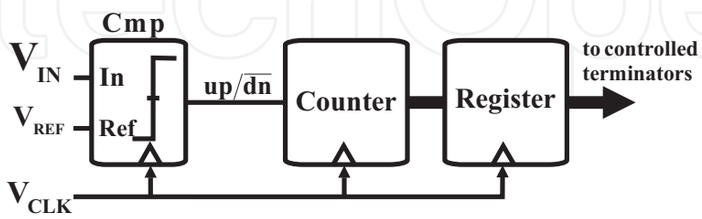


Fig. 15. Digital control for automatic impedance matching.

Another approach used in the control of automatic impedance matching is shown in Fig. 16 which is a simplified version of the one presented in (Ramachandran N. et. al., 2003). This circuit is designed to adapt directly the output impedance of an analog driver to the interconnection line by controlling a variable resistor at the output stage of the driver. The

input signals to this control circuit are the input and the output of the line driver, they are processed by the first stage which is a peak to peak detector. The second stage is a differential difference amplifier (DDA) and its output is the analog control voltage. The drawback of this analog technique is that the driver speed is limited by the frequency response of the control circuits due to the direct signal measurement in the input and output ports.

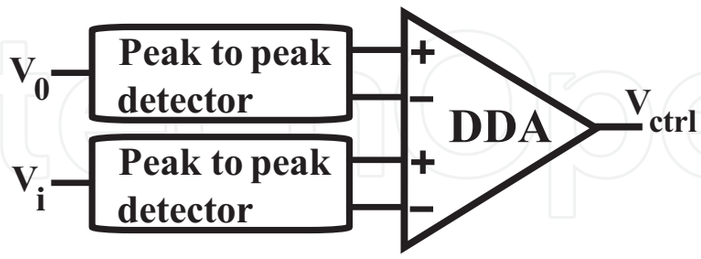


Fig. 16. DDA based analog control for automatic impedance matching.

A second analog approach for the control of an impedance matching system is shown in Fig. 17 which consists of a feedback amplifier. In this circuit the drawback of limited speed of the driver is eliminated by implementing an off-line matching of the impedance, i. e. a replica of the matching impedance is implemented in order to generate the reference signal and no measurements are made from the ports of the driver. The problem with this system is that variations in the interconnection impedance are not taken into account in the process of matching.

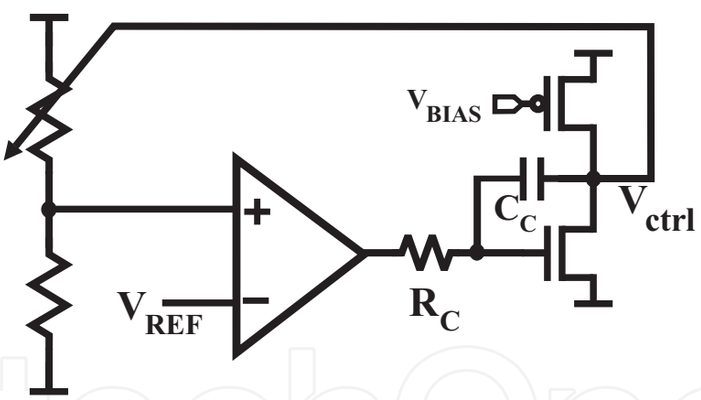


Fig. 17. Feedback amplifier based analog control for automatic impedance matching.

3.2 Reference signal generating circuits

In this section some of the most popular reference signal generating circuits are presented. Reference signals are an important subject in automatic impedance matching because they establish the value that the variable impedance must reach in order to fulfill the matching condition.

One of the most used circuits for reference signal generating is shown in Fig. 18, (Fan Y. & Smith J., 2003), (Koo K. et. al., 2006) and (Tae-Hyoung K. et. al., 2005). It consists of an off-chip precision resistor R_{REF} connected in series with a replica of the on-chip variable impedance used to match the interconnection R_v. The reference voltage V_{REF} is obtained from the node located between the resistors and its optimal value is the half rail voltage $V_{DD}/2$. An

advantage of this technique is that the matching operation is independent from the driver data rate because measurements are not taken from the signal lines. The drawback is that an external resistor is needed which increases the area of the PCB. Furthermore, impedance variations of the off-chip interconnection are not taken into account since the reference is generated off line.

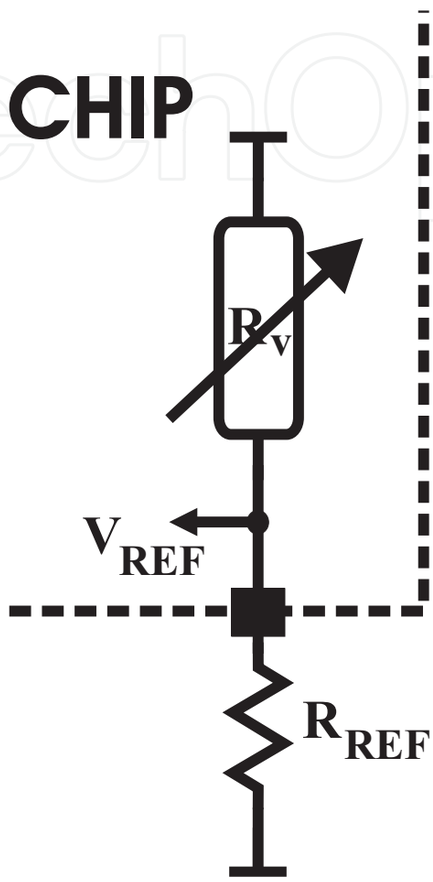


Fig. 18. Generation by dividing voltage.

An approach where current sources are implemented in order to generate voltage drops in a replica of the on chip variable impedance R_v and in an off-chip precision resistor R_{REF} is depicted in Fig. 19 (Dally & Poulton, 1998). Here, the two voltage references V_{REF} and V_{REF2} must have the same value in order to fulfill the matching condition of the impedance. As in the case of the circuit in Fig. 18, the off-chip resistor increases the area of the PCB which represents a disadvantage when high performance systems are needed. Also, variations in the interconnection impedance are not considered because references are generated in a circuit which is separated from the driver.

A modification of the circuit of Fig. 19 is shown in Fig. 20, (Koo K. et. al., 2001). In this case only the voltage drop from the on chip variable impedance R_v is considered as a voltage reference, avoiding the need of an off-chip resistor. In order to accomplish the automatic impedance matching operation, the reference voltage V_{REF} is compared against an internally generated voltage reference. The disadvantage of this technique is that the on-die process, voltage and temperature variations can move the internal reference away from its optimal

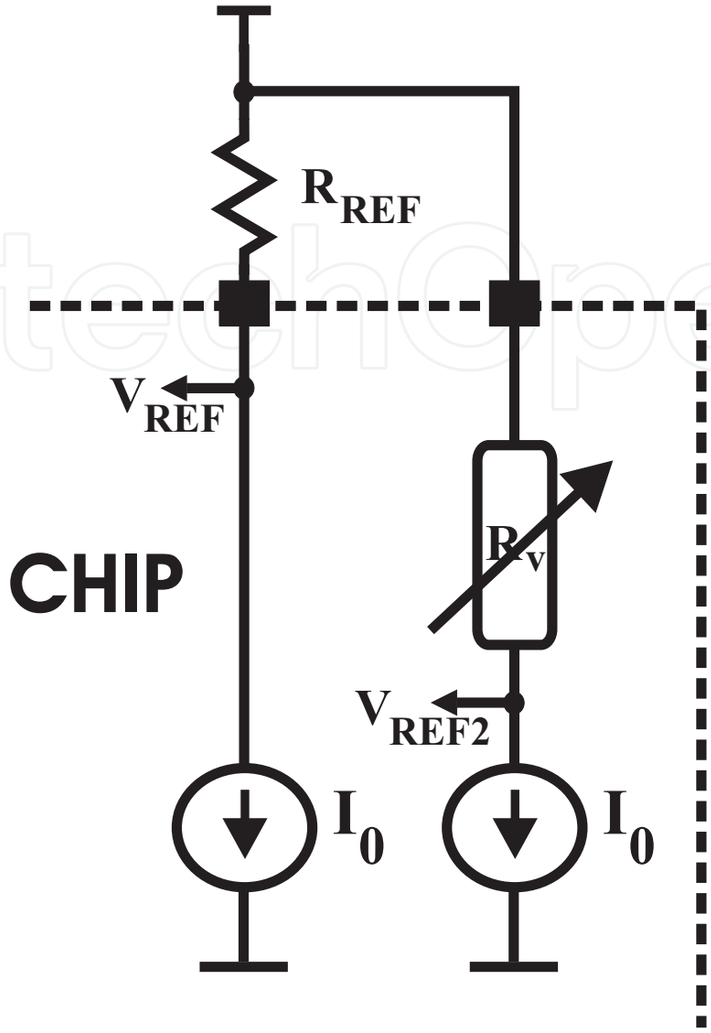


Fig. 19. Voltage drop reference generation.

value generating impedance errors. As in the case of the techniques presented before, the variations in the interconnection impedance are not considered.

In order to overcome the drawbacks related with the variations in the interconnection impedance, the technique shown in Fig. 21 has been implemented in (Dehon et. al., 1993) and (Dally & Poulton, 1998). In this case a voltage mode driver is implemented in order to drive an interconnection that is terminated with an open at the far end. The reference signal is taken from the node between the matching resistance and the interconnection channel and its shape is as shown at the bottom of the figure. This shape is composed by the signal arriving to the channel from the driver and the one reflected from the far end. In this case the matching condition is fulfilled when the middle part of the reference signal is the same as $V_{sw}/2$, where V_{sw} is the total swing of the transmitted signal. The drawback of this system is the difficulty in generating the correct timing signals in order to make the voltage comparisons in the correct time.

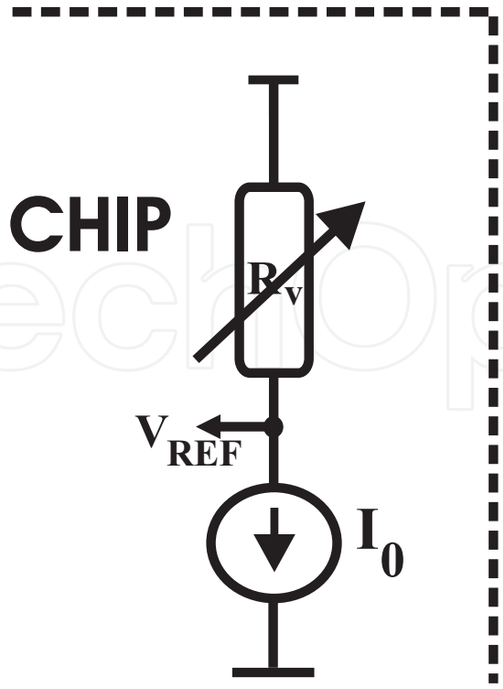


Fig. 20. On chip reference generation.

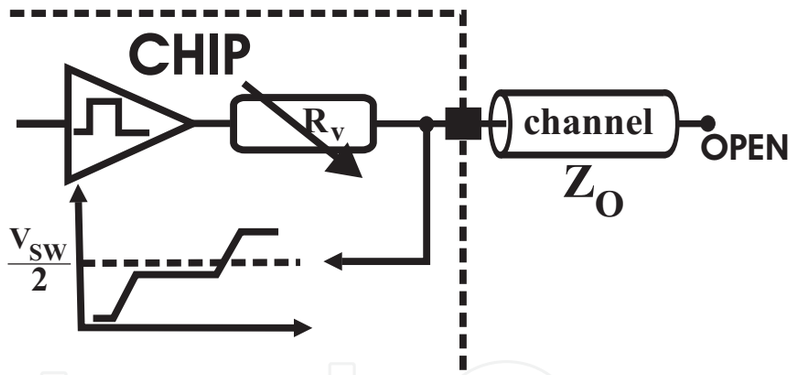


Fig. 21. Reference generation by signal reflection.

Finally, an approach for reference signal generation in current mode drivers is depicted in Fig. 22 which is an idea presented in (Munshi A. et. al., 1994). In this technique the current mode driver sinks or sources a current I_S from or to the interconnection which is in a parallel array with the matching impedance R_v. Then the matching condition in this scheme is fulfilled when the current I_v flowing though R_v is $I_v = I_0$, in other words, when $I_v = I_S/2$. The advantage of this method is that variations in the impedance of the interconnection are taken into account since reference signals are measured directly from the data link. The drawback is that measuring currents may modify the impedance branch.

In a similar way, reference signals for voltage mode interconnections can be obtained by considering the variable impedance and the interconnection line as a voltage divider. In this case, the reference voltage must be equal to $V_S/2$.

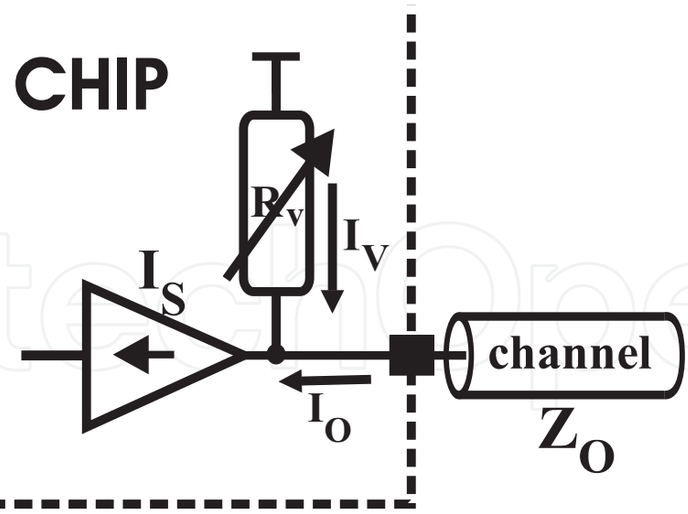


Fig. 22. Reference generation by current division.

4. Automatic impedance matching design based on the sign of the error

An automatic impedance matching based on an optimization algorithm that uses the sign of the error and the sign of the coupling branch current is proposed. A possible implementation of the system, simulation and experimental results are presented.

4.1 Mathematical approach

The mathematical formulation of the proposed method for impedance matching is based on Fig. 23, which is a modification of the system proposed in (Munshi A. et. al., 1994). In this system the output driver is modeled with a simple time variant current source and its output impedance is set to infinity. The current is divided between two branches, one is the transmission line with characteristic impedance Z_0 and the other is the matching branch Z_g which is used to avoid reflections in the line. This matching impedance is mainly composed by two elements, a current dependent voltage source V_g and a fixed impedance Z_P. The output voltage V_S is the voltage drop that results when the output current I_S flows through the parallel configuration of Z_g and Z_0. Then the system can be seen either by its current or by its voltage characteristics.

As shown in equation (7), the voltage dependent source V_g has a linear relationship with the coupling branch current I_g.

$$V_g = H_g I_g \tag{7}$$

where, the transimpedance H_g is a variable parameter with units of Ohms (Ω).

By analyzing the Fig 23 it can be deduced that the current I_g, flowing in the coupling branch, can be expressed as in the equation (8).

$$I_g = \frac{1}{Z_P}(V_S - V_g) \tag{8}$$

From equation (8), and making some mathematical manipulation, it is posible to prove that the matching impedance is given in terms of the fixed impedance Z_P and the transimpedance

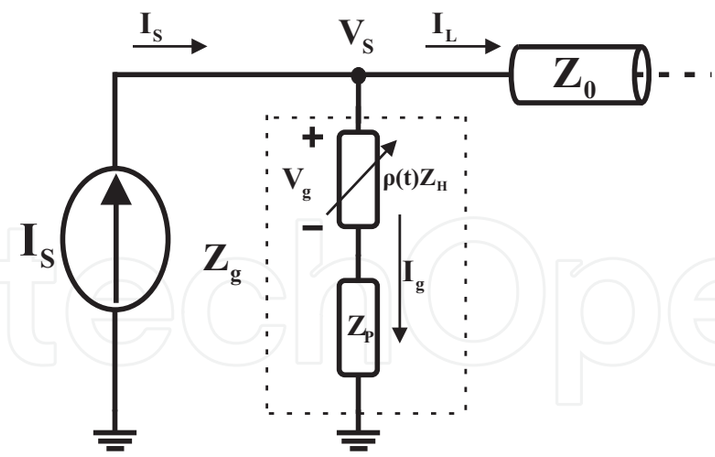


Fig. 23. Impedance Matching Synthesis Circuit

H_g. This is shown in the equation (9).

$$\frac{V_S}{I_g} = Z_g = Z_P + H_g \tag{9}$$

From equation (9) it can be inferred that H_g should be modified in order to achieve an impedance value $Z_g = Z_0$, which is the coupling condition. In consequence, H_g is defined as:

$$H_g(t) = \rho(t) Z_H \tag{10}$$

where, Z_H is constant and has units of Ohms(Ω) and $\rho(t)$ is an impedance matching coefficient and its optimal value is achieved when the impedance matching condition $Z_g = Z_L$ is fulfilled. It is clear that the fulfillment of the condition implies: $I_g = I_L = 1/2 I_S$. From this expression, the impedance matching error e is defined as in equation (11).

$$e = \frac{1}{2} I_S - I_g \tag{11}$$

From equations (7), (10) and (11), the goal of the system is to dynamically adapt the coefficient $\rho(t)$ in such a way that the error e is minimized. A suitable technique to accomplish this goal is the LMS (Least Mean Square) (Carusone A. & Johns D., 2000), in which the criteria is to optimize temporal estimations of $E[e^2]$. Then, it is possible to express ρ as follows:

$$\rho(t) = -2\mu \int_{-\infty}^{t} e(u) \nabla_\rho e(u) du \tag{12}$$

where, μ is constant and establishes the speed of adaptation of the system, $\nabla_\rho e(u)$ represents the gradient of the error related with the parameter ρ . Also, for the equation 12 is considered that e^2 is a noisy estimation of $E[e^2]$.

Once established the conditions and the optimization method, it is necessary to find ρ as a function of the system parameters. Then, by substituting equation (8) in (11), the impedance matching error is given by:

$$e = \frac{1}{2} I_S - \frac{1}{Z_P} (V_S - V_g) \tag{13}$$

From equations (7),(10) and (13), it is possible to find the gradient of the error as shown in equation (14).

$$\nabla_\rho e = -\frac{1}{Z_P} Z_H I_g \tag{14}$$

Finally, from equations (14) and (12) the coefficient ρ as a function of the system parameters is presented in (15).

$$\rho(t) = \frac{2\mu Z_H}{Z_P} \int_{-\infty}^{t} e(u) I_g(u) du \tag{15}$$

It can be seen from (15) that for practical implementation the silicon area can be large due to the multiplication operation. In order to simplify the system, the SS-LMS (Sign-Sign LMS) algorithm, (Carusone A. & Johns D., 2000), is considered, where the sign function is applied to the error and to the matching branch signals. Thus, the multiplication results in a trivial operation. Consequently, the impedance matching coefficient become:

$$\rho(t) = \alpha \int_{-\infty}^{t} Sgn(e(u)) Sgn(I_g(u)) du \tag{16}$$

where, $\alpha = \frac{2\mu Z_i}{Z_P}$ is constant.

Based on equation (16), the block diagram of the proposed system for automatic impedance matching is depicted in Fig. 24. The system input is the driver voltage V_S and the reference for the error signal is the driver current divided by two. The block $\frac{1}{Z_p}$ represents the fixed impedance and the transimpedance block $H(\alpha)$ performs the dependent source V_g. The impedance optimization is made by the sign blocks together with the multiplication and integration blocks. The coefficient α specifies the speed of matching and the error level around the optimal impedance.

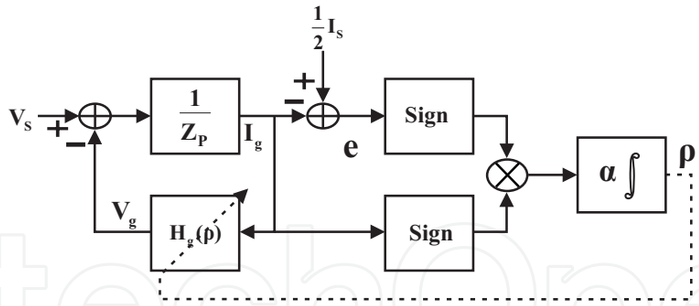


Fig. 24. Block Diagram for Impedance Matching.

4.2 Proposed implementation

One condition that must be established for the circuit implementation of the system of Fig. 24 is that the impedance Z_P is real and that its value is smaller than the load impedance Z_0. It means that Z_P must accomplish the following conditions: $0 < Z_P < Z_0$ and $Z_P = Re(Z_P)$. Also, the sign operation for the error can be expressed as:

$$\begin{aligned} Sgn(e) &= Sgn\left(\frac{1}{2} I_S - I_g\right) \\ &= Sgn\left(\frac{1}{2} Z_P I_S - Z_P I_g\right) \end{aligned} \tag{17}$$

In the same way, the sign operation for I_g is:

$$Sgn(I_g) = Sgn(Z_P I_g) \tag{18}$$

As shown in (17) and (18), the sign operation can be implemented as a voltage level comparator. In this way, the inputs for (17) are the voltage across the fixed impedance Z_P and the reference voltage across the impedance with the same value as Z_P.

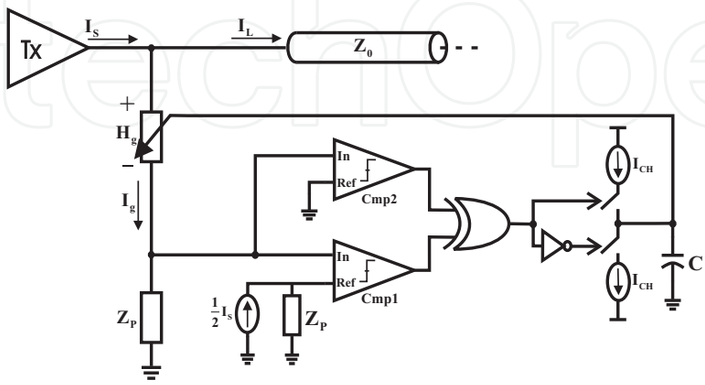


Fig. 25. Automatic Impedance Matching System Implementation.

The proposed circuit implementation for the automatic impedance matching system is shown in Fig. 25, where it can be seen that the error signal sign and the sign of the current in the coupling branch give as a result logic levels, then the multiplication is trivial and is implemented with a Xor logic gate, as shown in (19).

$$Sgn(e)Sgn(I_S) \Rightarrow Sgn(e) \oplus Sgn(I_S) \tag{19}$$

Another important operation for the system is the integration, which is implemented by means of a charge pump and a filter (Lopez et al., 2009). The current I_{CH} of the pump is directly related with the parameter α, as a consequence, the matching speed is established by this current. Finally, the current dependent voltage source $V_g = H_g I_g$ is implemented with a variable resistance, and its value is controlled by the voltage in the charge pump filter.

4.3 Proposed test vehicle

As stated before the mathematical representation of the system to be implemented is that shown in equation (20).

$$\rho(t) = \beta \int_{-\infty}^{t} Sgn\left(\frac{1}{2} I_S(u) - I_g(u)\right) Sgn(I_g(u)) du \tag{20}$$

Even though equation (20) is expressed in terms of branch currents, it is difficult to achieve a practical implementation for it. This is due to the fact that sensing a branch current is more complicated than sensing a node voltage. Therefore in the proposed implementation shown in Fig. 26, the inputs to the calibration circuit are voltages. The core of the scheme is the unipolar current mode differential driver (Dally & Poulton, 1998). This driver sinks the current I_S from its outputs depending on the logic state of its inputs Dat and $\overline{Dat}$. The terminators Z_g are programmable resistors that can be analog programmed via V_{CTRL} to match the interconnection impedance Z_0. The voltage reference V_{REF} is generated by sinking

a current $\frac{I_S}{2}$ from a replica of the programmable resistance Z_g. The voltages V_{Out} of the driver and V_{REF} are the inputs for the impedance calibration circuit. This circuit generates the control voltage V_{CTRL} by implementing equation (20).

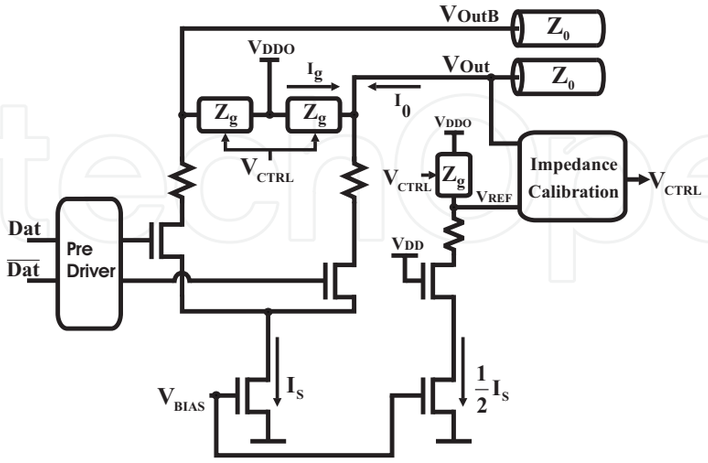


Fig. 26. Proposed Implementation.

By analyzing Fig. 26 one can find that the output voltage V_{Out} and the reference voltage V_{REF} are those described by equations (21) and (22), respectively.

$$V_{Out} = V_{DD0} - I_g Z_g. \tag{21}$$

$$V_{REF} = V_{DD0} - \frac{I_s}{2} Z_g. \tag{22}$$

Using equations (21) and (22) we can define the voltage mode error as follows:

$$e_V = V_{Out} - V_{REF} = Z_g \left(\frac{I_S}{2} - I_g \right). \tag{23}$$

Also, by assuming that $Z_g > 0$, it is inferred that the sign of the errors in voltage and in current mode are the same, this can be verified by equation (24), moreover, the function $Sgn(I_g)$ can be calculated directly from the input to the driver Dat. Consequently this shows that measuring voltages instead of currents is a good option to implement the SS-LMS technique without affecting the operation of the driver.

$$Sgn \left(\frac{I_S}{2} - I_g \right) = Sgn \left(Z_g \left(\frac{I_S}{2} - I_g \right) \right) \tag{24}$$

A print of the Mentor Graphics screen of the layout of the system is shown in Fig. 27 and it was designed in the $0.35\mu m$ C35B4C3 AMS technology. The circuit enclosed by the dashed line corresponds to the current mode driver, the pre-driver, the programmable resistors and the voltage reference circuit. The SS-LMS based impedance matching algorithm is shown outside the dashed line.

In order to verify the performance of the impedance calibration circuit, the system was simulated with post layout extractions using Mentor Graphics tools. To test the circuit, different resistive loads (45Ω, 50Ω and 55Ω) were attached to the circuit. The signal rate

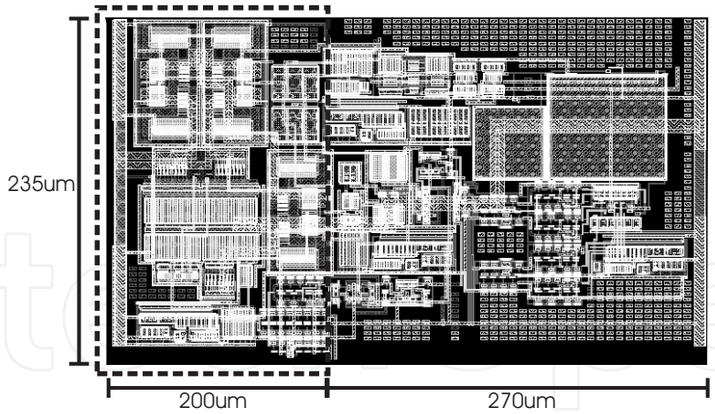


Fig. 27. System Layout.

of the data inputs to the system Dat and $\overline{Dat}$ is $1Gb/s$ and clock frequency for the impedance calibration circuit is established at $300MHz$.

In Fig. 28 the time domain signals for the output and the reference signal are shown. In this case, the load impedance for the system is set to 50Ω. As can be seen, the system adapts after some time.

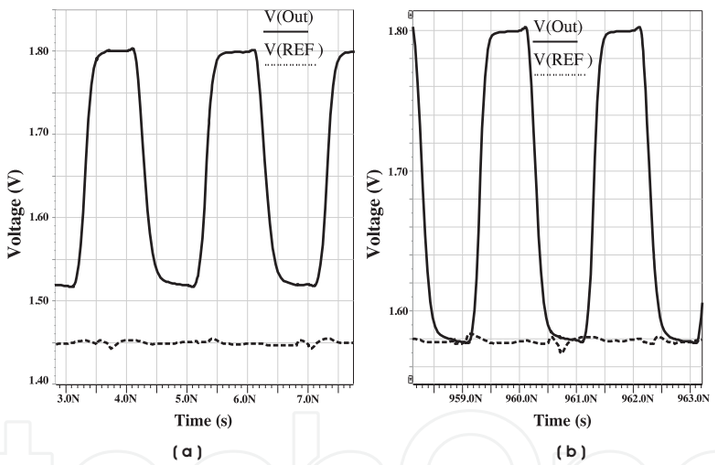


Fig. 28. Time domain analysis, (a) before and (b) after adaptation.

In Fig. 29, learning curves are shown for the 50Ω load impedance case (Fig. 29a) and for 45Ω and 55Ω (Fig. 29b). Those curves are normalized error signals in dB as a function of time and the adaptation time can be seen on them.

The last post layout simulations deal with worst case power and speed scenarios as well as temperature. The Mentor Graphics kit is used to perform this task. Only worst power and speed cases are presented because they result in the poorest performance compared with the others. Figs. 30a, Fig. 30b and Fig. 30c show the simulation results for worst power, worst speed and temperature variations (100 degree Celsius) respectively. As can be observed in the figure, the error always converges to a level bellow the $-30dB$.

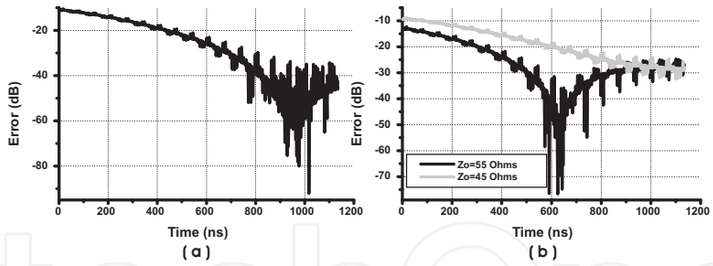


Fig. 29. Error for (a) 50 Ohms and (b) 45 and 55 Ohms loads.

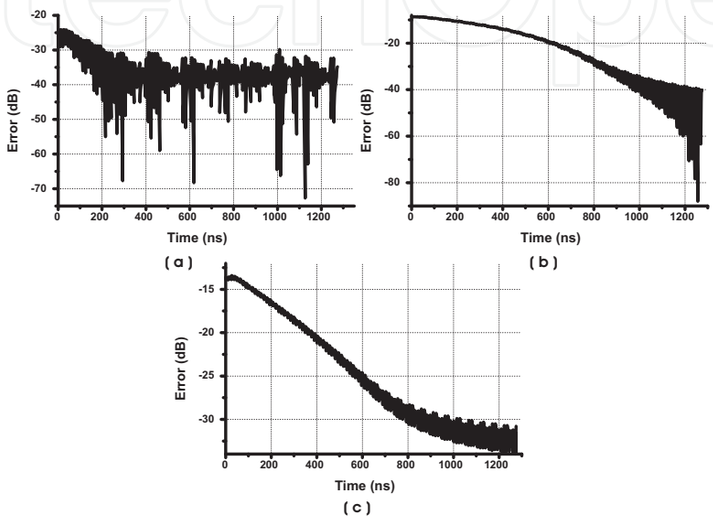


Fig. 30. Error in the (a) worst power, (b) worst speed and (c) temperature variation cases.

5. Knowledge-based impedace matching control design

Formulation of a complete mathematical model for impedance mismatch is a very complex process, since the parameters involved depend on many factors like process variations, length variations of the interconnection lines, temperature, etc. In this sense, knowledge based algorithms represent interesting alternatives which can be explored when looking for solutions to the impedance mismatch problem using adaptive schemes.

Fuzzy logic formalizes the treatment of vague knowledge, and approximates reasoning through inference rules (Zadeh, L. 1999). It establishes the mechanisms to generate practical solutions to problems where traditional methods, which may require precise mathematical models, may not be suitable. Because of this, fuzzy control represents a good alternative to solve the impedance mismatch problem through on-chip adaptive mechanisms (Arroyo et al., 2009).

Fig. 31 shows the general structure of the fuzzy controller used to adapt the system. The structure is simple and was designed in UMC 90nm CMOS technology. The membership functions are implemeted using differential pairs, while the multipliers are four-quadrant multipliers. The controller was designed to work in current-mode, therefore the sum operation is simply the sum of the currents in a node. Since the implementation of the divisor circuit is not trivial, a normalizer circuit can be used as an alternative.

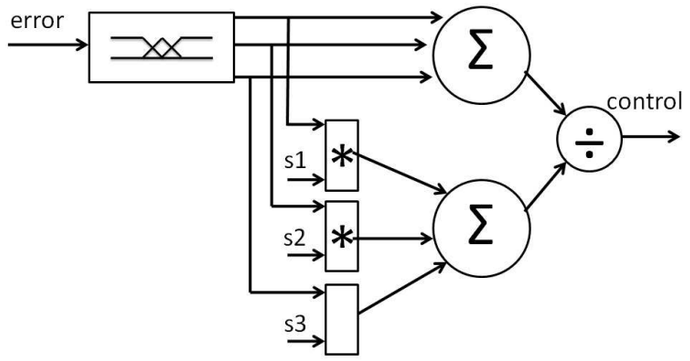


Fig. 31. General structure of the fuzzy controller

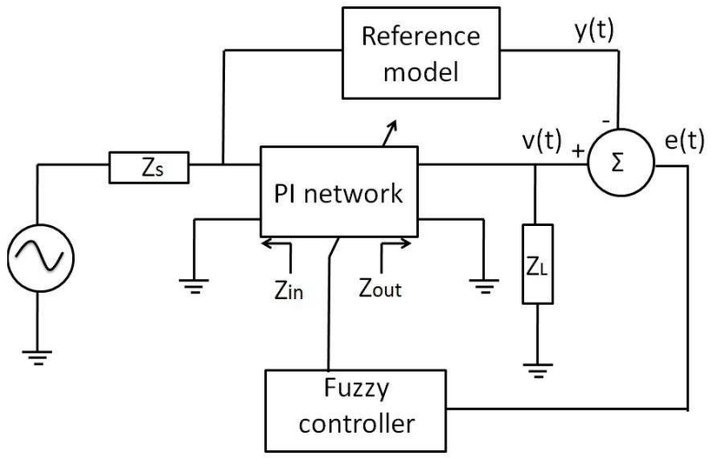


Fig. 32. Impedance matching system

Fig. 32 depicts a block diagram of the fuzzy control-based scheme for the impedance matching system. In order to allow the impedance matching process, a two port network with a standard π configuration is inserted between the source and the load. It is considered that both, the source impedance Z_S and the load impedance Z_L, allow complex values in the general case. The reference model is used to generate the reference signal $y(t)$, which is necessary to obtain the error. The error signal is used as the input to the fuzzy controller and is given by

$$e(t) = v(t)1 - y(t) \tag{25}$$

where $e(t)$ is the error, $v(t)$ is the current output of the system and $y(t)$ is the desired output. The output of the fuzzy controller is used to adaptively change the value of one of the capacitors of the π network. The system iterates until the impedance matching condition given by (2) is fulfilled, i.e.

$$Z_L = Z_{out}^* \tag{26}$$

where $(*)$ denotes the complex conjugate. It is clear that the fulfillment of this condition implies: $e(t) = 0$. Fig. 33 and Fig. 34 show the evolution in time of the absolute value of the adapted impedance and the normalized mean square error, respectively. As can be seen, the

fuzzy controller adapts the impedance matching network, leading the system in every case to match the value of the load impedance.

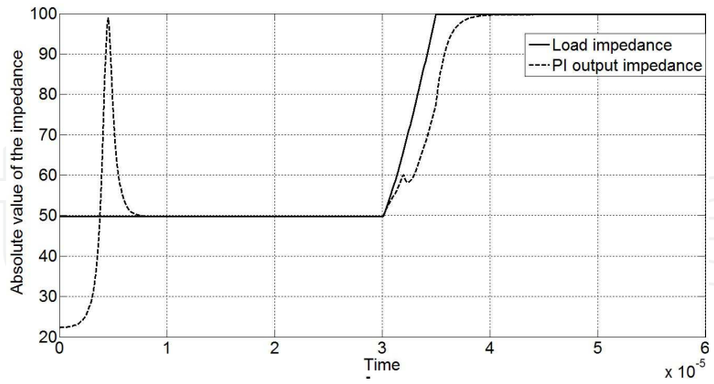


Fig. 33. Adaptation process of the impedance matching system

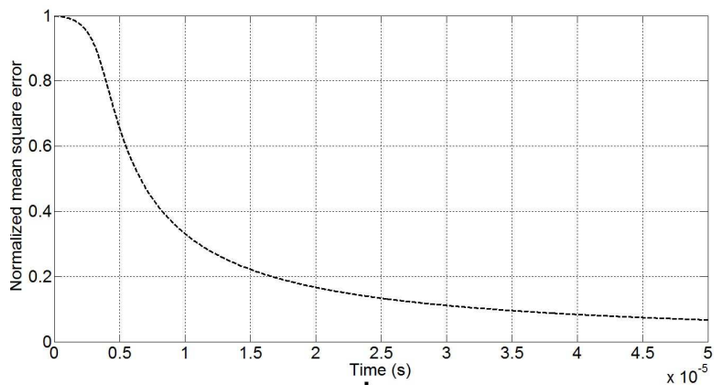


Fig. 34. Normalized mean square error

6. Conclusion

In this chapter systems for on-die automatic impedance matching for off-chip signaling were described. A review of different techniques for impedance matching was presented. Based on that, two algorithms were proposed and implemented in order to perform the automatic impedance matching control: the first one is based on the integration of the sign of the impedance matching error and the sign of the coupling branch current, the second one uses a fuzzy controller in the feedback path in order to adapt the impedance of the matching network. Advantages and performance of these algorithms were discussed and proved by presenting computer simulations of layout extractions.

7. References

Dally W. J. & Poulton J. W. (1998). *Digital Systems Engineering*, Cambridge University Press.

Juan F. (2007). *CMOS Current-Mode Circuits for Data Communications*, Springer.

DeHon A. et. al (1993). Automatic impedance control, *IEEE International Conference on Solid State Circuits*, pp. 164 - 165, Feb. 1993.

Ramachandran N. et. al. (2003), A 3.3-v cmos adaptive analog video line driver with low distortion performance, *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 1051 - 1058.

Deutschmann B. & Ostermann T. (2003). Cmos output drivers with reduced ground bounce and electromagnetic emission, *Proceedings of the 29th European Solid - State Circuits Conference, 2003*, ESSCIRC 03, pp. 537 - 540.

Svensson C. & Yuan J. (1991). High speed cmos chip to chip communication circuit, *IEEE International Sympoisum on Circuits and Systems*, vol. 4, pp. 2228 - 2231, June 1991.

Choy C. S. et. al. (1997). A low power-noise output driver with an adaptive characteristic applicable to a wide range of loading conditions, *IEEE Journal of Solid-State Circuits*, vol. 32, no. 6, pp. 913 - 917, June 1997.

Shin S. K. et. al. (2005). A slew rate-controlled output driver having a constant transition time over the variations of process, voltage and temperature, *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 231 - 234.

Balatsos A. (1998), Clock buffer ic with dynamic impedance matching and skew compensation, *Masters of Applied Science Thesis*, Toronto, Canada.

Carusone A. et. al. (2001). Differential signaling with a reduced number of signal paths, *IEEE Transactions on Circuits, and Systems II*, vol. 48, no. 3, pp. 294 - 300, Mar. 2001.

Wang T. & Yuan F. (2007), A new current-mode incremental signaling scheme with applications to gb/s parallel links, *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 2, pp. 255 - 267, Feb. 2007.

Young B. (2001). *Digital Signal Integrity Modeling and Simulation with Interconnects and Packages*, Prentice Hall PTR.

Brooks D. (2003), *Signal Integrity Issues and Printed Circuit Board Design*, Prentice Hall PTR.

Koo K. et. al. (2001). A new impedance control circuit for usb2.0 transceiver, *Proceedings of 27th European Solid State Circuits Conference*, pp. 237 - 240, Sept. 2001.

Koo K. et. al. (2006). A versatile i/o with robust impedance calibration for various memory interfaces, *IEEE International Symposium on Circuits and Systems*, pp. 1003 - 1006, May 2006.

Muljono H. et. al. (2003). A 400-mt/s 6.4-gb/s multiprocessor bus interface, *IEEE Journal of Solid-State Circuits*, vol. 38, no. 11, pp. 1846 - 1856, Nov. 2003.

Fan Y. & Smith J. (2003). On-die termination resistors with analog impedance control for standard cmos technology, *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 361 - 364, Feb. 2003.

Tae-Hyoung K. et. al. (2005). A 1.2v multi gb/s/pin memory interface circuits with high linearity and low mismatch, *IEEE International Sympoisum on Circuits and Systems*, vol. 2, pp. 1847 - 1850, May 2005.

Munshi A. et. al. (1994). Adaptive impedance matching, *IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 69 - 72.

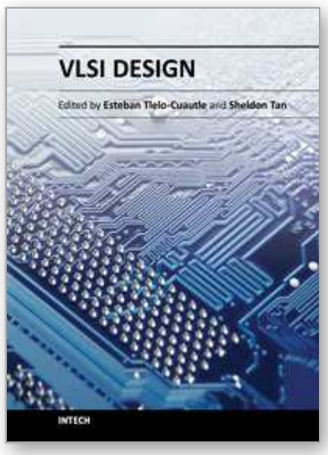
Carusone A. & Johns D. (2000). Analog adaptive filters: Past and present, *IEE Proceedings Circuits, Devices and Systems*, vol. 174, no. 1, pp.82 - 90, Feb. 2000.

Zadeh, L. (1965). *Fuzzy sets*, Information and Control, page numbers (338-353), Academic Press.

Arroyo-Huerta, E.; Díaz Méndez, A.; Ramírez-Cortés, J.M. & Sánchez-García, J.C. (2009). An adaptive impedance matching approach based on fuzzy control, *52nd IEEE Midwest Symposium on Circuits and Systems*, ISBN: 978-1-4244-4479-3, Cancún, México, August 2009.

Thierauf S.(2004). A High-Speed Circuit Board Signal Integrity, *Artech House, Inc.*, 2004

E. Lopez-Delgadillo, J.A. Diaz-Mendez, M.A. Garcia-Andrade, M.E. Magana, F. Maloberti (2009). A Self Tuning System for On-Die Terminators in Current Mode Off-Chip Signaling, *52nd IEEE Midwest Symposium on Circuits and Systems*, Cancún, México, August 2009.



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This book provides some recent advances in design nanometer VLSI chips. The selected topics try to present some open problems and challenges with important topics ranging from design tools, new post-silicon devices, GPU-based parallel computing, emerging 3D integration, and antenna design. The book consists of two parts, with chapters such as: VLSI design for multi-sensor smart systems on a chip, Three-dimensional integrated circuits design for thousand-core processors, Parallel symbolic analysis of large analog circuits on GPU platforms, Algorithms for CAD tools VLSI design, A multilevel memetic algorithm for large SAT-encoded problems, etc.

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