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Double Patterning for Memory ICs

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1. Introduction

In order to continue technology shrink roadmaps and to provide year by year smaller chips with more functionality, nearly all of the leading edge semiconductor companies have adopted double patterning process technologies in their fabrication lines to bridge the time until next generation EUV lithography reaches production maturity. Double patterning technology can be classified into two major main streams, however its implementation and especially the details of the process integration vary strongly among the semiconductor company and every manufacturer found his own optimum.

Therefore the given schemata will focus on the key principles. We will not stress material combinations, but point out particular challenges, show some detailed analyses, and sketch solutions.

2. Double patterning by litho-etch-litho-etch

The most straightforward approach of doing double patterning is splitting a given pattern into two parts by separating neighbouring patterns (see figure 1a). By doing this the minimum pitch of each split will be enlarged and becomes again printable with standard ARF immersion exposure tools. At the first lithography step, a photo mask containing only the blue part of the pattern will be used. As one can easily see from figure 1b, the pitch of blue only pattern is about two times larger than in the original layout. However, in order to achieve a good optical contrast during imaging as well as to get sufficient (photo resist) process window for the patterning, the pattern will usually be biased on the mask as shown in figure 1c.

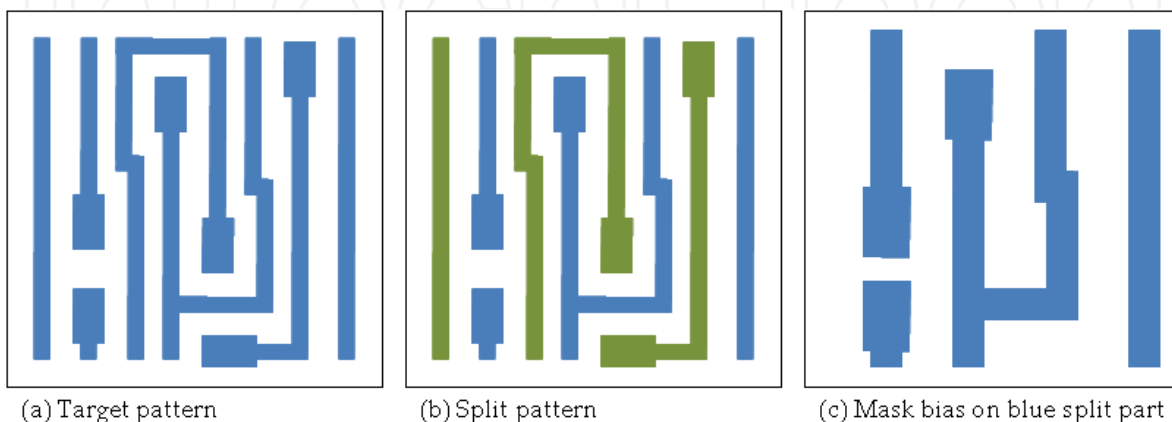


Fig. 1. Example of decomposing an irregular structure for double patterning processing.

Triangular conflicts deserve special attention. They can for instance be solved by using junctions to bridge split part features with each other as shown in figure 2. Another way is to restrict the layout to full splits and to use separate interconnects. Despite the need of such kind of additional rules, LELE can handle complex layout and modern CAD tools do support pitch splitting well.

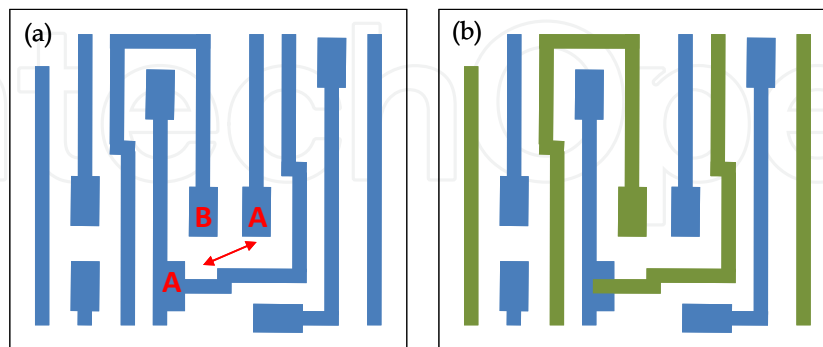


Fig. 2. Topological conflict (a) and a possible decomposition by a junction bridge (b).

To achieve the intended structure dimensions, the applied bias must be removed again. Overexposing the photo resist is commonly used to reduce the bias, but there are limits for process stability reasons. Therefore further bias reduction might be required. Often this will be done in subsequent etch steps, which also have the function of “freezing” the pattern, so that it will not be destroyed when the second part of the pattern will be added. Figure 3 shows a sample sequence.

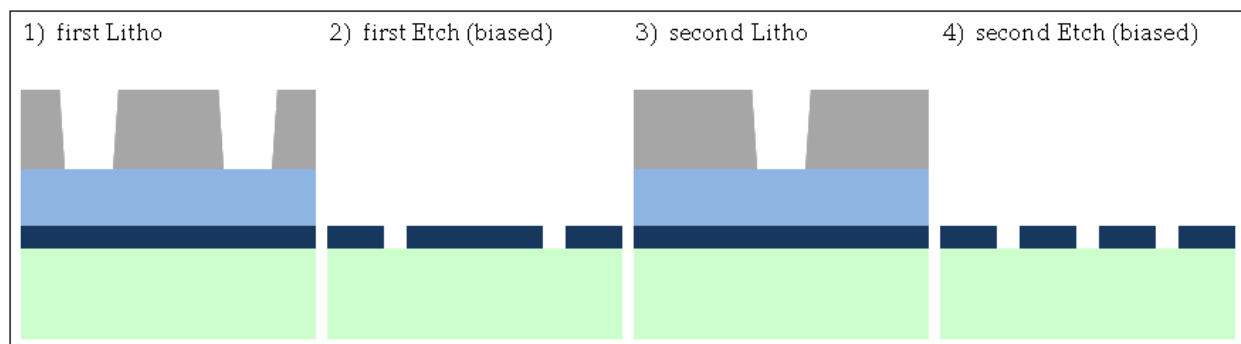


Fig. 3. Process sequence for litho-etch-litho-etch double patterning.

The first pattern freeze is typically done in a thin sacrificial hard mask. Although this thin sacrificial hard mask adds process complexity and thus fabrication cost, there are two good arguments for introducing it. The argument #1 is as follows: It is easier to assemble all pattern elements first within a thin sacrificial layer and later transfer them altogether to the intended layer stack, rather than structuring the full intended layer stack step by step. This is because the intended structures on wafers tend to have large aspect ratios. But once the second lithography gets carried out, the topography of the wafer must be nearly flat. Otherwise resist spin-on gets problematic and one has to struggle with reflective notching and local CD (critical dimension) variation. That means, without using the sacrificial thin hard mask, complex planarization steps would be necessary. However, the thin hard mask topography differences can easily be covered by BARC / bottom layer coatings, which have to be applied for ARF resist systems anyway. The argument #2 is: Hard masks are typically

needed for the plasma etch process of the intended layer stack anyway. The limits of the plasma etch selectivities and the aspect ratios require the usage of sophisticated hard mask stacks. Etching a complex stack twice is also more costly than doing the double patterning etch sequences only on the thin hard mask and perform the complex and expensive full stack etch only once. Last for the sake of completeness we want to mention here, that for cost and complexity reasons techniques of freezing the first split pattern directly in photo resist system are showing up in the industry.

Splitting the given pattern into two parts allows complex designs. Therefore this type of double patterning is the preferred choice for logic manufactures. But since two lithography steps must be done to achieve the patterning for one layer, the intra-layer overlay must be controlled with a very high degree of precision. This was challenging in the past, because first and second generation ARF immersion tools could hardly achieve overlay control beyond 6-8nm, which is above the needed budget for 36nm...32nm and 28nm...24nm technologies. Around 2010, lithography tool makers removed this blocking point by introducing a third generation of ARF immersion tools with can meet double patterning overlay control requirements. This double patterning technique is usually referenced with Litho-Etch-Litho-Etch (LELE) but other names such as Brute Force or Pitch Splitting exist as well.

For the extremely regular arrays of memory chips like e.g. NAND flash memories, aggressive double patterning technology nodes have been introduced already in 2008, before exposure tools with improved overlay control became available. Memory chip manufacturers have therefore driven another double patterning main stream, which we will describe in the next paragraph.

3. Self aligned double patterning

The second main stream is often called self aligned double patterning. Some people call this technique pitch fragmentation and you might often hear spacer based double patterning, because for most of this techniques spacer-like approaches are used to double the number of features.

Self aligned double patterning comes with strong layout limitations. However, it is well suited for regular patterns e.g. of memory chips. The design process is more complex than LELE and the pattern on the photo masks look different compared to the final pattern. This creates a first challenge, because layout versus schematic checks require additional CAD tooling to transform the self aligned double patterning mask data into the final layout data. The transformation in the other direction - from final layout to double patterning layout - is even more challenging. Automated tools are rare and manual interaction of the designers is required. This is limiting the application to a manageable number of layout features and is the main reason why self aligned double patterning is mostly only used by memory manufactures.

The big advantage of self aligned double patterning is that only one main feature lithography step has to be done. However, one or two additional assist lithography steps with considerably reduced resolution requirements are used to form the edges of the regular pattern within the memory array as well as the transition from the regular array towards the remaining area of the chip, containing the control function elements of the memory.

The lithography tool overlay requirement is only driven by the inter-layer technology demands and not by the intra-layer alignment as for LELE.

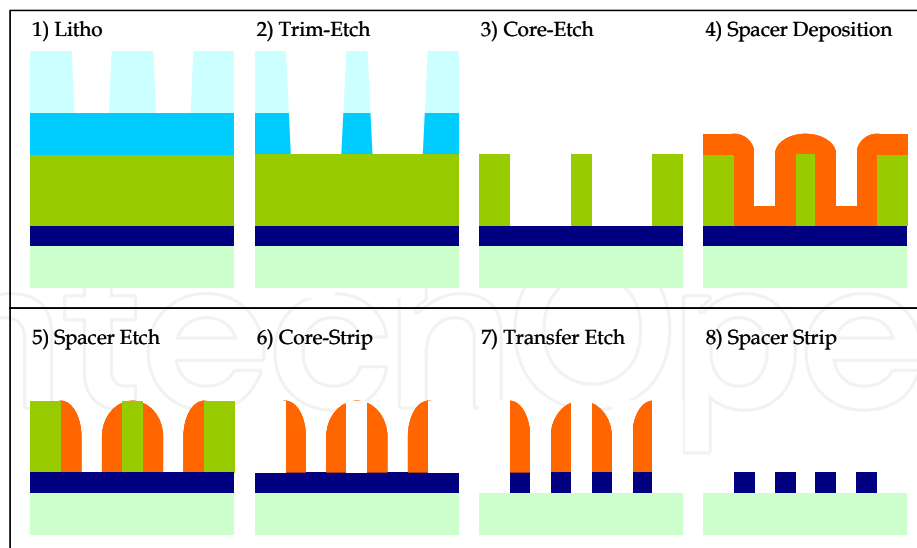


Fig. 4. Sketch of a process sequence for “line by space” double patterning.

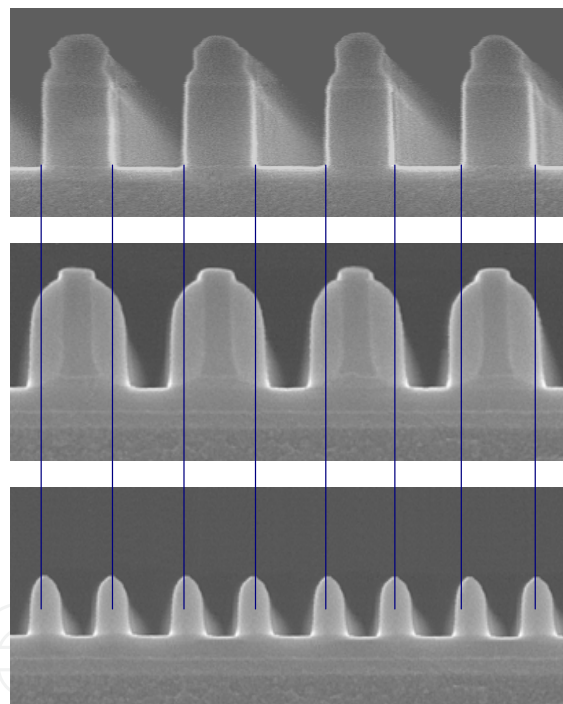


Fig. 5. Example of a process sequence “line by spacer”: The SEM cross section at the top reveals the primary line pattern as defined by lithography, after print and dry etch. The cross section in the middle shows the primary lines now covered by (sacrificial) spacers, after spacer deposition and spacer etch. The bottom picture is taken after removal of the primary lines. The sacrificial spacers have become now a regular pattern of twice the spatial frequency compared to the primary pattern, and can be further used as a hard mask for the subsequent patterning of the desired stacks.

With the main lithography step, a so called “primary” or “core” pattern is printed on the wafer. This pattern has a pitch twice as large as the final structures and gets usually biased for process window reasons. Out of this pattern, a tall rectangular-shaped core structure

with an aspect ratio of typical 1:3 to 1:5 is formed. This can be done directly in the photo resist system, or - more common - can be transferred by reactive ion etch into a relative thick underlying hard mask. Afterwards a thin conformal liner will be deposited onto the core shape. Now a spacer etch is performed and the core pattern gets stripped out. Finally the spacer structures will be transferred into another under laying thin hard mask and the spacer will be taken off as well. Figure 4 and 5 show such a process sequence. A detailed process description including key process parameters is listed in table 1. For this sequence the final line structure width is defined by the deposited thickness of the sacrificial spacer. Therefore this scheme is called "line by space" (LBS). All created lines will have the width of the sacrificial spacer. There is no degree of freedom for the chip layouter to modify the line width. Only the space between the lines can be varied by layout.

Process Step	Target
Deposition of CVD carbon hard mask	150nm (should to be adjusted to layer requirement)
Anneal carbon	630°C, 60min
Deposition of CVD multi-layer stack (double patterning hard mask)	25nm SiON + 25nm a-Si + 35nm SiON + 150nm a-Si + 20nm TEOS (from bottom to top)
Litho 193nm immersion	72nm line / 72 nm space CD uniformity < 3nm
Trim etch of poly mask	~ 42nm line CD uniformity < 2nm taper within the array: 90 deg
Strip Resist	
Clean Wet	minimum attack of SiON
Etch Wet TEOS	high selectivity, minimum attack of SiON
Deposition CVD HARP liner	36nm thickness thickness uniformity < 0,5nm
Etch Spacer Oxide	
Etch Recess Poly	complete carrier a-Si removal
Etch Plasma SiON	spacer transfer etch, stop on a-Si
Etch Wet Oxide	remove space; minimum attack of SiON
Subtractive Patterning	etch SiON selective to a-Si
Additive Patterning	etch aSi with SiON and resist mask with stop on SiON

Table 1. Process Sequence for Spacer Transfer Scheme (LBS) with process targets for the gate layer in a 36nm NAND flash chip.

Some applications however require lines with well-defined different line widths, but can accept equal spaces. This can be realized by a slight modification of the described processing sequence: filling the pattern after the spacer etch followed by a controlled recess etch and spacer material strip. Figure 6 demonstrates an example for a process flow which is called "line by fill" (LBF).

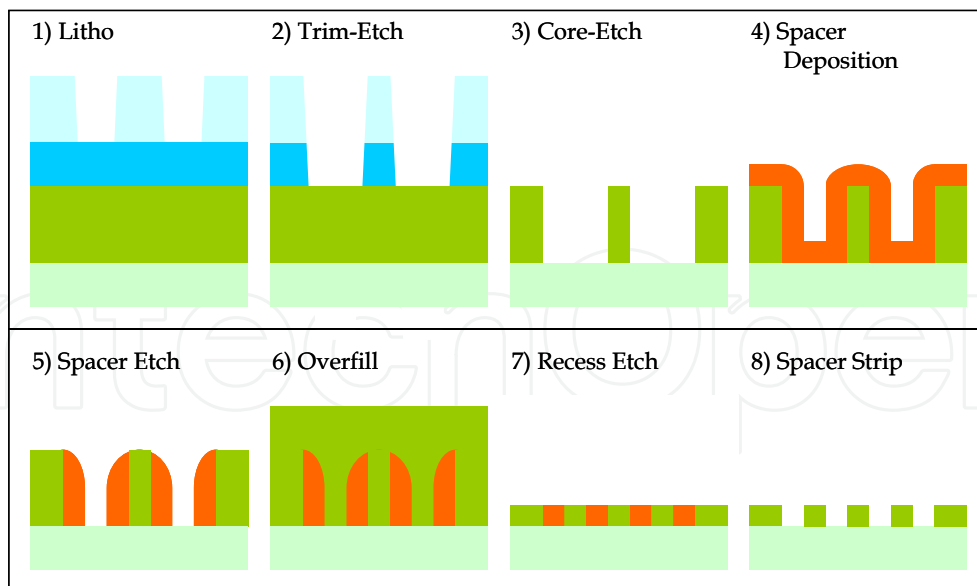


Fig. 6. Sketch of a process scheme for “line by fill” double patterning.

3.1 Line by space (LBS) – Line by fill (LBF)

The decision for either of the two basic self-aligned double patterning schemes LBS or LBF has to be taken for each lithography layer individually. In general, LBS is advantageous if the tolerances in line width are most critical for the electrical functionality of the product, and LBF is the preferred option if the distance between the lines are most critical for the product functionality. Figure 7 illustrates this difference. Therefore, sound knowledge of the fabrication process tolerances and thorough simulation are mandatory.

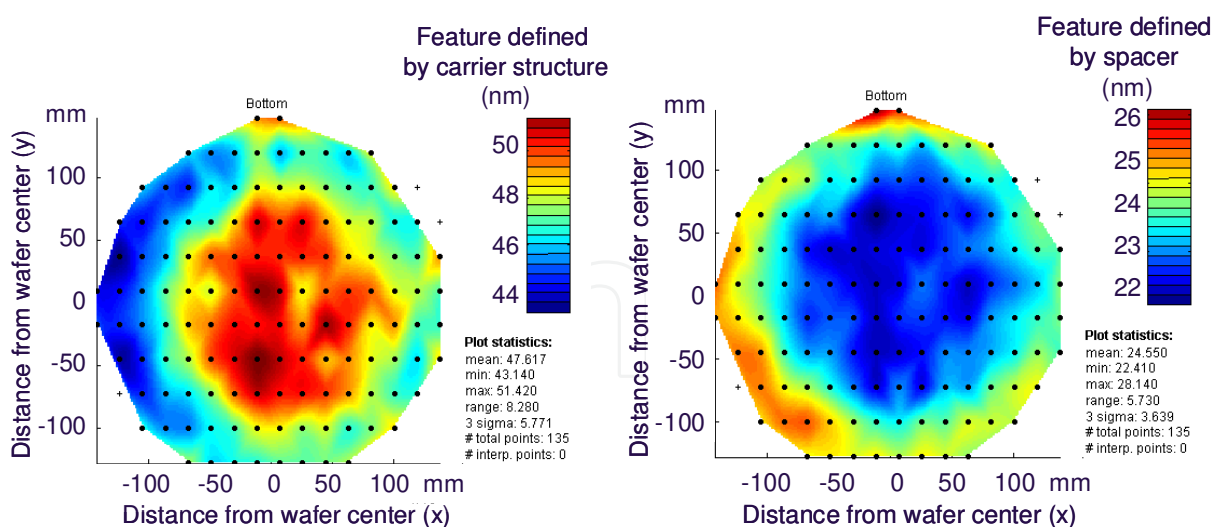


Fig. 7. Critical dimension of the gate hard mask, measured across the full wafer. The left hand graph shows the hard mask spaces, the “space-1”, being defined by the primary line, whereas the right hand graph represents the hard mask “lines”, being formed by the sacrificial spacers. The hardmask lines show a much smaller spread in width than the hard mask spaces. Note that the hardmask lines are narrower than the intended gates: this is to compensate for the gate etch bias.

3.1.1 Process tolerances

One of the biggest challenges for self aligned double patterning is the control of the critical dimensions. Compared to the traditional litho, when CD control was more or less managed by lithography, self aligned double patterning relies also on tight process control for etch and deposition processes. For the example sequence sketched in figure 4, the line width is defined by the thickness of the deposited (spacer) liner and the subsequent spacer etch. Extremely low process variations, exact reproducibility, uniformity are mandatory. Therefore, special care has to be dedicated to the search of well controlled deposition processes with reasonable process cost.

The first process choice for a well-controlled deposition process could be LPCVD. However, most of the LPCVD furnace processes require process temperatures above 500°C. Front-end application might allow such temperatures, but in the back-end of line such high temperature would destroy the already manufactured metal lines or contact junctions. Therefore, LPCVD cannot be applied to critical metal layers.

PECVD processes can run at lower temperatures and come with acceptable cost. However, still most of the PECVD deposition processes are not suitable for spacer based double patterning, because the deposition mechanism is transport limited. In other words: the new material deposition reaction is very fast and is limited by how fast and how much new material can be transported out of the plasma to the wafer. The “stream” of new material is limited in time and will be distributed over the wafer surface. As a consequence the thickness of the deposited liner will vary with the surface area. Therefore dense structure areas with larger surface will see thinner liner thicknesses compared to isolated structures. Unfortunately this so-called micro-loading has quite some range and will create dozens of array edge line with different line width. As a result, PECVD processes cannot deliver tight in-chip CD control.

A highly promising process candidate is atomic layer deposition (ALD). They come with extreme good thickness uniformity and can be done at very low temperatures. The first ALD processes had the drawback of a relatively slow process speed, resulting in high process cost. However, the original ALD with its slow atom-by-atom like deposition has experienced considerable improvements. Nowadays modified ALD processes are available like e.g. catalytic (fast) ALD, spatial ALD, molecular layer depositions or pulsed plasma depositions. Some of these advanced deposition processes can be done at temperature around or even below 100°C. This enables spacer liner depositions directly on photo resist type core materials.

The liner thickness variations are not the only critical parameter. Also for other process steps, the control of critical dimensions is challenging. The CD variation of the “primary” or “core” space results from both litho and core-etch non-uniformity. The line width variation depends on spacer deposition and etch uniformity. The “secondary” or remaining space in principle will suffer from the sum of both variations. In order to keep the “secondary” or remaining space within the allowed technology variation specifications, one has either to run each process with very tight specifications or to implement an advanced feedforward / feedback APC system. Such a system is capable e.g. of tuning the etch-bias as a function of the photo resist CD after the lithography patterning.

The uniformity of the line width is affected by the topography of the environment. There are both short-range effects and long-range effects. Transport processes and reaction kinetics of chemical and plasma reactions are sensitive to the effective surface in the vicinity of a considered line as well as to the macroscopic location on the wafer. In addition to the structure dimension of interest, monitoring structures need to be developed for a fast and reliable monitoring of the mass production.

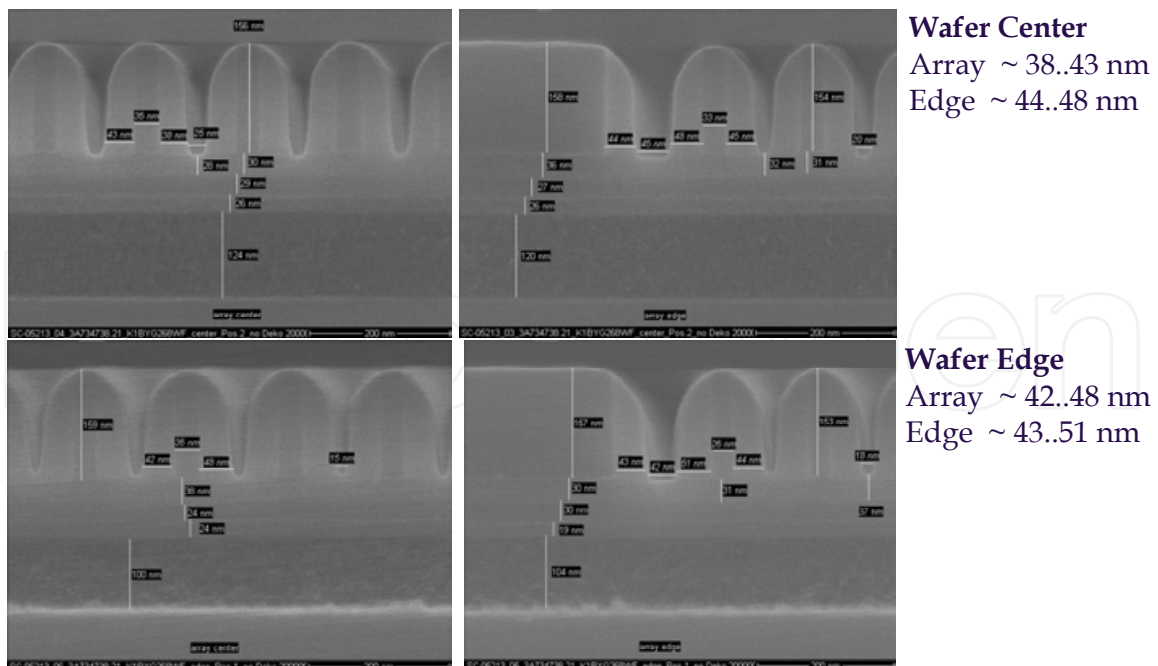


Fig. 8. Micro loading in the double patterning hard mask for the gate level of a 36nm NAND Flash. The hard mask is made for the line by space (LBS) scheme.

We have selected the gate layer of a 36nm flash memory as an example of micro loading. Figure 8 shows measurements taken from cross-sections after the formation of the sacrificial spacer at the sides of the primary lines. The hard mask is not yet structured. An in-line measurement at this process step will reveal the sum of the width of the primary line plus two adjacent spacer thicknesses, equalling roughly the desired line with plus two spaces. An intuitive way of plotting this in-line measurement number is shown in Figure 9.

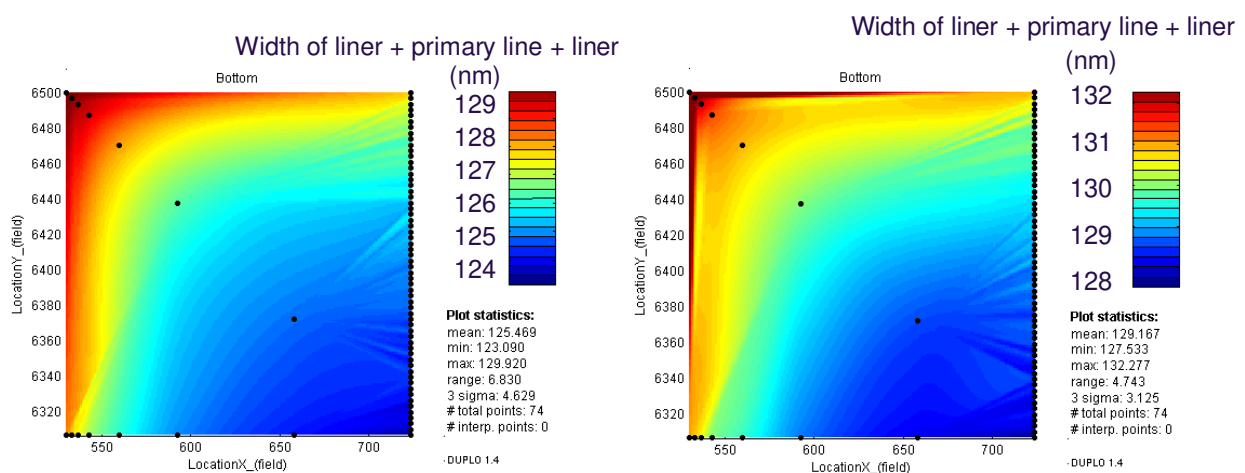


Fig. 9. Plot of the in-line measured line width consisting of the primarily formed line plus two adjacent spacers. The coloured area represents a quarter of the regular gate array. The center of the array is located at the bottom right of the plot, the corner of the array corresponds to the top left corner of the plot. Obviously, the line width increases from the center of the array towards the corners. The right hand graph was taken from an improved spacer deposition process, showing a narrower width distribution.

After removing the primary lines and transforming the sacrificial spacers into the hard mask, one obtains values as given in Table 2.

Wafer Uniformity Center to Edge	3nm
Micro Loading Array to Select Gate Edge	2..3nm
Micro Loading Gate Array Edge	6..10nm
Micro Loading Array to Litho Monitor (nested)	10nm
Micro Loading Array to Litho Monitor (isolated)	17nm

Table 2. Experimental data for uniformity and micro loading and uniformity of the the gate layer of a 36nm NAND flash patterned by LBS.

3.1.2 Gate

In general, the gate length is critical, requiring LBS (line by spacer) for the gate level. Typical electrical parameters of relevance are:

- Narrow distribution of IV characteristics of the transistors, mainly for:
- Large on-currents: short gates are preferable
- Source-Drain leakage: long gates are preferable
- Hot carrier effects: long gates are preferable

In the case of a flash memory, another electrical parameter comes into play: the coupling ratio, which determines mainly the programming and erase characteristics of the flash transistors. The coupling ratio is affected by the capacitance between the floating gate and the active area, i.e. the CD variations of both the (floating) gate and the active area cause a spread in programming and erase performance.

As a result, a carefully controlled balance of the gate length in all kinds of chips is more important than the control of the gate spaces.

3.1.3 Active area / STI

For the active area, the following elements are relevant:

- Transistor on-current: active area width variations translate directly into transistor current variations.
- Coupling ratio of flash transistors: active area width variations translate into the program and erase speed.
- Transistor leakage: The STI (shallow trench isolation) fill turns out to be highly sensitive to the STI trench width. Trap centers at the boundary of transistor channel edge and STI fill can result in undesired leakage currents, both along the channel direction and across the source/drain junction into the substrate.

The balance of the mentioned three arguments led the authors to the decision of LBF (line by fill) for the active area layer.

3.1.4 Bit line contact

NAND-Flash memory arrays require single rows of so called dense bit line contacts. They connect the metal bit lines to the active area, and they are following the critical pitch. The special challenge consists in the lack of any room for overlay tolerances and in the extreme asymmetry of the pattern: the contact row can be considered an isolated structure in one dimension, and in the orthogonal dimension a periodic structure with minimum pitch.

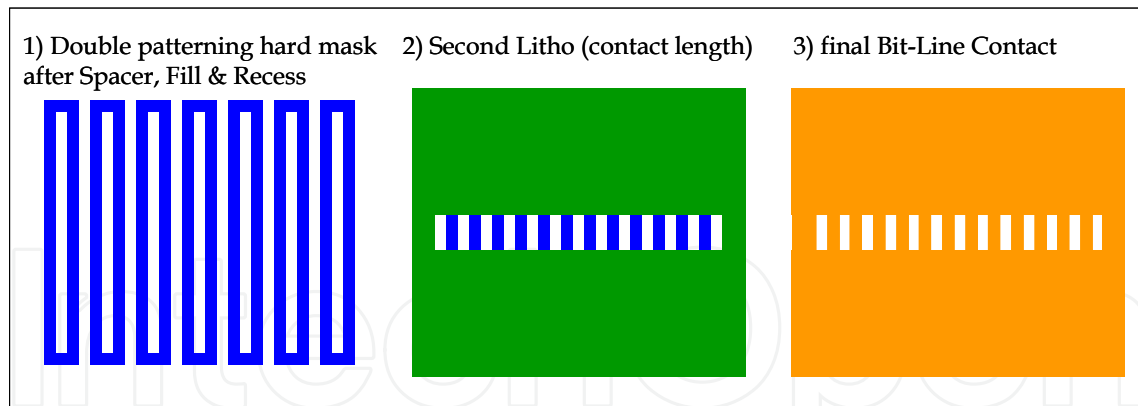


Fig. 10. A two-mask process for the formation of a single row of on-pitch contacts.

Figure 10 shows one example how to realize elongated dense bit line contacts. In a first step a dense array-like hard mask is created by double patterning. The lines and spaces of this array-like hard mask define the bit line contact widths and the contact to contact distances, respectively. The array is much larger than the intended contacts in order to reach a good imaging in the lithography tool. A second lithography layer is used to cut out only a small region of the array-like hard mask. This second litho step prints a long opening in a resist mask across the array-like hard mask. The width of this long opening defines the length of the contacts. The following etch process is to open only the regions which are neither covered by the spacer nor by the photo resist.

3.1.5 Tight pitch metal layer

The predominant issues for the selection of the proper double patterning scheme for metallization are

- dielectric breakthrough,
- variations of capacitive coupling,
- variations of resistance,
- feasibility of landing pads for contacts / vias for the electrical connection to layers beyond or beneath.

Typically, bit lines are supposed to run fast electrical signal pulses with lowest possible loss and lowest possible cross-talk. This requirement suggests that a lower limit of the metal space might be important in order to minimize RC losses. Simulations have been performed for the bit line capacitance in a flash memory for both the LBF (line by fill) and the LBS (line by space) process scheme. The results led to the conclusion that both LBS and LBF show nearly identical variations with respect to the capacitive coupling between adjacent bit lines. The resistivity variations, however, are clearly in favour of the LBS scheme, which has a well controlled metal line width, i.e. the resistance tolerances are much better than for LBF. But in the end, deeper study of process architecture and complexity and cost led to the decision of LBF.

Two-dimensional electric field and capacitance simulations have been performed for LBF (figure 11) and LBS. The calculations include fringing fields for up the third neighbour bit line as well as the capacitance to the top and bottom layers of the chip. Worst and best cases, i.e. largest and lowest capacities have been calculated. For the variations, not only the double patterning induced line and space variations have been considered, but also variations in bit line thickness. The target thickness of the considered example is 60nm for the full metal stack, the tolerance is +/- 10nm.

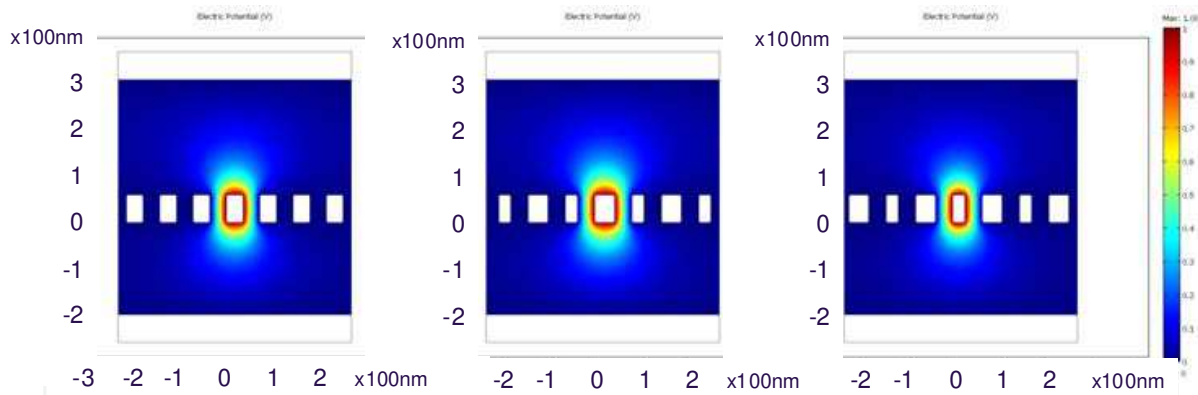


Fig. 11. Electric field simulations for bit line capacitance calculations, depicted for the LBF process.

It is not upfront clear by intuition, which combination of double patterning variations will result in the largest and lowest bit line capacitance, respectively. For example, in the LBS scheme, the smallest bit line capacitance does not occur for the largest primary space. The reason is the linear (inter-)dependence of the four parameters: The sum of two spaces and two lines is fixed to twice the pitch, 144 nm in our example. An illustration of the line / space variations towards lower capacitances is given in figure 12. The lowest possible value for LBS (3 sigma geometrical variations assumed) is $2,01 \times 10^{-10}$ F/m, which is 10% below the value of the target geometry ($2,23 \times 10^{-10}$ F/m).

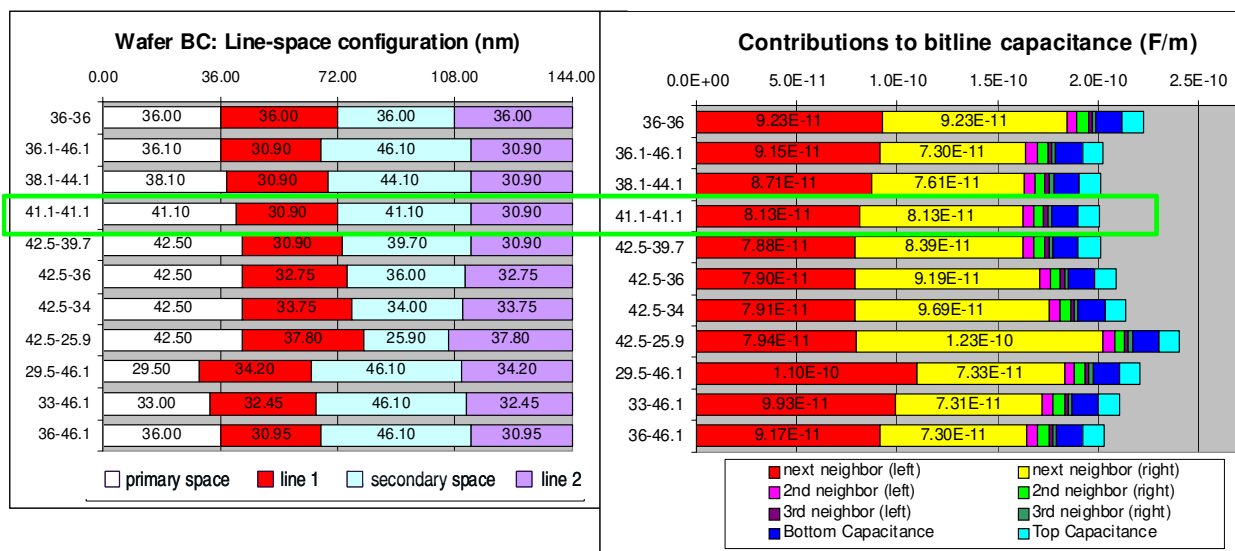


Fig. 12. Bit line capacitance for various extreme geometry parameters in the LBS scheme, for lowest capacitances from process variations (“best case”). A totally symmetric configuration of 41.1 nm for both the primary and the secondary space and a line width of 30.9 nm is found to be the best case, resulting in a total capacitance of $2,01 \times 10^{-10}$ F/m.

A summary of the results is depicted in figure 13 and listed in table 3. The outcome of the considerations is a tiny preference for the LBS scheme.

The feasibility of process architecture finally requires a clear decision between the two double patterning schemes. A reliable connection to the bit line contact and a robust process

margin require some kind of so called landing pad, i.e. a local enlargement (landing pad) of the bit line around the bit line contact. This is only feasibly by LBF, since only in the LBF, the layouter can intentionally modify the width of the bit line. The LBS would ascribe the bit lines a well-defined, fixed width.

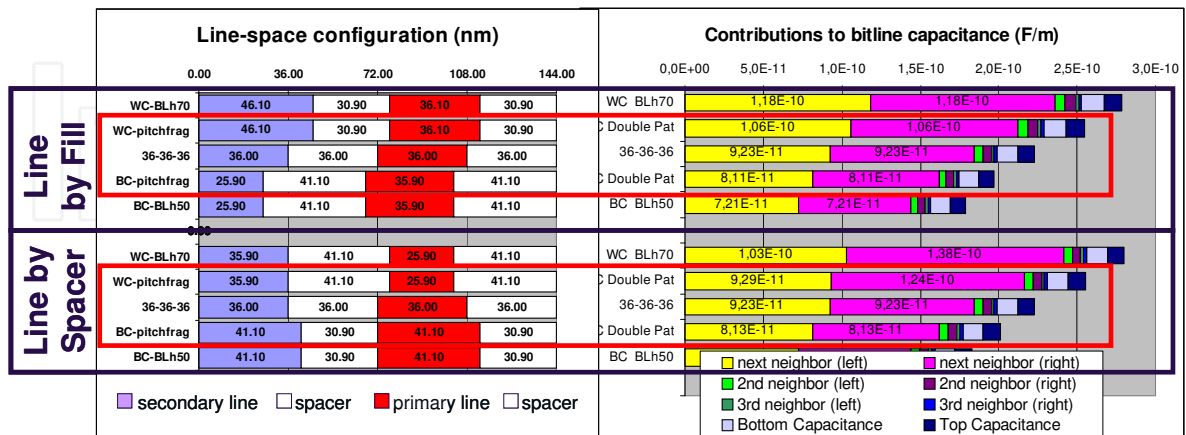


Fig. 13. Bit line capacitance in a 36nm flash M0 layer for the extreme 3 sigma cases of double patterning variations, marked by the red boxes, and in addition bit line height variations of +/- 10nm.

	LBF (10 ⁻¹⁰ F/m)	LBF (%)	LBS (10 ⁻¹⁰ F/m)	LBS (%)
WC incl. BL height (3 σ)	2,61	17	2,61	17
WC (double patt. only) (3 σ)	2,54	14	2,55	14
Target dimension	2,23	0	2,23	0
BC (double patt. only) (3 σ)	1,97	-12	2,01	-10
BC incl. BL height (3 σ)	1,90	-15	1,93	-14

Table 3. Bit line capacitance (numbers absolute and relative to the geometrical target dimensions) for LBF and LBS. All variations represent 3 sigma values. The range between the largest, i.e. worst case (WC) capacitance and the lowest, i.e. best case (BC) capacitance is roughly identical for both double patterning schemes. Besides the pure double patterning effects, the table also considers a calculation of the bit line height variations. Altogether, the two double patterning schemes do not exhibit a significant difference.

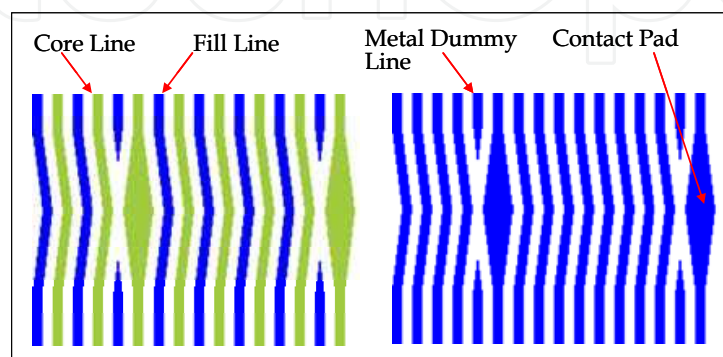


Fig. 14. LBF allows local enlargements of the bit line width.

In an NAND flash, the regular bit line pattern exhibits periodic interruptions which are needed for the source line contacts. This enables the introduction of some dummy extra bit lines. They are used to allow tiny landing pads on top of the bit line contacts. Figure 14 shows an example for bit line landing pads.

3.2 Fan-out

So far, we have focussed our discussion mainly on the regular array. The edge of the array deserves special attention.

Self-aligned double patterning naturally creates lines or spaces which are connected pairwise. In general, this is not desired. Therefore after the array formation by double patterning, the edge of the array is cut by applying a second uncritical litho & etch step, as illustrated in figure 15. Preferably, this step is applied to the hard mask before etching the full stack.

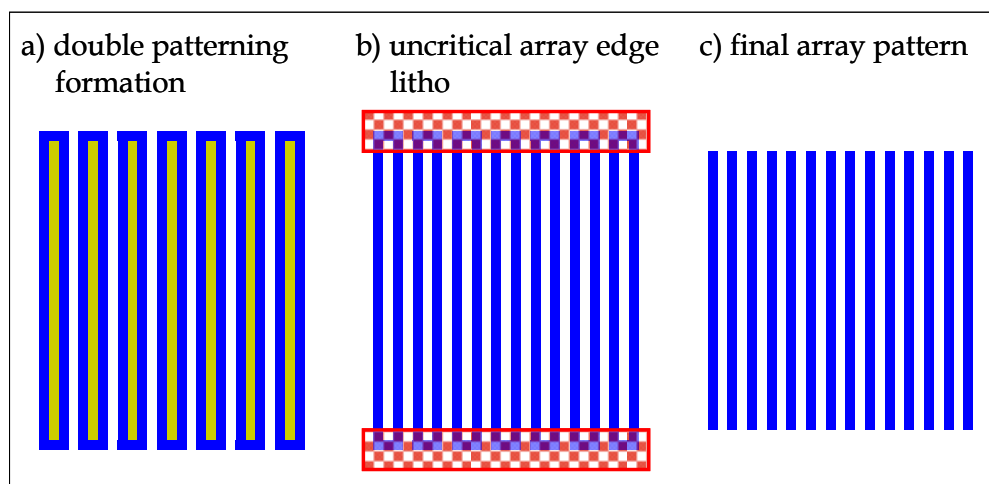


Fig. 15. An uncritical litho & etch step is used to remove the unintended pair-wise connections of the double patterning lines.

The array lines have to be connected electrically to other functional elements on the chip. This requires a so-called fan-out, a topological connection between the double patterning elements and the structures printed by direct lithography.

A possible process sequence of a “Christmas tree” fan-out for the gate layer of a NAND flash is shown in figure 16. The ends of the lines formed by primary lithography are drawn in a shape as depicted in figure 16 (a). The first lithography step prints the primary lines, having twice the array pitch, and forms the fan-out core. The spacer covering the sidewalls of the primary lines follows the core edges and routes each array line into the Christmas tree fan out (figure 16 (b)). The spacer has the intended pitch within the array and is transformed into array lines. They are connected in pairs. Therefore an additional (uncritical) litho & etch cut step must be performed (figure 16 (c)). Finally, landing pads are added for better overall process robustness (figure 16 (d)). The additive structuring requires one more litho & etch, which is usually combined with the periphery patterning. For the additive structuring, the combination of the already formed double patterning hard mask and the add-on photo resist act as an etch mask for the final etch.

A SEM photography of such a “Christmas tree” word line fan-out is given in figure 17.

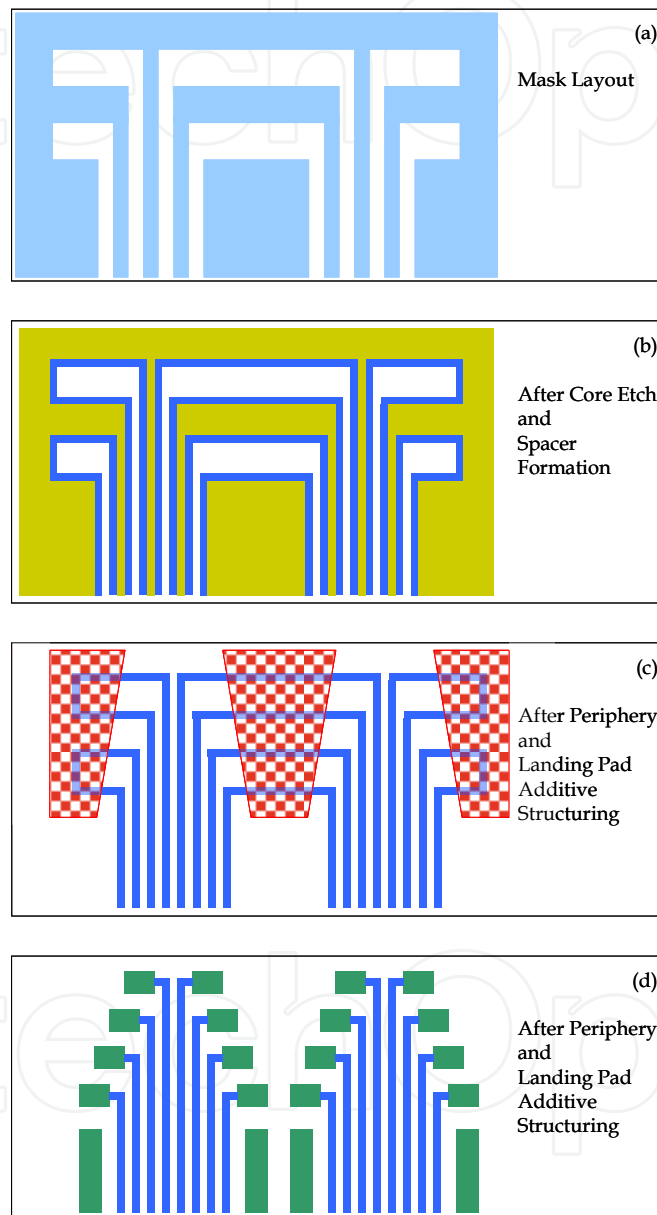


Fig. 16. "Christmas tree" fan-out for the gate layer of a NAND flash.

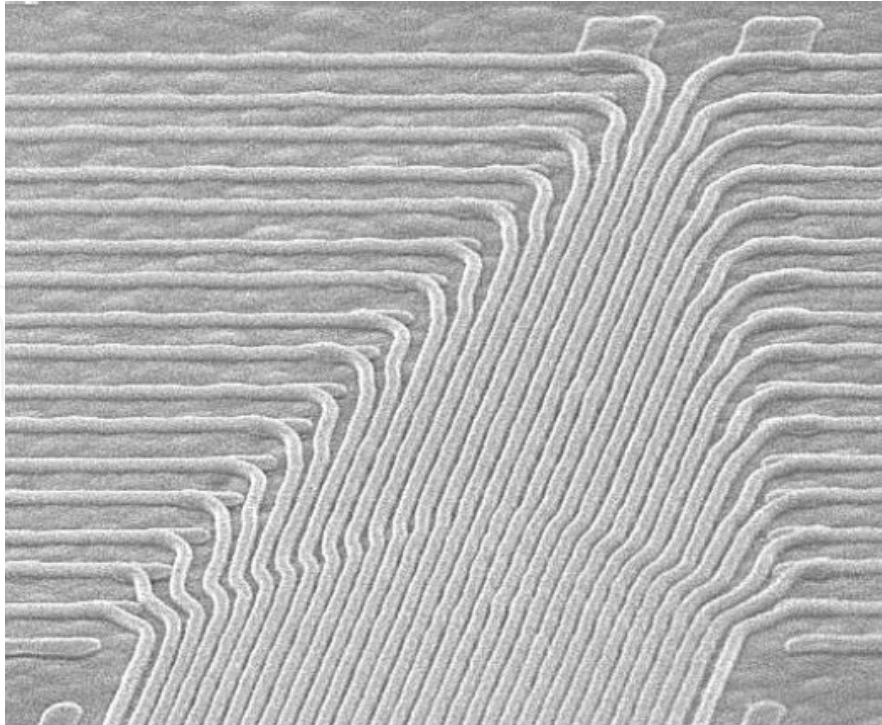


Fig. 17. SEM view of a word line (gate) fan-out for a 36nm half pitch array.

4. Conclusion

Double Patterning has become an important technique for advanced microelectronics devices. Cost-competitive memory chips have structure dimensions which are well below the diffraction limit of any available productive lithography tool. The generation EUV lithography is still on its way towards production maturity.

We have shown a classification of double patterning and have discussed possible implementations. Their specific challenges and advantages have been considered. For a 36nm NAND flash as an example, process flows have been presented.

5. Acknowledgment

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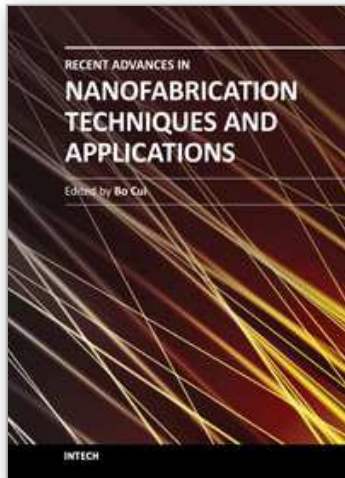
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Nanotechnology has experienced a rapid growth in the past decade, largely owing to the rapid advances in nanofabrication techniques employed to fabricate nano-devices. Nanofabrication can be divided into two categories: "bottom up" approach using chemical synthesis or self assembly, and "top down" approach using nanolithography, thin film deposition and etching techniques. Both topics are covered, though with a focus on the second category. This book contains twenty nine chapters and aims to provide the fundamentals and recent advances of nanofabrication techniques, as well as its device applications. Most chapters focus on in-depth studies of a particular research field, and are thus targeted for researchers, though some chapters focus on the basics of lithographic techniques accessible for upper year undergraduate students. Divided into five parts, this book covers electron beam, focused ion beam, nanoimprint, deep and extreme UV, X-ray, scanning probe, interference, two-photon, and nanosphere lithography.

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