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Cascaded NPC/H-Bridge Inverter with Simplified Control Strategy and Superior Harmonic Suppression

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1. Introduction

In recent decades the electric power systems has suffered significant power quality problems caused by the proliferation of non linear loads, such as arc furnace lighting loads adjustable ac drives etc., which causes a large amount of characteristic harmonics, low power factor and significantly deteriorates the power quality of the distribution system (Benslimane, 2007; Franquelo et. al., 2008; Gupta et al., 2008). The increasing restrictive regulations on power quality have significantly stimulated the development of power quality mitigation equipments. For high power grid connected systems, the classical two level or three level converters topology are insufficient due to the rating limitations imposed by the power semiconductors (Holmes & McGrath, 2001; Koura et al., 2007). Hence considerable attention has been focused on multilevel inverter topologies. This important multilevel technology has found widespread application in medium and high voltage electric drives, renewable energy – grid interface, power conditioning, and power quality application (Lai & Peng, 1996; Peng et al., 1996; Rodriguez et al., 2002; Sinha & Lipo, 1996; Tolbert et al., 1999).

Multilevel converters offer several advantages compared to their conventional counterparts (Manjrekar & Lipo, 1988, 1998, 200; Corzine & Familiant, 2002; Lund et. al., 1999; Sneineh et. al., 2006; Park et. al., 2003; Zhang et al., 2002; Ding et. al., 2004; Duarte et al., 1997; Rojas &. Ohnishi, 1997). By synthesizing the AC output terminal voltage from several voltage levels, staircase waveforms can be produced, which in their turn approach the sinusoidal waveform with low harmonic distortion, thus reducing filters requirements. However the several sources on the DC side of the converter make multilevel technology difficult to control by the need to balance the several DC voltages. For the class of multilevel inverter called diode clamped, if a higher output voltage is required one of the viable methods is to increase the number of inverter voltage levels. For Neutral Point Clamped (NPC) inverter voltage can only be increased up to five level beyond which DC voltage balancing becomes impossible. For single Phase H Bridge inverter, an increase in the number levels leads to increase in the number of separate DC sources, thus the proposed hybrid model is developed by combining the NPC and H- bridge topologies (Wu et al., 1999).

A lot of research has been done on single phase H- Bridge inverter where each inverter level generate three different voltage outputs, $+V_{dc}$, *0*, and $-V_{dc}$ by connecting the dc source to the ac output using different combinations of the four switches of the Bridge (Peng et al., 1996). There has also been more emphasis on modeling and control of a five level NPC/H-bridge inverter without cascading the bridge (Cheng & Wu, 2007). This fails to address the principle of realizing a general cascaded n- level NPC/H-Bridge. It is on this need of realizing a higher voltage output with simplified control algorithm that this book chapter proposes a simplified control strategy for a cascaded NPC/H-bridge inverter with reduced harmonic content. Because of the modularity of the model only two cascaded cells which gives a 9 level cascaded NPC/H-bridge inverter is considered. The new control strategy is achieved by decomposing the nine level output into four separate and independent three-level NPC PWM output. By combining the three- level NPC PWM back to back using DC sources and properly phase shifting the modulating wave and carrier a simplified control strategy is achieved with reduced number of components. The control strategy is applied on cascaded NPC/H-bridge inverter that combines features from NPC inverter and cascaded H-Bridge inverter. For higher voltage applications, this structure can be easily extended to an n- level by cascaded NPC/H-Bridge PWM inverters.

The article starts by developing a control algorithm based on novel phase shifted PWM technique on the proposed inverter model. This is done on a two cell of the cascaded model to realize nine level voltage output. A theoretical harmonic analysis of the model with the proposed control algorithm is carried out based on double Fourier principle. Spectral characteristics of the output waveforms for all operating conditions are studied for a five-level and nine- level voltage output. Theoretical results are verified using MATLAB simulation.The results shows that the spectrum can be made to only consist of the multiples of fourth order for a five level and with proper phase shift combination, a multiple of eighth order is achieved for nine level voltage output. The results are compared with those of a conventional multicarrier PWM approach; it is shown that with the proposed phase shifted PWM approach, the inverter exhibits reduced harmonic content are present. Finally the article compares the components count of the the model with the convetional cascaded H-bridge inverter, it is clealry shown that the proposed model requires a lesser number of separate dc sources as compared to conventional cascaded H-bridge inverter.

2. System topology and switching technique

2.1 Main system configuration

Fig 1 shows the circuit configuration of the proposed nine- level cascaded NPC/H-Bridge PWM inverter which consists of two legs for each cell connected to a common bus. Four active switches, four freewheeling diodes and two diodes clamped to neutral are adopted in each leg. The voltage stress of all the eight power switches is equal to half of DC bus voltage. The power switches in each leg are operated in high frequency using phase shifted PWM control technique to generate the three voltage levels on the ac terminal to neutral voltage point

The building block of the whole topology consists of two identical NPC cascaded cells. The inverter phase voltage V_{an} is the sum of the two cascaded cells, i.e.,

$$V_{an} = V_{01} + V_{02} \tag{1}$$

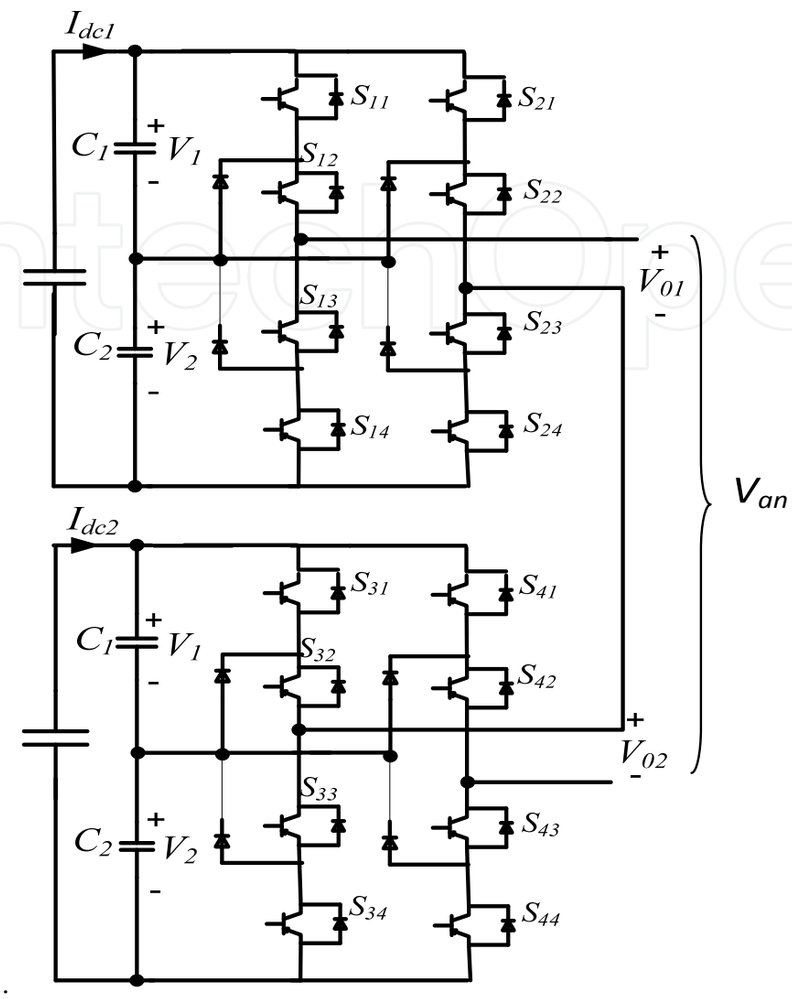


Fig. 1. Schematic diagram of the proposed cascaded NPC/H-bridge inverter model

Assuming that the two capacitor voltages on the DC bus voltage are equal, five different voltage levels +2Vdc, $+V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$, are generated on the ac terminal V_{01} which consist of two legs. Same applies to V_{02} fig. 2 shows the switching model for a nine- level output [6]. This implies that by cascading two NPC/H-Bridge inverters (V_{01} and V_{02}) and properly phase shifting the modulating wave and carriers, a nine- level PWM output is achieved. The number of output voltage levels is given by

$$m = 4N + 1 \tag{2}$$

Where N is the number of series connected NPC/H-Bridges. The topology is made up of four three level legs and each leg has four active switches and four freewheeling diodes.

2.2 System operation

Most of the past research on modeling of cascaded multilevel inverter has concentrated on realizing a switching model of conventional H- bridge inverter without giving a guideline

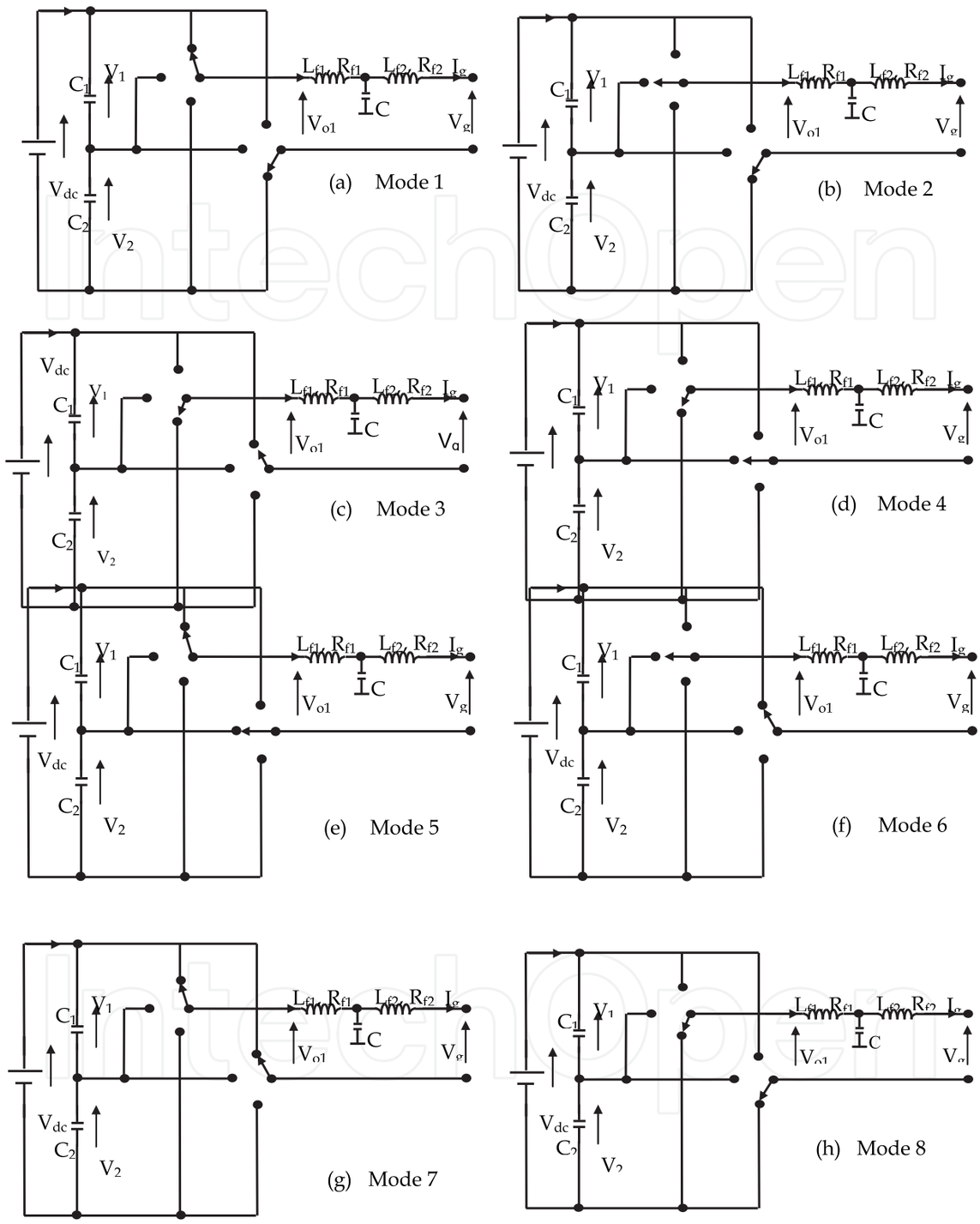


Fig. 2. Operating modes of one cell of NPC/H-Bridge inverter

on how one can get operating modes of cascaded NPC/H-bridge inverter and hence obtain a valid model for the topology. This section analyses eight valid operating modes of one cell of the proposed topology. The following assumptions are made in the modeling and analysis process:

- All components (power switches and capacitors) are ideal.
- The DC- link capacitors V_1, V_2, V_3 and V_4 have the same capacitance.
- PV cells supplies constant and equal voltages to the four DC link capacitors.
- The reference phase voltage is assumed to be a constant value during one switching period.

Figure 3 shows the operation modes for one NPC/H-bridge cell from the 9-level inverter.
In mode 1 the power switches S_{11} & S_{12} and S_{23} & S_{24} are turned on to supply voltage at the output of first NPC/H-bridge cell that is equal to $V_{01}= V_1+ V_2$. The capacitors C_1 and C_2 are discharged as they supply power to the utility as shown in figure 2 (a). The modes 2 to 8 are as shown in figures 2 (b) to 2 (h) respectively. In mode 2 the output voltage is $V_{01}= V_2$, in mode 3: $V_{01}= - (V_1+ V_2)$, in mode 4: $V_{01}= -V_2$, in mode 5: $V_{01}= V_1$, in mode 6: $V_{01}= -V_1$: in mode 7: $V_{01}= 0$ and in mode 8: $V_{01}= 0$.
Based on the analysis of the operation model, the state variable equation for the proposed inverter can be estimated. To prevent the top and bottom power switched in each inverter leg from conducting at the same time, the constraints of power switches can be expressed as:

$$S_{i1} + S_{i3} = 1;\ S_{i2} + S_{i4} = 1\} \tag{3}$$

Where i = 1, 2. Let's define the switch operator as: $T_1 = S_{11} \& S_{12}$; $T_2 = S_{13} \& S_{13}$; $T_3 = S_{21} \& S_{22}$ $T_4 = S_{23} \& S_{24}$. The four valid expressions are given by:

$$T_1 = \begin{cases} 1\ if\ both\ S_{11} \& S_{12}\ are\ ON \\ 0\ Otherwise \end{cases} \tag{4}$$

$$T_2 = \begin{cases} 1\ if\ both\ S_{13} \& S_{14}\ are\ ON \\ 0\ Otherwise \end{cases} \tag{5}$$

$$T_3 = \begin{cases} 1\ if\ both\ S_{21} \& S_{22}\ are\ ON \\ 0\ Otherwise \end{cases} \tag{6}$$

$$T_4 = \begin{cases} 1\ if\ both\ S_{23} \& S_{24}\ are\ ON \\ 0\ Otherwise \end{cases} \tag{7}$$

From fig. 4 taking two legs for each cell to be *a* and *b,* the equivalent switching function are:

$$K_a = \begin{cases} 1\ if\ T_1 = 1 \\ 0\ if\ S_{12}\ \ 1 \\ -1\ if\ T_2 = 1 \end{cases} \&\ K_b = \begin{cases} 1\ if\ T_3 = 1 \\ 0\ if\ S_{22}\ \ 1 \\ -1\ if\ T_4 = 1 \end{cases} \tag{8}$$

Using equation (3 – 7), a switching state and corresponding voltage output V_{o1} can be generated as shown in table 1 which clearly indicates that there are 8 valid switching states;
From table 1, the voltage V_{01} generate by the inverter can be expressed as:

$$V_{01} = V_a + V_b \tag{9}$$

For the control technique stated above; the voltage level for one leg of the cell is given as:

K_a	K_b	T_1	T_2	S_{12}	T_3	T_4	S_{21}	V_a	V_b	V_{01}	Mode
1	-1	1	0	1	0	1	0	V_1	$-V_2$	$V_1+ V_2$	1
0	-1	0	0	1	0	1	0	0	$-V_2$	V_2	2
-1	0	0	1	0	0	0	1	0	V_2	$-V_2$	3
1	0	1	0	1	0	0	1	V_1	0	V_1	4
0	1	0	0	1	1	0	1	$-V_1$	0	$-V_1$	5
1	1	1	0	1	1	0	1	V_1	V_1	0	6
-1	-1	0	1	1	0	1	1	V_2	V_2	0	7
-1	-1	0	1	0	1	0	1	V_2	V_1	$-V_1- V_2$	8

Table 1. Switching States and Corresponding Voltage(s) for One Cell of NPC/H-bridge Inverter

$$V_a = K_a\left(\frac{K_a+1}{2}\right)V_1 - K_a\left(\frac{K_a-1}{2}\right)V_2 \tag{10}$$

Similarly for the second leg the expression is given by (11)

$$V_b = K_b\left(\frac{K_b+1}{2}\right)V_1 - K_b\left(\frac{K_b-1}{2}\right)V_2 \tag{11}$$

S_{11}	S_{12}	S_{21}	S_{22}	S_{31}	S_{32}	S_{41}	S_{42}	V_{01}	V_{02}	V_{an}
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	$-V_{dc}$	0	$-V_{dc}$
0	0	0	1	0	0	0	1	$-V_{dc}$	$-V_{dc}$	$-2V_{dc}$
0	0	0	1	0	0	1	1	$-V_{dc}$	$-2V_{dc}$	$-3V_{dc}$
0	0	0	1	0	1	0	0	$-V_{dc}$	V_{dc}	0
0	0	0	1	1	1	0	0	$-V_{dc}$	$2V_{dc}$	V_{dc}
0	0	1	1	0	0	0	0	$-2V_{dc}$	0	$-2V_{dc}$
0	0	1	1	0	0	0	0	$-2V_{dc}$	$-V_{dc}$	$-3V_{dc}$
0	0	1	1	0	0	1	0	$-2V_{dc}$	$-2V_{dc}$	$-4V_{dc}$
0	0	1	1	0	1	0	0	$-2V_{dc}$	V_{dc}	$-V_{dc}$
0	0	1	1	1	1	0	0	$-2V_{dc}$	$2V_{dc}$	0
0	1	0	0	0	0	0	0	V_{dc}	0	V_{dc}
0	1	0	0	0	0	0	1	V_{dc}	$-V_{dc}$	0
0	1	0	0	0	0	1	1	V_{dc}	$-2V_{dc}$	$-V_{dc}$
0	1	0	0	0	1	0	0	V_{dc}	V_{dc}	$2V_{dc}$
0	1	0	0	1	1	0	0	V_{dc}	$2V_{dc}$	$3V_{dc}$
1	1	0	0	0	0	0	0	$2V_{dc}$	0	$2V_{dc}$
1	1	0	0	0	0	0	1	$2V_{dc}$	$-V_{dc}$	V_{dc}
1	1	0	0	0	0	1	1	$2V_{dc}$	$-2V_{dc}$	0
1	1	0	0	0	1	0	0	$2V_{dc}$	V_{dc}	$3V_{dc}$
1	1	0	0	1	1	0	0	$2V_{dc}$	$2V_{dc}$	$4V_{dc}$
1	1	1	1	1	1	1	1	0	0	0

Table 2. Switching scheme for one phase leg of a nine level cascaded NPC/H- bridge inverter

From equation (9), the voltage output for one cell of the model can be deduced as;

$$V_{01} = \frac{K_a - K_b}{2}(V_1 + V_2) + \frac{K^2{}_a - K^2{}_b}{2}(V_1 - V_2) \tag{12}$$

For the compound nine level inverter let's assume that $V_1 = V_2 = V_3 = V_4 = V$, the switching states are as shown in Table 2.
For a nine level cascaded NPC/H-bridge inverter, there are 22 valid switching states though two of the switching states are short circuits and thus cannot compensate the DC capacitor as current do not pass through either of the four DC- link capacitors.

3. Mathematical analysis

Most of the past research on modeling of cascaded multilevel inverter has concentrated on realizing a switching model of conventional H- bridge inverter without giving a guideline on how one can get operating modes of cascaded NPC/H-bridge inverter and hence obtain a valid model for the topology. This section analyses eight valid operating modes of one cell of the proposed topology and proposes an equivalent circuit for the topology.
The following assumptions are made for deriving the mathematical model of the cascaded H-bridge inverters.

- The grid is assumed to be AC current source,
- The power losses of the whole system are categorized as series loss and parallel loss. The series loss and interfacing inductor loss are represented as equivalent series resistance (ESR). Parallel losses are represented as shunt connected resistances across the dc-link capacitors.

The differential equations describing the dynamics of the coupling inductor between the NPC/H-bridge inverter and the grid of the model shown in fig. 1 can be derived as:

$$\begin{cases} L_{f1}\dfrac{di_{fx}}{dt} = -V_{cx} - i_{fx}R_{f1x} + \delta_{1x}V_1 + \delta_{2x}V_2 \\ L_{f2}\dfrac{di_{sx}}{dt} = -V_{cx} - i_{sx}R_{f2x} - V_{sx} \end{cases} \tag{13}$$

According to Kirchhoff's law, the currents flowing into the dc link capacitors C_1 and C_2 can be expressed as:

$$\begin{cases} i_{C1} = C_1\dfrac{dV_1}{dt} = \delta_{1x}i_{fx}\dfrac{V_1}{R} + \dfrac{V_2}{R} \\ i_{C2} = C_2\dfrac{dV_2}{dt} = -\delta_{2x}i_{fx}\dfrac{V_1}{R} + \dfrac{V_2}{R} \\ i_{CX} = C_f\dfrac{dV_{fx}}{dt} = i_{fx} - i_{sx} \\ C_1\dfrac{dV_1}{dt} - C_2\dfrac{dV_2}{dt} = \delta_3 i_{fx} \end{cases} \tag{14}$$

The equations (13) and (14) can be rearranged as:

$$\begin{cases} \dfrac{di_{fx}}{dt} = \dfrac{R_{f1x}}{L_{f1}} - \dfrac{V_{cx}}{L_{f1}} + \dfrac{\delta_{1x}V_1}{L_{f1}} + \dfrac{\delta_{2x}V_2}{L_{f1}} \\ \dfrac{di_{sx}}{dt} = \dfrac{V_{cx}}{L_{f2}} - \dfrac{R_{f1}}{L_{f2}} - \dfrac{V_{sx}}{L_{f2}} \\ \dfrac{dV_1}{dt} = \dfrac{\delta_{1x}i_{fx}}{C_1} - \left(\dfrac{V_1}{RC_1} + \dfrac{V_2}{RC_1}\right) \\ \dfrac{dV_2}{dt} = \dfrac{\delta_{2x}i_{fx}}{C_2} - \left(\dfrac{V_1}{RC_2} + \dfrac{V_2}{RC_2}\right) \\ \dfrac{dV_f}{dt} = \dfrac{i_{fx}}{C_f} - \dfrac{i_{sx}}{C_f} \\ \delta_3 i_{fx} = C_1\dfrac{dV_1}{dt} - C_2\dfrac{dV_2}{dt} \end{cases} \tag{15}$$

Equation (16) can be written in the format of:

$$Z\dot{x} = Ax + B \tag{16}$$

Capacitor current, inverter current and utility line current and DC- Link capacitors are taken as state variables:

$$x = [i_{fx}\ i_{sx}\ V_c\ V_1\ V_2]^T \tag{17}$$

$$Z = \begin{bmatrix} L_{f1} & 0 & 0 & 0 & 0 \\ 0 & L_{f2} & 1 & 0 & 0 \\ 0 & 0 & C & 0 & 0 \\ 0 & 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & 0 & C_2 \end{bmatrix} \tag{18}$$

$$B = [0\ -V_s\ 0\ 0\ 0\ ]^T \tag{19}$$

Matrix A depends on each operating mode as such

- For $V_{01} = +V_2$

$$A_1 = \begin{bmatrix} -R_{f1} & 0 & -1 & 0 & 1 \\ 0 & -R_{f2} & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & R^{-1} & R^{-1} \\ -1 & 0 & 0 & R^{-1} & R^{-1} \end{bmatrix} \tag{20}$$

- For $V_{01} = -V_2$

$$A_5 = A_1{}^T \tag{21}$$

- For $V_{01} = +V_1$

$$A_2 = \begin{bmatrix} -R_{f1} & 0 & -1 & 1 & 0 \\ 0 & -R_{f2} & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ -1 & 0 & 0 & R^{-1} & R^{-1} \\ 0 & 0 & 0 & R^{-1} & R^{-1} \end{bmatrix} \tag{22}$$

- For $V_{01} = - V_1$

$$A_6 = A_2^{\,T} \tag{23}$$

- For $V_{01} = 0$

$$A_4 = \begin{bmatrix} -R_{f1} & 0 & -1 & -1 & -1 \\ 0 & -R_{f2} & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{24}$$

Considering the same assumption made earlier that the dc link capacitors have the same capacitance $C_1 = C_2 = C$ which implies $V_1 = V_2 = V_{dc}/2$, the state space equation (17) can be simplified to:

$$Z^{'}\dot{x} = A^{'}x + B^{'} \tag{25}$$

With

$$x = [i_{fx}\ i_{sx}\ V_c\ V_{dc}\ /\ 2]^T \tag{26}$$

$$Z^{'} = \begin{bmatrix} L_{f1} & 0 & 0 & 0 \\ 0 & L_{f2} & 1 & 0 \\ 0 & 0 & C & 0 \\ 0 & 0 & 0 & C_T \end{bmatrix} \tag{27}$$

$$B = [0\ V_s\ 0\ 0\ 0\ ]^T \tag{28}$$

$$A^{'} = \begin{bmatrix} -R_{f1} & 0 & -k & k \\ 0 & -R_{f2} & k & 0 \\ k & -1 & 0 & 0 \\ -k & 0 & 0 & 0 \end{bmatrix} \tag{29}$$

Where k depends on the operating mode and can take five different values: 1. 0.5 0, -05, -1.

For a three phase system, V_s is replaced $V_s(\cos\omega_o t)$, $V_s(\cos\omega_o - 2\pi/3)$ and $V_s(\cos\omega_o + 2\pi/3$. similarly the Z, A and B matrices are expanded accordingly to three phase. Where V_s is the grid voltage.

3.1 Harmonic analysis of a nine level cascaded NPC/H-bridge inverter

Having realized a nine- level output from the a cascaded 9- level model, it is important to theoretically investigate its harmonic structure and show how harmonic suppression is achieved. Based on the principle of double Fourier integral (Holmes & Thomas, 2003). the first modulation between triangular carrier v_{cr1}, and the positive sinusoidal waveform a naturally sampled PMW output $V_p(t)$ of equation (30). Where M is the modulation index, V_{dc} is the DC link voltage of the PWM inverter and J_n is the n^{th} order Bessel function of the first kind. Using v_{cr2} which is the same carrier but displaced by minus unity, the naturally sampled PWM output V_n is as given in equation (31)

$$V_p(t) = \begin{cases} \dfrac{V_{dc1}}{2} + \dfrac{V_{dc1}M}{2}\cos\omega_s t + \dfrac{2V_{dc1}}{\pi}\displaystyle\sum_{m=1}^{\infty}\frac{1}{m}J_0\left(m\frac{\pi}{2}M\right) \\ \sin m\dfrac{\pi}{2}\cos\omega_s t + \dfrac{2V_{dc1}}{\pi}\displaystyle\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\mp 0}}^{\infty}\frac{1}{m}J_n \\ \left(m\dfrac{\pi}{2}M\right)\sin(m+n)\dfrac{\pi}{2}\cos(n\omega_c t + n\omega_s t) \end{cases} \tag{30}$$

$$V_n(t) = \begin{cases} \dfrac{V_{dc1}}{2} - \dfrac{V_{dc1}M}{2}\cos\omega_s t - \dfrac{2V_{dc1}}{\pi}\displaystyle\sum_{m=1}^{\infty}\frac{1}{m}J_0\left(m\frac{\pi}{2}M\right) \\ \sin m\dfrac{\pi}{2}\cos\omega_s t + \dfrac{2V_{dc1}}{\pi}\displaystyle\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\mp 0}}^{\infty}\frac{1}{m}J_n \\ \left(m\dfrac{\pi}{2}M\right)\sin(m+n)\dfrac{\pi}{2}\cos(n\omega_c t + n\omega_s t) \end{cases} \tag{31}$$

The output of leg 'a' is given by V_a (t) = V_p (t) – V_n (t) which is:

$$V_a(t) = \begin{cases} V_{dc1}\cos(\omega_s t) + \dfrac{4V_{dc1}}{\pi}\displaystyle\sum_{m=2,4,6}^{\infty}\sum_{n=\pm1\pm3\pm5}^{\infty}\frac{1}{m}J_n \\ \left(m\dfrac{\pi}{2}M\right)\cos(m\omega_c t + n\omega_s t) \end{cases} \tag{32}$$

The output of leg 'b' is realized by replacing ω_s with $\omega_s + \pi$ and using v_{cr2} which is same as phase displacing v_{cr1} by minus unity which gives

$$V_b(t) = \begin{cases} -V_{dc1}\cos(\omega_s t) - \dfrac{4V_{dc1}}{\pi}\displaystyle\sum_{m=2,4,6}^{\infty}\sum_{n=\pm1\pm3\pm5}^{\infty}\frac{(-1)^{m+n}}{m}J_n \\ \left(m\dfrac{\pi}{2}M\right)\cos(m\omega_c t + n\omega_s t) \end{cases} \tag{33}$$

From equations (32) and (33), it can be clearly deduced that that odd carrier harmonics and even sideband harmonics around even carrier harmonic orders are completely eliminated. Five- level obtained by taking the differential output between the two legs and is given by (35). Similarly the output between the other two legs of the second cell of the hybrid model is achieved by replacing ω_s with $\omega_s + \pi$ and ω_c with ωc + $\pi/4$ which gives another five level inverter for equation given by equation (34)

$$V_{01}(t) = \begin{cases} 2V_{dc1}\cos(\omega_s t) + \dfrac{8V_{dc1}}{\pi} \displaystyle\sum_{m=4,8,12}^{\infty} \sum_{n=\pm1\pm3\pm5}^{\infty} \frac{1}{m} J_n \\ (m\frac{\pi}{2}M)\cos(m\omega_c t + n\omega_s t) \end{cases} \tag{34}$$

$$V_{02}(t) = \begin{cases} -2V_{dc1}\cos(\omega_s t) - \dfrac{8V_{dc1}}{\pi} \displaystyle\sum_{m=4,8,12}^{\infty} \sum_{n=\pm1\pm3\pm5}^{\infty} \frac{(-1)^{\frac{m}{4}+n}}{m} J_n \\ (m\frac{\pi}{2}M)\cos(m\omega_c t + n\omega_s t) \end{cases} \tag{35}$$

Equations (34) and (35) clearly show that for five- level inverter, the proposed control strategy has achieved; Suppression of carrier harmonics to multiples of four; Elimination of even side harmonics around multiples of four carrier harmonics of Multiples of four carrier harmonics. Finally the output for a nine level is achieved differentiating the output voltage between the two cells of the five level cells and this is given by equation (36). It can be concluded that for a cascaded N-level inverter the carrier harmonic order is pushed up by factor of $4N$ where N is the number of cascaded hybrid inverters. The output voltages and spectral waveforms to confirm the validation of the control strategy using this approach of double Fourier transform will be discussed later.

$$V_{an}(t) = \begin{cases} 4V_{dc1}\cos(\omega_s t) + \dfrac{8V_{dc1}}{\pi} \displaystyle\sum_{m=8,16,24}^{\infty} \sum_{n=\pm1\pm3\pm5}^{\infty} \frac{1}{m} J_n \\ (m\frac{\pi}{2}M)\cos(m\omega_c t + n\omega_s t) \end{cases} \tag{36}$$

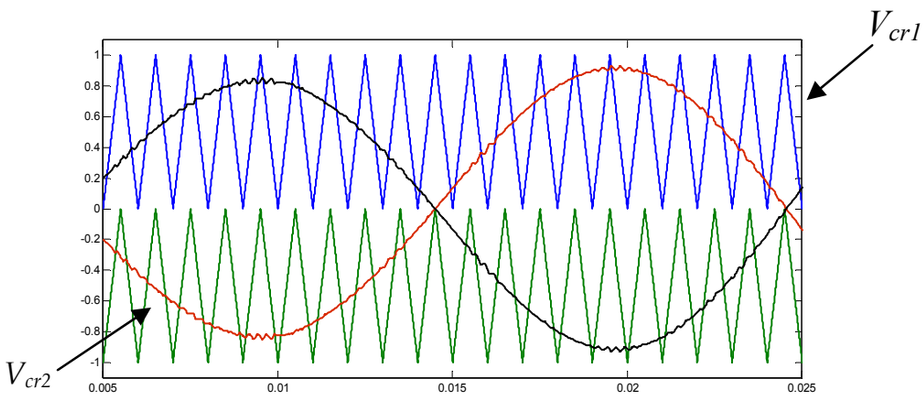
4. Proposed hybrid control method

The above section has illustrated in general the switching technque for one cell of the cascaded NPC/H-bridge model, because of the modularity of the model, two cells will be considered for modulatin and analysis in this section.For the two cells an improved strategy for realizing nine level output is proposed in this book chapter. The article uses the principle of decomposition where each leg is treated independently and gives a three level output (Naderi &. Rahmati, 2008).

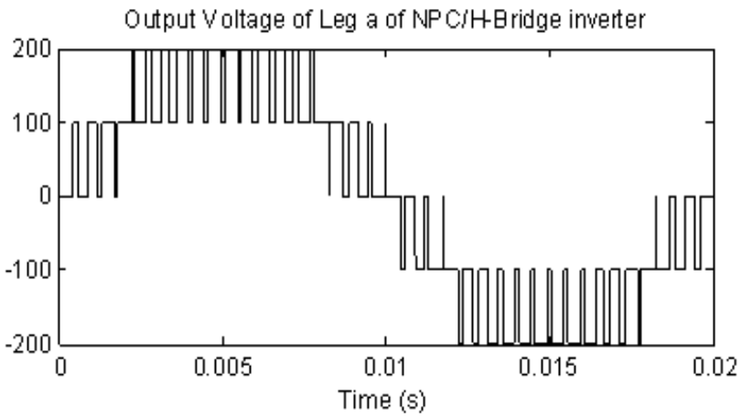
Positive and negative legs are connected together back to back and they share the same voltage source V_{dc}. PD modulation is used for achieving three level output (Rodriguez et al., 2002). To achieve a five level PWM output two triangular carriers V_{cr1} and V_{cr2} in phase but vertically disposed and modulating wave phase shifted by π are used. The multilevel converter model is modulated using phase shifted PWM technique as illustrated in fig. 3

and 4 for the two NPC/H-Bridge cells. Finally a nine- level PWM output is achieved by using the same two carriers but phase shifted by π/4 and modulating wave phase shifted by π as shown in fig. 5. This is a simple control strategy that can be easily implemented in a digital signal processor. The switching states for one phase leg of a nine- level NPC/H-bridge inverter is shown in table 2, as can be seen there several redundant states which can be utilized in DC voltage balance, this is not within the scope of this paper.

The control strategy has two advantages as compared to multicarrier PWM approach (Holmes & McGrath, 2001). First for an N-level cascaded NPC/H-bridge PWM inverter, we can use a switching frequency of 4N times less to achieve the same spectrum as multicarrier approach. This has an advantage of reducing the switching losses, which is an important feature in high power application. Secondly the multicarrier PWM approach requires 8 carriers to achieve nine level output, but the proposed control strategy requires only one carrier phase shifted by (N-1)π/4 where N is the number of series connected NPC/H-Bridge inverter.

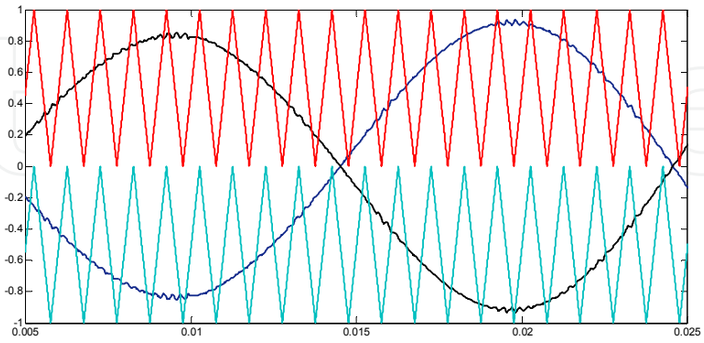


(a)

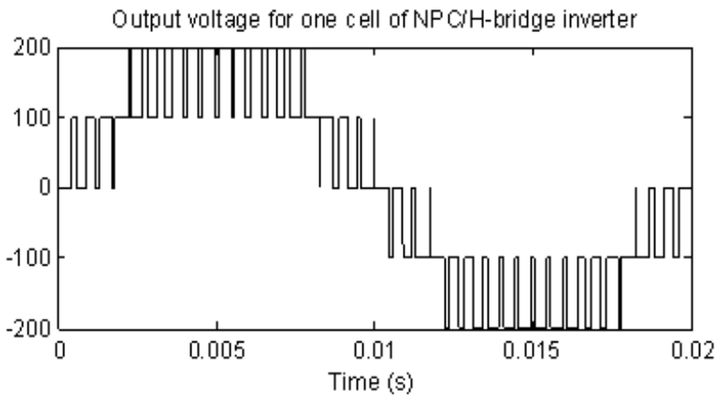


(b)

Fig. 3. (a) PWM scheme and (b) output voltage waveform for one cell of NPC/H-Bridge inverter

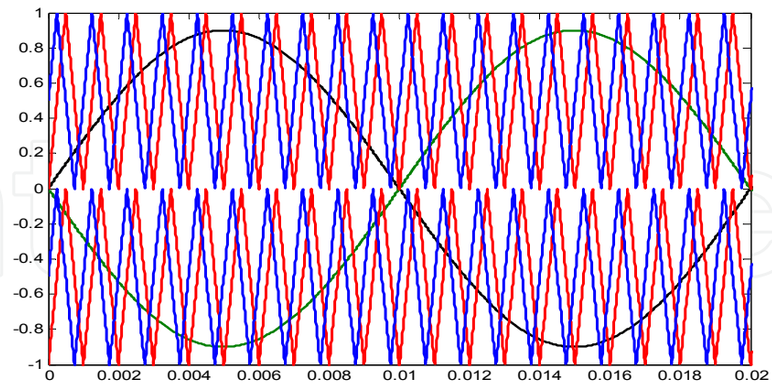


(a)

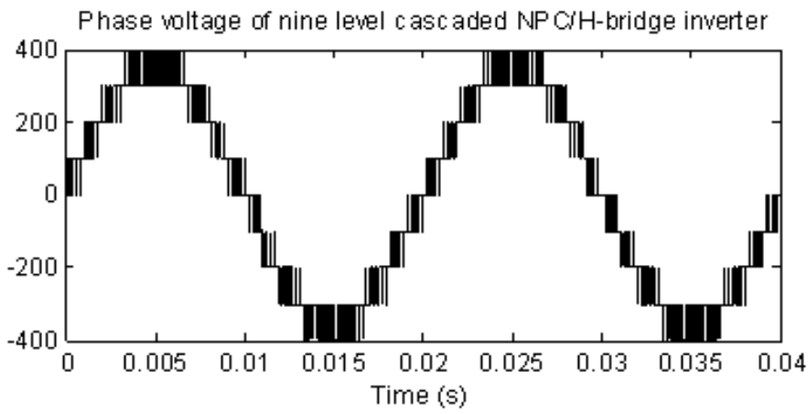


(b)

Fig. 4. (a) Phase shifted PWM scheme and (b) output voltage waveform for the second cell of cascaded NPC/H-Bridge inverter



(a)



(b)

Fig. 5. (a) PWM scheme and (b) output voltage waveform for a nine level cascaded NPC/H-Bridge inverter

5. MATLAB simulation

Part of the Matlab simulation has already been carried out in section 4 to investigate the proposed phase shifted PWM control technique. In order verify that a nine- level output is achieved by cascading two NPC/H-Bridge PWM inverter and properly phase shifting the carrier and the modulating wave, a model as shown in fig. 6 was developed and simulated in MATLAB. The control strategy to minimize harmonics was designed and developed in MATLAB as shown in fig. 7 (wanjekeche et.al., 2009). It is assumed that the dc voltage input for each module is E = 1OOV. The inverter operates under the condition of f_m=*50HZ,* m_f=*20* for a five level output and m_a=*0.9*. The device switching frequency is found from $f_{sw,dev}$= m_f/2 X f_m=500HZ

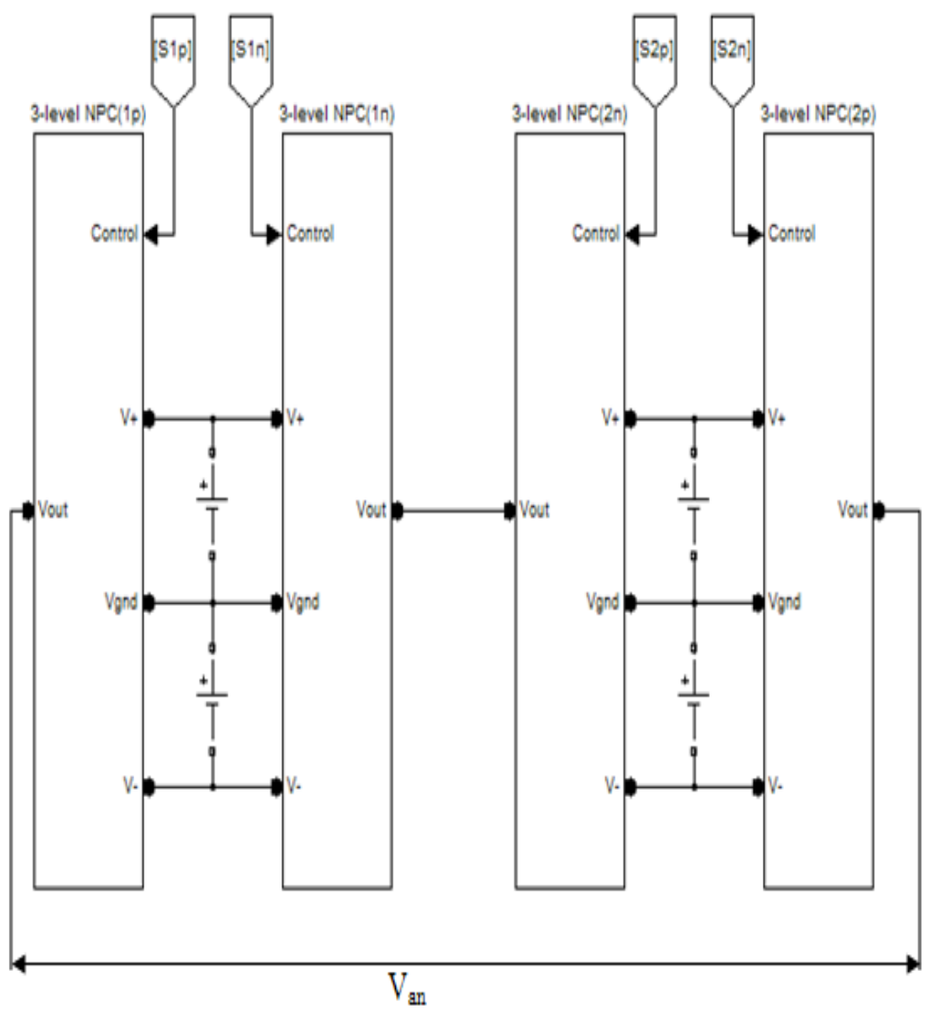


Fig. 6. Four legs of a nine-level cascaded NPC/H-bridge inverter

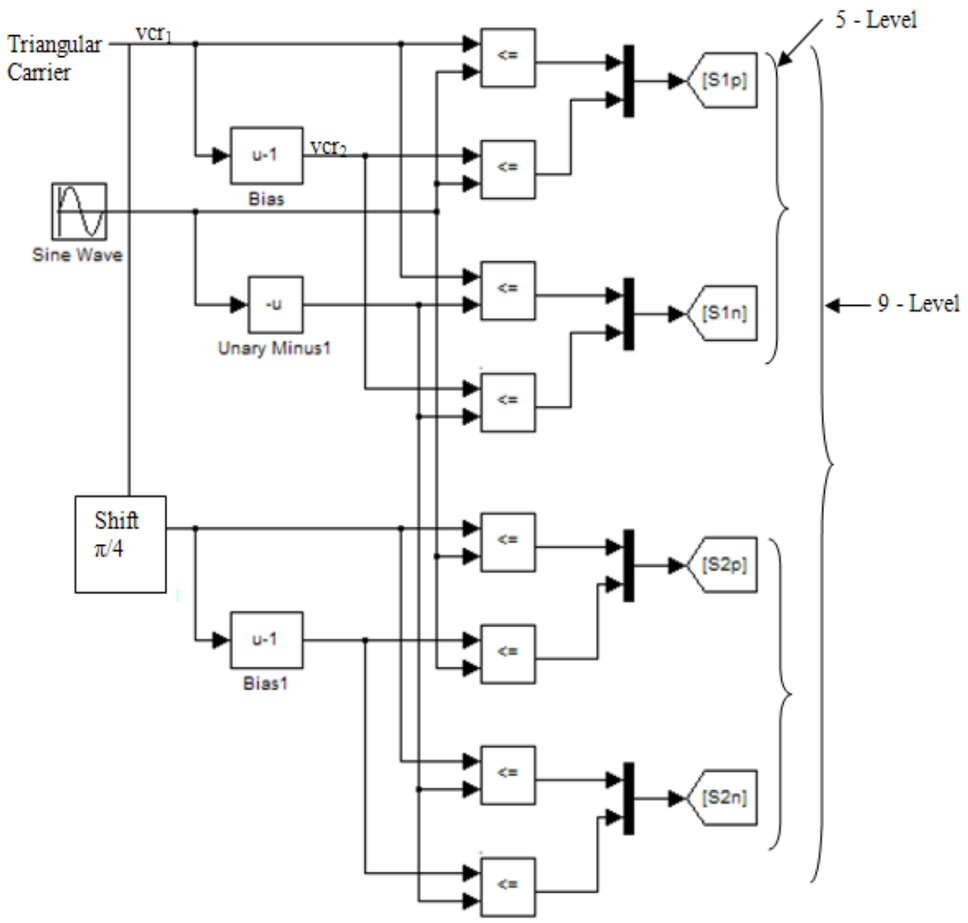
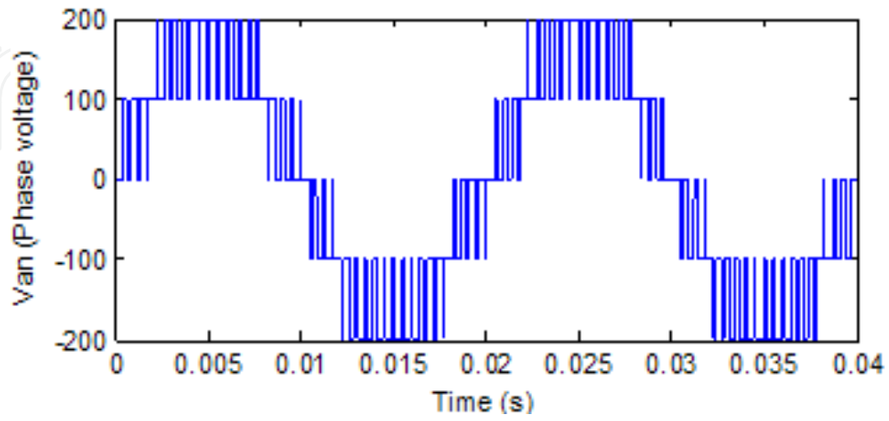


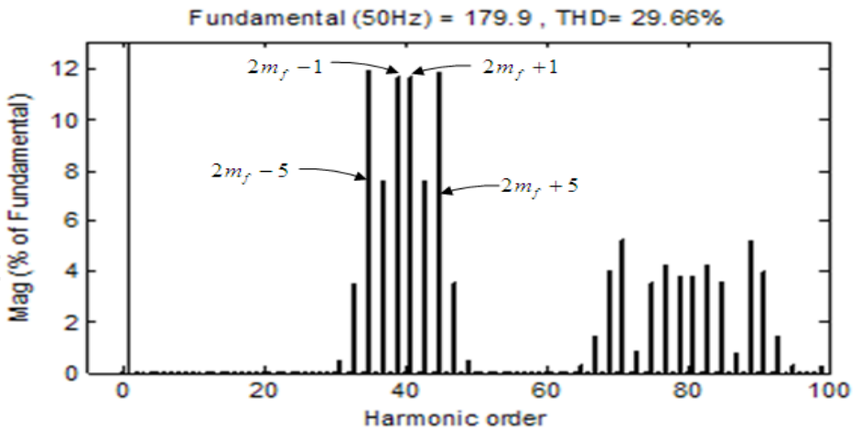
Fig. 7. Control strategy for a nine-level cascaded NPC/H-bridge inverter

5.1 Simulation results and discussion

Five- level inverter output are shown in figs.8, 9 and 10 for various switching frequency. Fig.8 shows the simulated waveform for the phase voltage V_{01} of the NPC/H-Bridge PWM inverter and its harmonic content. The waveform V_{01} is a five voltage levels, whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$, $6m_f$. This simulation verifies analytical equation (34) which shows that the phase voltage does not contain harmonics lower than the 31st, but has odd order harmonics (i.e. n=±1±3±5) centered around m=4, 8, 12. Figs. 9 & 10 shows five- level NPC/H-Bridge inverter output for device inverter switching frequency of 1000HZ and 200HZ respectively.

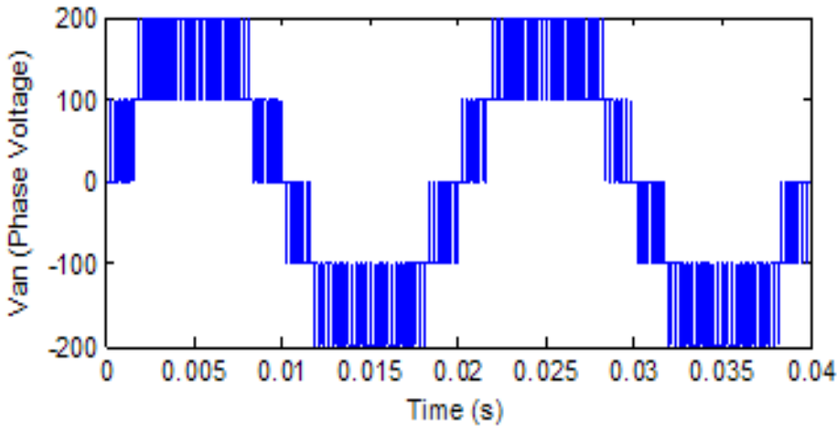


(a)

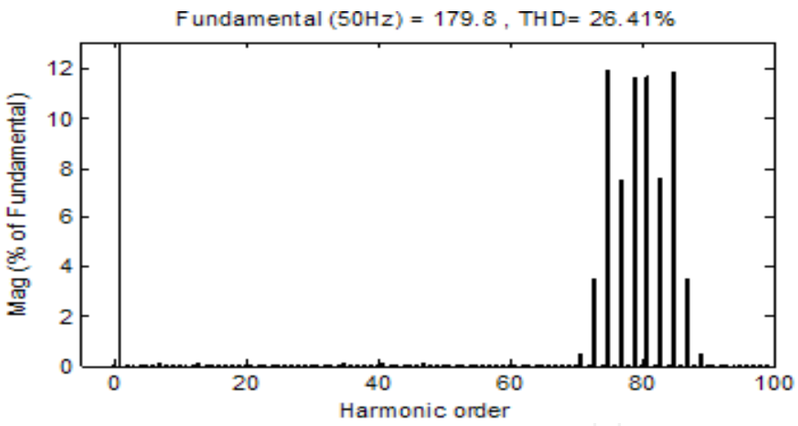


(b)

Fig. 8. (a) Waveform and (b) Spectrum for a five level NPC/H-Bridge inverter phase voltage (f_m=50HZ, $f_{sw,dev}$=500HZ, m_f=20, m_a=0.9)

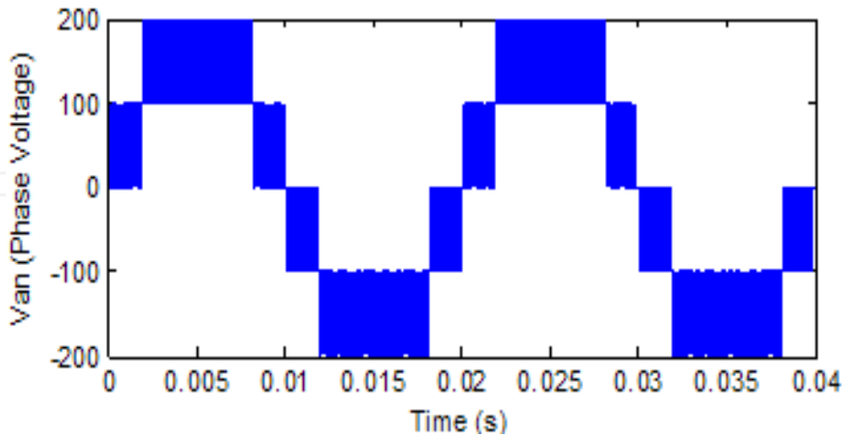


(a)

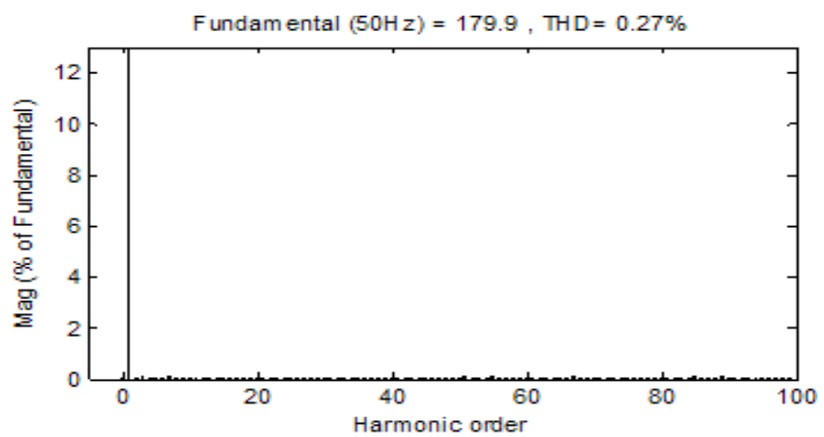


(b)

Fig. 9. (a) Waveform and (b) Spectrum for a five level NPC/H-Bridge inverter phase voltage (f_m=50HZ, $f_{sw,dev}$=1000HZ, m_f=40, m_a=0.9)



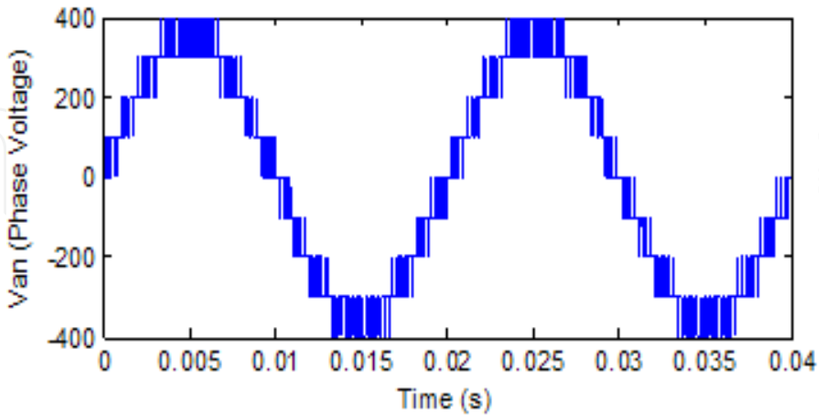
(a)



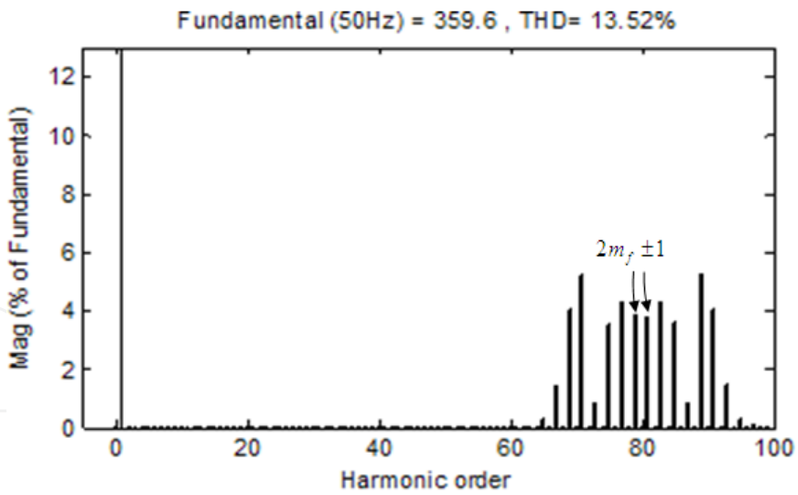
(b)

Fig. 10. (a) Waveform and (b) Spectrum for a five level NPC/H-Bridge inverter phase voltage (f_m=50HZ, $f_{sw,dev}$=2000HZ, m_f=80, m_a=0.9

Fig. 11 shows the waveform of the phase voltage of a nine level NPC/H-Bridge PWM inverter. It has sidebands around $4m_f$ and its multiples, this shows further suppression in harmonic content. This topology operates under the condition of f_m=*50HZ*, m_f=*40* and m_a=*0.9*. The device switching frequency is found from $f_{sw,dev}$= $m_f/4$ X f_m=500HZ. This simulation verifies analytical equation (36) which shows that the phase voltage does not contain harmonics lower than the 67th, but has odd order harmonics (i.e. n=±1±3±5) centered around m=8, 16, 32. As can be seen from fig. 12, a switching frequency of 1KHZ which fits most of high power switching devices has a THD of 0.18% this makes the topology a perfect fit for most high power application such as utility interface power quality control and Medium Voltage drives.

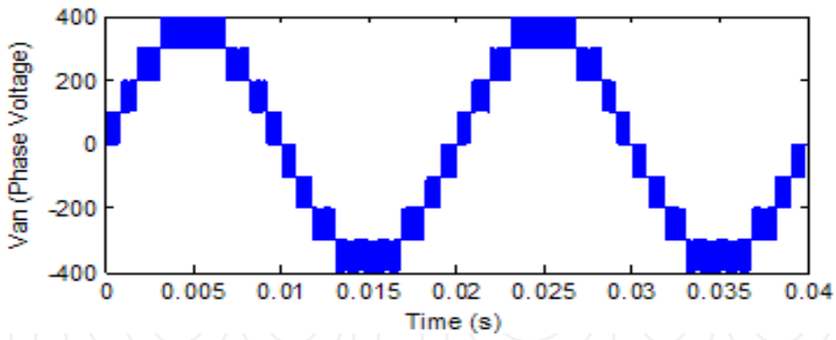


(a)

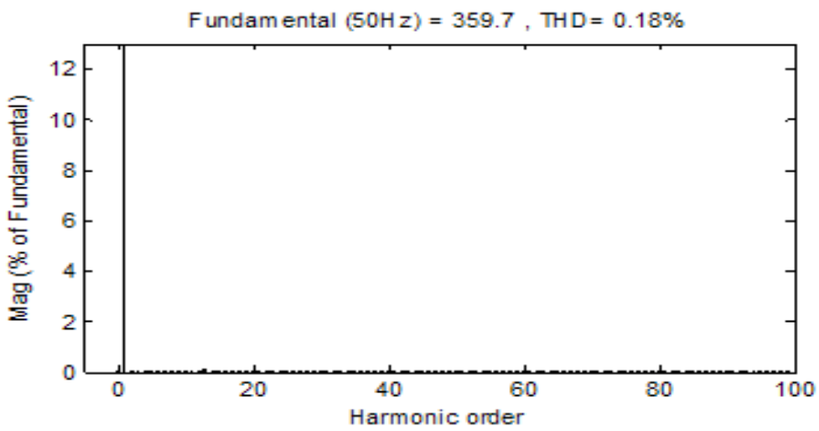


(b)

Fig. 11. (a) Waveform and (b) Spectrum for a nine- level cascaded NPC/H-Bridge inverter phase voltage (f_m=50HZ, $f_{sw,dev}$=500HZ, m_f=40, m_a=0.9)



(a)



(b)

Fig. 12. (a) Waveform and (b) Spectrum for a nine- level cascaded NPC/H-Bridge inverter phase voltage (f_m=50HZ, $f_{sw,dev}$=1000HZ, m_f=80, m_a=0.9)

6. Comparison of the proposed control technique with conventional PWM multicarrier approach

As can be seen from fig. 1, to achieve the same voltage levels *N* for each phase, only *(N-1)/4* separate dc sources are needed for one phase leg converter of the cascaded NPC/H-bridge model, whereas *(N-1)/2* separate voltage voltages is need for cascaded H –bridge inverter. Thus for an n- cascaded NPC/H-bridge inverter, the number of separate DC sources S is given by:

$$S = \frac{N-1}{4} \tag{37}$$

Table 3 shows comparison on the number of components for various multilevel inverters, cascaded NPC/H-bridge inverter requires 16 switching devices just as the other topologies but used only two carriers for any level of voltage output. For comparison between the two cascaded inverters it is readily shown in table 4 that the NPC/H-bridge inverter has an advantage of realizing the same voltage level as cascaded H-bridge inverter with a half number of separate DC sources which is more expensive as compared to clamping diodes.

Topology / No. of Components	Diode clamped	Flying capacitor	Cascaded H- bridge	Cascaded NPC/H-bridge
Switching devices	16	16	16	16
Clamping diodes	56	0	0	8
Flying capacitors	0	56	0	0
Carriers	8	8	4	2
Separate cells	0	0	4	2
Separate dc sources	1	0	4	2

Table 3. Component comaprison for different multilevel inverters for nine level voltage output

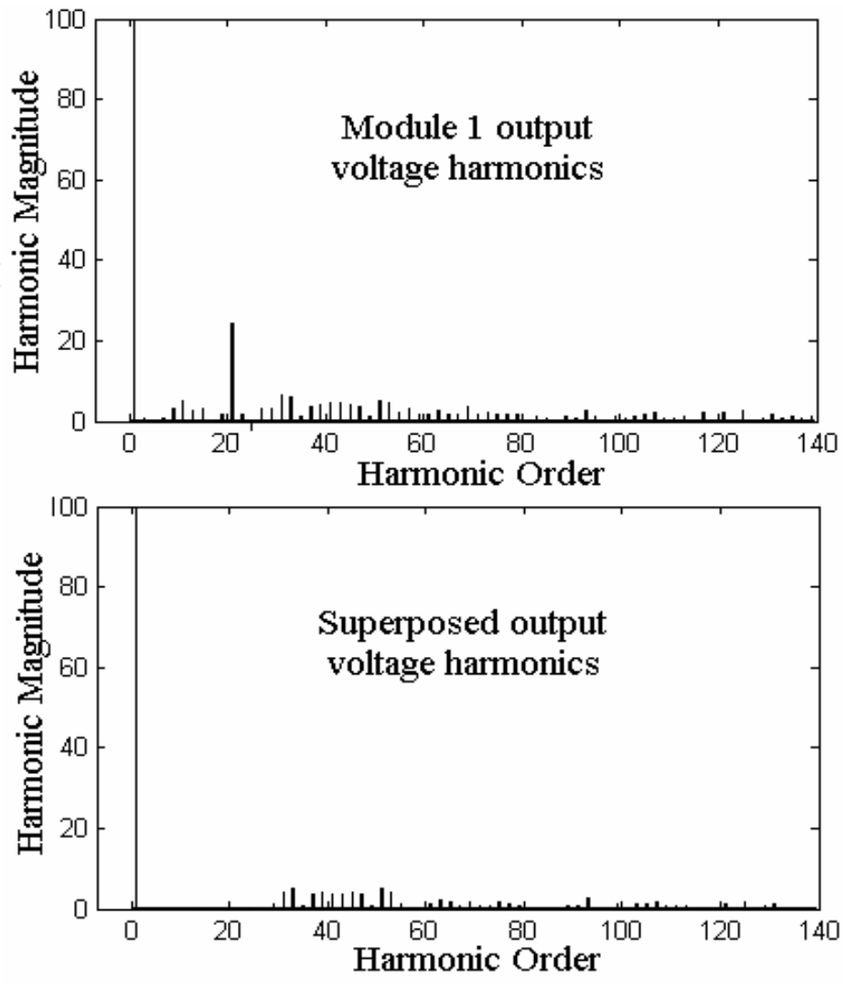
Topology / No. of Components	Cascaded H- bridge	Cascaded NPC/H-bridge
Switching devices	2N-1	2N-1
Clamping diodes	0	N-1
Flying capacitors	0	0
Carriers	(N-1)/2	2
Separate cells	(N-1)/2	(N-1)/4
Separate dc sources	(N-1)/2	(N-1)/4

Table 4. Component comaprison for different multilevel inverters for nine level voltage output

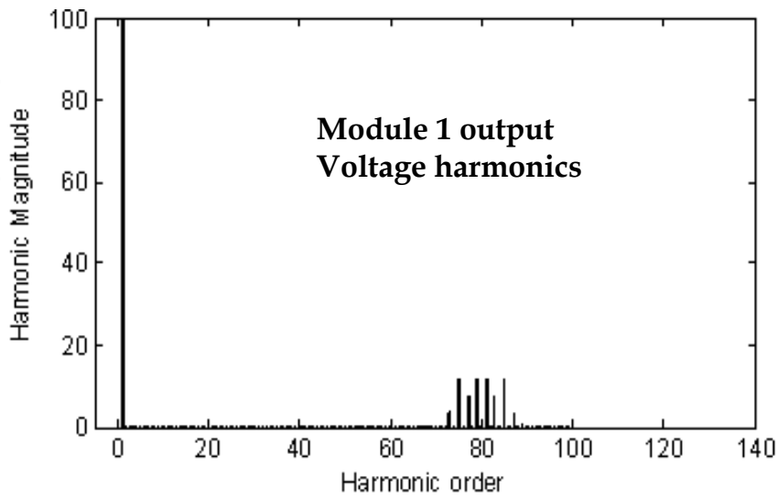
6.1 Comparison of the MATLAB simulation results of the two PWM control methods

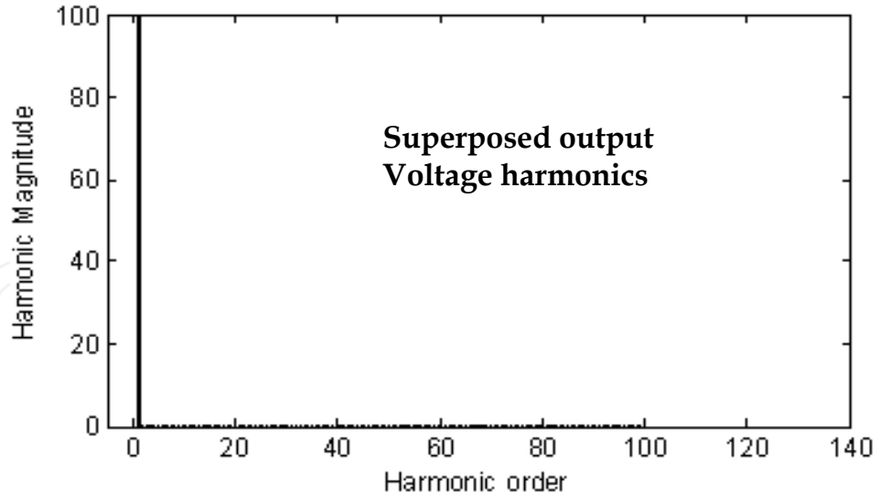
To clearly investigate the superiority of the model under the proposed PWM control technique, Matlab simulation results was carried out on a cascaded NPC/H-bridge nine level inverter model under the conditions of f_m=50HZ, fc =1000Hz and m_a=0.9.

With the proposed Phase – shifted PWM technique, there is further harmonic suppression as shown in fig. 13 (b), as compared to conventional PWM Phase shifted approach. This is clearly illustrated in fig. 13 (a) where Phase Disposition and Phase shifted PWM modulation strategy is adopted (Jinghua & Zhengxi, 2008). This is beacuse with conventional PWM multicarrier approach, optimum harmonic cancellation is achieved by phase shifting each carrier by $(i-1)\pi/N$ (Holmes & Thomas, 2003). where i is the i^{th} converter, N is the number of series – connected single the multicarrier PWM approach requires 8 carriers to achieve nine level output, but the proposed control strategy requires only one carrier phase shifted by (N-1)π/4 as stated in section 4.1(Wanjekeche et al., 2009).


Module 1 output
voltage harmonics
Harmonic Magnitude
Harmonic Order
Superposed output
voltage harmonics
Harmonic Magnitude
Harmonic Order

(a)


Module 1 output
Voltage harmonics
Harmonic Magnitude
Harmonic order



(b)

Fig. 13. Spectra voltage waveforms of NPC/H-bridge topology using (a) conventional multicarrier phase shifted PWM approach (b) proposed phase shifted PWM approach

7. Conclusion

In this chapter it has been demonstrates with proper modeling of the converter, the operating characteristic and the control technique to be applied on the model can be easily found. This can be used to develop standard model for cascaded NPC/H-bridge inverter which is currently not available.

The article has developed an improved topology that can be used to achieve a nine- level NPC/H-Bridge PWM inverter. It has been clearly shown that five level NPC/H-Bridge inverter that has been proposed by many researchers gives a higher THD which is not acceptable in most high and medium power application unless a filter is used. And since there is limited research on cascaded this important hybrid model, the chapter has developed a novel phase shifted PWM control technique that was tested on a two cell cascaded NPC/H-bridge model. In the proposed control technique it has been shown that by properly phase shifting both the modulating wave and the carrier, a nine- level voltage output can be achieved with a reduced harmonic content. With a THD of 0.18% without a filter, this makes the control strategy for a cascaded nine level NPC/H-bridge inverter a good option for medium and high power application such as utility interface and medium drives.

The simulation results obtained clearly verifies the analytical equations from double Fourier transform, showing that a nine- level output has multiples of eighth- order cross modulated harmonics. From the mathematical analysis it has been shown that cross modulated harmonics for a generalized m- level cascaded NPC/H-Bridge inverter is a multiple of $4N$ where N is the number of series connected NPC/H-Bridge inverter

And finally the superiority of the proposed phase shifted PWM control technique is validated by comparing its waveform spectra with that of the conventional phase shifted PWM technique and it was shown the inverter exhibits reduced harmonic content

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MATLAB - A Ubiquitous Tool for the Practical Engineer

Edited by Prof. Clara Ionescu

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A well-known statement says that the PID controller is the â€œbread and butterâ€ of the control engineer. This is indeed true, from a scientific standpoint. However, nowadays, in the era of computer science, when the paper and pencil have been replaced by the keyboard and the display of computers, one may equally say that MATLAB is the â€œbreadâ€ in the above statement. MATLAB has became a de facto tool for the modern system engineer. This book is written for both engineering students, as well as for practicing engineers. The wide range of applications in which MATLAB is the working framework, shows that it is a powerful, comprehensive and easy-to-use environment for performing technical computations. The book includes various excellent applications in which MATLAB is employed: from pure algebraic computations to data acquisition in real-life experiments, from control strategies to image processing algorithms, from graphical user interface design for educational purposes to Simulink embedded systems.

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