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Compensation of Reactive Power and Sag Voltage Using Superconducting Magnetic Energy Storage System

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1. Introduction

Technological developments such as Flexible AC Transmission Systems (FACTS) can improve the power quality of the power system and can respond to the ever-increasing demand for electrical energy. Superconducting magnetic energy storage (SMES) is a FACTS device that has been used for several years at utility and industrial sites throughout the United States, Japan, Europe, and South Africa to provide both transmission voltage support and power quality to customers who are vulnerable to fluctuating power quality [1]-[3]. SMES systems are classified into two groups: voltage source inverter (VSI) and current source inverter (CSI) SMES. The VSI SMES has many advantages when compared with the CSI SMES; for example, in the VSI SMES, the power rating of power electronic devices that are used in the inverter is much less than that of the CSI SMES, resulting in fewer switching and power losses. Also, the VSI SMES can be used as a Static synchronous Compensator (STATCOM) when its chopper is out of service. Moreover, for the same condition, the VSI SMES can store more energy than the CSI SMES; these advantages encouraged the authors to study VSI SMES.

This type of SMES is composed of a magnetic energy storage coil with various structures and power conditioning systems that are also composed of different parts, such as AC-DC filters, a multi-level chopper, a capacitor bank, and a multi-level converter (i.e. an inverter or rectifier). These power conditioning systems are also used in many different sustainable energy systems, such as bio fuels, solar power, wind power, wave power, geothermal power, and tidal power.

The converter is an interface between the power network and the capacitor bank and controls the electrical energy exchange between the two. Likewise, the chopper is also an interface between the magnetic energy storage coil and the capacitor bank, and controls electrical energy exchange between them. To store the electrical energy in the capacitor bank and the magnetic energy storage coil in the range of mega joules, it is necessary to employ high power-rating converters; to overcome the limitations of the current and voltage range of the semiconductors, multi-level converters are used. The advantages of using such converters include reducing voltage on the switches, harmonic order correction, decreasing or eliminating lateral equipment, decreasing switching frequency, decreasing total harmonic distortion (THD), decreasing switching losses, and decreasing the output current ripple.

Multi-level converters, on the other hand, have some disadvantages associated with their use, such as the complexity of the control systems, increasing the number of power electronic devices, and increasing the asymmetry of the capacitor voltages during charge and discharge [4]-[8]. However, the trend toward increasing the speed of electronic processors and the steady decrease in the cost of power electronic devices, coupled with the ability to implement advanced modulation methods such as the SVPWM, encourage engineers to ignore the disadvantages of multi-level converters. There are three different multi-level voltage source converters: diode-clamped, flying capacitor, and cascade H-bridge. For the same voltage level, there are fewer capacitors in a diode-clamped multi-level converter than in the other multi-level converters, making it much more cost-effective than other two converters. When there are three voltage levels, a three-level diode-clamped converter is referred to as a neutral point clamped (NPC). With respect to the fact that an appropriate choice of switching strategy for SVPWM effectively reduces the low order harmonics, a novel and optimized switching strategy for SVPWM has been proposed for the first work in this chapter in order to mitigate some low order harmonics in the NPC voltage source inverter [9]-[13].

Depending on its application, a SMES device is controlled in two ways: first, the transmitted active and reactive power to the network is controlled using a NPC voltage source inverter and the capacitor voltage is stabilized using a chopper. In the second approach, the NPC voltage source inverter controls the transmitted reactive power to the network while stabilizing the capacitors voltage and the chopper controls the transmitted active power to the network. It should be noted that if the capacitors voltage is stabilized during all switching operations, low-capacity capacitors can be used in the SMES system, resulting in a lower cost of configuration. The voltage variation in low-capacity capacitors is faster during the course of supplying the power network by the SMES; consequently, a controller with a differential part, i.e. PID, will make the capacitor's voltage unstable and will transmit any noise to the power electronic devices of the chopper. Thus, PI controllers are used in this study to stabilize the capacitors voltage of the SMES by generating the real-time duty cycles of the three-level chopper in different operation modes. Stabilization of capacitors voltage will correct any imbalance due to asymmetry within the SMES circuit and its operation.

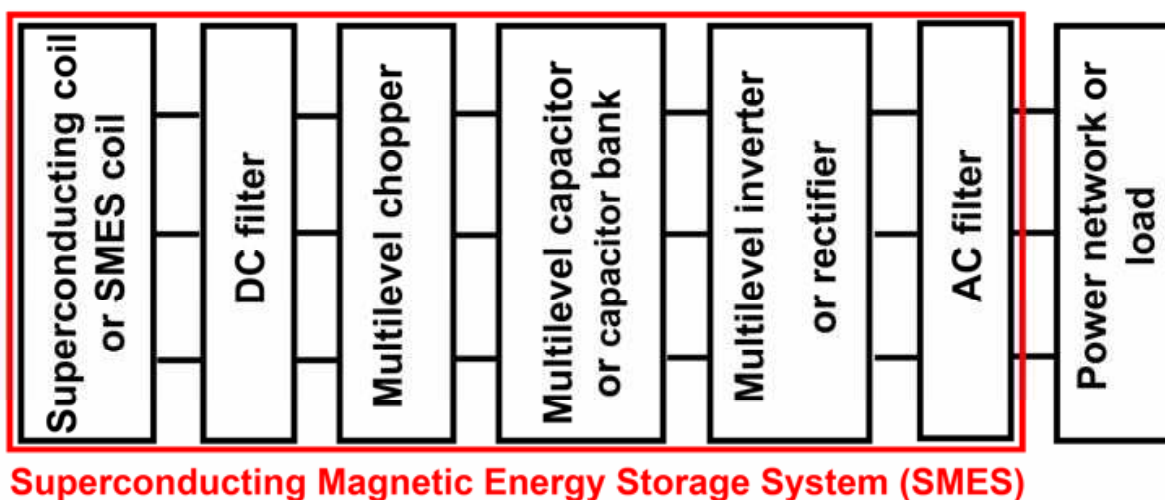


Fig. 1. The VSI SMES

Power quality is involved with a wide range of electromagnetic phenomena such as transient state, short- and long-term variations, voltage imbalance and variations, wave distortion, and frequency oscillations in power systems. In fact, the magnitude of variations in voltage, current, and frequency within power systems determines the power quality. In recent years, the voltage quality has been hailed as the most important index of power quality. Among voltage quality indicators, voltage sag has been shown to be especially important; voltage sag is defined as a temporary voltage drop that lasts between 0.5 and 30 cycles, and has a typical magnitude of 0.1 to 0.9 per unit range [14], [15].

A voltage sag can cause the same amount of downtime as a complete loss of power, especially if, for example, machines need to be rebooted or production processes need to be restarted. This issue poses a major challenge when estimating the economic cost of power interruptions and power-quality events. One way to compensate for voltage sag is to use VSI SMES, which is studied as a second work in this chapter by proposing a novel compensation algorithm. So this chapter presents a novel and optimized switching strategy and control approach for a three-level two-quadrant chopper in a three-level Neutral point clamped (NPC) voltage source inverter (VSI) superconducting magnetic energy storage (SMES). Using the proposed switching strategy, the voltage of the inverter capacitors in SMES can be independently controlled; also, the minimum power and switching losses - as well as the proper convection - can be achieved using this same strategy. The simulation results indicate that when combined with a proportional-integral (PI) control approach the proposed switching strategy can be easily implemented in the power networks and can balance and stabilize the multi-level inverters' capacitor voltage level. The voltage variation of the capacitors in the steady state condition is less than (0.062%) which is 15 times better than the IEEE standard requirement (1%). To investigate the effectiveness and reliability of the proposed approach in stabilizing capacitor voltage, SMES performance using the presented approach is compared with that of SMES when the capacitors of the three-level inverter are replaced with equal and ideal voltage sources. This comparison is carried out from the power quality point of view and it is shown that the proposed switching strategy with a PI controller is highly reliable [16]- [17]. Considering that the Space Vector Pulse Width Modulation (SVPWM) is highly effective in decreasing low order harmonics, this article utilizes this type of modulation when it is combined with the most optimized switching strategy.

In addition, this chapter proposes a new algorithm for SMES to compensate the voltage sag in the power networks. Simulation results show that the VSI SMES, when combined with the proposed algorithm, is able to compensate the voltage sag and phase voltage in less than one cycle, which is 5 times better than other voltage sag compensators.

2. Switching strategies of the three-level NPC inverter

Fig. 2 shows a case study in which a three-level NPC inverter supplies the three phase power network. A filter is used between the inverter and the power network to eliminate the high order harmonics; it is noted that parts of the low order harmonics are mitigated by applying SVPWM. Different switching states of the three-level NPC inverter are shown in Table 1: 1 and 0 indicate the on/off states of the switches, respectively. As seen in this table, in order to prevent a capacitor leg short-circuit, all switches in a leg are never turned on simultaneously.

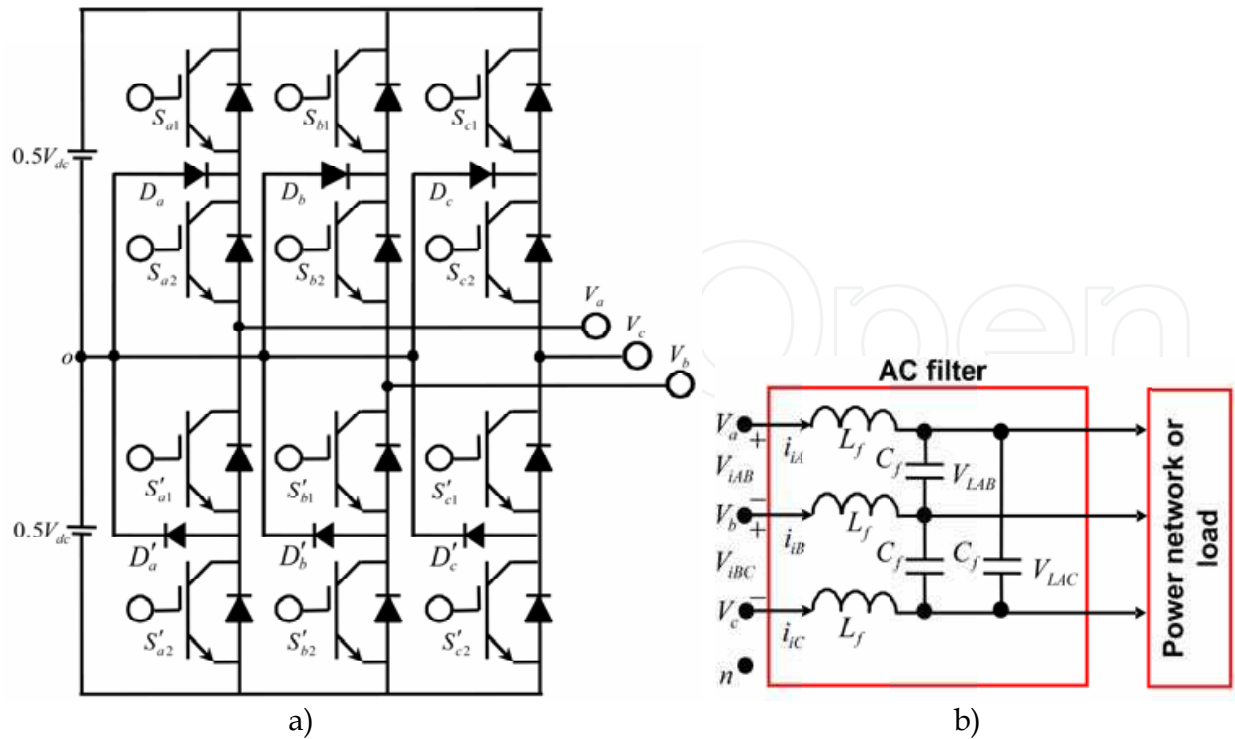


Fig. 2. a) The three-level three-phase Inverter, b) The power network (Load) and the LC Filter

C_i	S_{i1}	S_{i2}	S'_{i2}	S'_{i1}
1	1	1	0	0
0	0	1	1	0
-1	0	0	1	1

Table 1. Different switching states of the three-level inverter

From Fig. 2 and Table 1:

$$V_{io} = C_i V_{dc} / 2 \quad i = a, b, c \tag{1}$$

Assuming that the inverter output voltage is balanced and symmetrical:

$$V_{in} = V_{io} - V_{no} \tag{2}$$

$$V_{an} + V_{bn} + V_{cn} = 0 \tag{3}$$

Replacing (2) in (3) results in:

$$V_{no} = (V_{ao} + V_{bo} + V_{co}) / 3 \tag{4}$$

Also, substituting (1) and (4) in (2) gives:

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} \tag{5}$$

If $(\omega t = 0)$, Park's transformation gives :

$$\vec{V}_{ref} = V_d + jV_q = \sqrt{\frac{2}{3}} (V_{an} + aV_{bn} + a^2V_{cn}), a = e^{j2\pi/3} \quad (6)$$

$$\vec{V}_{ref} = \frac{V_{dc}}{\sqrt{6}} (C_a + aC_b + a^2C_c) \quad (7)$$

Using (7) and the values of (C_a, C_b, C_c) that are given in Table 1, 27 space vectors are obtained; the corresponding space vector plan is shown in Fig. 3 and shows that the vectors $V_{14}, V_7,$ and V_0 will short-circuit the load. In fact, these vectors are zero voltage vectors in the space vector plan; the other space vectors are active vectors. The active vectors V_{21} to V_{26} that have a magnitude of $2V_{dc} / \sqrt{6}$ form a large hexagon; the active vectors V_{15} to V_{20} that have a magnitude of $V_{dc} / \sqrt{2}$ form a medium hexagon, while the active vectors that have a magnitude of $V_{dc} / \sqrt{6}$ draw a small hexagon in the space vector plan. As seen in Fig. 3, each hexagon is divided into six sectors; moreover, each sector in the large hexagon is divided into four triangles. So there are 24 triangles in the large hexagon. At any instant, the vector \vec{V}_{ref} is located inside one of the 24 triangles. The average value of the output voltage (\vec{V}_{ref}) is computed from the linear composition of the vectors of the triangle in which \vec{V}_{ref} is located, as is shown in Fig. 4.

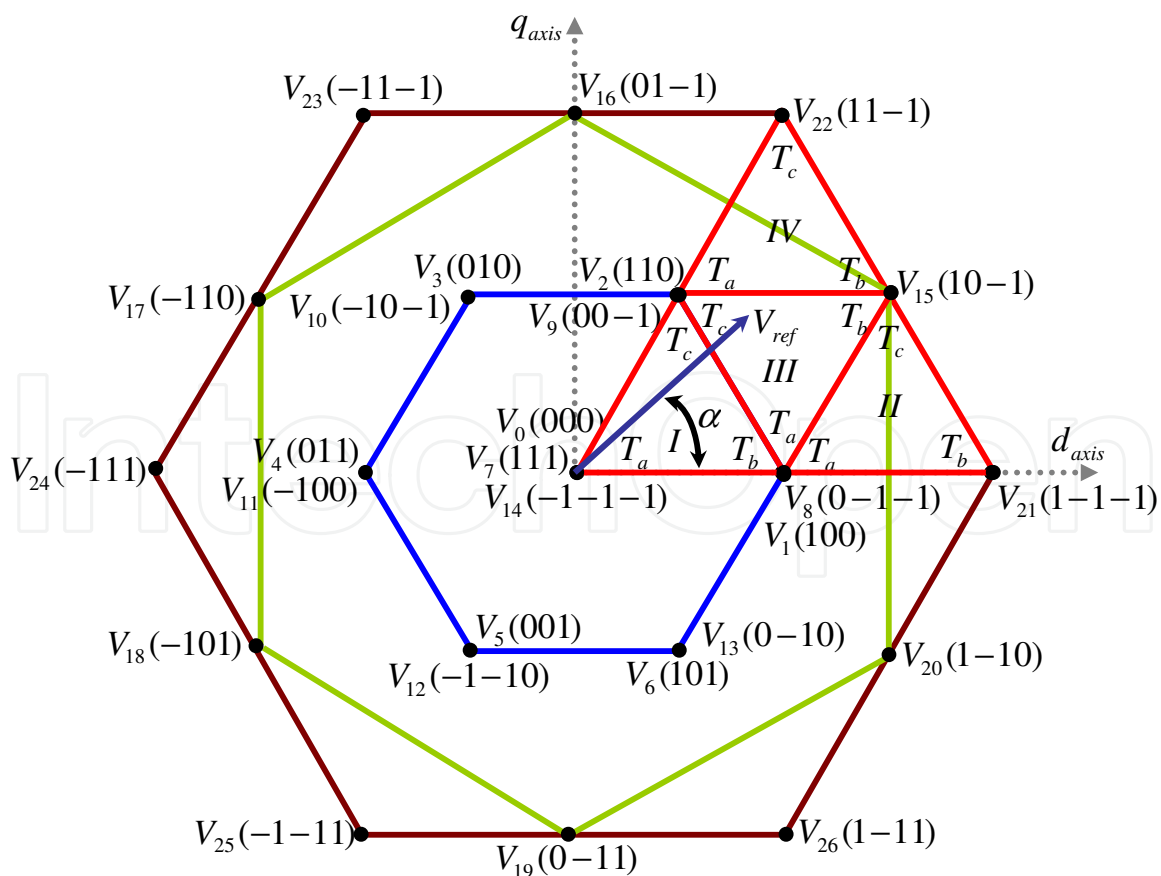


Fig. 3. The space vector plan

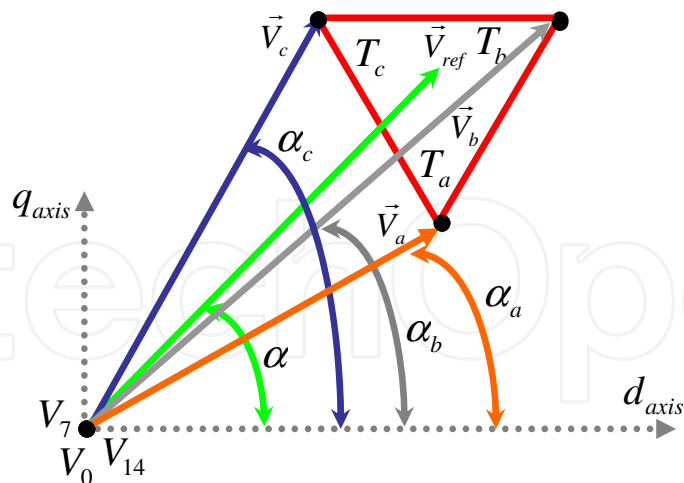


Fig. 4. Operation time calculation of each triangle vector

$$\int_0^{T_s} \vec{V}_{ref} dt = \int_0^{T_a} \vec{V}_a dt + \int_{T_a}^{T_a+T_b} \vec{V}_b dt + \int_{T_a+T_b}^{T_s} \vec{V}_c dt \quad (8)$$

$$T_s \vec{V}_{ref} = T_a \vec{V}_a + T_b \vec{V}_b + T_c \vec{V}_c \quad (9)$$

The projection of the vectors in (9) on the d-q axis and composing the obtained vectors results in:

$$T_s |\vec{V}_{ref}| \cos \alpha = T_a |\vec{V}_a| \cos \alpha_a + T_b |\vec{V}_b| \cos \alpha_b + T_c |\vec{V}_c| \cos \alpha_c \quad (10)$$

$$T_s |\vec{V}_{ref}| \sin \alpha = T_a |\vec{V}_a| \sin \alpha_a + T_b |\vec{V}_b| \sin \alpha_b + T_c |\vec{V}_c| \sin \alpha_c \quad (11)$$

$$m_a = |\vec{V}_{ref}| / \left(\frac{2}{\sqrt{6}} V_{dc} \right), \quad (12)$$

$$T_a + T_b + T_c = T_s,$$

$$\omega t + \varphi_{inv} = 2\pi f t = \alpha$$

where m_a is the modulation index, T_s is the switching period [the inverse of the switching frequency (f_s)], φ_{inv} is the inverter phase, and f is the frequency of the inverter output voltage. Assuming that the switching period, the phase, and the magnitude of the vectors $|\vec{V}_{ref}|$, $|\vec{V}_a|$, $|\vec{V}_b|$, and $|\vec{V}_c|$ are known, solving equations (10), (11), and (12) gives T_a , T_b , and T_c . These, shown in each triangle in Fig. 3, determine the operation time of the triangle vectors. Note that by knowing the value of $\omega t + \varphi_{inv}$ at any time, the number of the space sector in which \vec{V}_{ref} is located can be determined. The above equations can be extended to all sectors of the large hexagon by changing α to $\alpha - ((n-1)\pi/3)$ where $n=1, \dots, 6$ is the sector number. Table 2 gives the operation times of the vectors of the 4 triangles created in the n^{th} sector.

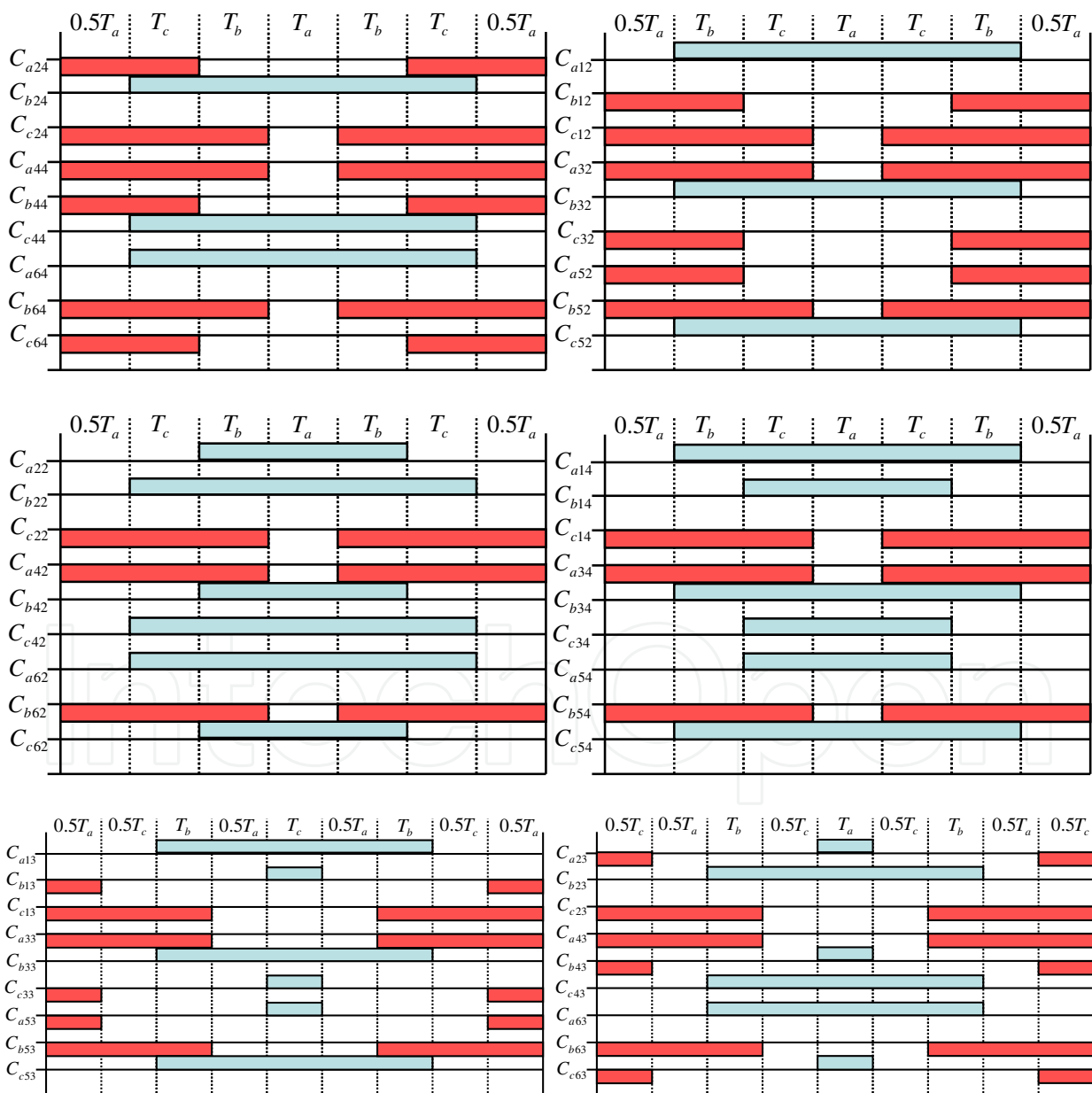
triangles' number	$T_i \quad i = a, b, c$
I	$T_a = T_s - T_b - T_c$
	$T_b = 2\sqrt{2} V_{ref} T_s \sin(-\alpha + n\pi / 3) / V_{dc}$
	$T_c = 2\sqrt{2} V_{ref} T_s \sin(\alpha - (n - 1)\pi / 3) / V_{dc}$
II	$T_a = T_s - T_b - T_c$
	$T_b = 2\sqrt{2} V_{ref} T_s \sin(-\alpha + n\pi / 3) / V_{dc}$
	$T_c = 2\sqrt{2} V_{ref} T_s \sin \alpha / V_{dc}$
III	$T_a = T_s - T_b - T_c$
	$T_b = -T_s + 2\sqrt{2} V_{ref} T_s \cos(\alpha + (1 - 2n)\pi / 6) / V_{dc}$
	$T_c = T_s - 2\sqrt{2} V_{ref} T_s \sin(-\alpha + n\pi / 3) / V_{dc}$
IV	$T_a = T_s - T_b - T_c$
	$T_b = 2\sqrt{2} V_{ref} T_s \sin(-\alpha + n\pi / 3) / V_{dc}$
	$T_c = -T_s + 2\sqrt{2} V_{ref} T_s \sin(\alpha - (n - 1)\pi / 3) / V_{dc}$

Table 2. The operation times of the vectors of 4 triangles of the n^{th} sector

Depending on the number of space vectors in each sector and the operation time of each space vector in generating \vec{V}_{ref} , many different switching strategies can be presented. The authors of the present work demonstrated that, in order to minimize THD in the inverter output voltage, the zero vectors should be distributed at the beginning, middle, and end of the switching periods in each sector whenever possible, [23]-[24]. Also, to minimize the switching losses, this distribution should be performed so that the minimum number of displacements in the switching states in each switching period of each sector occurs. The switching strategy of the space vector pulse width modulation is shown in Table 3; this strategy is based on the 24 triangles that were generated in the large hexagon as previously indicated. This switching strategy is implemented such that both the minimum THD and the minimum switching losses are realized. Note that C_{aij} in this table indicates the switching states in the inverter leg-a at sector i in triangle j . It should also be noted that the operation time of the vectors of each triangle in this switching strategy is determined by the times indicated in each triangle shown in Fig. 3. The switching strategy shown in Table 3 is the most appropriate strategy among the other switching strategies of the SVPWM [23] because it:

- Minimizes the THD in the line voltage
- Has the minimum THD in the phase voltage in 60% of the modulation index interval
- Creates the minimum number of the harmonic orders in both the line and the phase voltage, resulting in the minimum distortion power losses
- Has the minimum ratio of harmonic orders to the fundamental order
- Has the minimum switching losses to switching frequency ratio

- Has a low dependency of the THD on the high harmonic orders in the high modulation index.
- Reduces the size of the filter inductance (L_f). This is because the order of the low order harmonic (LOH) increases
- Creates the minimum power and switching losses in the 50% and 100% modulation index interval, respectively
- Produces the maximum number of levels in the line or phase voltage
- Provides rapid damping of the distortion factor (DF) of the line and the phase voltage versus the switching frequency. Because of this rapid damping, DF is independent of the switching frequency
- Reduces the transient time for one cycle period to obtain a sinusoidal voltage and load current



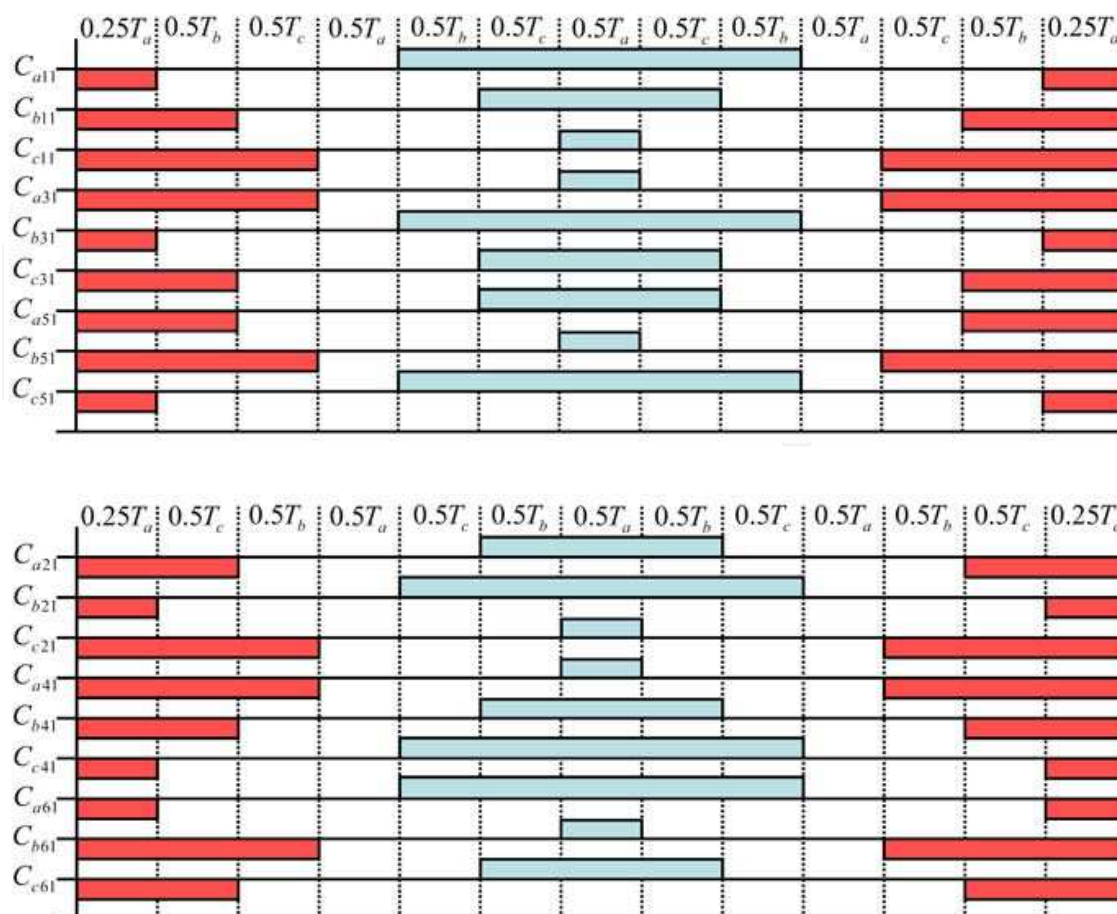


Table 3. The implemented switching strategy in the three-level NPC inverter with Space Vector Pulse Width Modulation

3. A novel switching strategy for the two-quadrant three-level chopper

As was previously discussed, the SMES control methods for stabilizing capacitors voltage depends upon the power networks. In the first control approach, the transmitted active and reactive power to the network is controlled by a NPC voltage source inverter, while the capacitors voltage is stabilized using a chopper. This approach is used to investigate the interaction between the SMES and the power networks. This control approach is easily implemented if an optimized and appropriate switching strategy for the chopper is defined; 5 shows a two-quadrant three-level chopper that was studied in this work.

In Table 4, all possible switching states in the three-level chopper as well as the SMES coil current path are provided. One of the main requirements for the switching strategy of the multi-level choppers is to minimize both the switching losses and the frequency in order to eliminate the need for high frequency electronic switches. Moreover, minimization of the power loss is obtained by minimizing the number of on-switches with the minimum on-time in each switching period. Therefore, the switching states in which each chopper switching period creates the minimum number of displacements in the switching states are selected as the best states for the SMES coil charge and discharge modes. The optimum switching states are highlighted in Table 4; other switching states that do not satisfy the aforementioned conditions were not used [28].

Mode	V_{load}	$(S_{d1}, S_{d2}, S'_{d1}, S'_{d2})$	Current path
FCM	$V_{C1} + V_{C2}$	(1111)	$S'_{d1}, S'_{d2}, S_{d1}, S_{d2}$
CM	V_{C2}	(0111)	$S'_{d1}, S'_{d2}, D_d, S_{d2}$
	0	(0110)	$S'_{d1}, D'_d, D_d, S_{d2}$
	V_{C1}	(1110)	$S'_{d1}, D'_d, S_{d1}, S_{d2}$
FDM	$-V_{C1} - V_{C2}$	(0000)	D_e, D'_e
DM	$-V_{C2}$	(0010)	S'_{d1}, D'_d, D'_e
	0	(0110)	$S'_{d1}, D'_d, D_d, S_{d2}$
	$-V_{C1}$	(0100)	D_e, D_d, S_{d2}
Unusable	0	(1100)	D_e, S_{d1}, S_{d2}
	0	(1101)	D_e, S_{d1}, S_{d2}
	0	(1011)	S'_{d1}, S'_{d2}, D'_e
	0	(0011)	S'_{d1}, S'_{d2}, D'_e
	$-V_{C1}$	(0101)	D_e, D_d, S_{d2}
	$-V_{C1} - V_{C2}$	(1010)	D_e, D'_e
	$-V_{C1} - V_{C2}$	(1001)	D_e, D'_e
	$-V_{C1} - V_{C2}$	(1000)	D_e, D'_e
	$-V_{C1} - V_{C2}$	(0001)	D_e, D'_e

Table 4. Switching states in a two-quadrant three-level chopper

Another requirement in the switching strategy of the multi-level choppers is the independent action of the capacitors voltage controllers. The switching strategy that satisfies the two cited requirements is outlined in Table 5. The charge and discharge modes (CM and DM) in Table 5 are obtained from the proper states in Table 4, assuming that the chopper switching period is $2T_{ch}$.

Note that T_o and T_u are, respectively, the operation times that the voltage of the upper and lower capacitors are connected to the positive and the negative polarities of the load during the charge and the discharge modes. Also, T_z is the chopper operation time when the load is short circuit; this occurs at both the charge and discharge modes. Hence, the duty cycles of the chopper can be defined as follows:

$$d_o = T_o/2T_{ch}, d_u = T_u/2T_{ch}, T_o + T_u + T_z = 2T_{ch} \quad (13)$$

From this equation, it can be seen that d_o , d_u , and d_z vary within the range $[0, 1]$. Also, Table 5 shows that in the charge and the discharge modes, $d_o + d_u$ is always less than one, which means that the required time for compensating the capacitor voltage to the reference voltage is less than a single switching period of the chopper. In other words, if $d_o + d_u$ is more than one, the required time for the compensation of the capacitors voltage to the reference voltage will be more than a single switching period of the chopper.

In this case, the compensation of the capacitors voltage to the reference voltage should be performed simultaneously. The fast charge and discharge (FCM and FDM) modes have

been considered for this case; note that in changing from the fast charge mode to the charge mode, or from the fast discharge mode to the discharge mode and vice versa, the minimum number of switch displacements of each chopper switching period occurs, resulting in a minimum of switching losses presenting an advantage of the proposed switching strategy.

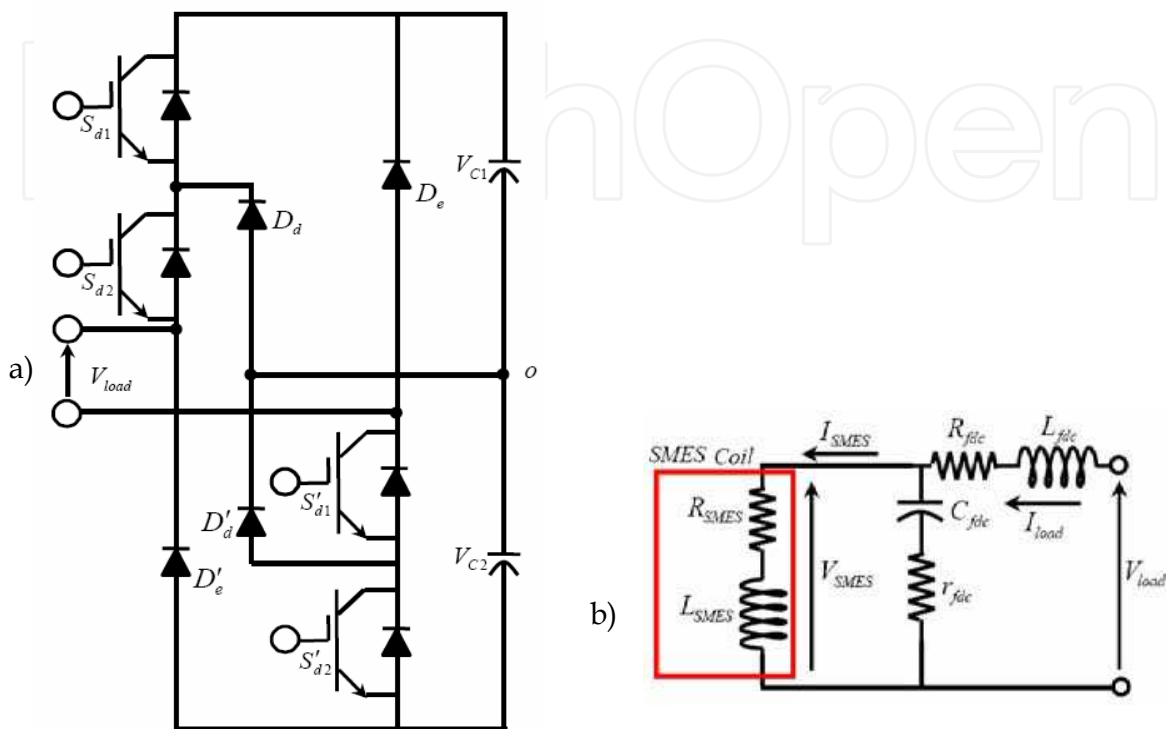


Fig. 5. a) The two-quadrant three-level chopper, b) The load (DC filter and SMES coil)

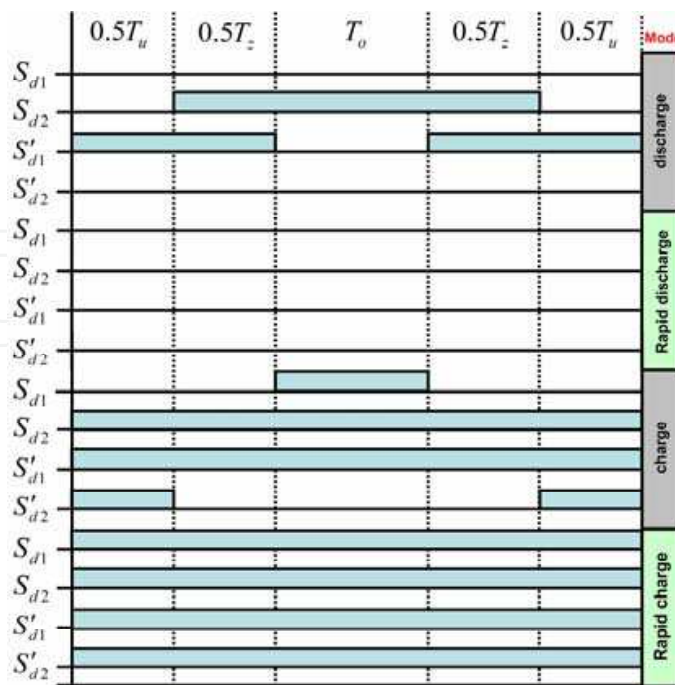


Table 5. The implemented switching strategy in the two-quadrant three-level chopper

4. Chopper duty cycle controller design

In this section, a block diagram for generating the duty cycle of CM and FCM is presented (Fig. 6). To enhance the system dynamic response when balancing the capacitors voltage, it is necessary to ensure that the capacitors voltages are equal prior to connecting the inverter to the power network. To achieve this, the voltages of the upper and the lower capacitors are compared with the reference voltage, which is assumed to be $0.5V_{dc}$, as seen in Fig. 6. Subsequently, the difference in the voltages is passed through the limiters with $[0 \ 0.5]$ interval. These limiters work so that each capacitor is charged for only 50% of the switching period; in fact, the outputs of these limiters can only produce the charge mode (CM). After connecting the inverter to the power network, the PI controllers begin operating and the voltage errors are fed to these controllers. Using the signal holders, the outputs of the PI controllers are sampled every $2T_{ch}$ period. The signal holders with a $2T_{ch}$ sampling time are used to avoid abrupt variations in the duty cycles. If the duty cycles vary abruptly, the turn on/off times should be zero, but this is practically impossible. The signal holder outputs are passed through the limiters with $[0 \ 1]$ interval; these limiters can produce both the charge and the fast charge modes (CM, FCM).

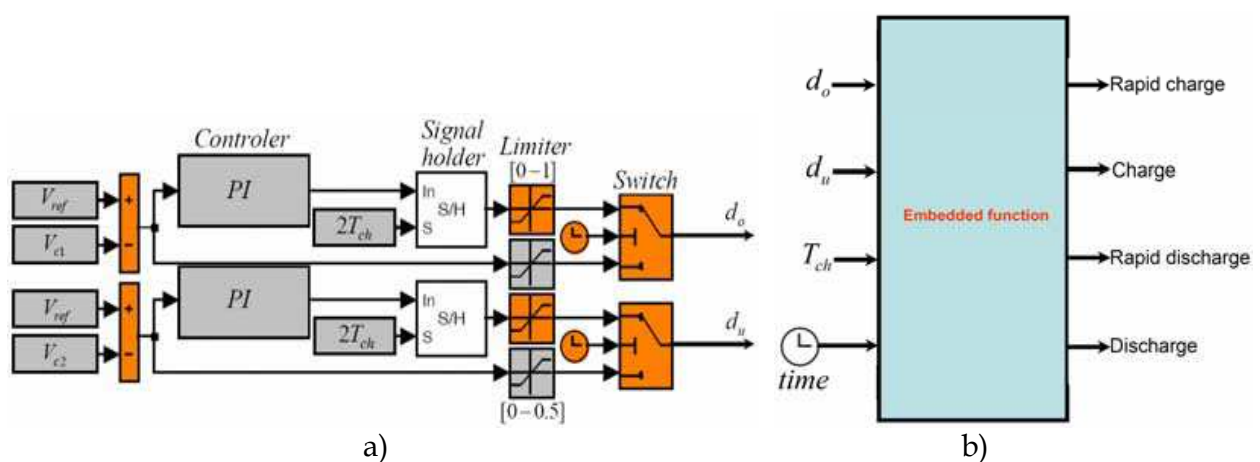


Fig. 6. The chopper duty cycle controller

With the availability of d_o , d_u , T_{ch} , and by using the Embedded MATLAB Functions shown in Fig. 6, the various modes of the chopper (CM, FCM, DM, and FDM) can be determined. Finally using these modes, the corresponding switching strategies are applied to the chopper switches based on Table 5.

5. Simulation results of the switching strategy of the three-level chopper

In this section, the strategies presented in sections 2 through 4 are simulated using MATLAB® software. The power network to which the SMES is connected is shown in Fig. 7 and was modeled using the M-file in MATLAB®. The power network and the SMES parameters are given in Appendix I.

In Fig. 8, the SMES performance using the developed approaches is compared with that of the SMES when the capacitors of the three-level NPC inverter are replaced with equal and ideal voltage sources (SMES with ideal VSI). These comparisons are from the perspective of the THD and the DF of the inverter output line voltage. As seen in this figure, the

performance of the SMES using the chopper duty cycle controller is the same as that of the SMES with an ideal VSI.

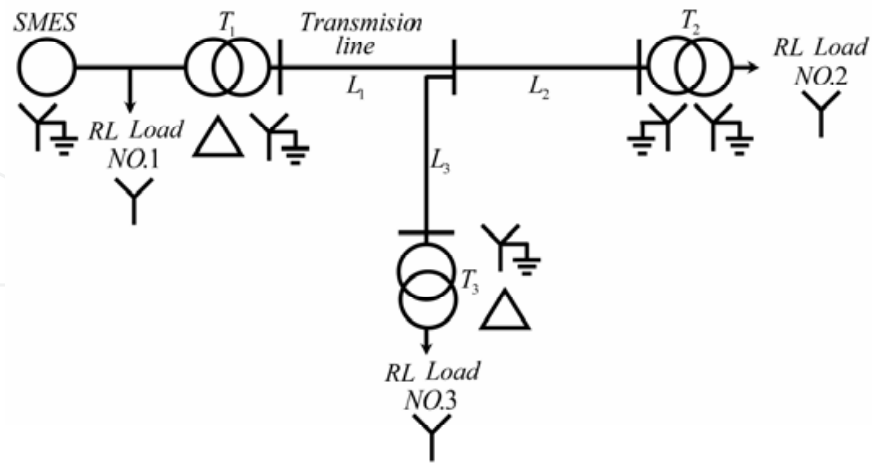


Fig. 7. The power network

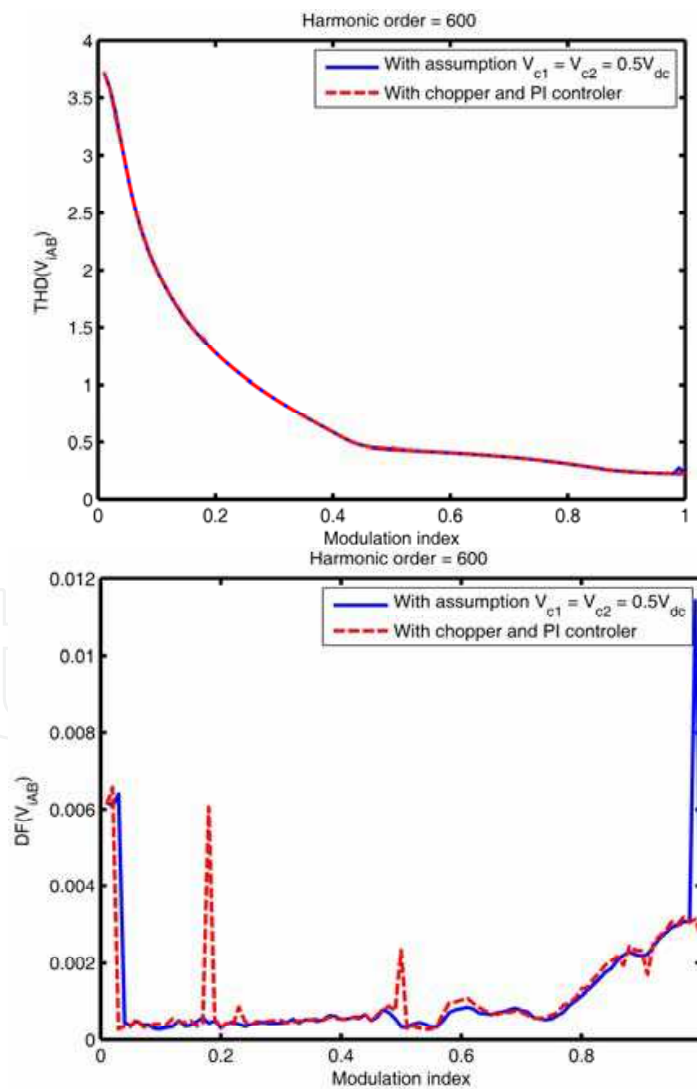


Fig. 8. THD and DF variation of the inverter output line voltage

Fig. 9 shows the voltage variation of the capacitors versus the modulation index; this figure indicates that the proposed schemes are capable of stabilizing the capacitors voltage to the reference voltage (with less than 0.5% error in the worst case scenario). The smallest voltage variation (with 0.0625% error) is obtained when the modulation index is 0.65, as shown in Figure 9. This is because PI controllers have been regulated for this modulation index; in short, the variation of the capacitor voltage depends on both the modulation index and the parameters of the PI controllers. Therefore, in order to obtain the best results, it is recommended that the parameters of the PI controllers be deregulated for each modulation index.

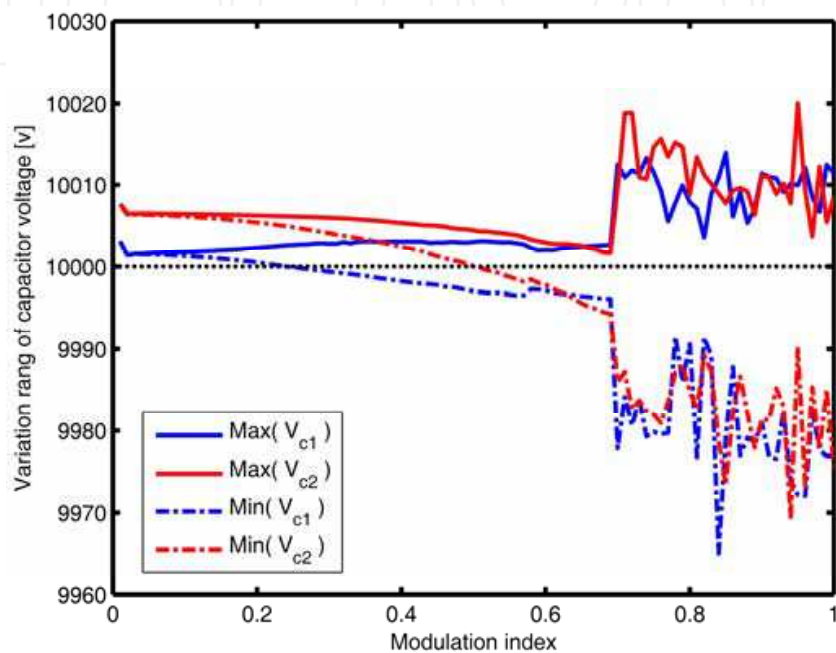


Fig. 9. The capacitors voltage variation versus index modulation

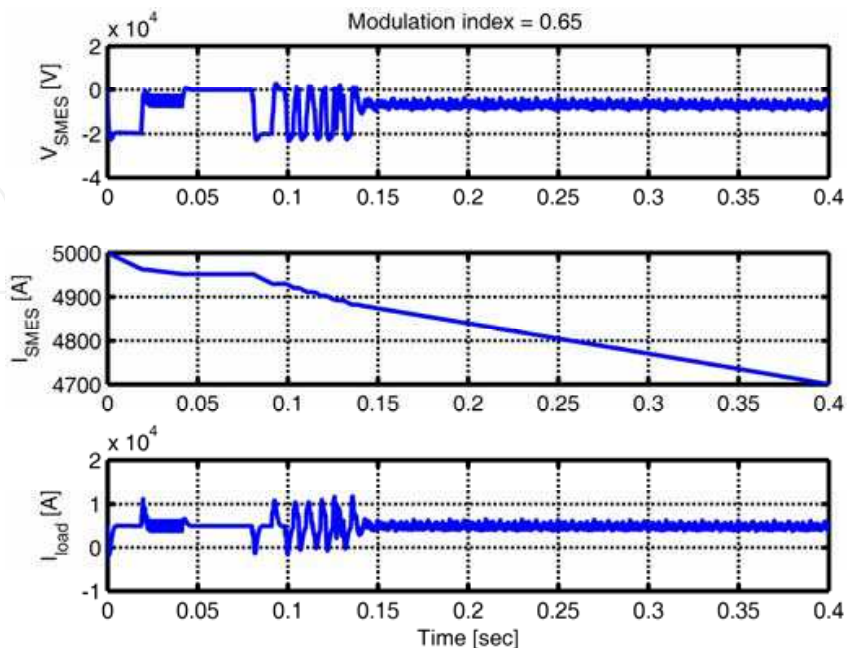


Fig. 10. The current and the voltage of the SMES coil and the current of the load

Fig. 10 shows the voltage and current of the SMES coil and the current of the load. From this figure, it can be seen that the current of the SMES coil is decreasing, or rather, that the stored energy in the coil is discharging. The discharged energy is transmitted to the chopper in the active power form because in this transmission, the current of the load and the voltage of the SMES coil remain constant.

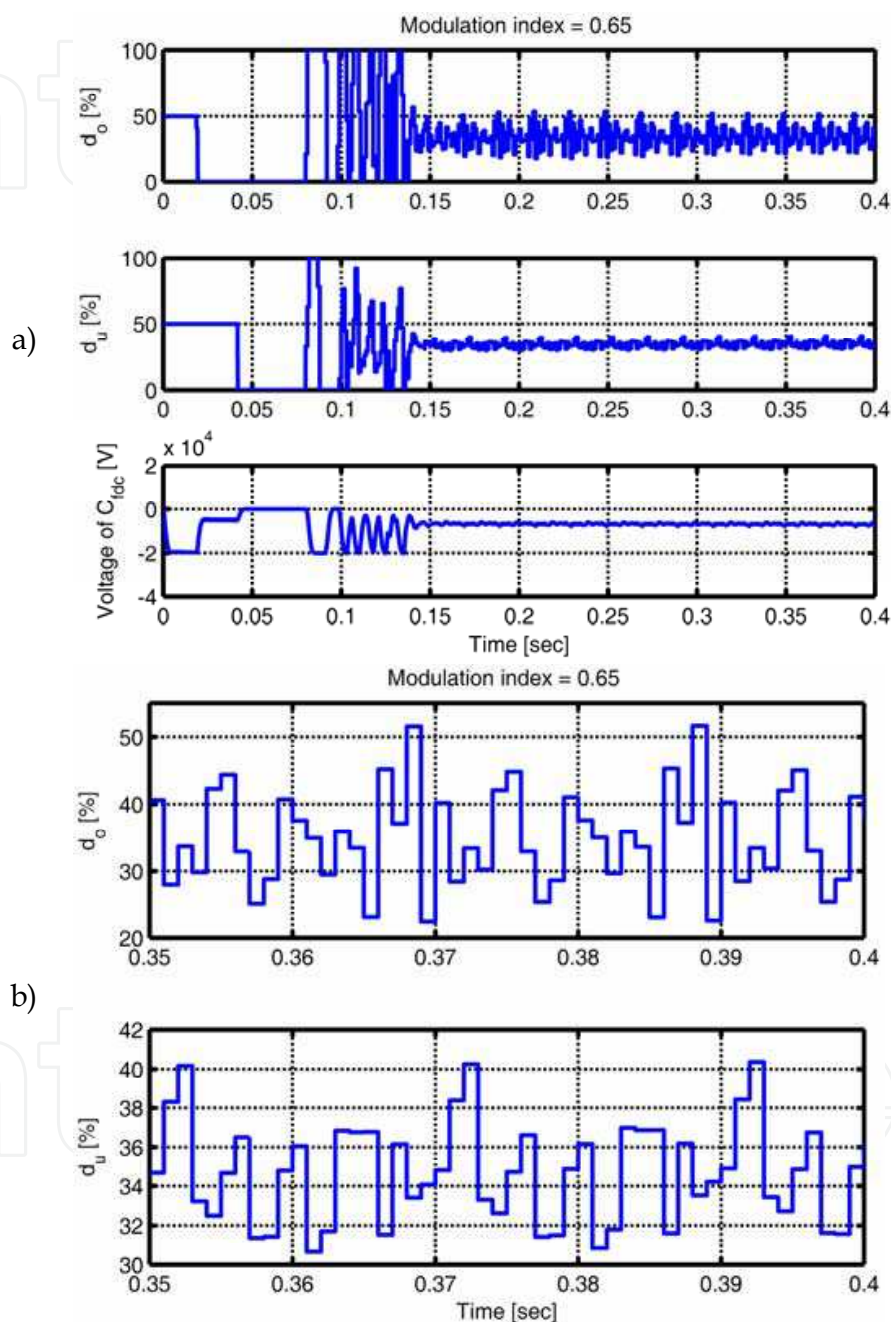


Fig. 11. a) The voltage of the capacitor C_{filt} and the chopper duty cycle percent, b) Steady state duty cycle percent

Fig. 11 depicts the variation of the chopper duty cycle and the voltage of the DC filter capacitor. In this figure, the inverter is connected to the power network at $t = 0.08$ [sec]. It is concluded from this figure that before $t = 0.08$ [sec], the CM mode has been selected by the

Embedded MATLAB function, and after this time, both the CM and the FCM modes have been selected as well. Also, as observed in Fig. 11a, the voltage of the C_{fdc} is important in stabilizing the voltage of the SMES coil; Fig. 11b shows that in steady state condition, only the CM mode occurs for this power network.

Fig. 12 shows the voltage variation of the capacitors; the initial voltages of the capacitors C_1 and C_2 were 9800 [V] and 9500 [V], respectively. As noticed in Fig. 12, the proposed switching strategy properly stabilizes the capacitors voltage before and after connecting the inverter to the power network. In Fig. 12, the voltage variations of the capacitors in the steady state condition, as can be verified in Fig. 9, is less than 6.25 [V] (0.062%) Compared with the values defined in the IEEE standard specifications and obtained in [27] (i.e. 1%), this value has been reduced approximately 15 times.

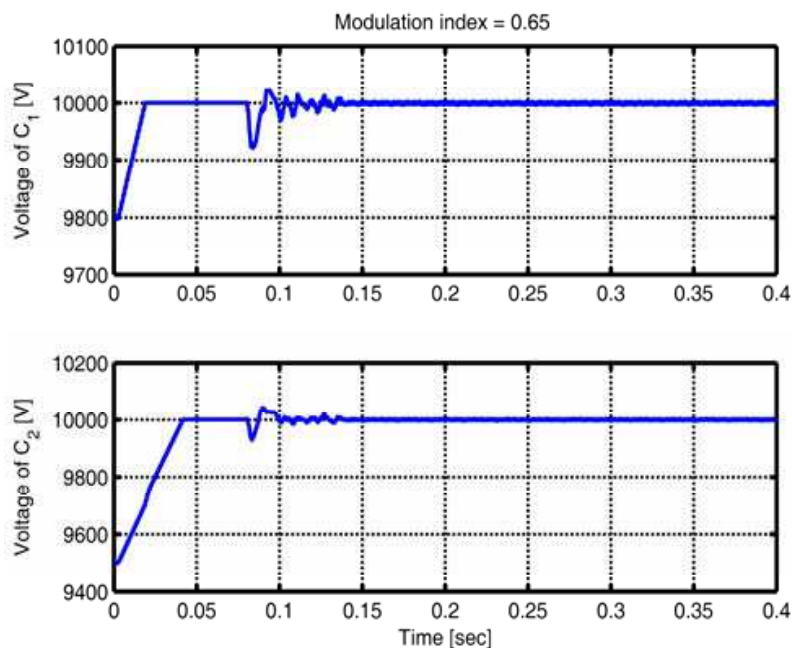


Fig. 12. Variation of the voltage of the capacitors C_1 and C_2

The parameters of the PI controllers, as seen in Appendix I, should be independently tuned for the upper and lower capacitors. This is because when using the SVPWM, the upper and the lower capacitors are not discharged at the same rate; consequently, the number of the PI controllers should be equal to that of the level of the inverters, and the parameters of each PI controller should be independently tuned. In fact, using this approach, the voltage of the inverter capacitors can be stabilized even when the power network is asymmetric and unbalanced. To verify the simulation results obtained by the proposed switching strategy given in Tables 3 and 4, part of the implemented switching strategy in the inverter and the three-level chopper are shown in Figs. 13 and 14, respectively. These figures show that the carrier waves of the chopper and the inverter are triangular, that the period of these carrier waves for the inverter and the chopper are $2T_s = 0.001$ [sec] and $2T_{ch} = 0.001$ [sec], and that their magnitudes are T_s and T_{ch} , respectively.

In Fig. 15, the steady state line voltage and the current of loads 2 and 3 are shown. Fig. 16 shows the steady state line voltage and the current of the inverter prior to filtering.

Comparisons of Figs. 15 and 16 show that the AC passive filter successfully filters out the current and the voltage harmonics that are produced by the inverter at the load terminals.

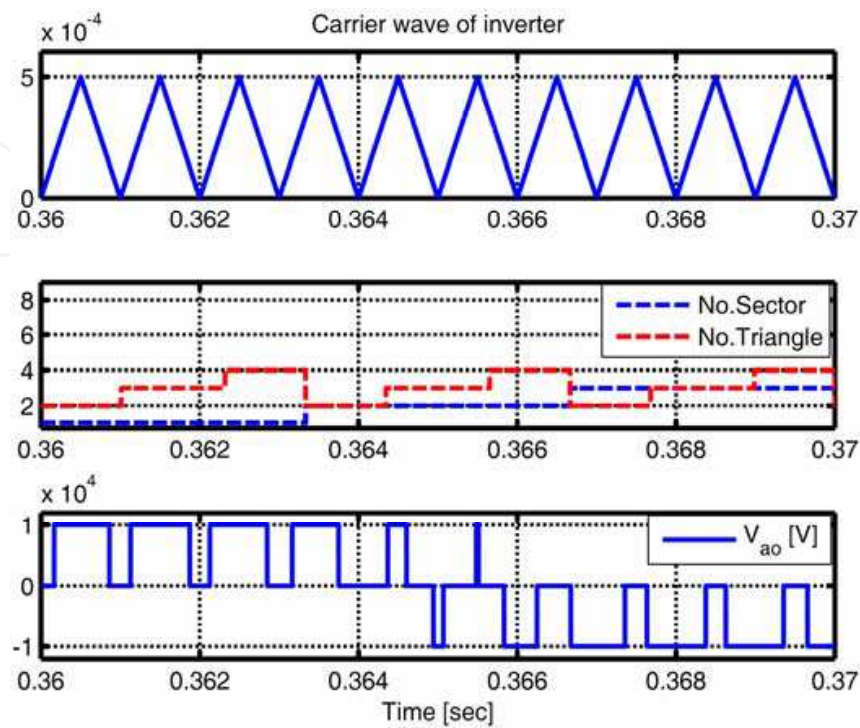


Fig. 13. Part of the proposed switching strategy for the inverter using the SVPWM

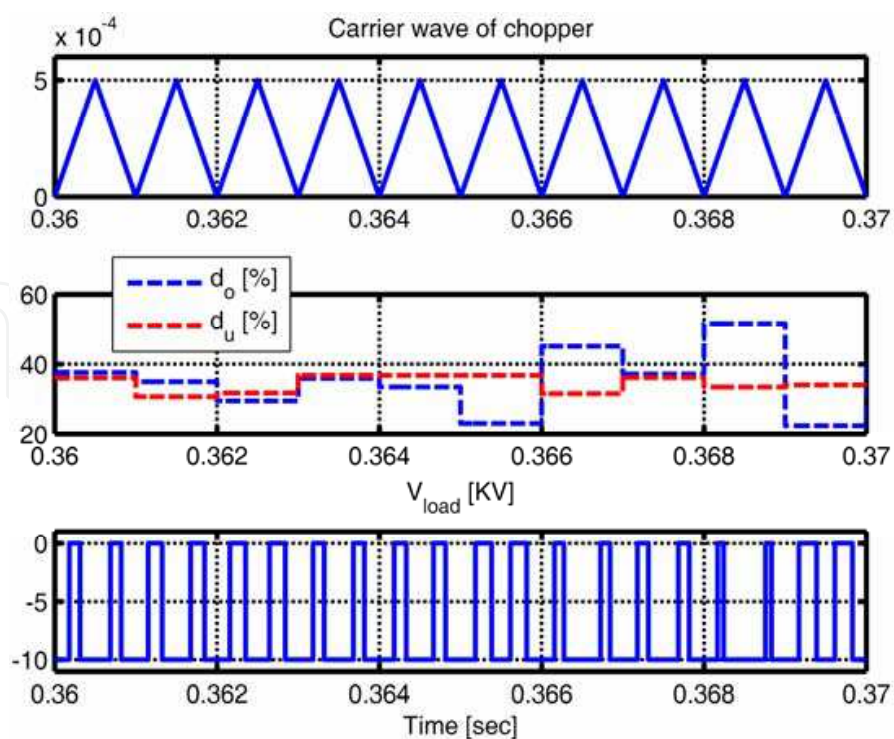
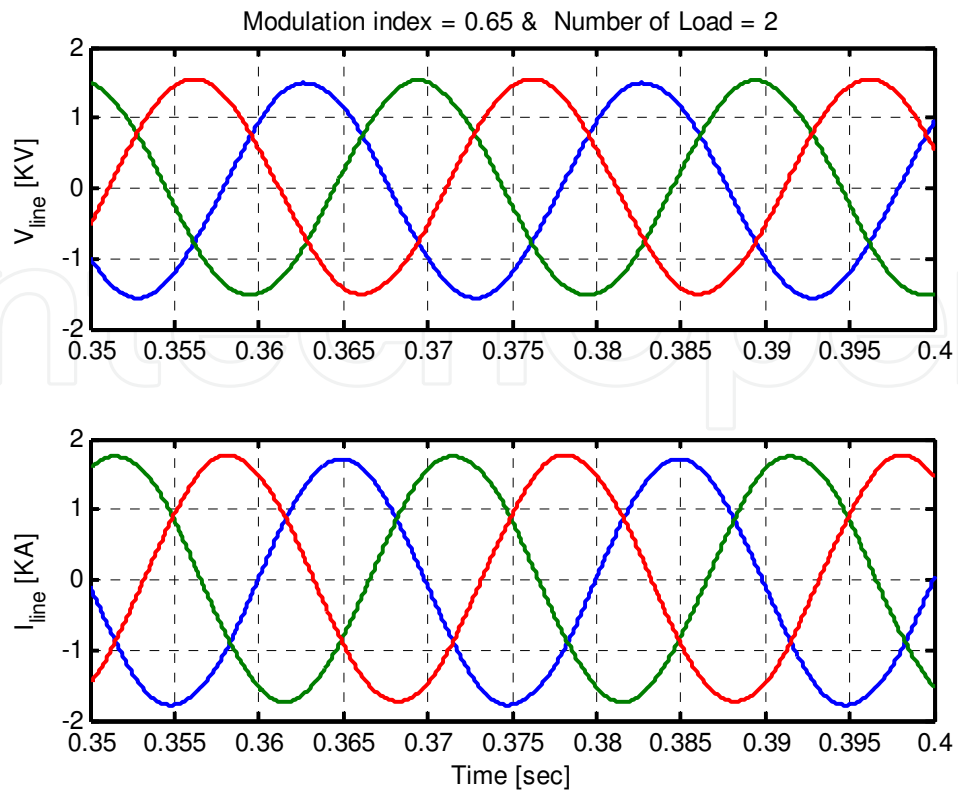
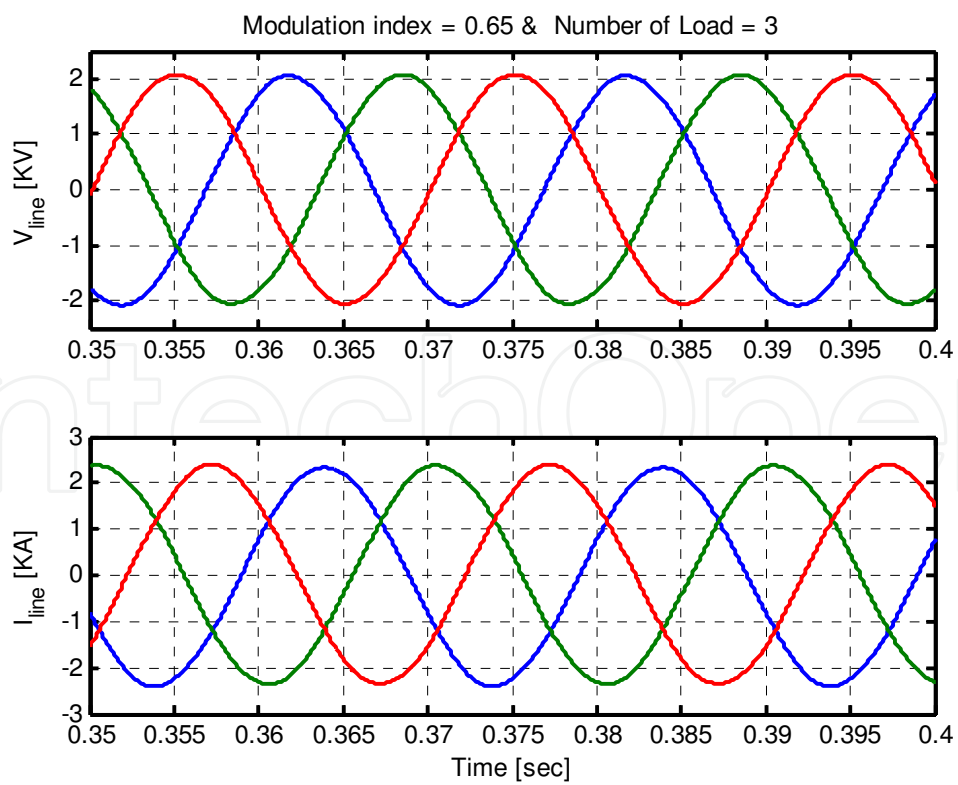


Fig. 14. Part of the proposed switching strategy for the three-level chopper



a)



b)

Fig. 15. Steady state line voltage and the current of the loads: a) No.2, b) No.3.

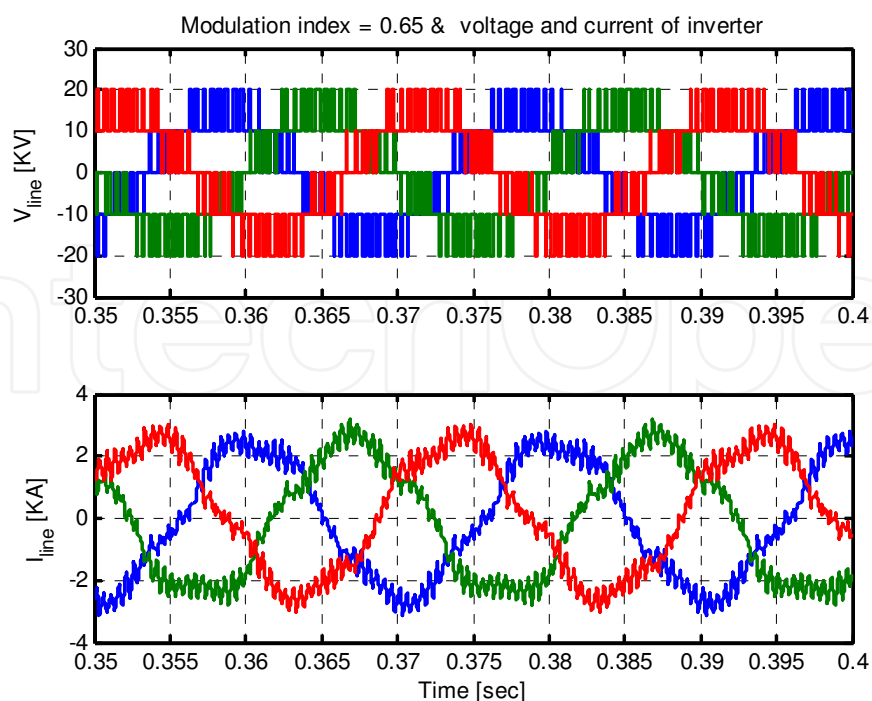


Fig. 16. The steady state output voltage and the current of the inverter

6. Voltage sag compensation algorithm

Here, a new algorithm is presented to compensate the sag voltage in an R-L load using SMES. Fig. 17 shows the configuration of the studied power network, the R-L loads, and the SMES.

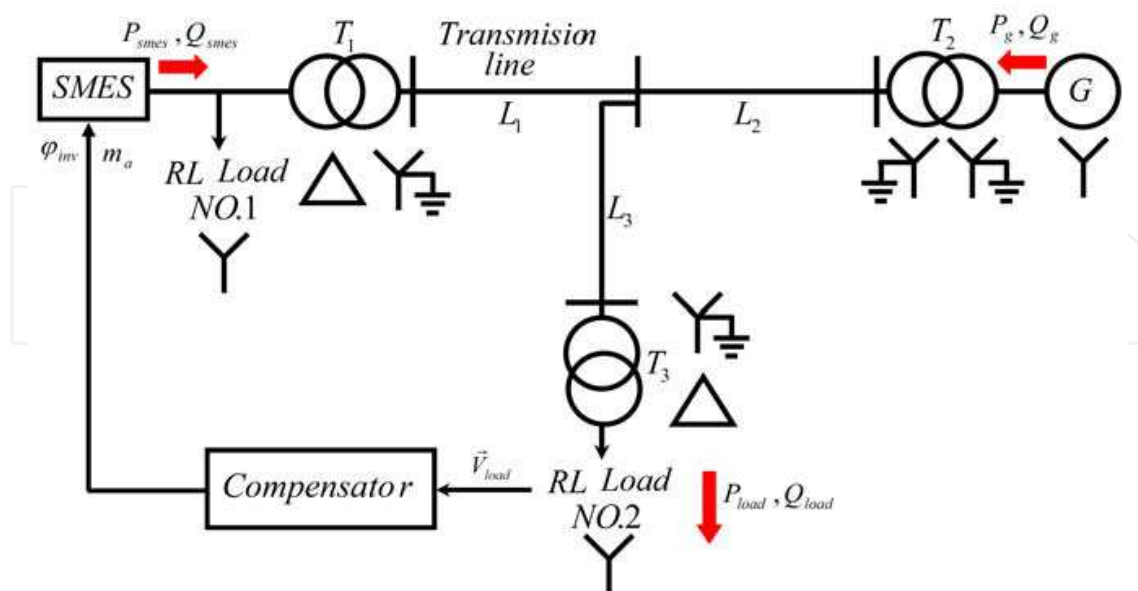


Fig. 17. Configuration of the R-L load, the SMES, and the power network

To compensate the voltage sag using SMES, it is necessary that the proper values of m_a and ϕ_{inv} be calculated and applied to the inverter. If the phasor voltage of the R-L load 2

(resulting only from the generator) before and after the voltage sag is shown by \vec{v}_p and \vec{v}_n , respectively, and the phasor voltage of this R-L load (resulting only from connecting the SMES to the power network) after the voltage sag is shown by \vec{v}_{smes} , then the phasor diagram of the R-L load voltage can be shown as given in Fig. 18, using which, the following equations can be obtained:

$$\varphi_{smes} = \tan^{-1} \left(\frac{v_p \sin \varphi_p - v_n \sin \varphi_n}{v_p \cos \varphi_p - v_n \cos \varphi_n} \right) \quad (14)$$

$$v_{smes} = (v_p \cos \varphi_p - v_n \cos \varphi_n) / \cos \varphi_{smes} \quad (15)$$

By calculating φ_{smes} and v_{smes} from (14) and (15), and by using the power flow that considers only the effect of the SMES system, the values of the m_a and φ_{mv} for applying to the three-level NPC inverter can be calculated.

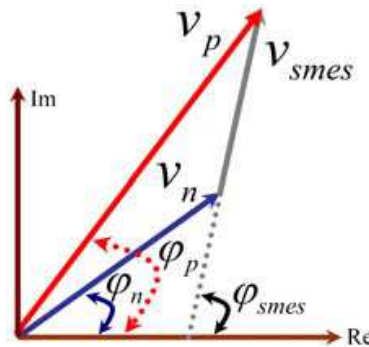


Fig. 18. The phasor diagram of the voltage sag compensation in the R-L load

7. Simulation results and discussion

The power network shown in Fig. 17 was simulated using MATLAB software; the parameters used in this figure are the same as those defined in Fig. 7, and the parameters for the generators are provided in Appendix I; in addition, the sag compensation of the voltage for load 2 using the SMES is shown in Fig. 19. In this study, the voltage of the generator drops to 0.5 [p.u.]; in Fig. 19a, the voltage immediately decreases at $t = 0.5$ [sec] from its full value to the sag value in essentially zero time, while in Fig. 19b, the same observation occurs during one cycle in ramp rate. In Figs. 19a and b, the *Compensator* begins sampling the magnitude and phase of the voltage of load 2 after one cycle and again after three cycles of voltage sag, respectively. As can be seen in this figure, the SMES successfully uses the proposed algorithm and compensates the load voltage in less than one cycle. Performance comparison shows that the dynamic response time of the SMES using the proposed algorithm when compensating for the voltage sag is 5 times faster than that which is presented in [32], and is equal to the responses obtained by the current source inverter (CSI) SMES presented in [33]-[36].

To study the active and reactive powers at steady state, in all other figures that are presented in this section, the *Compensator* is regulated to begin measuring and compensating after three cycles of the voltage sag. Fig. 20 shows the compensation of the phase and the

magnitude of the voltage of load 2. As seen in this figure, the SMES uses the presented algorithm to successfully compensate both the magnitude and the phase of the load voltage and return them to their initial values. In Fig. 20, the voltage variation of the load in steady state condition is approximately 1.1559 [V] (0.0365%), which is 136 times less than the IEEE-519 standard (5%).

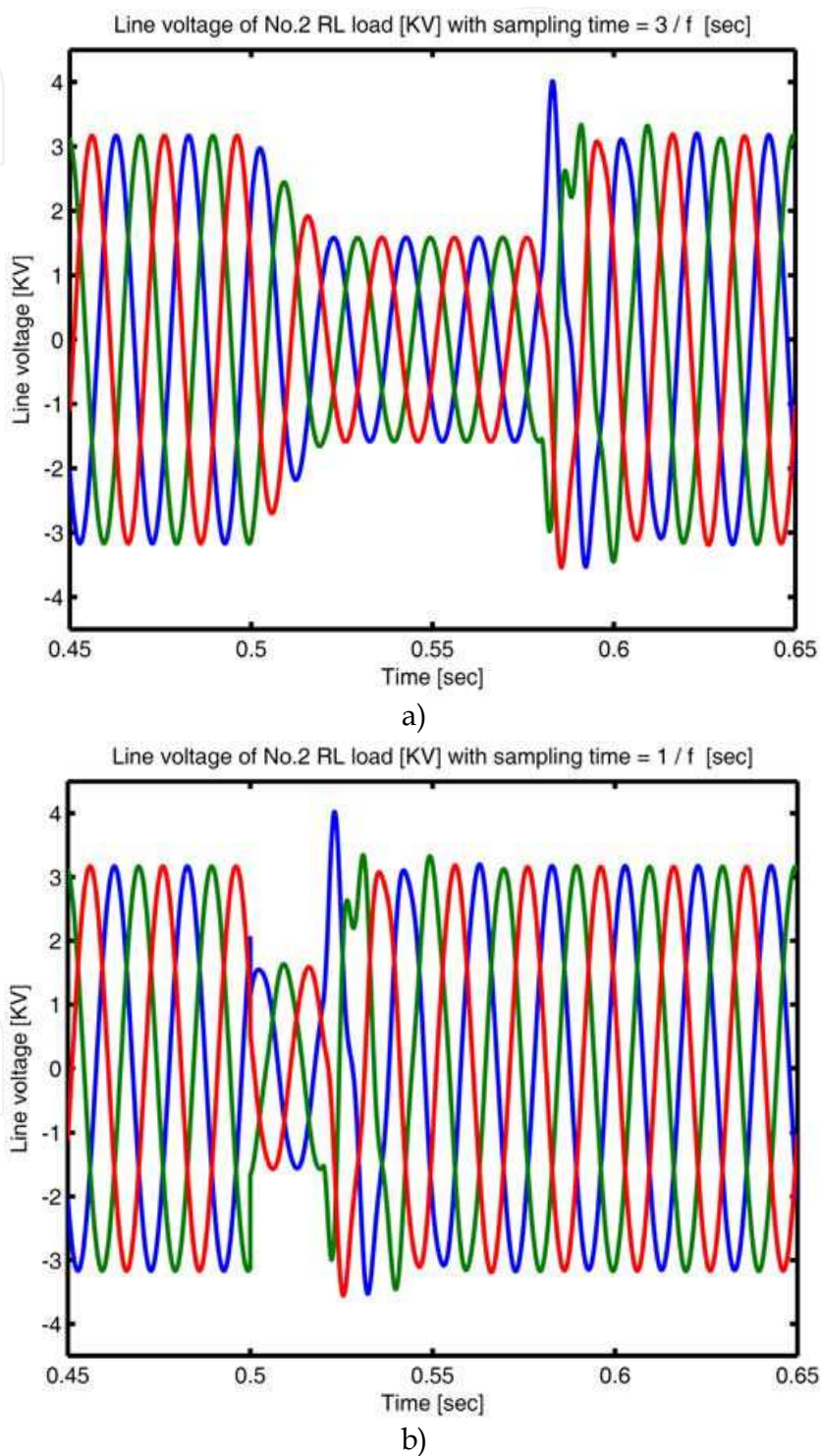


Fig. 19. The voltage sag compensation of the load No. 2

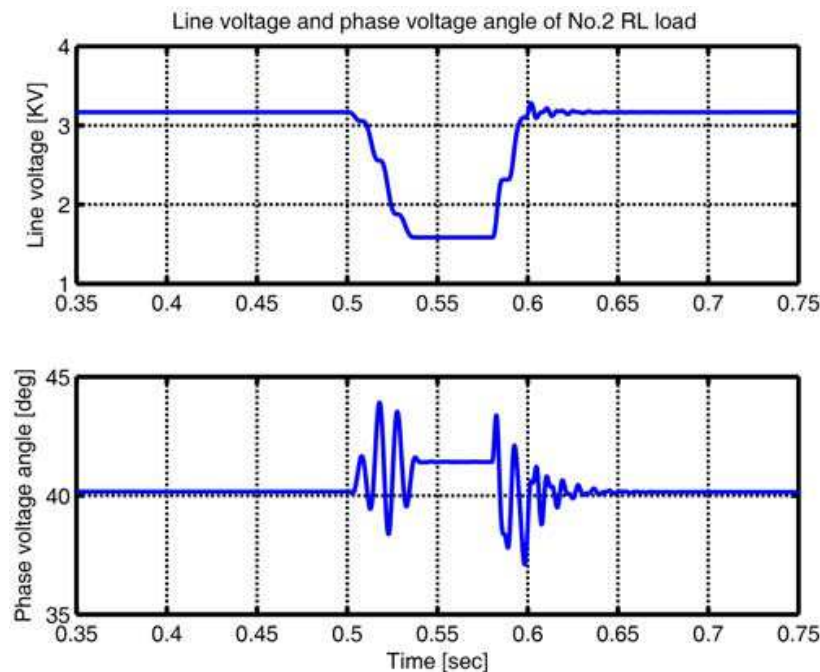


Fig. 20. Compensation of the phase and magnitude of the voltage of the load No. 2.

8. Conclusion

In this study an appropriate switching strategy for the NPC VSI with several advantages for the SMES regarding its ability to improve the performance of this device was presented. Some advantages of using this strategy for the NPC VSI presented in this chapter include:

- Optimizing power quality by implementing a proper switching strategy in SVPWM for VSI SMES
- Better stabilization of the capacitors voltage of the VSI SMES than that of the IEEE standard
- Implementing the rapid charge and discharge modes as opposed to the charge and discharge modes in order to increase the dynamic response time when stabilizing the capacitors voltage of the VSI SMES
- Independent control of the capacitors voltage in the VSI SMES for compensating asymmetric and unbalanced loads
- Minimizing the switching and power losses, resulting in easy and reliable convection from multi-level converter's switches
- Using the proposed switching strategies, resulting in the power quality becoming equal with the case in which the capacitors of the inverter are replaced with an ideal and equivalent voltage source (SMES with ideal VSI)
- Effective and highly reliable performance of the presented strategy when used with a PI control approach
- Compensating capacitors voltage of the VSI SMES prior to connecting the SMES to the power network (stand-by mode)
- Furthermore, an algorithm was presented for the VSI SMES in order to compensate the voltage sag. Some advantages of the proposed algorithm include:
- Compensating the voltage sag and the voltage phase of the load in less than one cycle

- Compensating the active and the reactive power in less than four cycles
- Load voltage stabilizing in good agreement with the IEEE-519 standard

9. Appendix I

The parameters of the PI controllers:

$$KP_O = 0.1, KI_O = 0.1, KP_U = 0.04, KI_U = 0.03$$

Specifications of the transmission line:

$$X_{L1} = 15 [\Omega], R_{L1} = 1.5 [\Omega], X_{L2} = 15 [\Omega], \\ R_{L2} = 1.5 [\Omega], X_{L3} = 30 [\Omega], R_{L3} = 3 [\Omega]$$

Specifications of the synchronous generator:

$$X_G = 0.15 [p.u.], R_G = 0.015 [p.u.], \\ V_G = 20 [KV], S_G = 50 [MVA]$$

Specifications of the transformers:

$$X_{T1} = 0.1 [p.u.], R_{T1} = 0.01 [p.u.], S_{T1} = 30 [MVA], \\ V_{T1} = 20 / 132 [KV], X_{T2} = 0.1 [p.u.], R_{T2} = 0.01 [p.u.], \\ S_{T2} = 30 [MVA], V_{T1} = 132 / 20 [KV], X_{T3} = 0.1 [p.u.], \\ R_{T3} = 0.01 [p.u.], S_{T3} = 50 [MVA], V_{T3} = 132 / 13.2 [KV]$$

Specifications of the R-L loads:

$$L_{RL1} = 2 [mH], R_{RL1} = 5 [\Omega], S_{RL1} = 30 [MVA], \\ V_{RL1} = 18 [KV], L_{RL2} = 0.2 [mH], R_{RL2} = 0.5 [\Omega], \\ S_{RL2} = 30 [MVA], V_{RL2} = 18 [KV], L_{RL3} = 0.2 [mH], \\ R_{RL3} = 0.5 [\Omega], S_{RL3} = 50 [MVA], V_{RL1} = 13.2 [KV]$$

Assumed specifications of the NPC VSI and the SMES:

$$IGBT : SEMIKRONSKM, R_{IGBT} = 0.75 [m\Omega], V_{FO} = 1.1 [V], \\ P_S = 0.05 [W], V_{dc} = 20 [KV], f_{ch} = 2 [KHz], C_f = 400 [\mu F] \\ L_f = 800 [\mu H], L_{fdc} = 1 [mH], R_{fdc} = 20 [m\Omega], M = 0.65, \\ f = 50 [Hz], L_{SMES} = 10 [H], R_{SMES} = 2 [\mu\Omega], C_2 = 200 [mF] \\ C_{fdc} = 700 [\mu F], r_{fdc} = 2 [\Omega], f_s = 2 [KHz], C_1 = 200 [mF]$$

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