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Pole-Zero-Cancellation Technique for DC-DC Converter

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1. Introduction

Many types of electric equipments are digitized in recent years. However, the configuration of switch mode power supply is still only analog circuit because the analog circuit is held down to low cost. The digitized system is operated on the basis of a processor. When the switch mode power supply is treated as a part of the system, it is difficult that switch mode power supply inhabit alone in the system as the analog-circuit. Therefore, the digitization of the switch mode power supply is necessary to harmonize with other electronic circuits in the system. So far, various examinations have been discussed about digitally controlled switch mode power supplies[1-5]. However, important parameters such as the switching frequency were impractical because the performance of processor was not so good. Recently, due to the development of the semiconductor manufacture technology, the performance of processor such as DSP and FPGA is developed remarkably. Hence, the expectation of the practical realization in the digitally controlled switch mode power supply becomes higher.

So far, in many case on digitally controlled switch mode power supply, the control system is constructed by very complicated, difficult modern control theory (nonlinear control theory) such as adaptive control or predictive control.

Moreover, also in the most popular and easiest control method such as PID control, the design method is not so clear, and the optimal design is difficult[6, 7].

On the other hand, there are two methods of controller design. One is the digital direct design. The other is the digital redesign. The digital redesign method converts the analog compensator which is designed on s-region into digital compensator. The digital redesign method has some advantages. For example, the control system is designed from classical control theory (linear control theory).

Therefore, many experiences and design techniques of the conventional analog compensator can be utilized. Moreover, from the practical stance, the digital redesign method is more realistic than digital direct design.

This paper investigates the digitally controlled switch mode power supply by means of classical control theory. Especially, the interesting control technique which is cancelled the transfer function of the converter by using pole-zero-cancellation technique is introduced. This technique is very simple and stability design of converter system is very easy.

Furthermore, the arbitrary frequency characteristics can be created by introducing a new frequency characteristic. Here, the design method and system stability of the proposed control technique is examined by using buck converter as a simple example.

2. Converter analysis

For the design of the control system, it is necessary to grasp correctly the characteristics of the converter in detail. The buck converter as a controlled object is shown in Fig. 1. The dynamic characteristics of buck converter can be derived by applying the state space averaging method[8,9]. The transfer function of duty to output voltage of buck converter is derived following equation;

$$G_{dv}(s) = \frac{\Delta V_o(s)}{\Delta D(s)} = \frac{G_{dvo}(s)}{P(s)} \tag{1}$$

where;

$$P(s) = \frac{s^2}{\omega_o^2} + s\frac{2\delta}{\omega_o} + 1 \tag{2}$$

$$G_{dvo}(s) = \left(\frac{s}{\omega_{esr}} + 1\right)\frac{R}{R + r_L}V_i \tag{3}$$
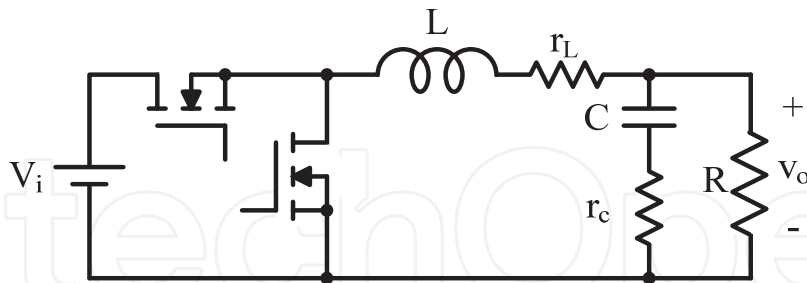
$$\omega_o = \sqrt{\frac{R + r_L}{LC(R + r_c)}} \tag{4}$$

Fig. 1. Synchronous buck converter.

$$\delta = \frac{L + C\{Rr_c + r_L(R + r_c)\}}{2\sqrt{LC(R + r_c)(R + r_L)}} \tag{5}$$

$$\omega_{esr} = \frac{1}{Cr_c} \tag{6}$$

Figure 2 shows the block diagram of analog system. From, Fig. 2, the loop gain of analog controlled converter can be derived following equation;

$$T(s) = \frac{\Delta V_o(s)}{\Delta V_o^*(s)} = \frac{G_{dvo}(s)}{P(s)} \cdot G_c(s) \cdot K \cdot K_s \cdot PWM \qquad (7)$$

where;

Gc(s) : Transfer function of phase compensator

K : DC gain of error amp.

Ks : Sense gain of output voltage

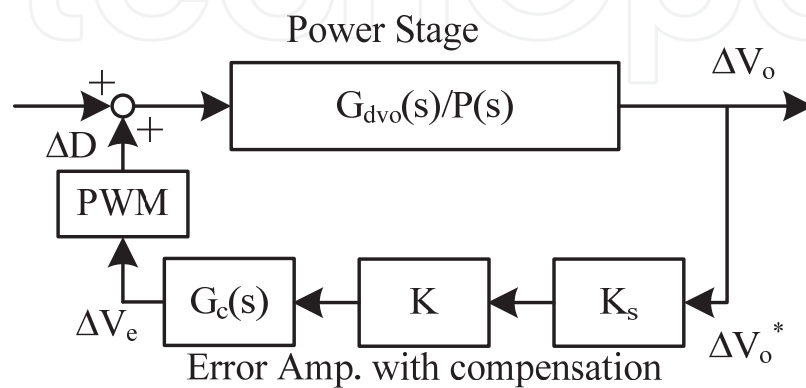PWM : transfer gain of voltage to duty

Fig. 2. Block diagram of analog system.

In order to evaluate the validity of the analytical result, the experimental circuit is implemented by means of the specifications and parameters shown in Table 1.

Symbol	Description	Value
V_i	Input Voltage	12V
V_o/I_o	Load Condition	2.5V/5A
L	Filter Inductor	22μH
C	Filter Capacitor	470μF
r_L	DC Resistance of L	100mΩ
r_c	ESR of C	10mΩ
R	Load Resistance	1Ω
K_s	Sense Gain	0.32
K	Feedback DC Gain	5
PWM	PWM Gain	0.5
fs	Switching Frequency	100kHz

Table 1. Circuit parameters and specifications.

Figure 3 shows the loop gain of the buck converter with p-control in analog control. As shown in Fig. 3, the analytical and experimental results are agreed well. However, as shown in Fig. 4, the big difference is shown in phase characteristics at high frequency side between analog control and digital control.
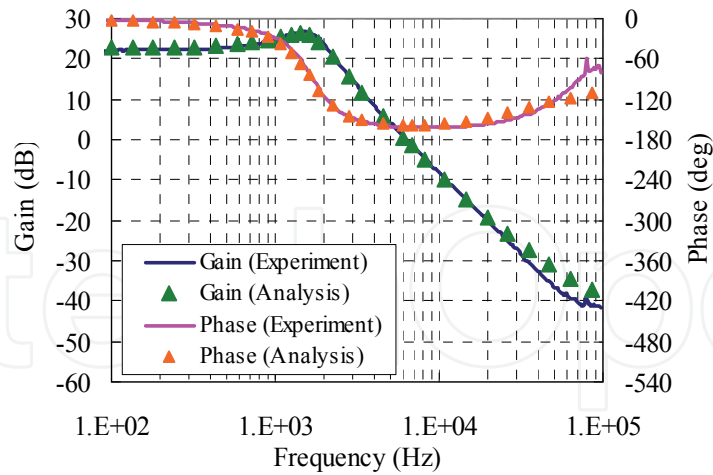
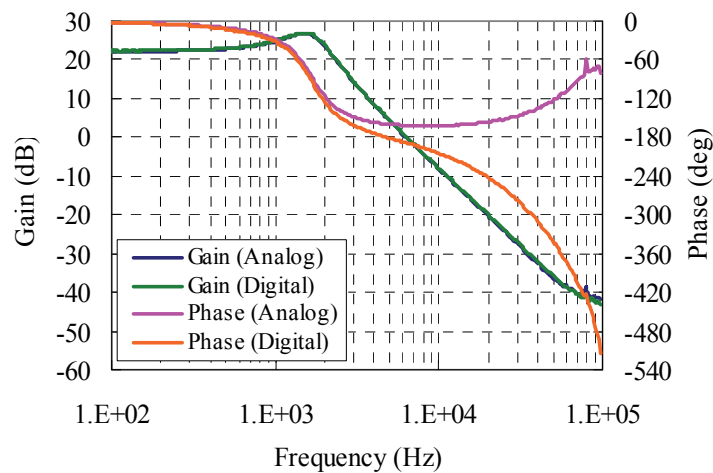Fig. 3. Frequency response of loop gain (analog control).

Fig. 4. Frequency response comparison of analog control and digital control (Experiment).

In digital control system, the output voltage as a detected signal is converted to digital signal by AD converter, after that the converted signal is calculated by DSP. Next, the calculated signal decides the duty ratio of next switching period. Hence, the information of the output voltage as the detected signal at certain switching period is reflected into the duty ratio of the next switching period.

Therefore, the dead time element He(s) is included into the control loop as shown in Fig. 5. From Fig. 5, the loop gain of digital controlled system can be derived following equation;

$$T(s) = \frac{\Delta V_o(s)}{\Delta V_o^*(s)} = \frac{G_{dvo}(s)}{P(s)} \cdot G_c(s) \cdot H_e(s) \cdot K \cdot K_s \cdot PWM \tag{8}$$

where;

$$H_e(s) = e^{-sT_{sample}} \tag{9}$$

Gc(s) : Transfer function of phase compensator
K : DC gain of error amp.
Ks : Sense gain of output voltage
PWM : transfer gain of voltage to duty
He(s) : Dead time component of digital controller
Tsample : Sampling period

Figure 6 shows the frequency response of dead time element He(s). As shown in Fig. 6, the gain characteristic does not depend on frequency and it is constant.
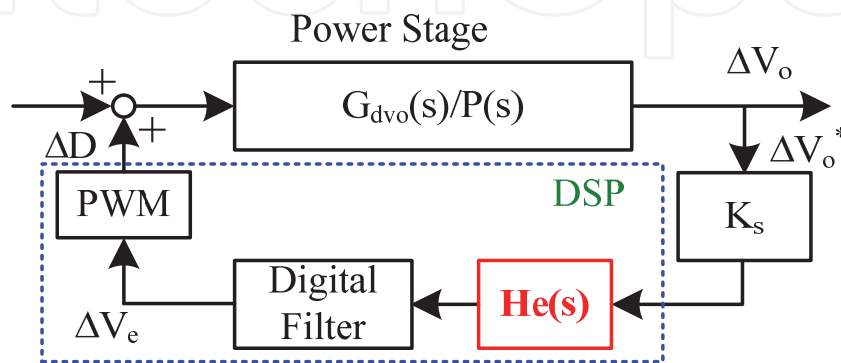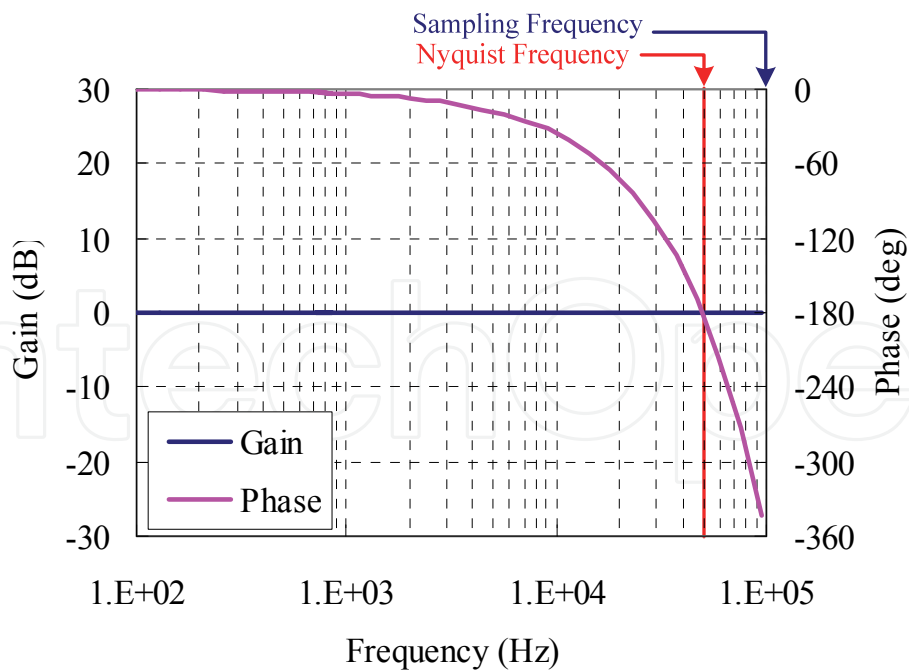

Fig. 5. Block diagram of digital system.

Fig. 6. Frequency response of dead time element He(s).

On the other hand, phase characteristic depends on frequency. The phase is rotated around 180 degrees at Nyquist frequency (=f/2), and it is rotated around 360 degrees at switching

frequency (sampling frequency). From these results, the phase is drastically rotated at high frequency side by the influence of dead time element He(s). In order to evaluate these discussions, the experimental circuit is implemented by means of the specifications and parameters shown in Table 1. Moreover, the experimental result is compared with analytical result. Figure 7 shows the loop gain of the buck converter with p-control in digital control. As shown in Fig. 7, the analytical and experimental results are agreed well. In analog control system, the phase characteristic of frequency response is improved at higher frequency side by the influence of ESR-Zero as shown in Fig. 4, and the system has stable operation.

On the other hand, in digital control system, the phase characteristic of frequency response is drastically rotated by the influence of the dead time element He(s) as shown in Fig. 7. As a result, the phase margin disappears, and the system becomes unstable.

In digital control system, the phase rotation is larger than analog control system by the influence of the dead time element He(s), so the phase compensation is necessary to keep the system stability.
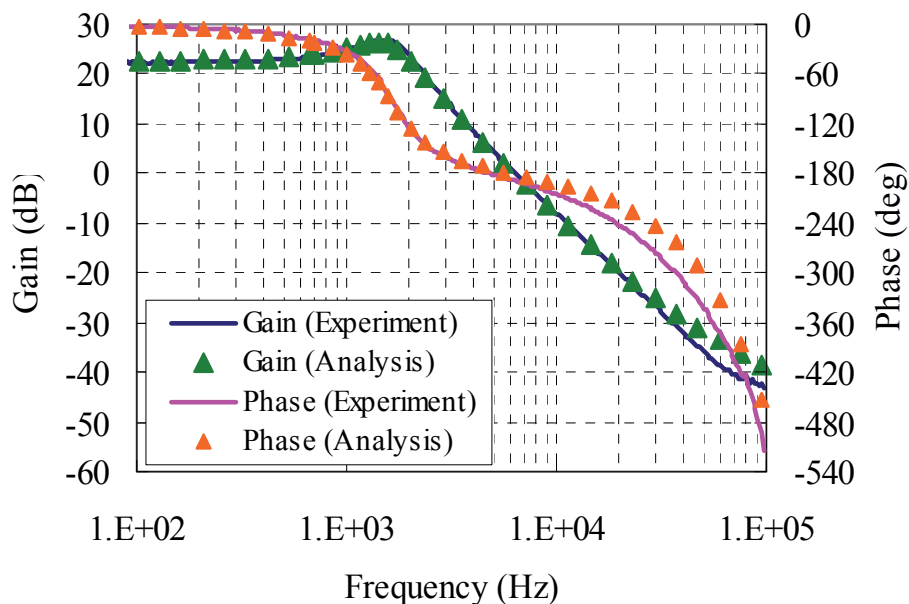

Fig. 7. Frequency response of loop gain (digital control).

3. Conventional phase compensation (Phase lead-lag compensation)

The phase compensation is usually used to improve the system stability. There is various phase compensation. Here, the phase lead-lag compensation is used as the most popular compensation. The digital filter is designed by digital redesign method. The transfer function of phase lead-lag compensation is given by following equation;

$$G_c(s) = \frac{\Delta v_e}{\Delta v_o{}^*} = \frac{K_c\left(\dfrac{s}{\omega_{z1}}+1\right)\left(\dfrac{s}{\omega_{z2}}+1\right)}{\left(\dfrac{s}{\omega_{p1}}+1\right)\left(\dfrac{s}{\omega_{p2}}+1\right)} \tag{10}$$

The digital filter can be realized by means of the bilinear transformation.

$$s = \frac{2}{T_{sample}} \cdot \frac{1 - z^{-1}}{1 + z^{-1}} \tag{11}$$

$$G_c(z) = \frac{\Delta v_e}{\Delta v_o{}^*} = k \frac{z^{-2}B_2 + z^{-1}B_1 + B_0}{z^{-2}A_2 + z^{-1}A_1 + A_0} \tag{12}$$

where;

$$k = K_c \frac{\omega_{p1}\omega_{p2}}{\omega_{z1}\omega_{z2}} \tag{13}$$

$$A_0 = \frac{4}{T_{sample}{}^2} + \frac{2\left(\omega_{p1} + \omega_{p2}\right)}{T_{sample}} + \omega_{p1}\omega_{p2} \tag{14}$$

$$A_1 = -\frac{8}{T_{sample}{}^2} + 2\omega_{p1}\omega_{p2} \tag{15}$$

$$A_2 = \frac{4}{T_{sample}{}^2} - \frac{2\left(\omega_{p1} + \omega_{p2}\right)}{T_{sample}} + \omega_{p1}\omega_{p2} \tag{16}$$

$$B_0 = \frac{4}{T_{sample}{}^2} + \frac{2\left(\omega_{z1} + \omega_{z2}\right)}{T_{sample}} + \omega_{z1}\omega_{z2} \tag{17}$$

$$B_1 = -\frac{8}{T_{sample}{}^2} + 2\omega_{z1}\omega_{z2} \tag{18}$$

$$B_2 = \frac{4}{T_{sample}{}^2} - \frac{2\left(\omega_{z1} + \omega_{z2}\right)}{T_{sample}} + \omega_{z1}\omega_{z2} \tag{19}$$

The determination of the compensator parameter is various. Here, these parameter decide from phase margin. Figure 8 shows the analytical result of loop gain frequency response with phase lead-lag compensation. Where, Kc=10000, fp1=0.03Hz, fz1=1.3kHz, fp2=20kHz, fz2=1.5kHz. As shown in Fig. 8, this system has the stable operation, and then the bandwidth is around 5.5kHz, the phase margin is around 45 degrees. Figure 9 shows the experimental result of loop gain frequency response with phase lead-lag compensation. In this case, the bandwidth is around 5kHz, and the phase margin is around 45 degrees. Moreover, the analytical and experimental results are agreed well. Thus, the observation of control object frequency response is needed in classical control theory (linear control theory).
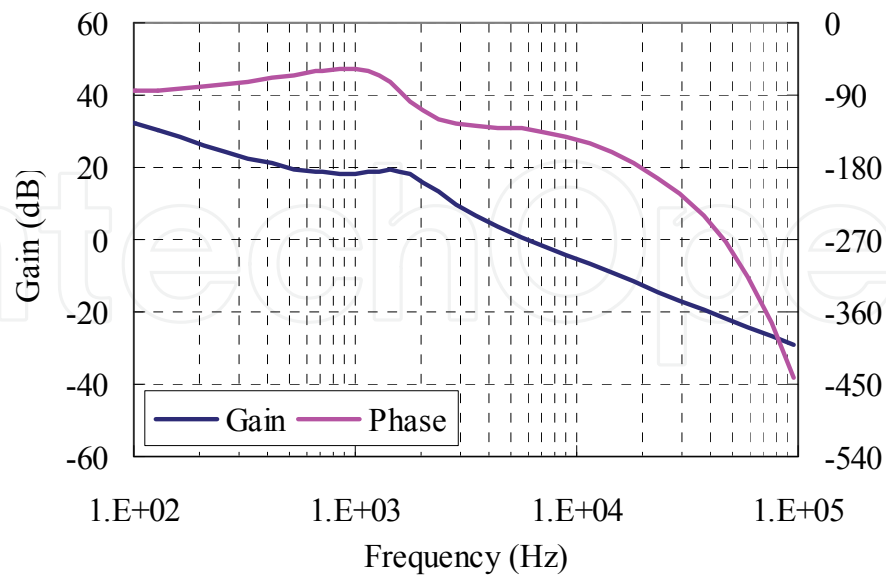
Fig. 8. Frequency response of loop gain with phase lead-lag compensation (analytical result).
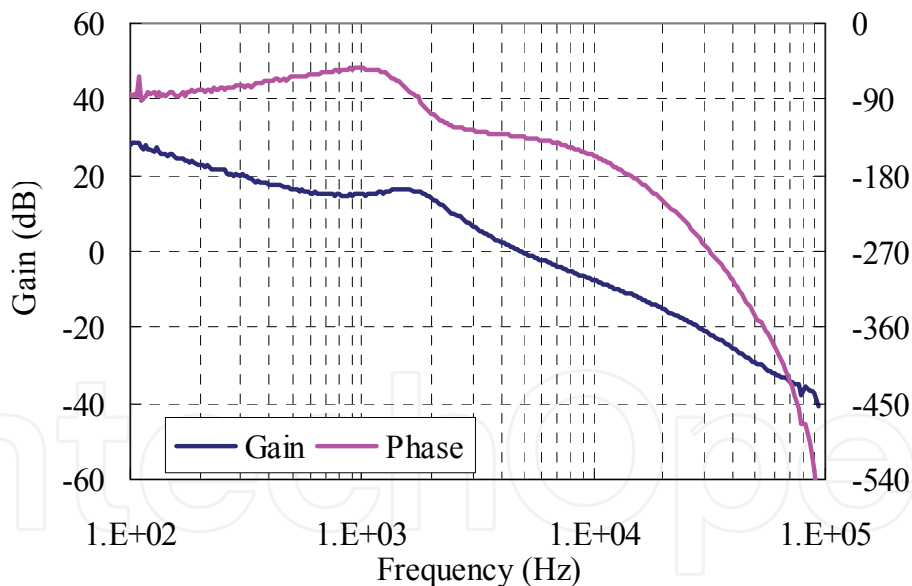

Fig. 9. Frequency response of loop gain with phase lead-lag compensation (experimental result).

Moreover, much experience and knowledge are needed for controller design, because many parameters in compensator should be decided. Therefore, the design method is not so clear and depends on knowledge and experience, and the optimal design is difficult.

The controller design becomes very simple if the controller design is enabled without considering the frequency response of the converter as the control object.

4. Principle of PZC technique

Reduction of the phase rotation is very important for system stability. Especially in the second order system, the phase is drastically rotated around 180 degrees at resonance peak. The stability of the system is improved remarkably if the phase rotation can be reduced.

This paper proposes the control technique which is cancelled the transfer function of the converter power stage by means of pole-zero-cancellation method. The phase rotation and gain change can be suppressed by cancelling the converter power stage characteristics. Furthermore, new characteristic can be designed in the system as the arbitrary transfer function. Figure 10 shows the block diagram of converter system including the pole-zero-cancellation technique.
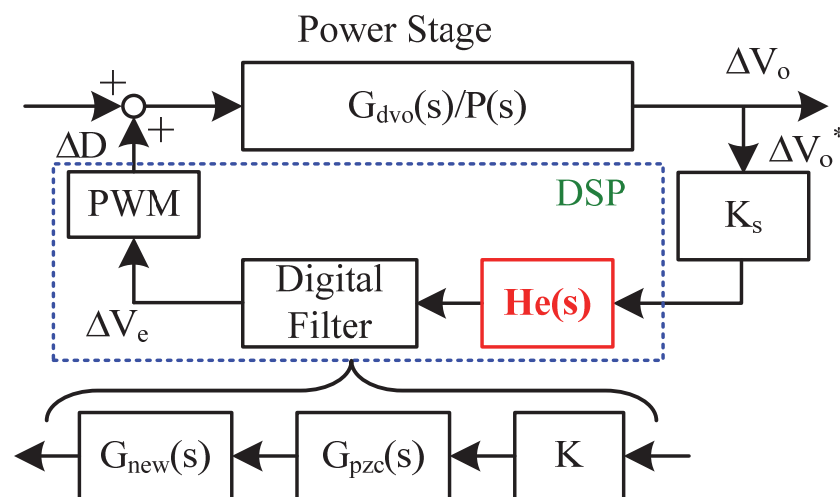

Fig. 10. Block diagram of digital system with PZC control.

From Fig. 10, the transfer function of compensator part is given following equation;

$$G_c(s) = G_{new}(s) \cdot G_{pzc}(s) \tag{20}$$

The Gnew(s) is the arbitrary transfer function. This transfer function decides the frequency response of converter system. Here, the Gnew(s) is defined as first-order low pass filter.

$$G_{new}(s) = \frac{K_c}{\dfrac{s}{\omega_c} + 1} \tag{21}$$

In buck converter case, the resonance peak and ESR-Zero are cancelled. The phase rotation of 180 degree is reduced by cancelling resonance peak. The transfer function of the pole-zero-cancellation Gpzc(s) is given following equation;

$$G_{pzc}(s) = \frac{\dfrac{s^2}{\omega_o{}^2} + s\dfrac{2\delta}{\omega_o} + 1}{\dfrac{s}{\omega_{esr}} + 1} \tag{22}$$

Moreover, the transfer function of the compensator is given following equation;

$$G_c(s) = K_c \frac{\dfrac{s^2}{\omega_o{}^2} + s\dfrac{2\delta}{\omega_o} + 1}{\left(\dfrac{s}{\omega_{esr}} + 1\right)\left(\dfrac{s}{\omega_c} + 1\right)} \tag{23}$$

The digital filter can be realized by means of the bilinear transformation (Eq. 11) as following equation;

$$G_c(z) = \frac{\Delta v_e}{\Delta v_o{}^*} = k\frac{z^{-2}B_2 + z^{-1}B_1 + B_0}{z^{-2}A_2 + z^{-1}A_1 + A_0} \tag{24}$$

where;

$$k = K_c \tag{25}$$

$$A_0 = \frac{4/\omega_{esr}\omega_c}{T_{sample}{}^2} + \frac{2\left(1/\omega_{esr} + 1/\omega_c\right)}{T_{sample}} + 1 \tag{26}$$

$$A_1 = -\frac{8/\omega_{esr}\omega_c}{T_{sample}{}^2} + 2 \tag{27}$$

$$A_2 = \frac{4/\omega_{esr}\omega_c}{T_{sample}{}^2} - \frac{2\left(1/\omega_{esr} + 1/\omega_c\right)}{T_{sample}} + 1 \tag{28}$$

$$B_0 = \frac{4/\omega_o{}^2}{T_{sample}{}^2} + \frac{4\delta/\omega_o}{T_{sample}} + 1 \tag{29}$$

$$B_1 = -\frac{8/\omega_o{}^2}{T_{sample}{}^2} + 2 \tag{30}$$

$$B_2 = \frac{4/\omega_o{}^2}{T_{sample}{}^2} - \frac{4\delta/\omega_o}{T_{sample}} + 1 \tag{31}$$

Figure 11 shows the frequency response of PZC part Gpzc(s). As shown in Fig. 11, the ant resonance peak is appeared at the same frequency of power stage frequency response. Figure 12 shows the analytical result of the loop gain frequency response with PZC technique. Where, Kc=5000, fc=0.01Hz. As shown in Fig. 12, this system has the stable operation, and then the bandwidth is around 400Hz, the phase margin is around 88 degrees.

Moreover, the resonance peak and ESR-Zero are completely cancelled, and this system becomes 1st order response. From these results, the converter frequency response is completely cancelled by the influence of PZC part, and the new characteristic is created (1st order characteristic).

Figure 13 shows the experimental result of loop gain frequency response with PZC technique. In this case, the bandwidth is around 400Hz, and the phase margin is around 89 degrees. Moreover, the analytical and experimental results are agreed well.
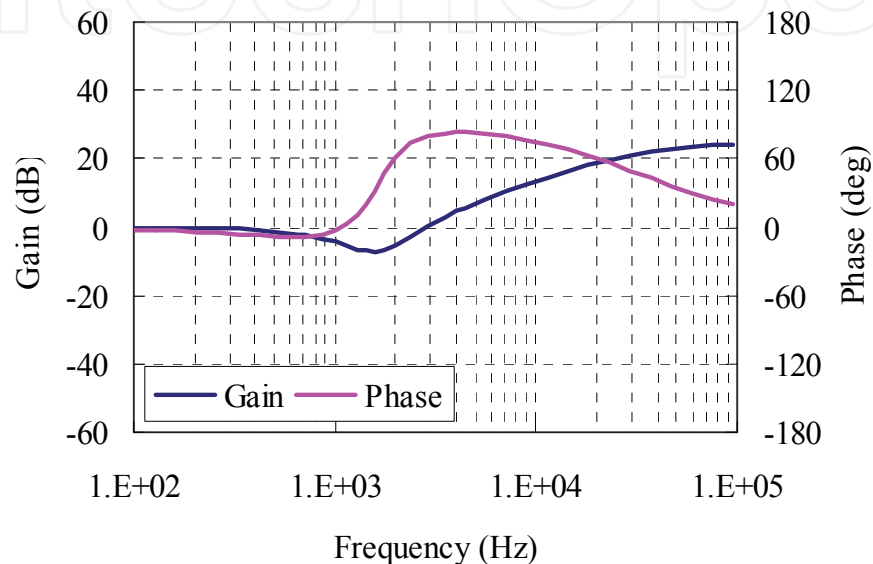
Fig. 11. Frequency response of PZC part (analytical result).
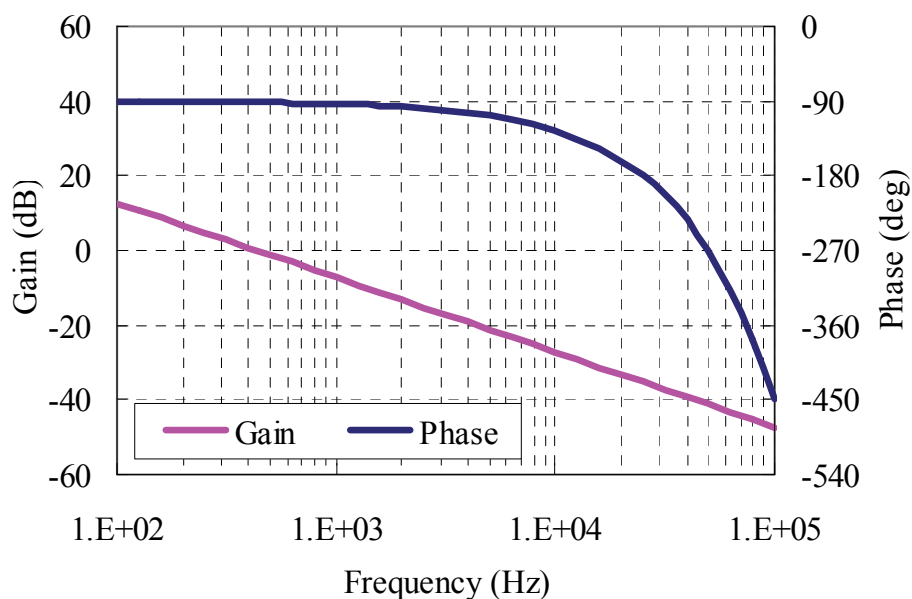
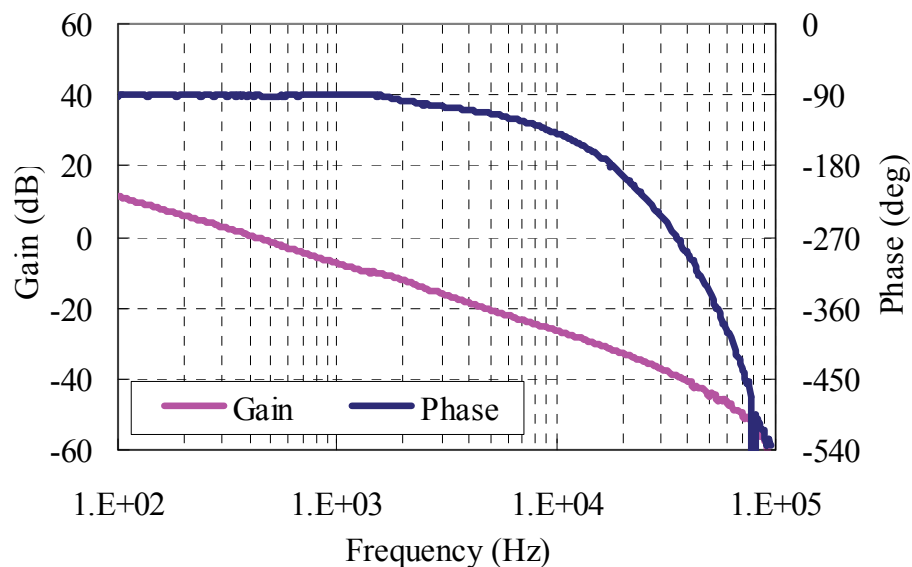Fig. 12. Frequency response of loop gain with PZC technique (analytical result).

Fig. 13. Frequency response of loop gain with PZC technique (experimental result).

5. Optimal design of the new transfer function

The first order low pass filter as Gnew(s) is designed for system stability at previous section. Here, the optimization of the Gnew(s) is considered. At first, the stability margin is investigated. In this case, the integrator is included, so the phase starts -90deg. In addition, the phase is shifted by the influence of dead time element He(s) as shown in Fig. 14. Therefore, when the crossover frequency sets to f_{BW}, the phase margin can be derived as follows;

$$P_m = 90 - \frac{360}{f_s} f_{BW} \tag{32}$$

When f=fs/4, the phase margin becomes zero.

Next, the gain margin is investigated. In this case, this system has 1st order response, so the slope of gain curve becomes -20dB/dec. Therefore, the gain margin can be derived following equation by using the crossover frequency f_{BW} and fs/4.

$$G_m = 20\log_{10}\left(\frac{f_s}{4f_{BW}}\right) \tag{32}$$

From eq. (31), (32), it is clarified that the phase margin and gain margin is automatically decided by the determination of crossover frequency f_{BW}. The Gnew(s) is optimized by means of crossover frequency f_{BW}. The Gnew(s) has two coefficients, ωc and Kc. The coefficient of ωc is decided from Kc and f_{BW}.

The steady state error depends on the output impedance, especially the low frequency component of the closed loop output impedance Zoc. The open loop output impedance can be derived by applying the state space averaging method as following equation;

$$Z_o(s) = \frac{s^2 LCr_c + s(L + Cr_L r_c) + r_L}{s^2 LC + sC(r_L + r_c) + 1} \tag{33}$$

Moreover, the closed loop output impedance given from eq. (7) and (33).

$$Z_{oc}(s) = \frac{Z_o(s)}{1 + T(s)} \tag{34}$$

Therefore, the low frequency component of the closed loop output impedance Zoc can be derived approximately as following equation.
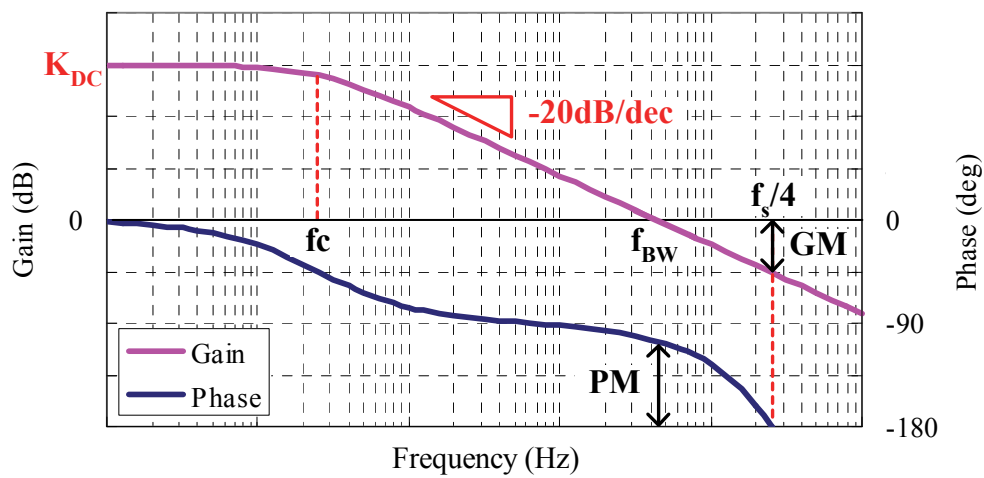

Fig. 14. Frequency response of loop gain with PZC technique for optimal filter design.

$$Z_{oc} = \frac{r_L}{K \cdot K_s \cdot K_c \cdot PWM \cdot V_{in}} \tag{35}$$

The steady state error of the output voltage ΔV is given by Zoc product output current variation ΔIo. Therefore, the coefficient Kc can be derived by determining the tolerance of the output voltage variation. From eq. (35), the coefficient of Kc can be derived approximately as following equation.

$$K_c = \frac{r_L}{Z_{oc} \cdot K \cdot K_s \cdot PWM \cdot V_{in}} \tag{36}$$

Moreover, the total DC gain K$_{DC}$ of loop gain T(s) becomes following equation.

$$K_{DC} = 20\log_{10}\left(K \cdot K_s \cdot K_c \cdot PWM \cdot V_{in}\right) = 20\log_{10}\left(\frac{r_L}{Z_{oc}}\right) \tag{37}$$

The bandwidth f$_{BW}$ and the coefficient of Kc are decided, and the slope of loop gain is -20dB/dec. From these parameters, the total DC gain K$_{DC}$ can be expressed by using f$_{BW}$ and fc as following equation.

$$K_{DC} = 20\log_{10}\left(\frac{f_{BW}}{f_c}\right) \tag{38}$$

From eq. (37), (38), the coefficient of fc is given as following equation.

$$f_c = \frac{Z_{oc}}{r_L} f_{BW} \qquad (39)$$

From mentioned above discussion, the coefficients fc and Kc is optimized. Here, the crossover frequency f_{BW} is set to 10kHz. In this case, the phase margin is around 54 degrees and the gain margin is round 8dB. Moreover, the each coefficient is Kc=42, fc=25Hz. Where, the output impedance is set to around 0.25mΩ.

Figure 15 shows the analytical results of the loop gain frequency response with optimal filter design. As shown in Fig. 15, the bandwidth is around 10kHz, the phase margin is around 50 degrees. Figure 16 shows the experimental results of the loop gain frequency response with optimal filter design. In this case, the bandwidth is around 10kHz, the phase margin is around 50 degrees. Moreover, the analytical and experimental results are agreed well.
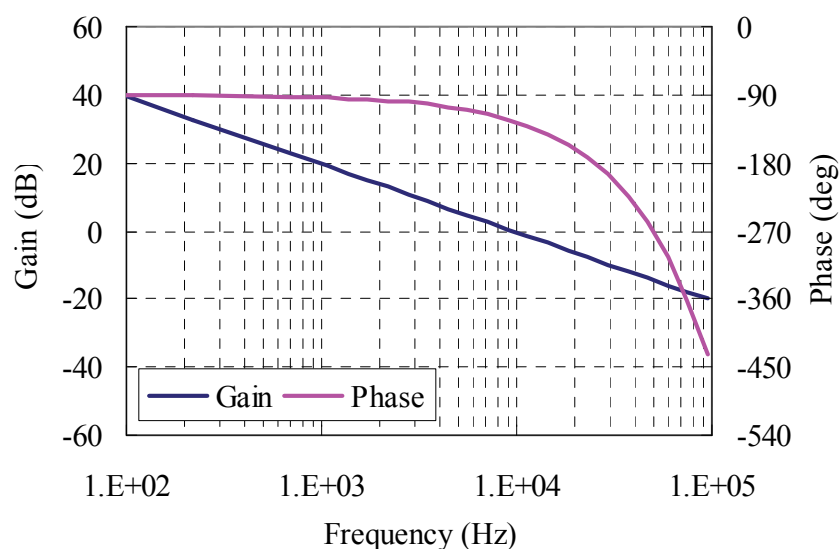

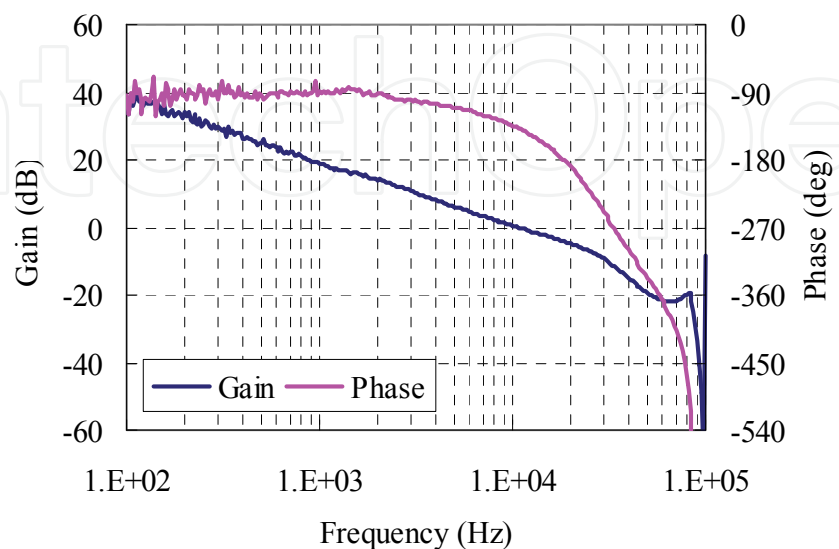Fig. 15. Optimal design of loop gain (analytical result).

Fig. 16. Optimal design of loop gain (experimental result).

Next, the transient response of the conventional phase lead-lag compensation and the PZC technique are measured using experimental circuit of 2.5V/5A during the step load transition from 1A to 4A (10A/µs). Figure 17, 18 shows the transient response of the conventional phase lead-lag compensation and PZC technique, respectively. In phase lead-lag comensation case, the output voltage drop is around 320mV and the transient time to the steady state is around 400µs. On the other hand, in the case with PZC technique, the output voltage drop is around 160mV and the transient time to the steady state is around 200µs as shown in Fig. 15, and the transient response is improved.
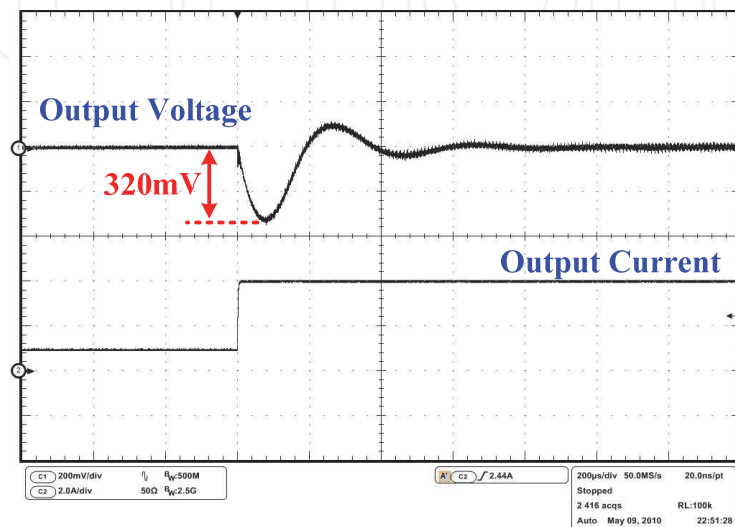

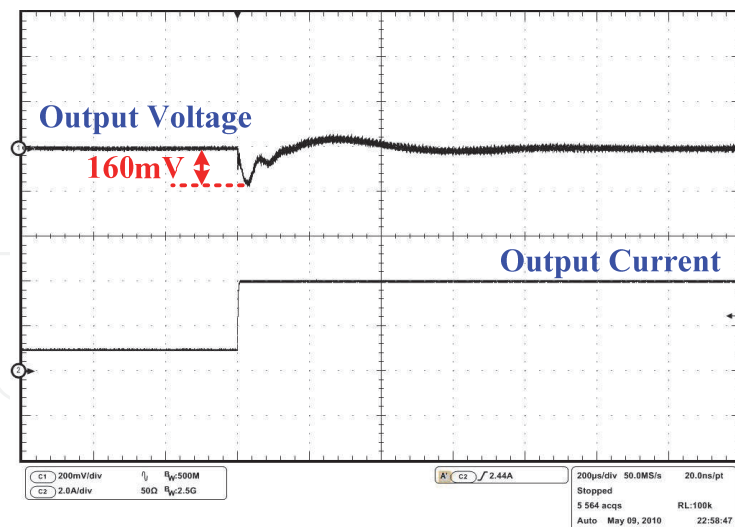Fig. 17. Transient response (Phase lead-lag compensation).

Fig. 18. Transient response (PZC technique).

6. Parameter tolerance

Here, the actual system implementation is discussed. So far, Conductive Polymer Aluminum Solid Capacitor (CPASC) is usually used as the output capacitor of low output voltage converter. However, the Ceramic chip capacitor is recently used by the demand of

diminution and thinness. The issue of Ceramic chip capacitor is that the capacitance is changed by the applied voltage. Conventionally, the controller is designed by means of power stage frequency response, and it is designed to have some stability margin. However, when the capacitance is changed by the output voltage, the power stage frequency response is changed. Then, the whole system frequency response is changed. Hence, the stability margin is changed, and then the system may become unstable. Moreover, the transient response becomes worse. As a result, prospective performance is not provided.

In order to keep the system stability, it is necessary to understand correctly the characteristics of capacitance variation in detail. Figure 19 shows the experimental measurements of capacitance vs. applied voltage.

The capacitors are used as follows;

Sample 1: CPASC

Nominal value : 470µF

Rated voltage : 10V

Sample 2: Ceramic chip capacitor

Nominal value : 100µF (5 parallel, Total : 500µF)

Rated voltage : 6.3V

As shown in Fig. 19, the capacitance is almost flat in CPASC. On the other hand, the capacitance is drastically changed in Ceramic chip capacitor. In this case, the capacitance variation is around 60%. When the applied voltage is 0V, the capacitance is 410µF, and when the applied voltage is 3.5V, the capacitance is 220µF. As mentioned above, when the capacitance is changed, the system stability is also changed.
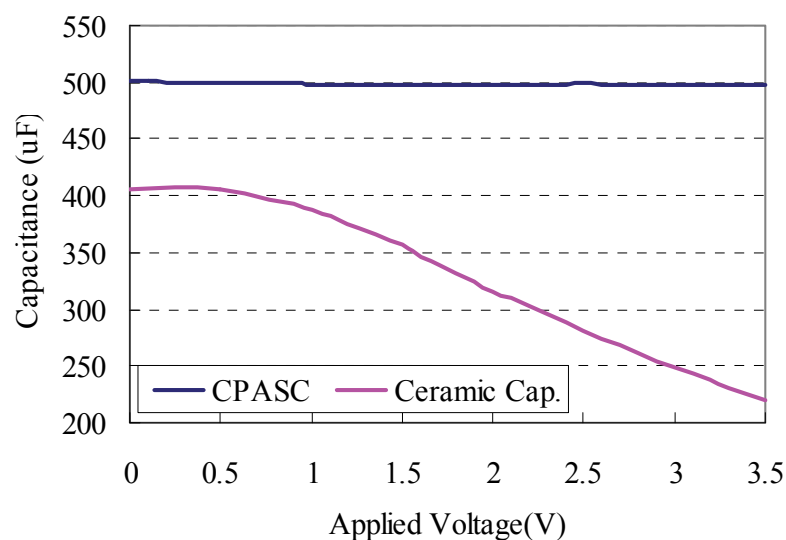

Fig. 19. Applied voltage vs. capacitance.

Figure 20 shows the analytical result of stability margin vs. applied voltage. Initially, the stability margin is set "9dB GM and 50deg PM" at CPASC. As shown in Fig. 20, the stability margin is flat for all voltage range at CPASC. On the other hand, the stability margin is reduced when the applied voltage becomes higher. At applied voltage 2.5V, the stability margin is changed form "9dB GM and 50deg PM" to "3dB GM and 25deg PM". Finally, when the applied voltage is 3.5V, the stability margin becomes limited.
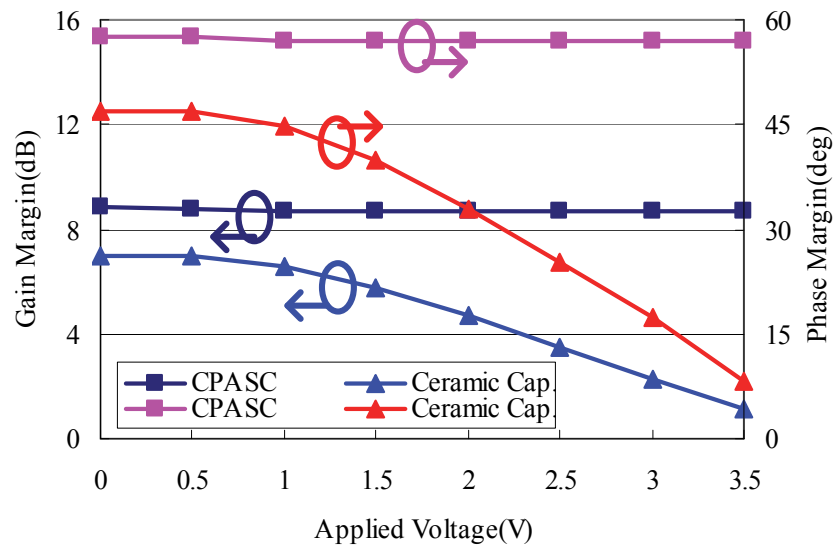
Fig. 20. Applied voltage vs. stability margin.

Figure 21 shows the analytical result of loop gain when the output voltage is 3.5V. Figure 19 has big difference compared with Fig. 15 as an initial condition. As shown in Fig. 19, the anti-resonance peak is appeared at around 1.8kHz. This anti-resonance peak is the influence of Gpzc(s).
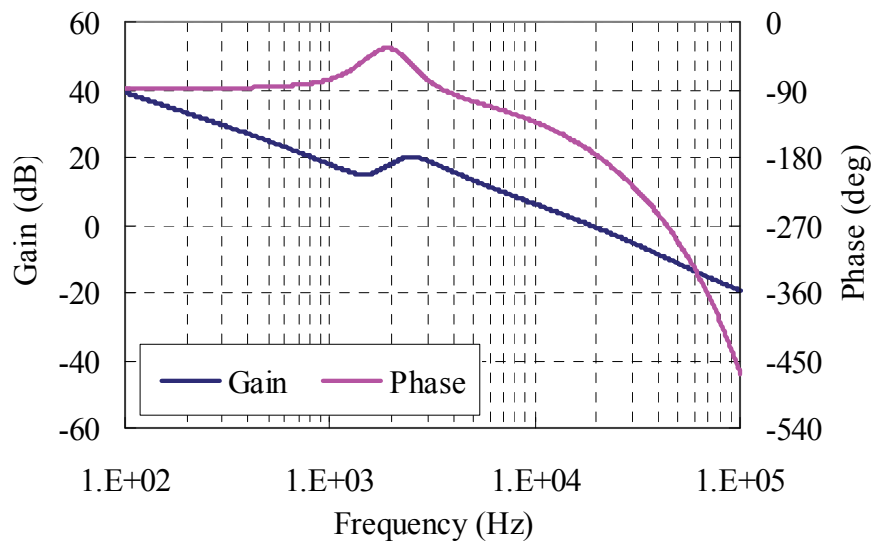

Fig. 21. Lop gain with PZC control when capacitance changes (analytical result).

This anti-resonance peak is cancelled by resonance peak of the power stage, essentially. However, the anti-resonance peak is appeared on frequency response because of the power stage resonance peak is shifted by the influence of parameter variation. Moreover, the resonance peak is appeared at around 2.5kHz. This resonance peak is power stage resonance peak.

In this case, the bandwidth is changed from 10kHz to 20kHz, and the stability margin becomes very few. The performance of the system is greatly affected by the parameter variation in this way. Therefore, the parameter tracking is needed to keep the system performance.

There are two methods of parameter tracking. One is perfect tracking method. Another is simplified tracking. The influence of parameter variation is completely cancelled by the perfect tracking method.

However, the accurate detection of the several mV high frequency voltage is very difficult. So, the perfect tracking is not available solution. Here, the simplified tracking method is examined. The data table is used in the simplified tracking method. Figure 22 shows the experimental measurements of capacitance vs. stability margin.
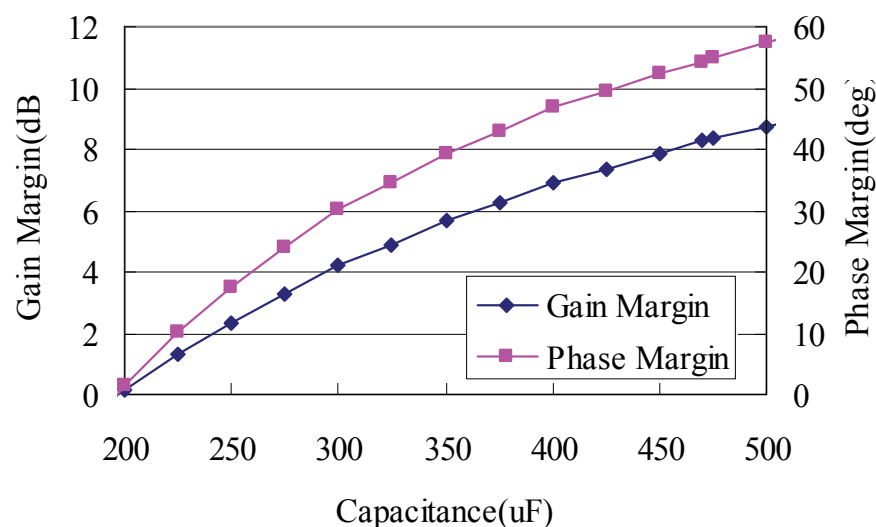

Fig. 22. Capacitance vs. stability margin.

From Fig. 19 and Fig. 22, The designed parameters are listed in Table 2. The auto parameter tracking can be realized by implementation of data table to DSP.

No.	Voltage Range (V)	Capacitance (μF)
1	0 - 0.5	500
2	0.5 – 1.0	400
3	1.0 – 1.5	350
4	1.5 – 2.0	310
5	2.0 – 2.5	270
6	2.5 – 3.0	240
7	3.0 – 3.5	200

Table 2. Parameter list.

Figure 23 shows the experimental result of loop gain when the output voltage is 3.5V. As shown in Fig. 23, the anti-resonance peak at around 1.8kHz is reduced. Moreover, the resonance peak at around 2.5kHz is also reduced. In this case, the bandwidth is around 10kHz, and the stability margin is improved. From these results, for parameter tracking, the system characteristics are kept initial conditions.
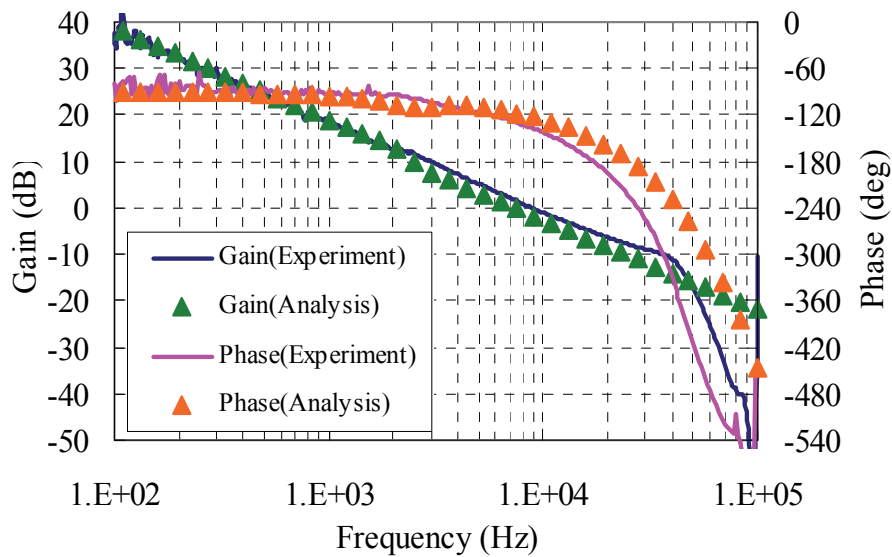
Fig. 23. Lop gain with parameter tracking.

7. Conclusions

This paper proposes the interesting control technique which is cancelled the transfer function of the converter by means of pole-zero-cancellation technique. This technique is very simple, and easy to stability design of converter system. Furthermore, the arbitrary frequency characteristics can be created by introducing a new frequency characteristic. Especially, optimal design of first-order low pass filter is considered and, the design method and system stability of the proposed control technique is examined analytically and experimentally by using buck converter. Furthermore, the parameter tracking is also examined.

As a result, the effectiveness of proposed control technique is confirmed. Moreover, it is confirmed that the characteristic cancellation of the converter can be realized very easy and can be set the arbitrary characteristic. Furthermore, the effective of parameter tracking is also confirmed.

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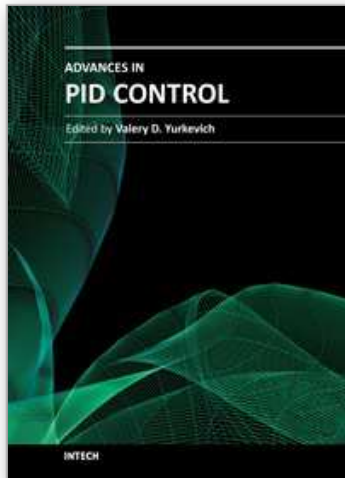
Advances in PID Control

Edited by Dr. Valery D. Yurkevich

Since the foundation and up to the current state-of-the-art in control engineering, the problems of PID control steadily attract great attention of numerous researchers and remain inexhaustible source of new ideas for process of control system design and industrial applications. PID control effectiveness is usually caused by the nature of dynamical processes, conditioned that the majority of the industrial dynamical processes are well described by simple dynamic model of the first or second order. The efficacy of PID controllers vastly falls in case of complicated dynamics, nonlinearities, and varying parameters of the plant. This gives a pulse to further researches in the field of PID control. Consequently, the problems of advanced PID control system design methodologies, rules of adaptive PID control, self-tuning procedures, and particularly robustness and transient performance for nonlinear systems, still remain as the areas of the lively interests for many scientists and researchers at the present time. The recent research results presented in this book provide new ideas for improved performance of PID control applications.

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