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Towards Affordable Home Health Care Devices Using Reconfigurable System-on-Chip Technology

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1. Introduction

Multi-channel data acquisition (DAQ) is a crucial component in digital instrumentation and control. It typically involves the sampling of multiple analog signals, and converting them into digital formats so that they can be processed either on-board or externally. In either cases, DAQ systems also involve microprocessors, microcontrollers, digital signal processing, and/or storage devices. Multi-channel DAQs, which utilize some sort of processing for simultaneous input channels, are needed in home health care monitoring devices. In this chapter, a low-cost real-time multi-channel Analog Signal Acquisition and Processing (ASAP) system is presented. It is divided into five systems. First, the Multi-channel Analog Signal Acquisition system is used to acquire multi-channel real-time analog signals. Second, Archiving system stores the acquired data into a Flash memory or SDRAM. Third, the Digital Signal Processing Unit performs digital signal processing. Fourth, the Frequency Deviation Monitoring (FREDM) system detects any change in input channels' frequencies. Finally, the Heterogeneous Maximal Service (HMS) Scheduler is presented to be integrated with FREDM system.

In home health care devices, storage is limited and power consumption need to be minimum. Therefore, fixed sampling rate is not the optimal solution for multi-channel human body data acquisition. Hence, heterogeneous sampling rates are identified for each channel, and optimized for best data quality with minimal storage requirement and power consumption. The fidelity of the ASAP system is increased by using reconfigurable chip technology, where flexibility, concurrency and reconfiguration can be achieved in hardware. The proposed ASAP allows for the sampling of up to 32 heterogeneous signals with a single high speed Analog to Digital Converter (ADC) taking into account the performance as well.

In the biomedical field, the first step of diagnose a patient is recording biomedical data. Monitoring the vital signs of the patient in acute life-threatening states or being under surgical procedures or anesthesia conditions requires online analysis and immediate visualization. If the immediate visualization is irrelevant, storage of the acquired data is needed. Electrocardiogram (ECG) devices are the most important diagnostic tools for heart patients. Respiratory problems represent one of the main causes of disease in our world. Most of research papers proposed in this field use computer-based devices to acquire signals from the human body. Moreover, there were no scheduling algorithms used. The proposed ASAP

system can be used to acquire human body signals such as the heart beat, pressure and the lung sound at home. Using a varying sampling rate per channel is the optimal solution in terms of scalability, power consumption and memory requirements. It is also considered as a versatile instrument that can be the base of developing a spectroscopic imaging. To date, the complexity associated with constructing a high-fidelity multi-channel, multi-frequency data acquisition instrument has limited widespread development of spectroscopic electrical impedance imaging concepts. To contribute to developing spectroscopic imaging systems, varying sampling rate need to be addressed.

Data acquisition systems (DAQ) are devices and/or software components used to collect information in order to monitor and/or analyze some phenomenon. As electronic technology advances, the data acquisition process has become accurate, versatile, and reliable. Typically, data acquisition devices interface to various sensors that specify the phenomenon under consideration. Most data acquisition systems obtain data from different kinds of transducers that produce analog signals. Many applications require digital signal processing. Therefore, analog signals are converted to a digital form via an Analog to Digital Converter (ADC) to be processed. Existing DAQs, can acquire single channel or multi-channel signals. Many applications require a multi-channel DAQ. Particularly, simultaneous multi-channel DAQs are employed in numerous applications such as medical diagnosis and environmental measurements. If the signals are simultaneously acquired, simultaneous acquisition of additional data can be used to obtain additional information within the same acquisition time. However, exiting computer based multi-channel DAQ systems are cumbersome, expensive, and/or require design redundancy to achieve high reliability and high speed acquisition. Therefore, embedded processing capability must be used to reduce the system size, avoid the design redundancy and reduce the cost and power consumption.

This research is necessary in wide-range applications, particularly demanding heterogeneous and large number of input signals. Therefore, this is the motivation of this research work to try to solve certain problems. One major problem is acquiring high-quality data from large number of input channels simultaneously without the need of computers. This will in turn help the reduction of the cost of the system, and the reduction of the circuit size. Exiting computer-based multi-channel DAQ systems are cumbersome, expensive, and/or require design redundancy to achieve high reliability and high speed acquisition. Contrary to single channel data acquisition, in acquiring multi-channel input signals using a single shared multiplexed ADC, the sampling rate must be much greater than twice the highest frequency component of the input channels. This limits the number of channels being acquired. To increase the number of the input channels, a faster and more expensive ADC must be used in existing technology. In this work, a design of an optimal scheduling module of the ADC with the multiplexer is done. It adaptively selects the proper sampling rate for each channel without affecting the quality of the high frequency input channels or oversampling low frequency spectrum channels. It minimizes the required speed of the single shared ADC, and hence reduces the overall cost of the system, for the same number of heterogeneous input channels. In addition, it minimizes the amount of data being acquired. This leads to minimize the storage requirements. Oversampling low frequency spectrum channels leads to unnecessary data acquisition, which in turn requires extra storage requirements. Hence, an optimization problem is solved in order to compromise between the acquisition quality and amount of data being acquired.

While solving the problem, certain goals will be achieved:

- The total cost of the system should be minimized. The cost can be determined by adding up the cost of every component in the system.
- The circuit size should be minimized. The circuit size will be measured in terms of the number of the gates and logic blocks used in the FPGA chip.
- The system performance should be maximized. For fastest performance, real time operation systems cannot be used. The performance will be measured in terms of:
  - Root Mean Square of errors of the acquired signals
  - The number of channels that can be acquired using the system
  - The required ADC sampling rate for a given set heterogeneous input channels
  - The number of logic elements of FPGA resources
  - The memory requirements

To achieve these goals, one needs to accomplish certain objectives:

1. Heterogeneous multi-channel data acquisition using FPGA-based System-on-Chip
2. Data recording: acquired data has to be stored into Flash Memory for further analysis and/or archiving purposes.
3. Data monitoring: data has to be displayed into an integrated graphical display module.
4. Frequency monitoring: frequency of each channel has to be monitored and any change in frequency should be detected and reported.
5. Optimized sampling: adaptive pre-processing and scheduling techniques are required to sample heterogeneous signals, with adaptive multiplexer scheduling technique.

The efficient implementation of these objectives in FPGA-SoC chip technology has its unique challenges:

- The absence of real time operating system in the desired system leads to the design of all FPGA-SoC to peripheral communication drivers.
- The absence of peripheral drivers (Flash memory, ADC, Graphical display) in FPGA hardware or software. This leads to designing all needed drivers in FPGA. For hardware designed modules, thorough testing must be done for each module independently and collectively after system integration. There are no system simulation tools to guarantee that. Instead, timing simulation is used to verify independent component operation. Each module must be tested and accurate measurements must be verified for fast speed operation. When peripherals are integrated, a reassessment of timing must be done to insure that FPGA-SoC system as a whole performs correctly. Various verification cycles might be needed.
- Synchronization must be maintained between concurrent operating modules. This becomes a challenge when each module operates at different speed. This synchronization has to be implemented in hardware too.
- Adaptive sampling must take place on-the-fly. It needs a continuous monitoring of input channels' frequency.

To eliminate the need of cumbersome hardware, and a personnel computer, one has to map all the functions of a classical data acquisition system inside a single reconfigurable FPGA chip. All needed functions of the computer-based data acquisition and processing system are mapped into the proposed portable multi-functional ASAP system. Note that

the FPGA will be designed to manage all the aspects of processing, and storage, as needed. In particular, to make the proposed ASAP a low cost stand-alone reconfigurable system, the following capabilities have to be built: Capability 1: Accept various input signals with different amplitudes and frequencies. It is desired to acquire analog input voltage signals of amplitude range from mV to V range. Also, the desired input signal in the frequency range of Hz to MHz. This allows the system to accommodate for a variety of sensors at the same time (e.g., low frequency electric pulses, acoustic, ultra-sounds, etc). Multi-channel Analog Signal Acquisition (MASA) system is proposed to perform this capability. Capability 2: Perform automatic signal conditioning such as bias addition and removal, and signal scaling. In addition, it has the built-in capability to perform digital signal processing of FFT for one dimensional digital signal. In this research, Digital Signal Pre-processing Unit (DSPU) is proposed to perform this capability. In addition, it detects the input channels' frequencies. Capability 3: Store the acquired signals without the need of an external computer. A Flash memory controller is designed and integrated with other designed modules in the same FPGA to write data directly to a Flash memory card or the SDRAM. Capability 4: Display the acquired signals on real-time. A displaying capability was designed independently. It is integrated with the proposed design. The acquired analog signals are displayed into an integrated display module (Not Presented here). Capability 5: Detect and monitor frequency change of input channels. In addition, an appropriate action should be taken upon change. Frequency Deviation and Monitoring (FREDM) module is proposed to perform this capability. Capability 6: Perform adaptive heterogeneous maximal service scheduling for the ADC multiplexed interface, for variable number of channels. If all channels have the same characteristics, then it will be equivalent to a round-robin sampling technique (i.e. uniform sampling, one sample per channel per cycle). This increases the number of channels being acquired as well as reduces the required ADC sampling rate which in turn, reduces the cost, power consumption and storage requirements. Heterogeneous Maximal Service (HMS) scheduling technique is proposed to achieve these advantages.

Even though some of the above listed capabilities may be achieved by existing Data Acquisition (DAQ) technology for a limited and fixed number of channels, none of the existing DAQs are capable of performing automatic adaptive maximal service scheduling. In addition, existing DAQs have one or more of the disadvantages: cumbersomeness, high cost, and/or limited hardware scalability. The proposed ASAP system is unique, as compared with traditional existing DAQ systems. The uniqueness can be illustrated in different aspects. First, a novel real-time adaptive maximal service scheduling is designed in the proposed ASAP system. In the case of input signals with different bandwidths, it is the best way to optimize the ADC sampling rate. Meanwhile, it also reduces the overall sampling rate required which leads to reduce the cost of the required ADC with large number of channels especially in high frequency inputs as well as reduces the amount of acquired data which reduces the memory requirements. Second, instead of using multiple ADC for simultaneous multi-channel data acquisition, the proposed design uses a single high speed ADC along with a multiplexer to perform quasi-simultaneous data acquisition. A single high speed ADC can be used efficiently with an optimal sampling schedule to acquire multiple channels. Hence, this can reduce the circuit size, the cost, and the power consumption. Third, the proposed research provides a design philosophy that takes full advantage of the capabilities of the FPGA. Full system reconfigurability based on FPGA is the best solution in terms of fault tolerance, portability and the system can be reused with different configurations. In various applications, especially biomedical field, a fixed sampling rate is not the optimal

solution. The proposed Heterogeneous Maximal Service (HMS) Scheduler achieves the optimal solution for large number of channels. It also reduces total power consumption and memory requirements. If the input signals have different frequency bandwidths, then the proposed HMS is required to perform adaptive sampling instead of using the highest frequency as a fixed sampling rate for all channels. Oversampling low frequency spectrum channels leads to unnecessary data, which in turn requires extra storage capabilities and more power consumption.

2. Existing data acquisition systems

Many sophisticated data acquisition systems exist in the market. However, they are either expensive, cumbersome or both Arshak et al. (2008); Gray (n.d.); Pimentel et al. (2001); *Technical series on data acquisition* (n.d.). For example, the cost of an ADC board can be as high as $3000. Also, in another example, a computer-based biomedical DAQ system consumes 600 watts of power, and thus requires an isolated power supply unit. That system cost is around $5,500 not including a laptop Inc (n.d.). To make, for example, medical diagnosis affordable, one would want to be able to buy similar sophisticated device and use it at home. In such case, affordability plays a major role in the decision of a patient with chronic disease that requires frequent monitoring of some of his/her body signals.

2.1 Multi-channel data acquisition

Existing multi-channel DAQ systems of heterogeneous input signals either use a super fast ADC with homogeneous sampling rate Jackson et al. (1996); Lan et al. (1998); Luengo-garcia et al. (1997); Nadeemm et al. (1994); Posada & Liou (1991), or dedicated ADC for each channel Chang et al. (2004); Komarek et al. (2006); Morgado et al. (1991); Petrinovic (1998a); Xv et al. (2007). Both of these solutions are inefficient, and/or expensive. In addition, they become infeasible for the acquisition of large number of simultaneous channels. Moreover, they require high storage requirements and power consumption. Researches in Artukh et al. (2007); Artyukh, Bilinskis, Sudars & Vedin (2008); Artyukh et al. (2005); Artyukh, Bilinskis, Sudors & Vedin (2008); Bilinskis (2007); Bilinskis & Sudars (2008a;b); Bilinskis & Sudors (2007); Morgado & Domingues (1991); Sudars & Ziemelis (2007) provided a detailed discussion about the multi-channel DAQ. A special sampling technique, event timing, was employed. A sample value is taken at time instants when the input signal crosses a sinusoidal reference function. A prevailing limitation on the number of input channel was acknowledged. An extended research tried to reduce this limitation. However, there are still some drawbacks in this research. First, the reconfigurability is not achieved due to the use of a computer and only using the FPGA for controlling the time to digital converter (TDC). Second, amplitude, frequency, phase angle of the input channel signals have to be given in advance. Third, the acquisition quality depends on the frequency of the reference sinusoidal signal. Increasing of the reference signal frequency is limited. It was mentioned in these researches that these drawbacks have to be traded off with the low power consumption of their proposed system. The demand for this type of converter is based on the fact that physical processes in many cases directly generate events and their timing data carry valuable information. In other applications, sensors or transducers using voltage-to-frequency converters and pulse width modulators convert slowly varying signals into event streams at their outputs. Nallatech provides a stand-alone FPGA-based DAQ Nallatech (n.d.). Nallatech does utilize the FPGA in their dual 3Gsps ADC board (i.e., all main design modules are performed using FPGA), but they use a dedicated ADC per channel, which in turn increases the power consumption,

cost, and the circuit size. The cost of the Nallatech standalone BenADCï£¡-3G is $22,000 Nallatech (n.d.). It also has only dual channels. Therefore, it is not scalable. Some other DAQs such as in Lyrtech, Bittware, Hunt Engineering, and Southwest Research Institute Bittware (n.d.); Engineering (n.d.); Lyrtech (n.d.); Theis & Persyn (2006) only use the FPGA for limited purposes, where the FPGA works as a co-processor for fixed architecture based processing units. This prevents the design from achieving low cost and compact size advantages should the design have been fully integrated in a high capacity FPGA. In Table 1, the literature review on DAQ systems is summarized illustrating the contribution of some research teams and/or affiliations. From Table 1, one can see that the proposed system is unique, as compared with any of research teams appeared in the table.

3. Existing multi-channel data acquisition scheduling algorithms

In real-time single multiplexed ADC systems, input channels scheduling is crucial, because it ensures that input channels meet their requirements. In real-time bad timing can have severe consequences! In heterogeneous real-time systems, each input channel has different restrictions or deadlines. Existing scheduling algorithms can be classified as shown in Figure 1. Dynamic scheduling algorithms are done in run-time, and are more flexible, allowing schedule modifications as inputs change. But dynamic requires computation power that is not needed in static scheduling such as round-robin. In round-robin, processor time (ADC sampling rate) is equally divided among all processes (input channels), before any process is served (input channel is sampled). Each input channel gets equal time slot of the shared single ADC. If heterogeneous multi-rate input channels are scheduled by a single ADC, round-robin scheduling technique assigns the shared ADC to all input channels with a fixed sampling rate Leung & Anderson (2004). In Rate Monotonic (RM), channels are assigned different priorities. Tasks with higher priority will interrupt the current task and replace it. This also means that the system is preemptive. The priorities are assigned to channel based on their frequency. Priorities are assumed to be static, so the channel periods also need to be static. Hence, RM cannot be used if input channels have varying frequency Brucker (2007). Earliest Deadline First (EDF) places input channels in a priority queue. The channel which is closest to its deadline will be scheduled for execution. It has some drawbacks such as situations where deadlines are not known in advance, they are provided but subject to change and/or situations that require uniform sampling spacing Brucker (2007). EDF also does not guarantee equal time spacing between multiple sampling times of periodic signals.

Various research works have been presented in order to achieve adaptive dynamic sampling rate algorithm. Adaptive sampling can be traced back to the research on anti-aliasing in ray tracing Whitted (1980). For example, Painter and Sloan Painter & Sloan (1989) presented adaptively progressive refinement on the entire image plane to locate image features and place more samples along edges. Other research teams proposed different adaptive sampling algorithms in the field of realistic image synthesis. Based on the root mean square signal to noise ratio (RMS SNR), Dippe and Wold Dippe & Wold (1985) proposed an error estimate of the mean to do adaptive sampling. Lee et al. Lee et al. (1985) sampled the pixel adaptively based on the variance of sample values. Purgathofer Purgathofer (1987) used the confidence interval for adaptive sampling. Kirk and Arvo demonstrated a correction scheme to avoid the bias of variance based approaches. Rigau et al. Rigau et al. (2002; 2003a;b) introduced the Shannon entropy and also the f-divergences as the measure to conduct adaptive sampling. Mitchell Mitchell (1987), and later Simmons and Sequin Simmons & Sequin (2000), utilized the contrast to do adaptive sampling. Tamstorf and Jensen Tamstorf & Jensen (1997) refined

Research Work/Affiliations	Multi channel	Multiplexed ADC	Reconfig No	Partia
Four-Channel ADC, Nallatech Nallatech (n.d.)	Y	N	-	-
VHS-ADC Lyrtech Lyrtech (n.d.), Tetra-PMC Bittware Bittware (n.d.), HERON-IO5 Hunt Engineering Engineering (n.d.), HS ADC, Southwest Research Institute Theis & Persyn (2006)	Y	N	-	Y
LabVIEW FPGA, National Instruments Instruments (n.d.)	Y	Y	-	Y
HS ADC / European Atomic Energy Community , CERN in Portugal, Hewlett Packard University of Barcelona in Spain Bautista-Palacios et al. (2005); Cardoso et al. (2004); Loureiro & Correia (2002)	N	N	-	Y
HE ADC/ University of Zagreb in Croatia Meurer & Raulesfs (2000a)	Y	Y	Y	-
100MHz-ADC/ University of EST China Lin & Zhengou (2005) -/Wright State University Lee & Chen (2009)	N	N	-	-
Four Channel Event Timing Modular Multi-channel DAQ in Latvia Bilinskis (2007)-Artyukh et al. (2005)	Y	N	-	Y
ASAP proposed system at TTU, USA	Y	Y	-	-

Table 1. Summary of literature review

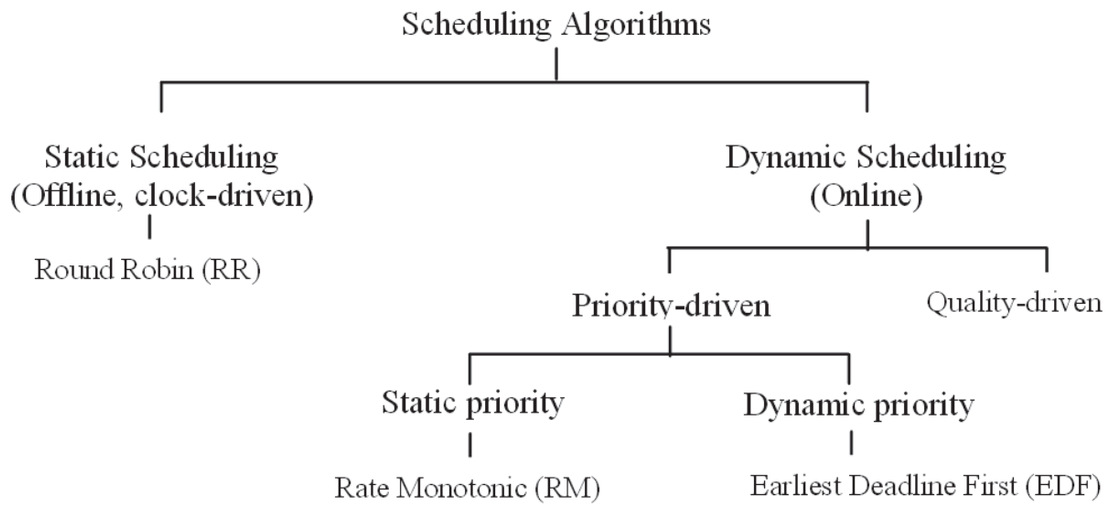


Fig. 1. Classification of existing scheduling algorithms

Purgathofer's approach to propose the tone operated confidence interval. Qing Xu et al. Xu & Sbert (2007) investigated the use of entropy in the domain of information theory to measure pixel quality and to do adaptive sampling based on the nonextensive Tsallis entropy. By utilizing the least-squares design, an entropic index can be obtained systematically to run adaptive sampling effectively.

As signal frequency increases, its corresponding sampling rate has to be increased proportionally in order to have a faithful reconstruction of the signal. It means that more signal samples are to be taken per unit time which means additional storage space is required. Widdershoven et al. Widdershoven & Hiasma (2007) proposed a patent to solve this extra storage issue. They proposed a dynamic shift register which can accommodate to the varying sampling rates in the system. J. Stefan Karlsson Edstrom et al. (2006) proposed a multi-channel modular-based wireless system for medical use. Sampling rate can be individually selected for each channel. The main goal is minimize the total amount of data being acquired to be transmitted. Alex Hartov et al. Hartov et al. (2007) used an under-sampling technique to accelerate data acquisition. Their work was used in developing electrical impedance spectroscopic.

Adaptive sampling is established as a practical method to reduce the sample data volume. Robert Rieger et al. Rieger & Taylor (2009) proposed a low-power analog system, which adjusts the converter clock rate to perform a peak-picking algorithm on the second derivative of the input signal. Their proposed ADC clocking scheme operates the converter at minimum sampling frequency and increases the clock rate only during phases of high curvature (i.e., second derivative) of the signal, essentially performing a peak-picking algorithm on this derivative. The system employs low-power analog circuits to set dynamically the required sample rate without involving the ADC or digital circuitry. Their main application is using this proposed system in the ECG.

From Table 1 and from the literature review, one can see that the proposed system is unique, as compared with any of research teams appeared in the literature review. One can notice that each listed research work has its own advantages. However, the proposed system is unique as related to existing technologies. Instead of using multiple ADC for simultaneous multi-channel data acquisition, the proposed design uses a single high speed ADC along

with a multiplexer to perform quasi-simultaneous data acquisition. In the medical field for example, where various biomedical signals are in the low frequency range from 25 Hz to 5 KHz Abdallah et al. (2009), the proposed DAQ can be appropriate without the need of additional hardware or cost. For applications that require very fast simultaneous multi-channel data acquisition, such as in the military field, dedicated ADC per channel will be more appropriate. A single super high speed ADC can be used efficiently with an optimal sampling schedule to acquire multiple channels. Hence, this can reduce the circuit size, the cost, the power consumption, the system scalability and the storage requirements. Second, full system reconfigurability based on FPGA is the best solution in terms of fault tolerance, portability, and the system can be reused with different configurations. Third, hardware real-time adaptive sampling is only available in the proposed system. It leads to the design security where using the hardware design immunes the reverse engineering and secure the design. In the case of input signals with different bandwidths, the hardware real-time adaptive sampling is the best way to optimize the ADC sampling rate. Meanwhile, it also reduce the overall sampling rate required which leads to reduce the cost of the required ADC with large number of channels especially in high frequency inputs.
Our proposed research provides a design philosophy that takes full advantage of the capabilities of the FPGA as well as using a single multiplexed ADC for multi-channel DAQP. This will lead to small size, cost, memory requirements, and power consumption for the DAQP as well as the design hardware scalability (i.e., to add more channels as desired without changing the system board). The optimal sampling capability of the device allows for the sampling of a large number of heterogeneous signals without increasing the size of the ADC.

4. Software acquisition and multiplexing approach

The software acquisition and multiplexing approach is employed using embedded C programming language and Hardware Description Language (HDL). As a rule of thumb, any time-critical task is implemented in hardware, while other functions are developed in software using embedded C programming language. Components of the computer-based data acquisition system are custom designed in the proposed system.

4.1 Archiving implementation in software

In the beginning, a design decision regarding which functions will be accomplished in hardware and which can be done in software has to be taken. In order to get benefit from the simplicity and flexibility of the embedded C programming, two main tasks are assigned to be performed by the NIOS II processor using embedded C programming. Storing the acquired data into the flash memory (SD card) and multiplexing between the multi-input analog channels are performed by the NIOS II processor. Storing the acquired data into the SD card consists of many other subtasks such as store the acquired data in the SDRAM as a temporary location, initialize the SD card, calculating the CRC, check the status of CRC response of a block and put the acquired data in a wave file format.

4.2 Software acquisition and multiplexing approach verification

In this subsection, a comparison study between the proposed MASA system with the archiving module and an existing technology DAQ system is presented. The National Instrument (NI) data acquisition card is chosen because it has the closest similarity to the proposed DAQ (although it is a computer-based, it uses adaptive sampling and a multiplexer). The NI test-bench is a PCI 6024E- 200 kS/s 16 channel DAQ card. National Instruments DAQ

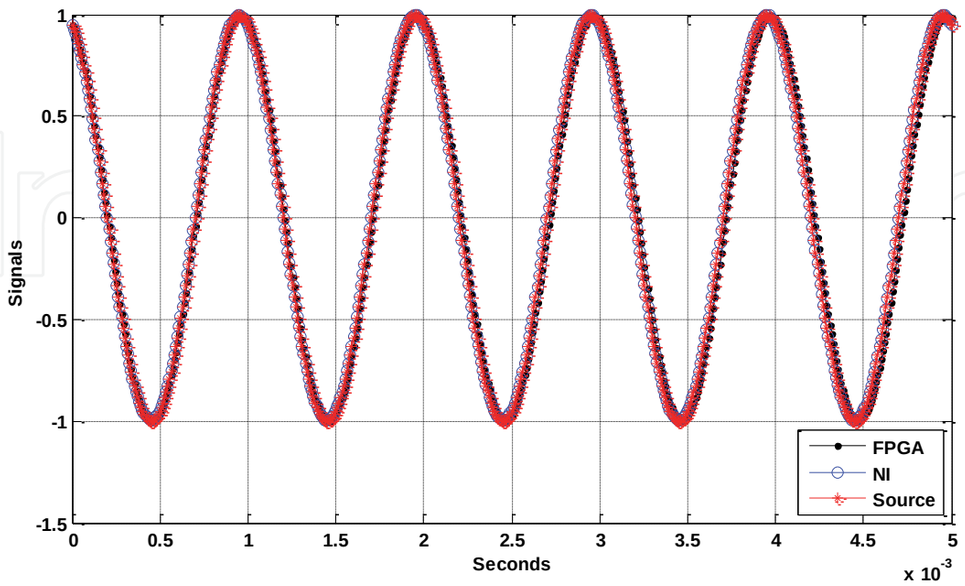
	Sequential Single Channel 100 KSPS	
Input signal	FPGA	NI
1 KHz	rms(e)= 0.0523	rms(e)= 0.016
4 KHz	rms(e)= 0.0754	rms(e)= 0.029
8 KHz	rms(e)= 0.3766	rms(e)= 0.0907
10 KHz	rms(e)= 0.3812	rms(e)= 0.11

Table 2. Root mean square of the error for the proposed software acquisition and multiplexing approach and NI-based DAQ (N= 1000 samples)

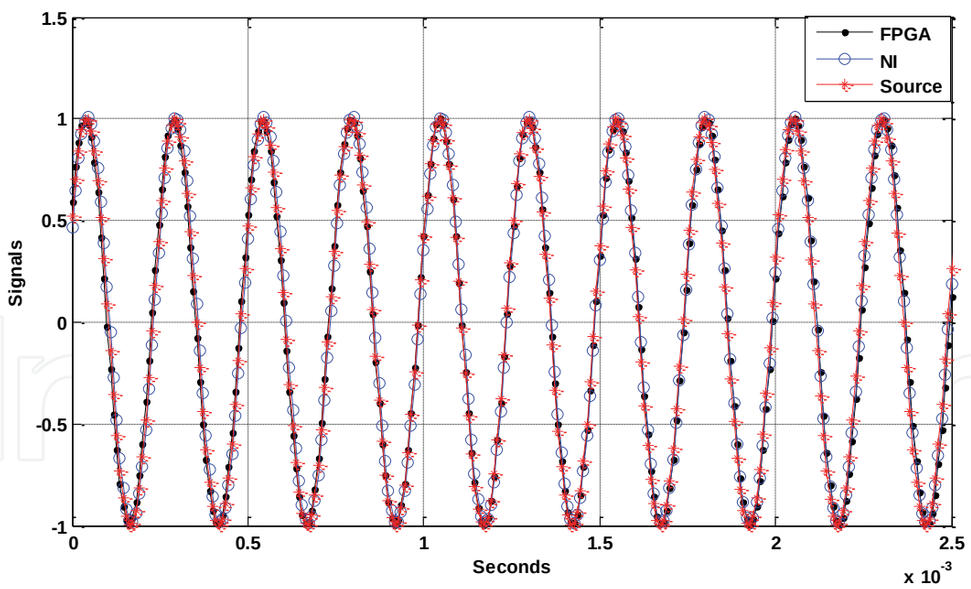
has been used as a comparison reference. It is a computer-based DAQ. For the sake of fairness, the sampling rate is fixed for both systems to be 100KSPS. Different signals have been applied to both systems. Acquired signals from both systems have been tested in terms of root mean square of errors.
Different signal generator has been used to generate 1 KHz, 4 KHz, 8 KHz and 10 KHz sine waves. Each signal has been applied into both DAQs. The input signals are applied to the input of the MUX. The proposed FPGA-based DAQ stores the input signal as a wav file into a flash memory. It works as stand-alone without any interfere from the computer. All the processing and control has been done by the FPGA. On the other hand, the NI-based DAQ needs a LabView program which run on a computer in order to store the input signal into a file in the computer attached with the card. Both acquired/stored signals by both systems have been tested by Matlab. The root mean square of errors has been used as an evaluation parameter. In Figure 2, three signals have been presented, the FPGA-based stored signal, NI-based stored signal, and the source signal for 1 KHz and 4 KHz sine waves.
In Table 2, the results of these experiments are listed in terms of the root mean square of errors.

4.3 Software acquisition and multiplexing approach problems

NIOS II processor instructions have a nonuniform execution time. In other words, the time between each acquired sample is not equal. The logic analyzer is used to proof this notice. The logic analyzer is connected to the acquisition clock of the NIOS II processor via one pin of I/O pins of the used FPGA. Figure 3 shows the nonuniformity of the generated acquisition clock of the NIOS II processor. This affects the frequency of the stored signal. So, one can find after some time that the stored signal starts to be slower and deviate from the original signal. It can be noticed from Table 2, the root mean square of errors for the proposed sequential MASA with archiving module system is greater than NI-based DAQ. If the root mean square of error is calculated for less number of samples, the root mean square of errors for the proposed system will be less than the numbers mentioned in Table 2. Figure 4 shows the frequency deviation from the source signal of the stored signal after some time.
This comes from the fact that NIOS II processor is instruction-based which makes the data acquisition nonuniform. In other words, the time between each acquired sample is not equal. This affects the frequency of the stored signal. In addition, the speed of data acquisition, processing and storing is slow. It reaches 100 seconds to process and store 8000 blocks of data where each block is 512 samples. Hence, another design approach will be adopted in the following section. Hardware acquisition and multiplexing design is proposed in order to get fast data acquisition, processing and storing system, as well as maintain an accurate signal reconstruction in terms of its frequency.



(a)



(b)

Fig. 2. Comparison between FPGA-based, NI-based DAQs (a) 1 KHz sine wave (b) 4 KHz sine wave in sequential channel DAQ

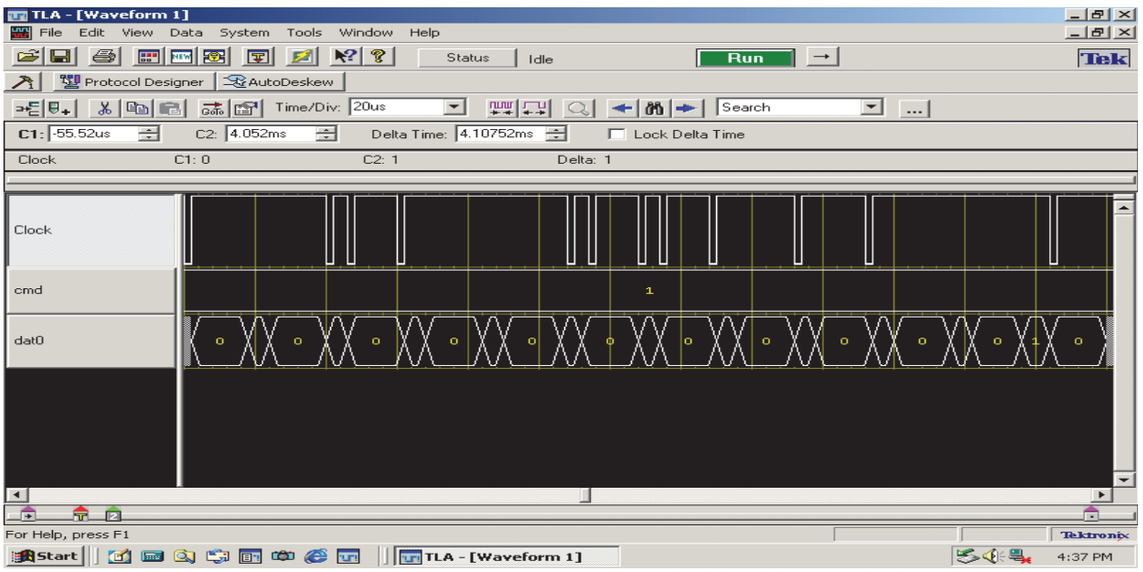


Fig. 3. Logic analyzer shows the nonuniform behavior of the NIOS II processor acquisition rate

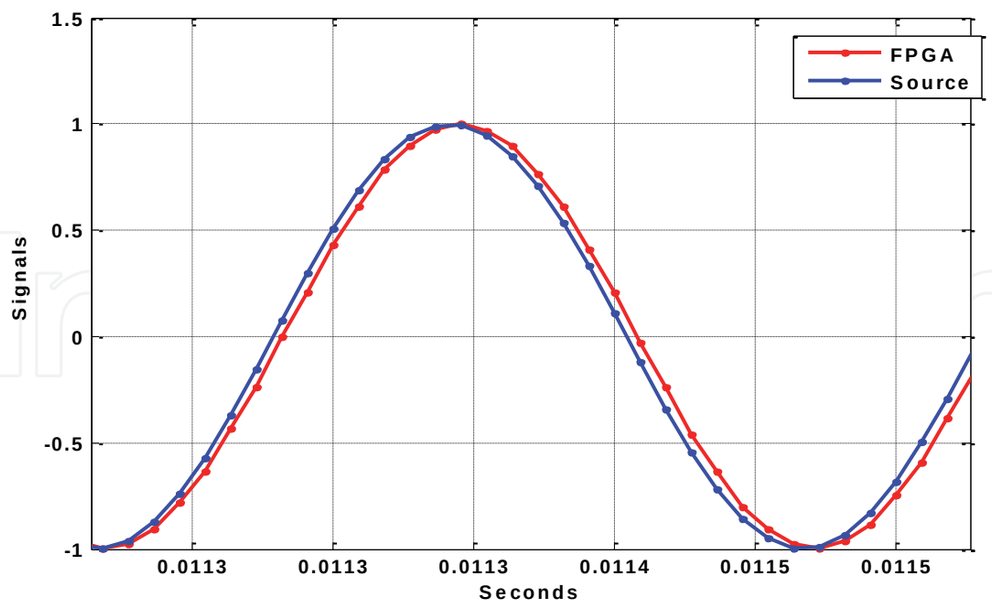


Fig. 4. Frequency deviation problem in the Software Acquisition Approach

		RMSe(proposed system) for(N) Samples			RMSe(NI-DAQ) for(N) Samples			%Improvment N=10000
OSR	Signal	100	1000	10000	100	1000	10000	
500	200Hz	0.009	0.017	0.018	0.013	0.020	0.0202	11
100	1KHz	0.014	0.015	0.015	0.018	0.016	0.0165	9
50	2KHz	0.02	0.027	0.027	0.039	0.04	0.0425	37
25	4KHz	0.02	0.029	0.029	0.029	0.029	0.0334	13
20	5KHz	0.05	0.057	0.057	0.061	0.069	0.06	5
12.5	8KHz	0.083	0.0832	0.082	0.0907	0.0907	0.1	18
6.667	15KHz	0.13	0.13	0.13	0.15	0.155	0.166	22

Table 3. Root mean square of the error for both proposed hardware FPGA-based acquisition and multiplexing design and NI-based DAQs (sequential MASA)

5. Hardware acquisition and multiplexing approach

Due to the previously mentioned problems of the software acquisition and multiplexing, another approach is used to implement the archiving system. All tasks have to be designed and implemented in hardware. No HAL drivers are used. Every peripheral driver and controller is built. The SDRAM controller is designed and implanted in Hardware Description Language. The Avalon fabric and its components are not used in the new approach. In this approach, the acquired data is stored in the SDRAM.

5.1 Hardware acquisition and multiplexing approach verification

The comparison of the acquired data is shown in Table 3. The root mean square of errors (RMS(e)) is used as an evaluating parameter. From Table 3, the performance of MASA with the archiving module is better than the NI-DAQ, although the NI card has two signal conditioning stages. First, adaptive programmable amplitude amplifier is used after the multiplexer and before the ADC inputs. Second, a dithering unit is used to enhance the resolution by 0.5 LSB. As shown from Table 3, seven analog sine waves (200 Hz to 15 kHz) signals are applied into the input of both DAQ systems. Different number of samples (N = 100 to 10,000) is considered. A comparison between the acquired/stored signals via both DAQ systems with respect to the source signal is done. The RMS(e) is calculated for both systems. As the number of samples increases, the RMS(e) is increased (it can be seen if you go right for each system in Table 3). As oversampling ratio (OSR) decreases, RMS(e) is also increased (it can be seen if you go down in a same column). The best performance for sequential MASA with the archiving module has 37% better (smaller) RMS(e) than NI-base DAQ in the case of 10000 sample of 2 KHz input signal. Figure 5 shows the stored signal by NI-based DAQ and the proposed system DAQ as well as the source signal for a 8 KHz sine wave in the case of MASA.

6. Why Heterogeneous Maximal Service (HMS) scheduling?

HMS is needed to sample a large number of heterogeneous signals without increasing the size of the ADC taking into account the performance as well. Sampling rate, resolution and number of channels can be selected and optimized in order to minimize the amount of data being acquired which eventually will be stored or transmitted. Accordingly, storage requirements and power consumption will be reduced. Moreover, a case study is introduced to show the importance of the HMS. In the single multiplexed ADC, it is known that the

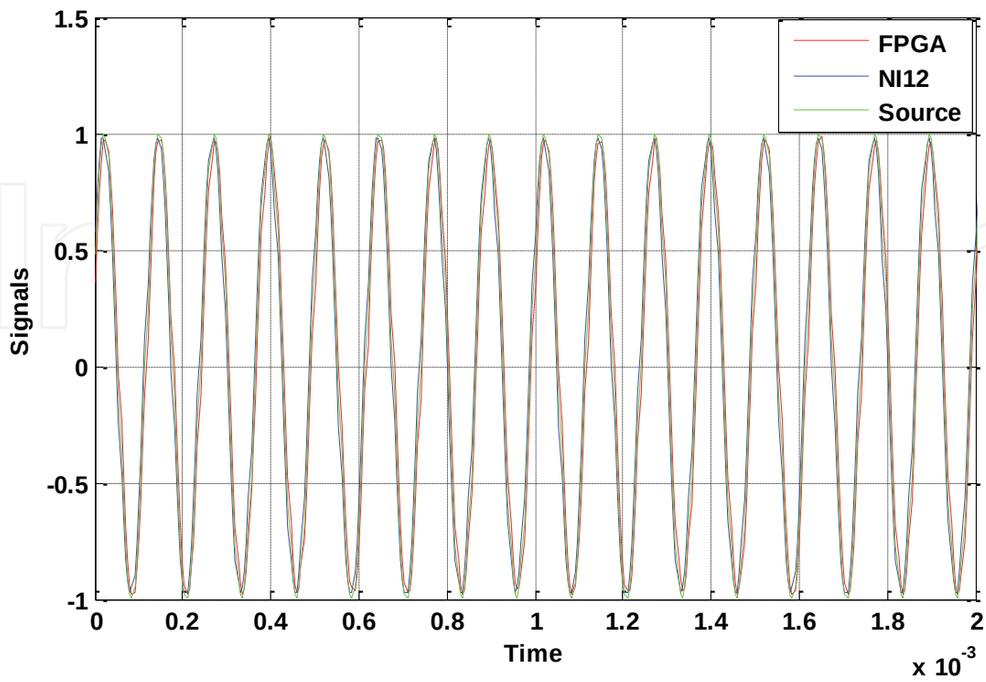


Fig. 5. 8 KHz sine wave acquired by the sequential (proposed FPGA-based system vs. NI-based)DAQ

sampling frequency F_s must be greater than the Nyquist's sampling frequency F_x:

$$F_x \geq N \times F_s, F_s \geq 2 \times B_w \tag{1}$$

where N is the total number of channels, and Bw is the highest frequency component of the input channels (widest bandwidth) Meurer & Raulesfs (2000b). This means that the single ADC must be faster than the Nyquist's rate multiplied by the number of channels. If input signals are not in the same frequency range, then an optimized ADC scheduler will be required to perform adaptive sampling, instead of using the highest frequency to set the sampling rate. It is a challenge to achieve the optimal control module of the ADC without affecting the quality of the high frequency input channels or oversampling low frequency spectrum channels. Oversampling low frequency spectrum channels leads to unnecessary data acquisition, which in turn requires extra storage capabilities and more power consumption. According to Equation 2, the dynamic power increases as the activity factor (α) increases, which in turn will increase the total power consumption. If the sampling rate increases, the activity factor will be increased.

$$P_{dynamic} = \alpha C V^2 F \tag{2}$$

where C is capacitance, V is voltage, F is processor clock frequency. Generally speaking, dynamic power can be reduced by using different smaller rates of activity factor for less frequent sampling for channels that require a much smaller minimum service rate as compared to channels with higher service rates.

Second, the determination of optimal maximal service scheduling requires identification of input features, which are generally not known at the design time. Hence, optimal maximal service scheduling cannot be static. A real-time dynamic (optimal) scheduling is proposed in this research. The timing of such scheduler must be accurate to avoid channel skipping or data corruption Petrinovic (1998b). It also has to adapt to changing input features from one application to the other. In addition, each channel will be modulated at the appropriate sampling frequency to maximize the total number of channel acquisition. An optimal ADC scheduler is needed to manage the variable switching time of the ADC multiplexer such that an arbitrary large number of channels can be sampled without loss of signal quality. Moreover, HMS maximizes the quality of rapidly changing channels as well as slow changing channels. On the other hand, round-robin scheduler maximizes the quality of slow changing channels over the rapid ones. In the next section, a comparison between the proposed HMS and round-robin scheduler techniques is introduced.

6.1 Optimization problem

The problem can be formulated as an optimization problem. Given a maximum sampling rate (F_s) of ADC and a total number (N) of channels, an optimized sampling rate (F_{si}) for each channel needs to be assigned.

$$Max \sum_{i=1}^{N} log_2(OSR_i) \tag{3}$$

$$subject\ to \sum_{i=1}^{N} f_{si} \leq F_s \qquad , i = 1, ..., N$$

$$T_{si} \% T_s = 0$$

$$T_{si} \times M1 \neq T_{sj} \times M2 + T_s \times M3$$

where oversampling ratio for channel (i) = $OSR_i = F_{si}/F_i$; i, j =1,„N; i $\neq$ j; $T_{si} = 1/F_{si}$; T_s= $1/F_s$; M1,M2,M3 are integers ($\leq$ 2 Max(T_{si})) ; M3 is the number of time periods (T_s) between channel (j) and channel (i). The objective of this optimization problem is to maximize the assigned sampling rate (or minimize sampling period) for each channel. However, there are various restrictions that limit the OSR_i. First, the summation of assigned sampling rates for all channels must be less than or equal the total sampling rate of the available ADC. Second, the assigned sampling rate for any channel cannot be an arbitrary number. Its inverse (i.e., the time period) must be a multiple of the inverse of the total sampling rate of the available ADC (T_s). Third, at any given time, no more than one channel can be sampled. For example, assume T_s is 0.625 nsec, Ch1 has T_{s1} is equal to 2.5 nsec, and Ch2 has T_{s2} is equal to 1.875 nsec, Figure 6 shows that there is a problem at time T=2.5 nsec. Both Ch1 and Ch2 need to be sampled at the same time. This problem is called Same Time Sampling (STS) Problem. This situation has to be avoided in order to maintain high signal reconstruction.

Therefore, in order to implement the proposed HMS scheduler, two main aspects should be considered. First, the frequency of each channel has to be determined. So, FFT has to be performed for each channel. The DSPU performs this task. Channels' frequencies may be changed overtime. So, adaptive scheduler is needed to monitor any change in frequency. FREDM takes care of this task. Hence, a combination of DSPU and FREDM is a basic tool to achieve the adaptive HMS scheduler.

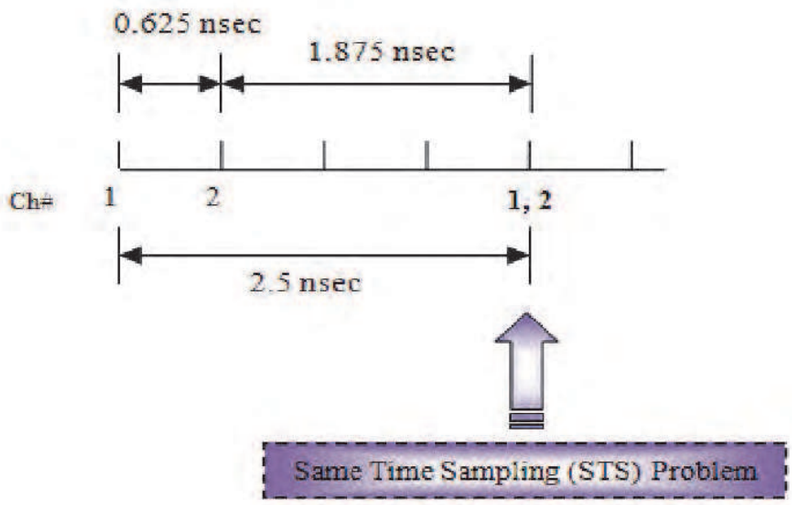


Fig. 6. Same Time Sampling (STS) Problem

7. Optimal sampling Heterogeneous Maximal Service (HMS) scheduler

An array of different analog sensors are connected to the ASAP system. If any channel has a known frequency, this frequency is stored in a lookup table. Otherwise, its frequency is determined by the FFT module in DSPU. The lookup table is updated via FREDM when any frequency change is detected.

7.1 HMS procedure

In Figure 7, HMS flow chart is presented. The inputs to the HMS are frequency bandwidths of input channels. The HMS technique starts with state 0 where each channel has its own sampling rate Fsi which equals to Nyquist's sampling rate. Therefore, each channel sampling period Tsi is calculated by inversing Fsi in state 1. Tsi should be multiples of Ts. If it is, the flow goes to state 2. Otherwise, Tsi should be updated to be multiplies of Ts. In state 2, Brute force search method is used. It is necessary to check the total summation of sampling frequencies of channels. If it exceeds the maximum sapling rate of the available ADC, the task will not be schedulable. Otherwise, the control goes to sate 3. Current sampling frequencies could be a solution. However, the STS problem should be checked before judging on the solution in hand. It comes to state 4 where channels order iterations will take place. In each order, STS problem will be checked. If there is an STS problem, a success rate will be calculated and then the control goes to state 4 again for the next iteration. If there is no STS problem, we have a valid solution and it is needed to be stored as a possible optimal solution. After storing the solution or after the whole iterations are finished without finding a solution, state 5 should be reached. In state 5 for each channel, Tsi will be decremented once by the value of Ts taking into account that Tsi cannot be smaller than Ts. Then, the flow goes again to state 2. One can notice from Figure 7 that there is a flag called start. It is used to determine whether the task in hand is not schedulable or it can be scheduled but there is an STS problem. If start is 0, it

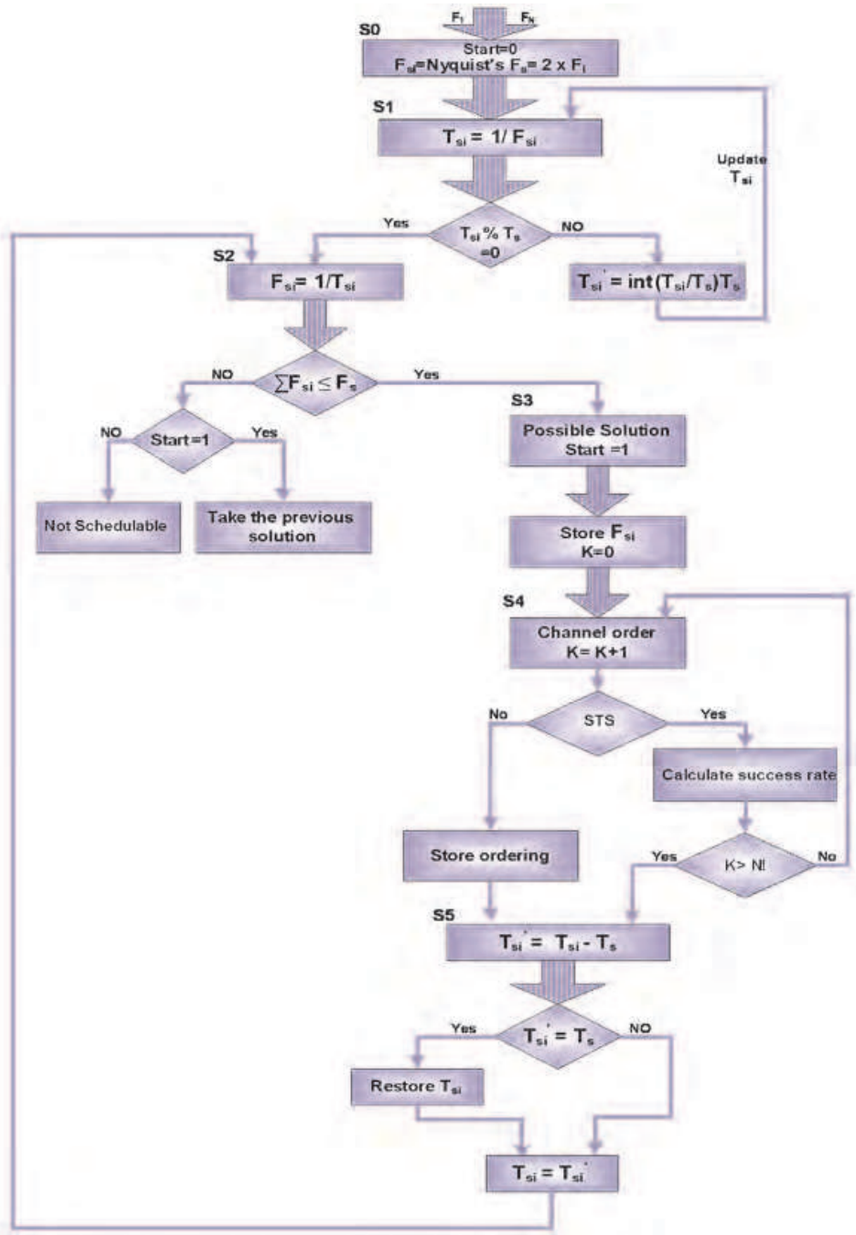


Fig. 7. HMS flowchart

means that no possible solution is achieved. But if start is 1, it means that there is a possible solution that can sample input signals but there is an STS problem. So, if such situation is faced, the previous valid solution should be the optimal solution.

8. Experimental setup

In this section, different experiments are implemented in order to test each subsystem. A multisignal generator (Sony Tektronix AFG310) is used to generate different sine waves as inputs to the proposed system. A Tektronix TLA610 Logic Analyzer is also used in the real-time experiments to verify frequency change of any channel.

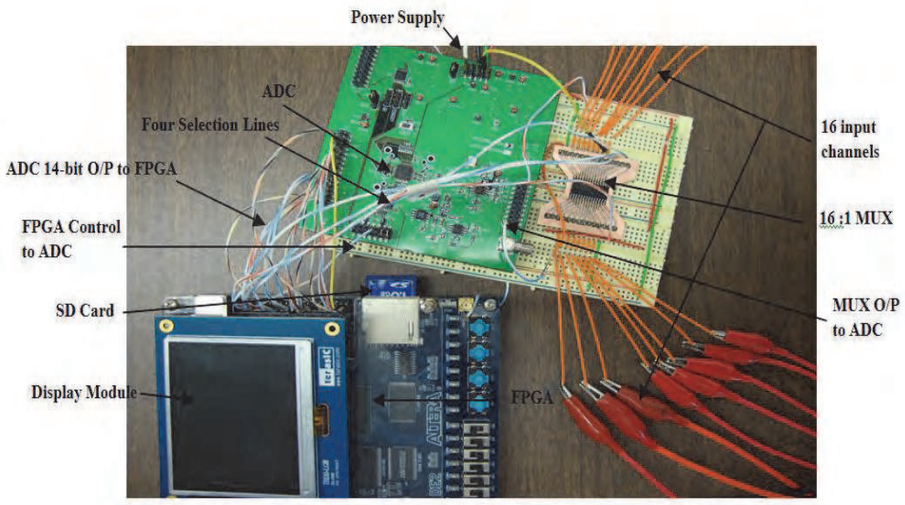


Fig. 8. FPGA Prototype of 16 multiplexed input channels ASAP

8.1 Specification

The designed FPGA ASAP prototype, shown in Figure 8, is set up with a Dual 16:1 Multiplexer/Demultiplexer (Analog Devices ADG506AKRZ), and a Texas Systems ADC (ads7891). This particular low power ADC consumes 85 mW. This ADC operates at clock frequency up to 3MHz. The sampling rate is fixed to be 100 kS/s per channel. This is to have enough data to be displayed and represent the input signal. If high sampling rate such as 3MSPS is chosen, and due to the limited memory in the logic analyzer, the acquired data will represent only a small part of the input signal.

The total number of channels is set via the board switches. The proposed system can handle up to 32 channels. The number of channels can easily be increased by only changing the multiplexer while maintaining everything of the proposed system. The selected FPGA is a Cyclone II (EP2C35F672C6) from Altera, with a main clock of 50 MHz.

9. Verification

The proposed system design is tested and evaluated in terms of signal preprocessing and FFT accuracy done by DSPU, frequency deviation monitoring capability by FREDM, and HMS significance. Each parameter is discussed in more details in this section. Verification using simulation and real-time experiments are considered. A Matlab and Altera simulation tool are used to verify the simulation results of FFT process done by DSPU. A Tektronix Logic Analyzer is used in the real-time experiments to verify frequency change of any channel detected by FREDM. A Matlab program is developed to test and verify the significance of the proposed HMS.

9.1 DSPU evaluation

9.1.1 FFT simulation results

For simulation and verification purposes, the Altera simulation tool is used. Let M= 512 input points. As shown in Figure 9, (*source_real*, *source_imag*) are the real part and the imaginary part of each output point, respectively. The signal (py) is the Power Spectral Density (PSD) of the first 255 points. The signal (*s_pyy_max*) is the highest PSD and (*s_pyy_max_index*) is its index. In other words, (*s_pyy_max_index*) is the location (fci) of the greatest frequency

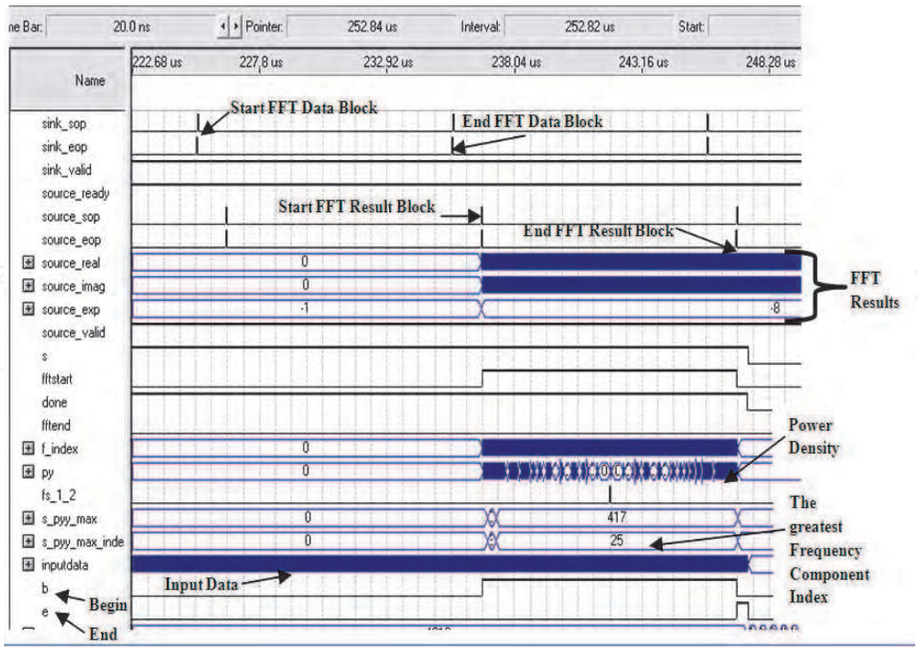


Fig. 9. FFT Simulation Results

component. The greatest frequency component (represents signal frequency) F_i can be easily calculated by

$$F_i = (fci/M) \times F_s, fci = 0, 1, 2, ..., M/2, i = 1, 2, 3, ..., N \quad (4)$$

where N is the number of channels and M is the number of output points of FFT and F_s is the sampling frequency (100 KSPS). A 5 KHz sine wave is the input to the simulation. As shown from Figure 9, ($s\_pyy\_max\_index$) which is the greatest frequency component index (fci) is equal to 25. Substituting in Equation 4 with fci = 25, one can find that the input frequency will be 5 KHz.

9.1.2 FFT Matlab-based merification

A Matlab script was written to generate the required input simulation files. To compare Matlab results with Altera FPGA FFT MegaCore function, one needs first to scale the FPGA output. FPGA scaling is done using the exponent output value:

$$FinalOutput = (MegaCoreFunctionOutput)/(2^{exp}) \quad (5)$$

In other words, FPGA gives a very well scaled output and then it is needed to divide it down. To divide by $2n$ in hardware, it is needed to shift right n bits and extend the sign bit n times. Remember the exponent varies according to FFT block values. In Matlab, results are close but with some rounding difference. Rounding was not done in the hardware module. For verification purposes, the same data set of a maximum frequency component of 5 KHz is considered for both FPGA-based and Matlab-based FFT process. The accuracy of the FPGA-based FFT module is 98% compared to the FFT function in Matlab. Moreover, the proposed FPGA-based FFT module accuracy can be increased via using more FFT points (M). Only 512 points are considered in this work. If M = 2048, the accuracy will be more than 99%. Figure 10 shows a comparison between the Matlab-based FFT and FPGA-based FFT done by DSPU for the same input signal (of a maximum frequency component of 5 KHz). The

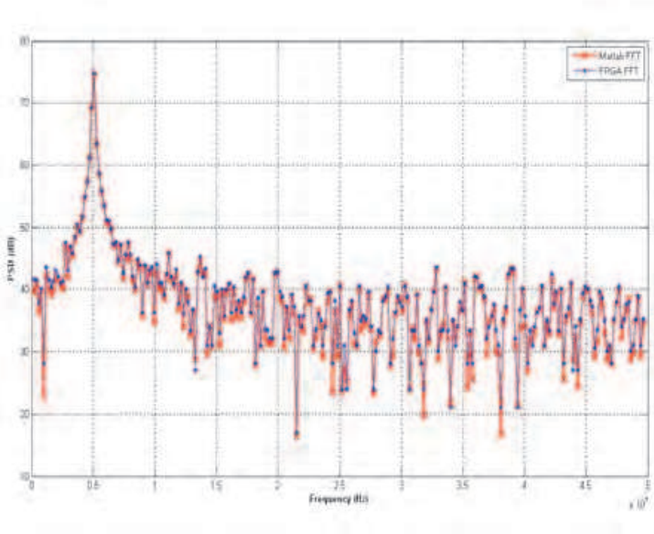


Fig. 10. Matlab FFT verification of a data set of a maximum frequency component of 5 KHz

Frequency	Frequency Component Index (fci)
5 kHz	25
10 kHz	50
15 kHz	76

Table 4. Frequency and the corresponding frequency component index (fci) from Equation 4

horizontal axis is the frequency in Hz and the vertical axis is the power spectrum density in dB. As shown in the figure, the maximum power density exits at frequency of $0.5x10^4$ which is 5 KHz.

9.2 FREDM evaluation

Two experiments are performed here. First, two input signals (15 KHz and 5 KHz) are connected to a multiplexer as inputs to the FREDM. Figure 11 (a) shows a snap shoot of the logic analyzer connected to the FPGA board for verification purposes. As seen in Figure 11, both channel number and its frequency component number are detected (see Equation 4). Table 4 shows both signal frequency and the corresponding frequency component index.
In the second experiment, 16 input channels are applied to the multiplexer. For simplicity, the logic analyzer considers channel 1 only. A 5 KHz sine wave is applied to the channel 1. A change in frequency is taken place to be 10 KHz. Figure 11 (b) illustrates frequency change detector capability of the proposed FREDM system. As seen from the figure, the fci of channel 1 is presented before and after the change. Enable signal is changed from (0 to 1) when frequency change is detected.

9.3 HMS evaluation and significance

A comparison between the proposed HMS and round-robin scheduling technique is presented here. A simulation Matlab program is developed. There are three possible scenarios. First, both techniques cannot schedule a given task (i.e., un-schedulable task). Second, both techniques can schedule it. Third, HMS can schedule it and round-robin cannot. Let's consider

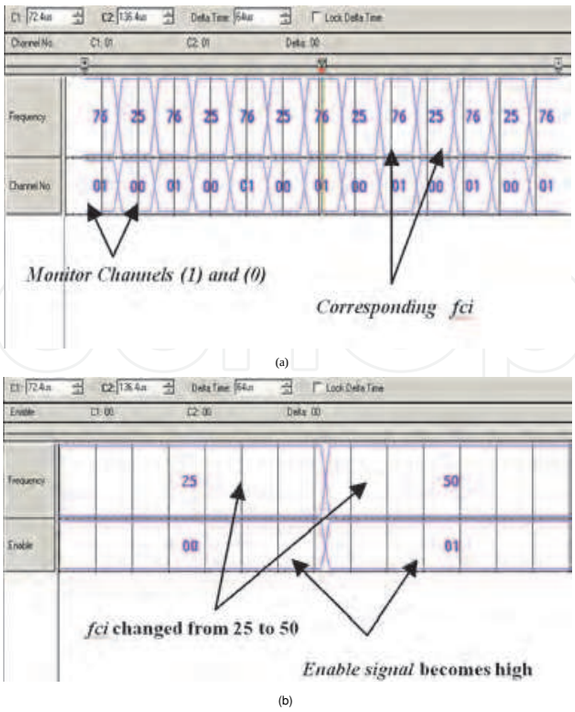


Fig. 11. FREDM verification (a) Real-time frequency monitoring and (b) frequency change/deviation detection

the second scenario where both techniques can give a solution to the given case study. A case study is considered with eight sinusoidal analog signals. The frequencies of the eight input channels are 500kHz, 200 kHz, 190 kHz, 185 kHz, 160 kHz, 100 kHz, 100 kHz, and 100 kHz. Let the maximum sampling rate Fs of the available ADC be 10 MSPS (Ts = 100 nsec). The HMS solution is presented in Figure 12. In this case, round-robin scheduling technique can schedule given signals with a fixed sampling rate for all channels (1/800nsec= 1.25MSPS). This leads to oversampling low frequency signals (such as the 100 kHz), which in turn causes extra memory storage requirements and power consumption as well. On the other hand, the HMS schedules the eight input channels to be sampled at a varying sampling rate. This reduces the amount of data being acquired, which in turn decreases the required memory as well as power consumption according to Equation 2. The total amount of data being acquired using the proposed HMS is less than that acquired by round-robin by 59%.

Now let's consider the third scenario where HMS can schedule the given task and round-robin cannot get a solution for the same task. Let the maximum sampling rate F_s of the given ADC be 100 kS/s. The time period is 10 μ sec. Three analog signals are applied to MASA system, 25 kHz, 10 kHz, and 2 kHz, respectively. In addition, assume that no channel has priority. Applying Nyquist's law, one can find the following. $F_{s1} \geq 50$ KS/s, $F_{s2} \geq 20$ KS/s, $F_{s3} \geq 4$ KS/s; where F_{si} is sampling frequency for channel (i). In other words, $T_{s1} \leq 20$ μsec, $T_{s2} \leq 50$ μsec, $T_{s3} \leq 250$ μsec; where T_{si} is sampling time period for channel (i). If round-robin sampling technique is applied, these three signals cannot be sampled using the available ADC. Applying HMS, these analog signals can be optimally scheduled using the available ADC. As shown in Figure 13, the optimal scheduling is T_{s1} = 20 μsec, T_{s2} = 40 μsec, T_{s3} = 240 μsec (F_{s1} = 50 KS/s, F_{s2} = 25 KS/s, F_{s3} = 4.166 KS/s). The three constraints are satisfied in the optimal maximal service scheduler.

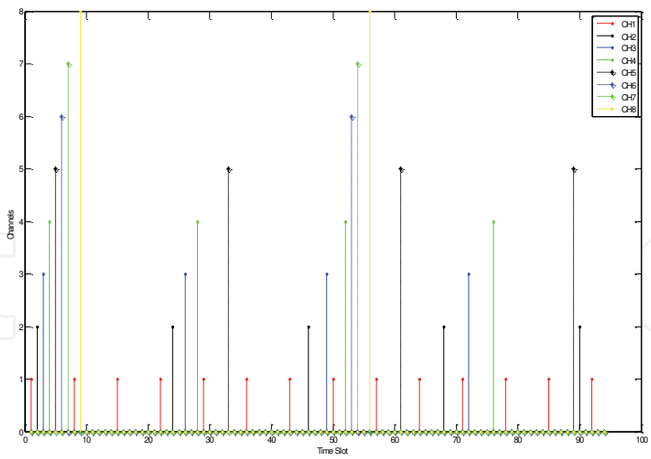
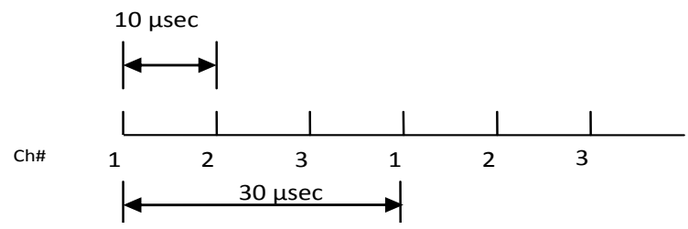
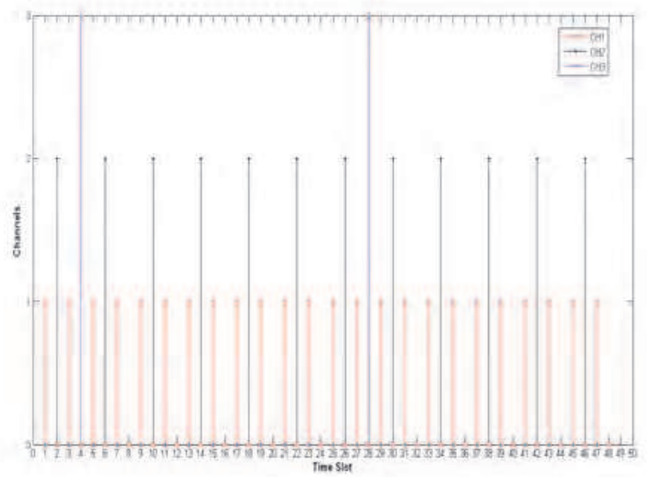


Fig. 12. Eight channels with a varying sampling rate



(a)



(b)

Fig. 13. Comparison between scheduling techniques(a) round-robin (cannot schedule the given signals) and (b) HMS (can optimally schedule them using the available ADC)

The horizontal axis represents the time slots where the period between each consecutive time slots is the (T_s) which is equal to 10 μsec in this example. The vertical axis represents the channel being sampled at a certain time slot. As shown in the figure, three channels are mentioned in the vertical axis. At time slots (1, 3, 5,etc), channel 1 is sampled. At time slots (2, 6, 10,etc), channel 2 is sampled. At time slots (4, 28,etc), channel 3 is sampled.

10. Conclusions

The proposed ASAP system can be used to acquire human body signals such as the heart beat, pressure and the lung sound at home. Using a varying sampling rate per channel is the optimal solution in terms of scalability, power consumption and memory requirements. It is also considered as a versatile instrument that can be the base of developing a spectroscopic imaging. To date, the complexity associated with constructing a high-fidelity multi-channel, multi-frequency data acquisition instrument has limited widespread development of spectroscopic electrical impedance imaging concepts. To contribute to developing spectroscopic imaging systems, varying sampling rate need to be addressed.

Existing computer-based multi-channel DAQ systems are cumbersome, expensive, and/or inefficient when various heterogeneous signals are acquired. Embedded microcontroller-based DAQ systems have some advantages such as low cost, compact size, and low power consumption. However, it is not reconfigurable due to its fixed hardware architecture and can not be used for reconfigurable heterogeneous sampling. So, another DAQs category is needed in order to overcome other categories problems. Reconfigurable FPGA is used in this research as the center piece of the proposed system. In addition, the proposed system is unique as related to existing technologies. It has the maximal service scheduling capability which efficiently utilizes the single ADC to acquire heterogeneous multi-channel input signals. This leads to reduction in the circuit size, cost, power consumption, and storage requirements. In addition, the proposed DAQ is used without the need to computing systems such as a PC. Full system reconfigurability based on FPGA as well as the adaptive sampling is only available in the proposed ASAP system.

Two design methodologies are used to implement the archiving. Software acquisition and multiplexing approach is done via Hardware Description Language (HDL) and embedded C programming language. This approach has some drawbacks. Therefore, a second approach, hardware acquisition and multiplexing, is proposed using only Verilog HDL.

In hardware acquisition and multiplexing approach, different signals were applied to the proposed system and the NI systems. Acquired signals by both DAQ systems were tested in terms of root mean square of errors. It is found that, the best performance for proposed system has 37% better (smaller) RMS(e) than NI-base DAQ in the case of 10000 sample of 2 KHz input signal.

FFT implementation is done to determine each channel frequency. The accuracy of the FPGA-based FFT module implemented inside the DSPU is 98% in the case of using 512 FFT points. It reaches more than 99% in the case of using 2048 FFT points. After detecting frequency bandwidths via DSPU, FREDM detects and monitor any change in frequency values at any input channel.

Finally, to acquire human body multichannel signals, a fixed sampling rate is not the optimal solution. The proposed Heterogeneous Maximal Service Scheduler (HMS) achieves the optimal solution for large number of channels. It also reduces total power consumption and memory requirements. If the input signals have different frequency bandwidths,

then the proposed HMS is required to perform adaptive sampling, instead of using the highest frequency as a fixed sampling rate for all channels. That is because oversampling low frequency spectrum channels leads to unnecessary data, which in turn requires extra storage capabilities and more power consumption. Different case studies are studied in this research. As a result, the proposed HMS can schedule given tasks that are not schedulable via round-robin technique. Even in scenarios that both round-robin and proposed HMS can successfully schedule the given task, proposed HMS reduces the amount of data being acquired by 59%, which in turn decreases memory requirements and power consumption as well.

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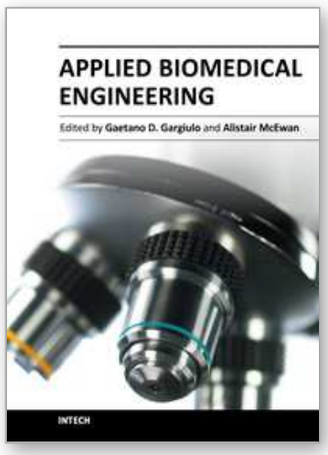

Applied Biomedical Engineering

Edited by Dr. Gaetano Gargiulo

ISBN 978-953-307-256-2
Hard cover, 500 pages
Publisher InTech
Published online 23, August, 2011
Published in print edition August, 2011

This book presents a collection of recent and extended academic works in selected topics of biomedical technology, biomedical instrumentations, biomedical signal processing and bio-imaging. This wide range of topics provide a valuable update to researchers in the multidisciplinary area of biomedical engineering and an interesting introduction for engineers new to the area. The techniques covered include modelling, experimentation and discussion with the application areas ranging from bio-sensors development to neurophysiology, telemedicine and biomedical signal classification.

How to reference

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Mohammed Abdallah and Omar Elkeelany (2011). Towards Affordable Home Health Care Devices Using Reconfigurable System-on-Chip Technology, Applied Biomedical Engineering, Dr. Gaetano Gargiulo (Ed.), ISBN: 978-953-307-256-2, InTech, Available from: http://www.intechopen.com/books/applied-biomedical-engineering/towards-affordable-home-health-care-devices-using-reconfigurable-system-on-chip-technology

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