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High Mass Molecular Ion Implantation

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1. Introduction

Semiconductor device manufacturing is facing stringent challenges in advanced COMS process technology nodes. Ion implantation technology has always been a good solution of last resort since it's got a much wider latitude and stronger flexibility to accommodate new challenges than any other process steps in device fabrication. It is not unusual that people utilize ion implantation not just for doping the silicon substrate, but also for compensating the shortfalls of other process steps. In the past decade, the process window, typically large enough for ion implant engineers to maneuver has gotten narrow, so narrow to a degree so that itself started to create problems which none other process steps can resolve, or compensate. These problems include dopant atoms activation, co-implant species of choice, pre-amorphization implant species of choice, implant damage control, runaway low-energy implant cost. High mass molecular (HMM) ion implantation is investigated in response to all these ion implant related problems.

Ion implantation is a process whereby energetic ions impinge on a target, penetrating below the target surface and giving rise to a controlled, predictable, ion distribution. Here we will focus on Si technology; hence the target will be mostly Si. Implanted ions are typically dopants, such as Boron, Phosphorus, Arsenic, Indium and Antimony. Table 1 shows these commonly used dopant elements in the periodic table of the elements. However, the scaling of device features into the sub-100nm regime has added species such as Ge, C, N, and Xe to this list. Implantation energies cover a wide range from 0.2 keV to >3 MeV; doses range from 1 x 10^{11} cm^2 to more than 1 x 10^{16} cm^2; incident angles cover normal incidence (a tilt angle of 0°) to 60°.

The industry has been using BF_2^+, as the molecular form of Boron, to implant in order to attain higher throughput for low-energy applications. This species has the disadvantage of co-implanting fluorine, which retards boron activation and increases contact resistance, both undesirable consequences for doping process (Foad, 2005). HMM implants have recently been introduced as an alternative. As the molecular structure shown in Fig. 1, Octadecaborane ($B_{18}H_{22}$), which has 18 effective dopant atoms in one molecule, has been proven a viable replacement for boron in poly-doping and BF_2 for ultra-shallow junction (USJ) formation.

Besides the advantage of higher productivity, HMM implant process advantages have been noticed and explored. Due to its heavy mass, HMM ion implant can eliminate the use of pre-amorphization implant (PAI). We can use the HMM ions that contains either dopant or co-implant species to replace PAI (Ameen, 2008). Implant damage control is also possible by the use of HMM ion implantation, due to germanium PAI elimination.

Table 1. Atomic dopant species that are commonly used in ion implantation.

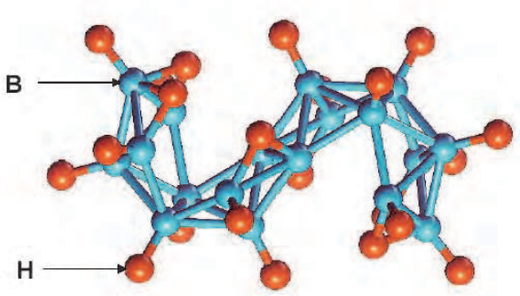

Fig. 1. Structure of Octadecaborane ($B_{18}H_{22}$) molecule.

Attempts have been made to implant molecular carbon ($C_{16}H_{10}$), of which the molecular structure is shown in Fig. 2, to replace Ge-PAI plus monomer carbon for advanced logic manufacturing. The latter mentioned monatomic implants are nowadays popular co-implants for USJ formation in the metal-oxide-semiconductor field-effect transistor (MOSFET) source and drain extension (SDE) doping process (Pawlak, 2006). Carbon is a standard co-implant in the MOSFET SDE implant sequence due to its capability of reducing dopant transient enhanced diffusion (TED). This is achieved through trapping of crystalline interstitial defects by the carbon atoms that are incorporated in the lattice substitutional sites (Carroll, 1998). Unless the silicon substrate is amorphized, the carbon implant could not be incorporated in the silicon lattice sites when undergone thermal annealing. In this case Ge-PAI is required, because carbon mass is too light to cause self-amorphization under most conditions. The use of molecular carbon opens up the possibility of replacing the traditionally used Ge-PAI, which is also known to leave residual damage leading to junction leakage.

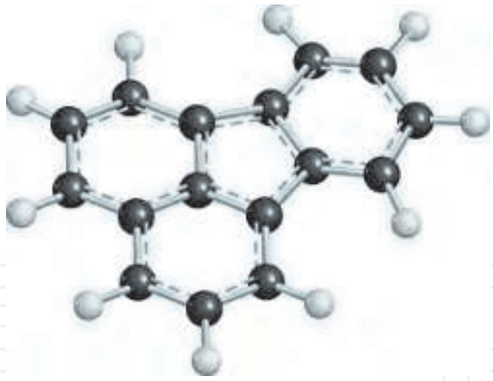

Fig. 2. Structure of $C_{16}H_{10}$ molecule

2. Overview

Semiconductor devices have become omnipresent due to their amazingly miniature in sizes, ever expanding functionalities in time, inexpensive manufacturing cost, and etc. Most of these reasons have to do with one historical event; the advent of commercial ion implanters. Impurity doping process is a major manufacturing step that needs to be repeated over and over for many times for the semiconductor material going from basic substrate to electrically functioning devices. Forty years ago, doping of semiconductor had been predominantly a thermal process, where the impurity is introduced at the substrate surface, and within a closed chamber at an elevated temperature, such as a furnace, the dopant atoms are allowed to diffuse into the substrate under a thermal equilibrium process. The speed, or the distance of impurity atom diffusion is dependent on the surface impurity concentration and process temperature. Usually, this temperature of operation is in the 1000 degree Celsius region. The atom diffusion energy is no greater than several eV's. This makes the doping process long and expensive.

Due to the advent of commercial ion implanters, the impurity doping process has shifted from predominantly thermally enhanced in nature to predominantly kinetically driven in nature. The impurity atoms are now being stripped of or bestowed with electrons in a part of the implanter called the "ion source", where they become ions to be accelerated in high electrical fields. Once the charge particles, or ions have gained the desired energies, they are collimated and then impinging into the substrate at high initial speeds. All of these actions are performed at room temperature. Although the process temperature for ion implantation is relatively low, the dopant ions acquire energies in the keV range. Therefore, the process time is less than one one-thousandth of that of a thermal process. Thus, the productivity is higher, and the cost is significantly lower too.

These advantages provide the semiconductor manufacturers with motivation to quickly adopt ion implantation in the process flow. They also give the process engineers and device engineers a lot of freedom to utilize the technique without having to wary of process constraints and tradeoffs too much. However, in the past decade, the process window, typically large enough for ion implant engineers to maneuver has gotten narrow, so narrow to a degree so that itself started to create problems, which none other process steps can resolve or compensate. These problems include insufficient dopant activation, co-implant species of choice, pre-amorphization implant species of choice, implant damage control, runaway low-energy implant cost

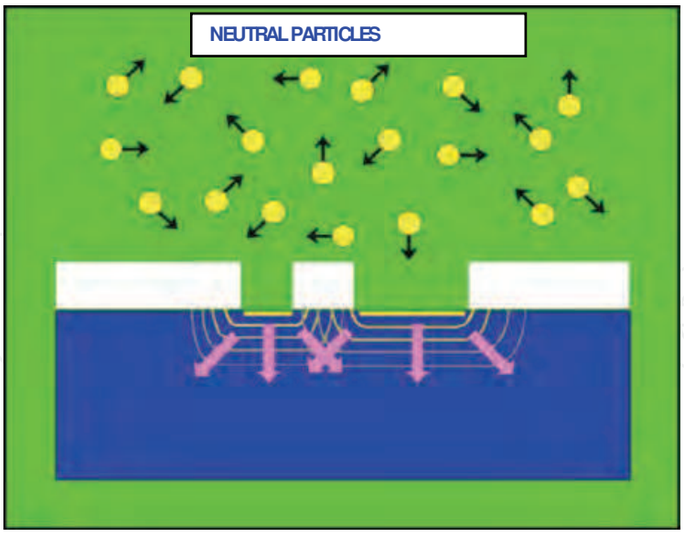

Fig. 3. a) Diffusion process is in thermodynamic equilibrium and energies are thermal (~eV) and random (isotropic)

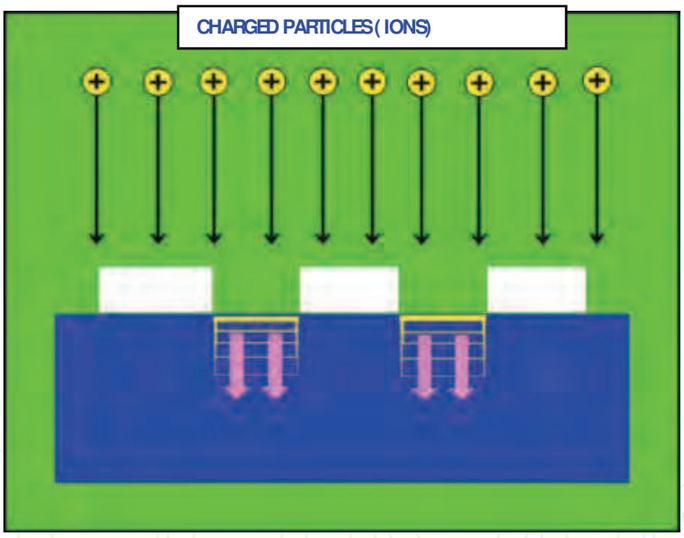

Fig. 3. b) Ion implantation is a process in which energetic, charged particles (atoms or molecules) are accelerated into the near surface of a target substrate at depths from ~10nm to ~1000nm (1 micron)

As time progresses, the process issue and cost issue are still the driving forces that motivate us to look at high mass molecular ion implantation, as oppose to monatomic implantation. However, among these two, the aspect of process requirements usually plays a dominant role in tool selection for semiconductor manufacturing. One obvious reason is that if people can quickly translate process benefits to device performance improvement, or geometry scaling down (in other words, device real estate saving), the cost it associated can be readily justified. In this chapter, we will also address the productivity and cost issue. However, the aspect of cost can hardly be the primary factor for choosing a process. We would like to

make sure the production method we choose today can be extended to cover for the future needs. Only by taking the whole picture into consideration, then one can start to appreciate molecular ion implantation being a production method for now and the future.

3. The process issues of implant damage

An ion implant process is basically putting the dopant atoms into the silicon substrate by bombarding the silicon wafers with very energetic ions. This process would inevitable result in crystal damage. The implant damage can take many different forms, such as non-equilibrium excess of vacant lattice sites (vacancies) and self-interstitial atoms (interstitials), vacancy clusters, interstitial clusters, dopant-interstitial and dopant-vacancy clusters, and locally amorphized regions of the crystalline silicon target. Iso-valent ions such as Si, or Ge are sometimes implanted to intentionally take advantage of this collateral damage. The annealing of this damage, and the electrical activation of the implanted dopants, requires that the implanted target receive a subsequent heat treatment. The as-implanted defect configurations evolve during post-implant thermal processing, giving rise to transient enhanced dopant diffusion (TED), and the formation of relatively stable dislocation arrays, which if present in active device regions can lead to degradation of electrical performance. An understanding of all these phenomena is therefore crucial to the design of the implant recipe and the post-implant thermal treatment.

In advanced CMOS processing, this amorphous layer plays important roles for several purposes. The top three are, 1) dopant channeling prevention; 2) dopant activation enhancement; 3) end-of-range (EOR) defect reduction. In other words, they represent the properties of controlled junction depth; higher conductivities; and lower junction leakage currents in the CMOS device respectively.

Achieving an implant profile without appreciable channeling is of practical importance to avoid that slight differences in beam orientation across the wafer result in radically different implant profiles. There are three different methods to prevent implant from channeling. As shown in fig. 4 a) the first choice is by tilting the wafer, which is the easiest way to achieve if it serves the purpose. However, only at high energies, where the critical angles are relatively small, this method can be effective. At low energies, the tradeoff between the amount of angle being tilted and the compromise it incurs to implant profile starts to become significant. If a low tilt angle is not sufficient for preventing implant channeling, we may have to go to a higher tilt angle. On the other hand, the implant shadowing effect, which is caused by device surface topology blocking the incident beam at an angle, starts to get intolerable. Therefore, merely by tilting the wafer plane away from beam incident angle might not be effective. The second alternative is to use sacrificial oxide to prevent implant channeling. This is shown in fig. 4 b). Since ion implantation may also introduce metal contamination to the wafer, it has been a common practice to use a thin layer of sacrificial oxide, from 100Å to 200Å thick to block the elemental contamination from penetrating the wafer surface. Once the implant process is done, this layer of sacrificial oxide would be stripped of from a wet bench using buffered oxide etching solution. However, due to advanced devices are very sensitive to "substrate loss", or so to speak "dopant loss", people have begun to move away from using sacrificial oxide. Finally, the most inconvenient method for preventing implant channeling is, as depicted in fig. 4 c), by inserting a pre-amorphization implant before dopant implant. Usually, this implant species of choice is non-electrically active, or iso-valent atom, such as germanium or silicon. It is indeed an

effective way to prevent implant channeling. The drawback is that it adds an additional implant step to the process.

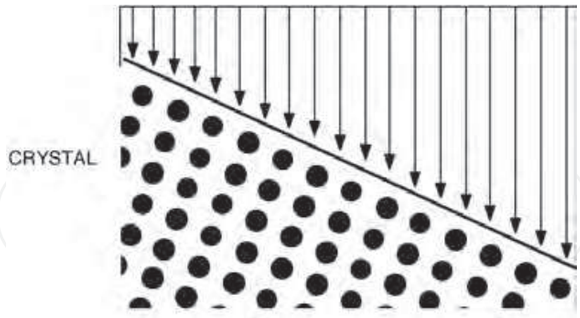

Fig. 4. a) Tilting wafer off the channeling plane.

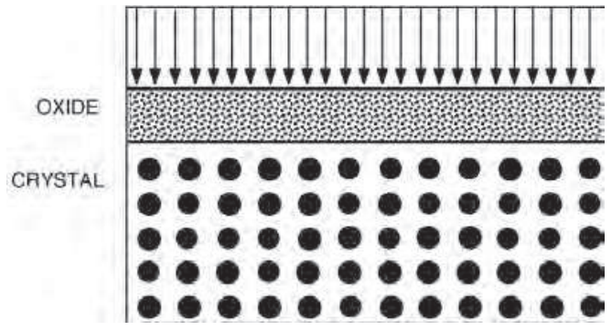

Fig. 4. b) Thin sacrificial oxide for randomizing the direction of incident ions.

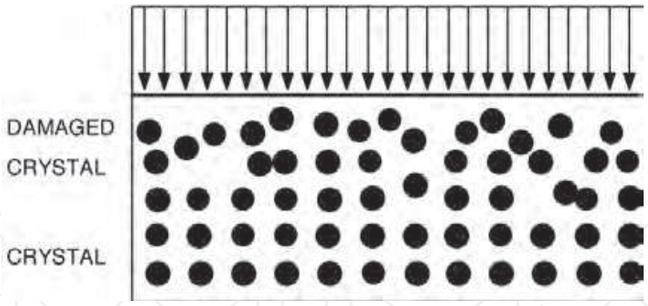

Fig. 4. c) Pre-amorphization implant to randomize the lattice atoms, thus destroy the crystal channels.

4. The process issues of thermal annealing

After ion implantation, the substrate needs to be treated with thermal processes. This is because the silicon substrate is damaged by ion bombardment, and needs to be "annealed", which is a thermal treatment to recover its crystalline structure. Meanwhile dopant atoms can be incorporated into the crystal lattice and become electrically active. As depicted in fig. 5, these two goals should be achieved simultaneously. Since this thermal treatment can also cause dopant diffusion, there would be some dopant redistribution.

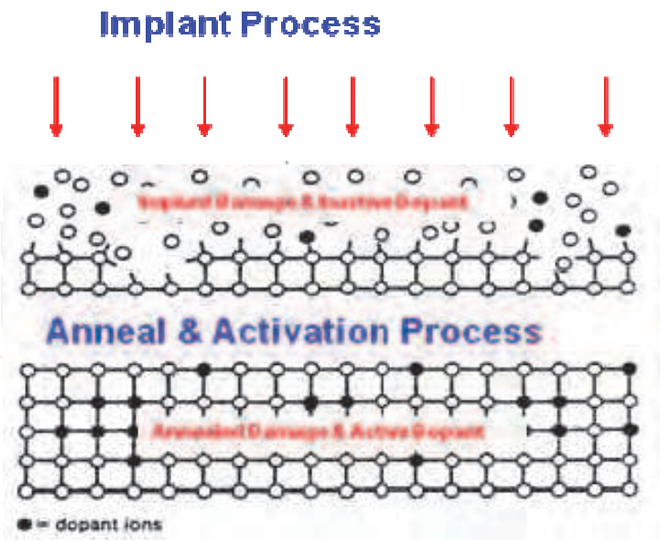

Fig. 5. The implant damage and inactive dopant atoms left in the silicon substrate need a post implant anneal to active the dopant and recover the crystalline structure.

From the logic manufacturing side, when the technology moved beyond 0.25um (deep sub-micron) era, the requirement of SDE is demanding USJ formation. This requirement is in response to the potential short channel effect (SCE) associated with device shrinkage. The geometry of device structure has to be tightly controlled now. In short, the "as implanted" dopant profile and dopant redistribution during anneal need to be well managed. For shallow junctions, dopant concentration levels can be very high. These implanted atoms tend to form high density crystal defects. The thermal budget for implant anneal has been greatly reduced for advanced logic devices due to the concern of excessive dopant re-distribution when the device is undergone high temperature thermal anneal. However, if the thermal budget is insufficient, the crystal defects could not be totally removed, and would lead to adverse effects on device performance, such as high device leakage currents.

It has been known for some time that boron diffusion can be enhanced by damage introduced by the implant process. For example, fig. 6 shows the enhanced diffusion of a boron marker produced by molecular beam epitaxy on a silicon substrate, which was subsequently damaged by $1x10^{14}$ cm^{-2} silicon implants at various energies and then subjected to a 950°C/30s anneal. The enhancement scales linearly with the projected range of the implant which is approximately where the damage induced excess interstitials are initially located (Agarwal, 1997; Gossmann, 2000).

The phenomenon of transient enhanced diffusion (TED) after ion implantation increases the challenge of forming ultra-shallow junctions (Agarwal, 1997, 1999a, 1999b). Ion implantation leads to the displacement of silicon atoms from their lattice positions, creating pairs of vacancies and interstitials. During the initial stage of post-implantation annealing most of the vacancies and interstitials recombine leaving behind a net excess of interstitials approximately equal to the implanted ion dose; this is also referred to as the "+1" approximation (Giles, 1991). These excess interstitials quickly coalesce into extended defects, such as {311}'s (Eaglasham 1994; Stolk, 1997), or more stable dislocation loops. While these extended defects have lower free energy than individual interstitials (Eaglasham 1994; Rafferty, 1996), they are still metastable and dissolve with continued annealing. As they dissolve, they release excess

interstitials into the lattice. Since boron diffuses by an interstitial mechanism (Gossmann, 1997) its diffusivity is enhanced by the excess interstitials with the time averaged diffusivity enhancement equal to the time averaged interstitial supersaturation . Both the interstitial supersaturation and the diffusivity enhancement end soon after the defects have dissolved. This phenomenon is depicted in fig. 7.

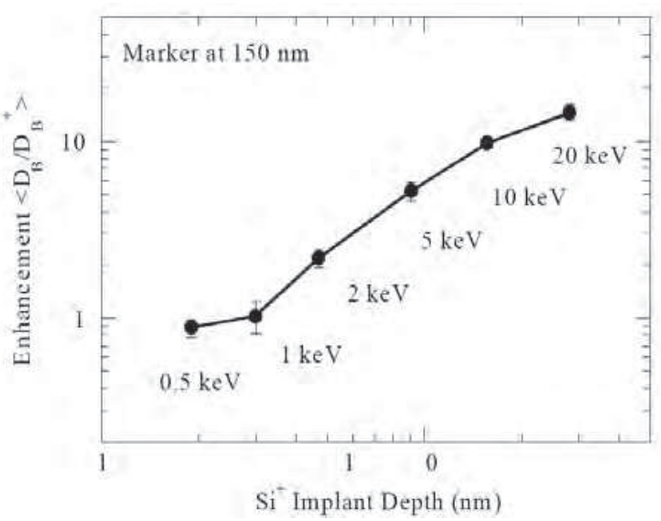

Fig. 6. Enhancement in diffusion of a boron marker layer, grown by molecular beam epitaxy during a 950°C/30s anneal, following implantation of $1x10^{14}$ cm^{-2} Si at various energies (Agarwal, 1997; Gossmann, 2000).

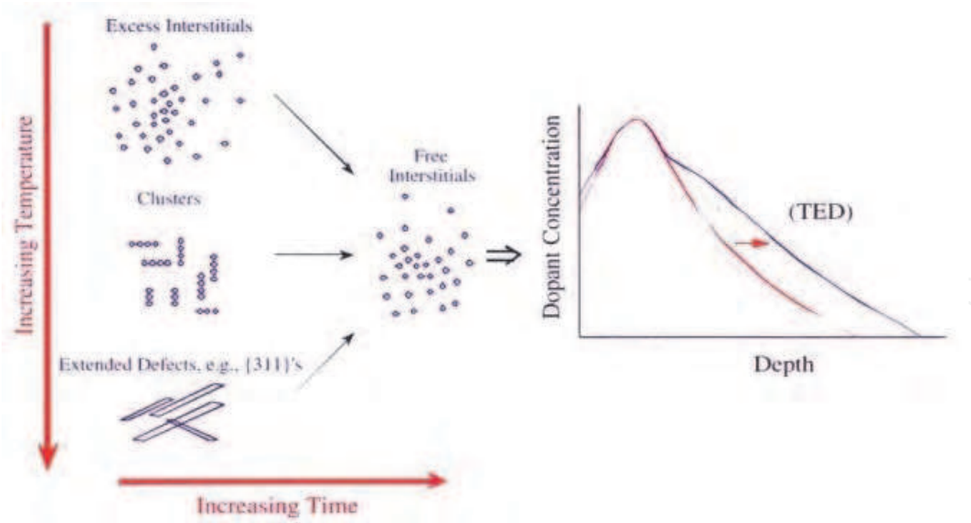

Fig. 7. Boron diffuses by an interstitial mechanism; its diffusivity is enhanced by the excess interstitials.

The increase in junction depth, Δx_j, due to TED to be expressed as (Gossmann, 1998; Rafferty, 1996)

$$\Delta x_j^2 \propto N \cdot R_p \cdot \exp[-(-1.4eV)/kT] \quad (1)$$

where N is the number of interstitials trapped in the defects (approximately equal to the implanted dose) and R_p is the projected ion range (where the excess interstitials are initially located). The linear dependence on Rp has been demonstrated experimentally, as shown in fig. 6. The activation energy of Δx_j^2 is negative because the interstitial supersaturation due to the presence of the extended defects is larger at lower temperatures. This implies that the final junction will be deeper if the defects are annealed out at a lower temperature than at a higher temperature. This is a key reason why junction anneals are done in a rapid thermal annealing (RTA) rather than in a conventional furnace with a ramp-up rate of a few degrees per minute. An RTA spends significantly less time during the temperature ramp-up at lower temperatures where the diffusivity enhancement is larger.
Since the increase in junction depth due to TED depends on the implant dose (Eq. 1), it is possible that for a high dose implant some damage will remain after a fast ramp-up, allowing TED to continue during the ramp down (Agarwal, 1999). As the ramp-up rate is increased, the temperature at which TED runs out is pushed up until the TED is pushed over to the ramp-down side of the anneal (Agarwal, 2000). This is illustrated in fig. 8.

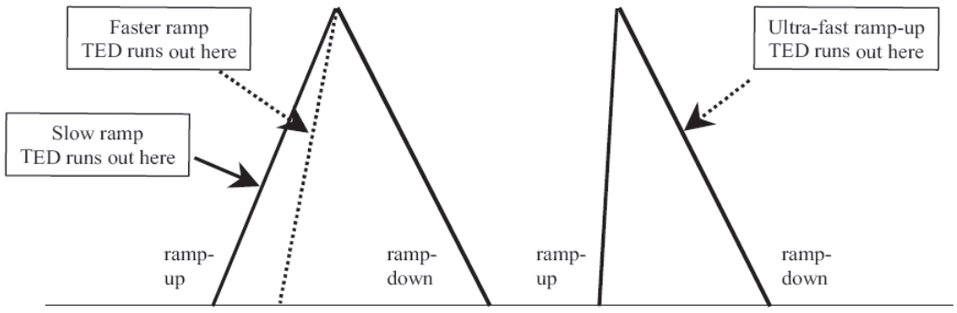

Fig. 8. Schematic illustration of TED continuing during ramp down of a spike anneal that is sufficiently fast (Agarwal, 2000).

In the sub-keV regime, there is more than one way to arrive at the same junction properties. It is very important to minimize the dose first, before reducing the energy further. The dependence of the sheet resistance and junction depth data on the different implant and annealing parameters is summarized in fig. 9. Increasing the ramp-up rate leads to a more shallow junction with higher resistivity. The same is also true when a smaller dose or energy is used. Modifying the implant parameters first helps avoid the risk of poor process repeatability which necessarily accompanies the use of higher ramp-up rates.
As the advanced logic manufacturers manage the implant and anneal together in an effort to meet the process requirements, the treadmill of device scaling is relentlessly pushing the implant dose higher and energy lower. The conventional USJ scaling is inevitably hitting the limits. The USJ formation for SDE is key for 65nm technology node and beyond (Foad, 2005). The obstacles include boron TED, low boron solubility limit in silicon, and most of all, post-anneal residual implant damage. For high dose applications, not all implant damage can be removed by the anneal process due to insufficient thermal budgets from "spike" RTA or ms laser spike anneal (LSA) processes. If this damage is in the wrong place, increased device leakage and catastrophic p-n junction shorts are probable. This scenario is depicted in fig. 10. Engineering the type, extent, and location of post-anneal residual implant damage is one of the primary objects of Front End of Line (FEOL) process integration.

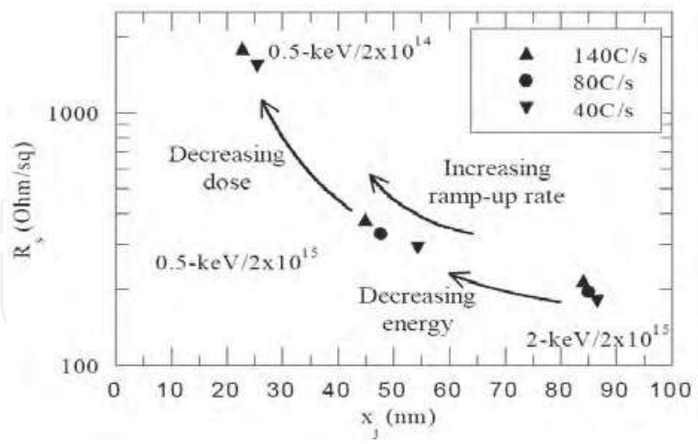

Fig. 9. Sheet resistance vs. junction depth as a function of ramp rate, implantation dose and implantation energy. Note the similarity between increasing the ramp-up rate or reducing the energy and dose (Agarwal, 1999, 2000).

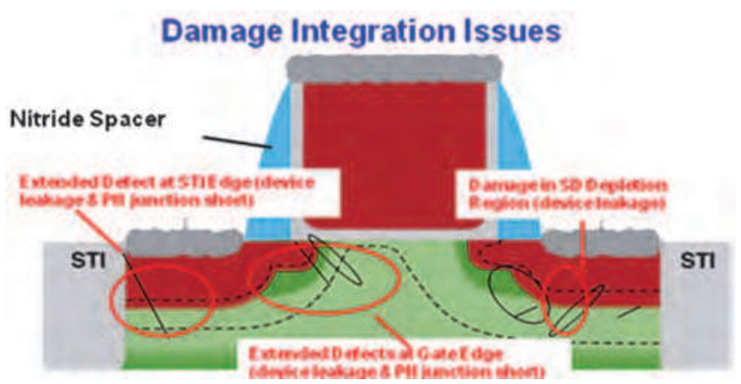

Fig. 10. When the EOR defect damage is in the wrong place, increased device leakage and catastrophic p-n junction shorts are probable.

5. Molecular implants

Molecular implants have long been considered by the IC manufactures as alternatives to atomic implants for low-energy applications (Jacobson, 2001). The major benefit of using molecular species implants is wafer throughput improvement due to higher effect beam currents when implanting at low energy. A molecular ion dissociates into its constituent atoms at the wafer surface. The constituent atoms then continue with a fraction of the total energy. This phenomenon can be utilized to gain wafer throughput in the sub-5.0keV range as implanters in general can deliver higher molecular beam currents at higher extraction voltages, and still provide equivalent processes to the low-energy monatomic implants.

A well-known and long-used example of this in production environments is BF_2^+ implantation as a means of delivering a lower effective energy boron as the molecular type of p-type dopant. More recent experimentation with molecular n-type dopants has

demonstrated that As_2 and P_2 can provide production-worthy beam current and throughput improvements with comparable process results (Chang, 2003).
The formation of aggressive n-type junctions has not posed as severe a challenge as p-type junctions in the past, due to the much larger atomic mass (75 amu for As, versus 11 amu for B) and lower diffusivity in Si. Arsenic dimer implant requires twice the ion energy of the monatomic implant. However, the effective fluence of a dimer implant is two times that of a monatomic implant, since both atoms in the dimer ion contribute to the total dopant dose. Therefore, it requires only half the dose of a monatomic implant. These conditions can be expressed by equations (2) and (3).

$$E_{eff} = E_{extraction} / 2 \tag{2}$$

$$I_{eff} = 2 \times I_{measured} \tag{3}$$

Since ion implanters can in general produce more I_{eff} (molecular) beam current than I_{eff} (atomic) beam current at $E_{extraction}$ under these operating conditions, a significant throughput advantage may in many cases be realized.

5.1 High mass molecular implants

In recent years significant advances have been made in the development of high mass molecular (HMM) beam sources for dopant implantations into silicon. The driver for the development of these sources has been the need for very low energy implants. Energy is partitioned between the atoms of a molecule in direct proportion to their mass. For example, the widely used molecular ion BF_2^+ with atomic mass ~49 having a single boron atom of mass ~11 results in the implantation of boron at an energy that is ~11/49 of the molecular ion energy, e.g. a 10 keV BF_2 implant, for example, is energetically equivalent to a 2.24 keV B implant.
A much more dramatic example of this energy partitioning may be achieved with decaborane ($B_{10}H_{14}$) (Jacobson, 2001) where a 10keV implant is equivalent to a ~1 keV implant. Recently, another large boron containing molecule, Octadecaborane ($B_{18}H_{22}$) has also been identified as a useful molecule for this application (Perel, 2001). It is important to note that with these molecules, one milliampere of ion beam current is equivalent to 10 (for decaborane) or 18 milliamperes (for octadecaborane) of boron current. For this reason the molecular beam obviates many of the space charge limitations associated with the ultra-low energy Boron beams. Conventional ion sources are not suitable for decaborane or octadecaborane implantation since the high arc chamber temperature causes disassociation of the molecule. Ionization chamber temperatures below 300°C are required and a different approach to electron impact ionization of the molecule is required. Figure 11 shows a commercially available octadecaborane ion source (Jacobson, 2005). Also, the ionization process results in a distribution of ions of the form $B_{10}H_x$ or $B_{18}H_x$ with the result that the mass resolved spectrum consists of a typically up to 10 peaks, all containing the same boron content but with varying hydrogen content. As a result, the acceptance of the mass resolving system must be increased to allow for maximum utilization of the available molecular ion current (Perel, 2001). Figure 12 gives a typical mass resolved spectrum obtained from a decaborane source (Jacobson, 2005).

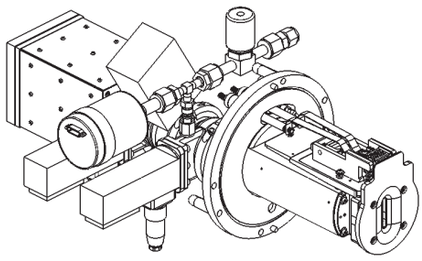

Fig. 11. Ion Source Suitable of Decaborane or Octadecaborane Ion Beam Generation (Jacobson, 2005).

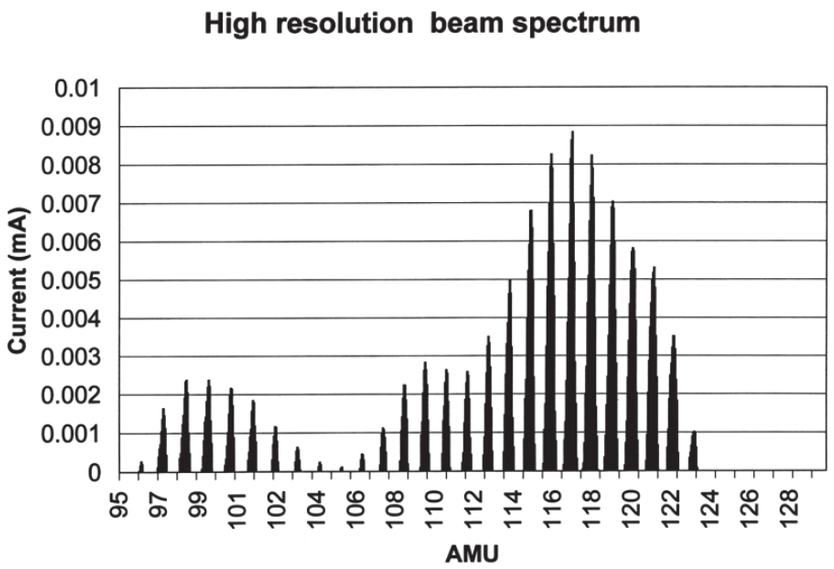

Fig. 12. Typical mass resolved spectrum obtained from a decaborane source.

5.2 High mass molecular implant application for DRAM

The aggressive scaling of DRAM puts severe constraints on the gate formation. Single work function polysilicon gate for PMOS with buried channel will suffer serious short channel effect as the scale shrinkage continues. Meanwhile, its high leakage is not tolerable for the requirements of low power high performance devices. The high leakage comes from the fact that the buried channel is away from the surface; hence, the gate can't control the channel as effectively as surface channel. As the dual work function poly gate shows the advantage of easiness of Vt control and resistance to short channel effects, Surface-channel PMOS with P+ poly gate will take substitution of buried-channel PMOS with N+ poly gate for advanced devices inevitably. Figure 13 shows the channel current flowing underneath the surface in a buried-channel PMOS device of the left, and on the surface in a surface-channel PMOS device on right.

Octadecaborane ($B_{18}H_{22}$) implant technology was evaluated for p+ poly gate doping process in a 72nm node stack DRAM device. For DRAM manufacturing, the 7x-nm-class is about the technology node where the device performance requires dual-poly gate structure for

tuning the PMOS and NMOS work functions separately. Since the gate poly is in-situly dosed with n-type dopant during CVD polysilicon deposition, the PMOS gate poly needs to be doped heavily with p-type dopant afterwards, in order to counter dope the gate and transform it from originally n-type to p-type poly. Therefore, it requires low energy (< 5keV) and high dose boron implant (> 5×10^{15} /cm^3). The evaluation criteria were to improve the productivity of the process, which was initially built with conventional atomic boron implantation (^{11}B), while maintaining process equivalency. Before implanting into device wafers, process matching to conventional boron implant was done using both crystalline silicon and poly-silicon on Si wafers (Chang, 2008). For the crystalline silicon wafers, the R_s of blanket $B_{18}H_X^+$ implants were compared to that of atomic boron. For the poly-Si silicon wafers, SIMS dopant profiles were compared. For the device wafers, boron penetration, gate depletion, and final yield were compared. In addition, $B_{18}H_{22}$ implant splits of various energies and doses have been studied for their sensitivities to the electrical performance of the p-MOSFET in the 72nm node stack DRAM devices. In this study, we have demonstrated that $B_{18}H_{22}$ can provide up to 5× wafer throughput advantage over conventional atomic boron process due to much higher effective beam currents. Besides the significant productivity improvement, $B_{18}H_{22}$ implant device characteristics were well matched to the baseline atomic boron process.

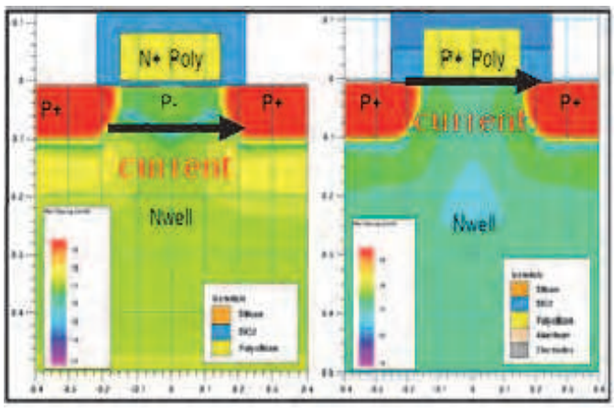

Fig. 13. The channel current flowing underneath the surface in a buried-channel PMOS device of the left, and on the surface in a surface-channel PMOS device on right.

In a BF_2^+ implant, the extraction energy is 49/11 times the desired Boron energy. Under the same principle, a $B_{18}H_{22}$ implant extraction energy is 210/11 times the desired Boron energy. These conditions can be expressed by equations (4) and (15).

$$E_{eff} = E_{extraction} \times \left(\frac{11}{210} \right) \tag{4}$$

$$I_{eff} = 18 \times I_{extraction} \tag{5}$$

Since ion implanters can in general produce more I_{eff} (molecular) than I_{eff} (atomic) at $E_{extraction}$ under these operating conditions, a beam current and thus throughput advantage may be realized. For example, a 2keV boron implant can be run using over 2.5mA of $B_{18}H_{22}^+$ beam current, or 45mA of effective boron current.

In this study, we used Axcelis' OptimaHD Imax implanter for molecular boron implants. The Imax was developed for ionizing, transporting and implanting molecular species such as $C_{16}H_{10}$ and $B_{18}H_{22}$. Figure 14 shows the R_s of B18 implant versus POR boron implant for the P+ gate poly process. The B18-implanted wafers require higher doses to match the POR R_s. The slightly under-dosing of the $B_{18}H_{22}$ implant in this case could be caused by a difference in dose retention between B18 and monomer boron. For low-energy implants, as dose increases, the fraction of dopant loss increases due to the sputtering, where near surface atoms leave the target during implantation due to recoil collisions. This phenomenon is depicted in fig. 15. While a detailed comparison of B18 and B has not been carried out, the retained dose of B18 as a function of energy has been reported (Harris, 2006). From the dose sensitivity test, a dose trim factor of 1.17 (17% higher dose) was determined for the P+ gate poly process, which has a lower target Rs.

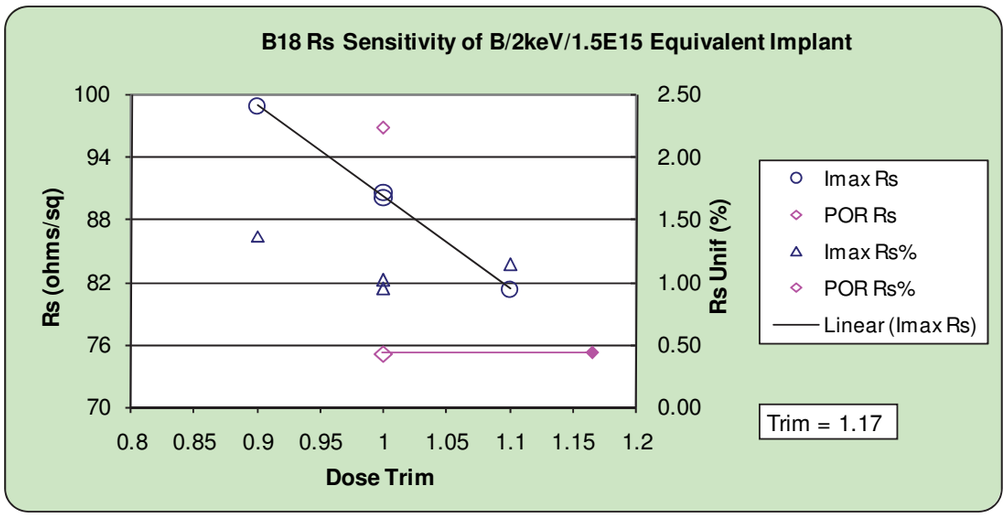

Fig. 14. P+ poly process R_s matching for the recipe of B/2keV/1.5×10^{15}cm^{-2}

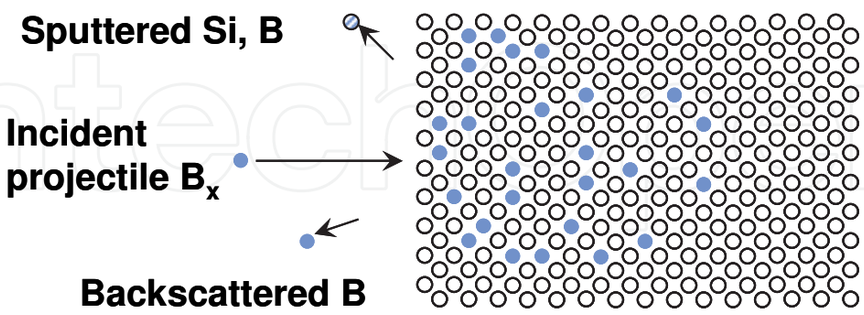

Fig. 15. For low-energy implants, as dose increases, the fraction of dopant loss increases due to the sputtering, where near surface atoms leave the target during implantation due to recoil collisions

In this test, wafers of poly implant conditions were subject to secondary ion mass spectrometry (SIMS) profile analysis. Figures 16 and 17 show the implant profiles of as-implanted and annealed implants from TPOR and Imax. The poly thickness is 90nmin this

case. The annealing condition is RTP for a 20s soak at 965C. The implant dose for B18 has been adjusted to account for dopant loss. Meanwhile, the split conditions were designed for a process window check. Table 2 shows the comparison of the accumulated doses in SIMS.

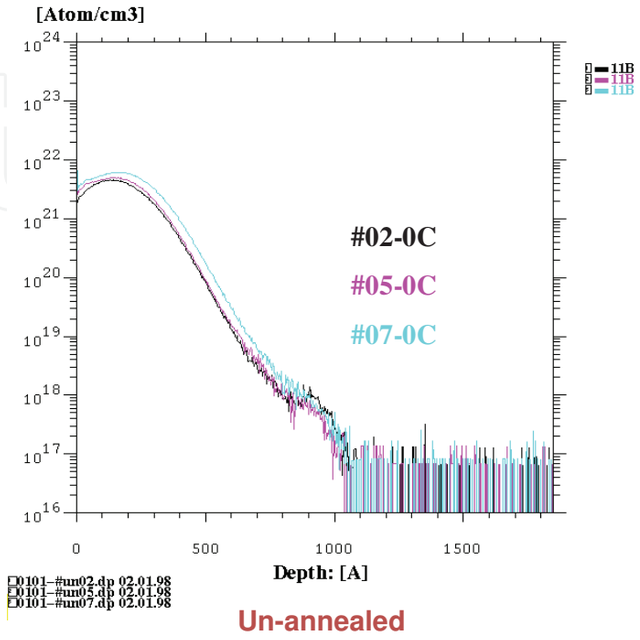

Fig. 16. As implanted SIMS profiles for B and B18 implants.

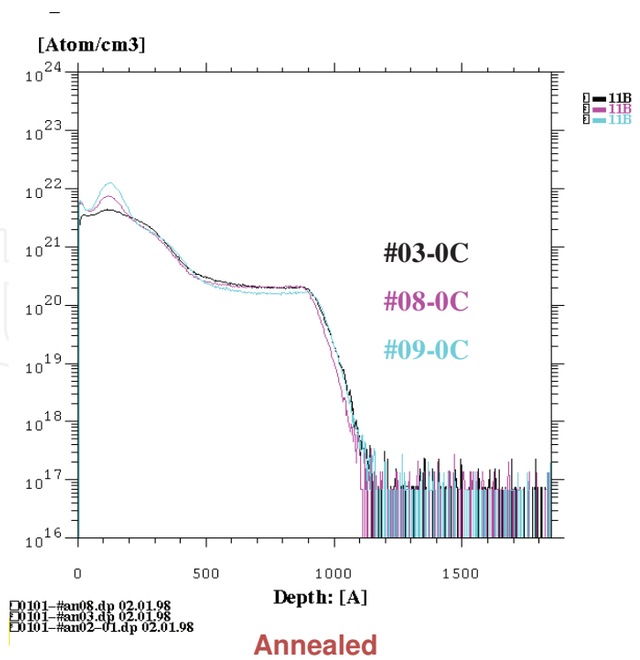

Fig. 17. Annealed SIMS profiles for B and B18 implants.

Remark	Sample no.	Dose (atom/cm^2)
POR (B11/4keV)	#2	1.202E+16
	#3 (anneal)	1.294E+16
IMAX (B18H22/76.8keV)	#5	1.382E+16
	#8 (anneal)	1.554E+16
IMAX (B18H22/80keV)	#7	1.828E+16
	#9 (anneal)	2.041E+16

Table 2. Accumulated SIMS dose for all samples.

Figure 17 shows that B18 implants seems to get a near surface bump as their signature. This could be due to the hydrogen effect. Since for every B18 ion implanted into the wafer, 22 hydrogen atoms would also be implanted. And hydrogen would enhance boron out diffusion. In some literatures, the possibility of hydrogen induced boron pile up in the surface has been discussed (Berry, 2008). Nevertheless, B and B18 implant profiles are matched at the oxide interface for as-implanted and annealed samples. Since the dopant concentrations match at the critical depth of the profile, we can view the SIMS profiles as matched in this case. Therefore, the implant matrix for the product wafers is to split the dose at target, ±10%, ±20% and ±30% for the P+ poly doping recipe. Device PMOS Vth does have a trend corresponding to different dosages. As the dosage gets high, the Vth gets high too. However, the biggest deviation is less than 10mV, we can say that the device results are all meeting the specification (Chang, 2008).

5.3 Molecular implant applications for advanced logic

As device scaling continues previously acceptable implant technologies for p-MOSFET SDE are struggling to meet advanced device requirements. There are three metrics that must be simultaneously achieved; those are device leakage, p-type dopant activation and junction depth control. In order to meet all of these goals, we found that molecular carbon implant is particularly well suited for USJ formation of the p-MOSFET SDE.

Due to preserving device geometry is of primary importance, junction depth control is the first thing to consider. Recent years, people have started to use carbon implant to suppress boron TED. The reason is that when carbon concentration is high enough (above $1\times10^{19}cm^{-3}$), it would create an interstitial "under-saturation" region (Carroll, 1998) (Moroz, 2005). Therefore, boron dopant atoms would less likely to be "kicked-out" by the excessive interstitials in the lattice, and implant profile remains stable during annealing. In order to incorporate carbon into silicon, the implant layer needs to be fully amorphized before annealing. Therefore, germanium pre-amorphization implant (Ge-PAI) was inserted in the process flow. Although it is a common practice to use Ge-PAI now, we all know that Ge-PAI is problematic due to it results in elevated end-of-range (EOR) defect damages, which have been identified as the leakage source for the devices. In the light of this concern, we put the constraints on Ge-PAI usage, so that it would not impact the junction quality. However, the trade-off between limiting Ge-PAI dosage and excessive residual implant damage may lead to an insufficient amorphous layer for carbon incorporation.

The other way to get around of this problem would be to increase the carbon implant dose, so that it reaches the critical dose for the formation of amorphous layer. However, carbon also leaves behind point defects (Mirabella, 2002), and causes device leakage. Although the effect of these point defects left behind by carbon implant are still under investigation, the

increase in sheet resistance is observable. This is due to carbon diffuses predominantly by a "kick-out" mechanism. If carbon concentration is too high, it would unavoidably compete with boron dopant atoms for occupying lattice sites, and kick the already electrically active boron atoms out of the lattice sites. Therefore, the use of carbon should be evaluated of its pro's and con's. If we go beyond a certain dosage of carbon, the benefits of activation improvement and diffusion suppression would be compromised by the excessive implant damage and dopant deactivation.

Since High Mass Molecular (HMM) implants have been known to create an amorphous layer as effectively as the heavy ion species (Krull, 2006), implanting molecular carbon is a potential technique to replace the process steps of Ge PAI plus monomer carbon implant. $C_{16}H_{10}$ is shown to be a consistently self-amorphizing method for introducing carbon into the extension region.

In a preliminary study, we used Axcelis' OptimaHD Imax implanter for molecular carbon implants. We proved that a single implant of $C_{16}H_{10}$ can effectively replace a two step Ge + C implant sequence. As logic device technologies advanced into the 40nm node, USJ requirements became very stringent. The x_j target of p-MOSFET SDE implant is very aggressive, less than 20nm per ITRS roadmap (ITRS 2005). In order to meet these requirements, both the implant and anneal of p-type species need to be considered simultaneously because their interaction is essential to the desired outcome. The process of record (POR) for Ge +C in this case is a Ge/12keV/1×10^{15}cm^{-2}+ C/2.5keV/1×10^{15}cm^{-2} implant sequence. We compared the B/400eV/1×10^{15}cm^{-2} implant Rs-Xj results with the presence of the Ge + C, against $C_{16}H_{10}$ implant of the equivalent carbon dose and energy. Figure 18 shows an XTEM image of a $C_{16}H_{10}$ implant at 2.5keV per carbon atom, with1×10^{15} cm^{-2} dose. The amorphous layer is around 12.9nm, whereas, the projected range of this carbon implant is at 10.2nm, according to SRIM. This result is in line with the data previously published (Mirabella, 2002), and sufficient for the purposes of this study.

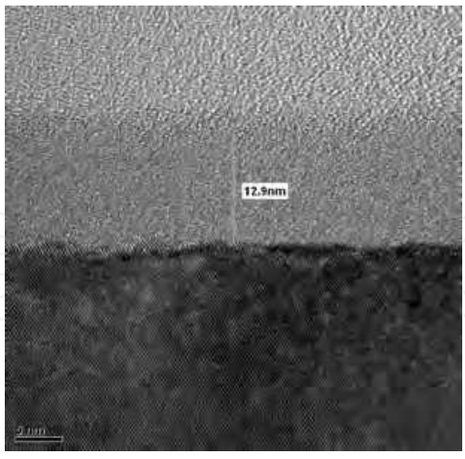

Fig. 18. XTEM image of a $C_{16}H_{10}$ implant at 2.5keV per carbon atom, with 1×10^{15}cm^{-2} dose

For the case of laser spike annealing (LSA) only, a comparison of POR co-implant against $C_{16}H_{10}$ implant effect on the boron SDE implant is made in figure 19. The R_s vs. X_j of the two implants indicate that if LSA only was used, it is easy to achieve the advanced logic process target. The Rs of the boron SDE implant with the one step $C_{16}H_{10}$ implant is comparable to that of the Ge + C co-implant's. However, one can see that monatomic co-implants may still

be insufficient for suppressing the boron diffusion above 15nm deep in the substrate. Although the amorphous layer created by Ge/12keV/1×10^{15}cm^{-2} is around 20nm, the total defects it creates could provide a lot of interstitials in the deeper region. If one pays attention to the boron profile, one can see the characteristic signal of the amorphous layer and crystalline layer interface at around 20nm deep. The carbon atoms would segregate at this interface, and influence the subsequent boron diffusion. However, one can argue that the tail region of the annealed boron profile for the Ge + C co-implanted case, being slightly higher at around 15nm is beyond the p-n junction. No matter how the defect damage is distributed, we would still expect that the one step $C_{16}H_{10}$ implant should cause much less implant damage and easier to be annealed. Frontier Semiconductor provides a metrology system that measures the non-contact sheet resistance, and leakage current, called RsL. The RsL leakage current measurement for Ge + C co-implanted USJ shows an average of 28 uA/cm^2 in this case. And the RsL leakage current measurement for Ge + C co-implanted USJ shows an average of 0.7 uA/cm^2 in this case. This is only one fourth of the leakage current from POR.

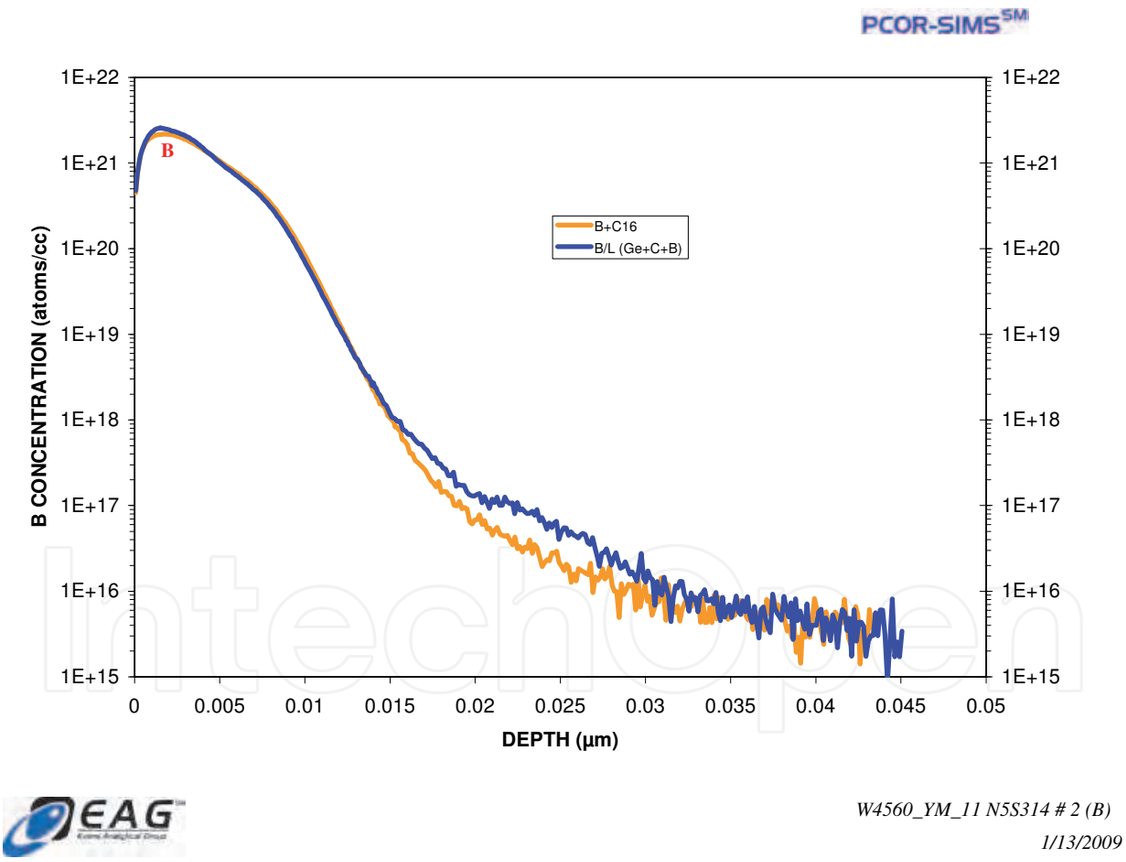

Fig. 19. Comparison of the B/400eV/1×10^{15}cm^{-2} LSA annealed dopant profile with the presence of the Ge + C, and $C_{16}H_{10}$ implant. The POR is a Ge/12keV/1×10^{15}cm^{-2}+ C/2.5keV/1×10^{15}cm^{-2} implant sequence, and $C_{16}H_{10}$ implant is of the equivalent carbon dose and energy.

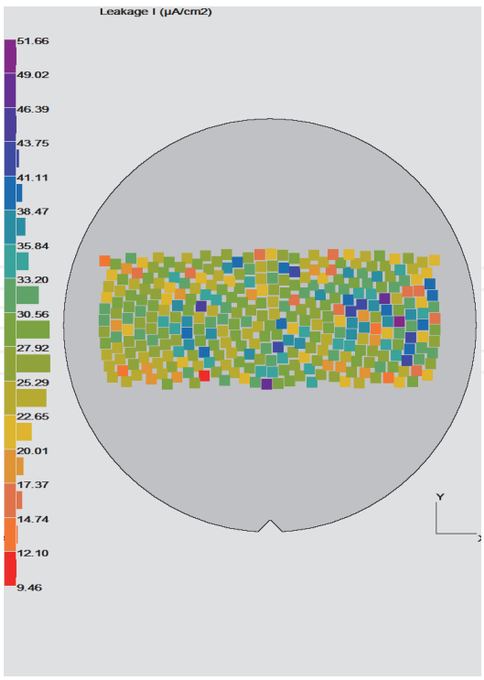

Fig. 20. RsL leakage current measurement for Ge + C co-implanted USJ shows an average of 28 uA/cm² in this case.

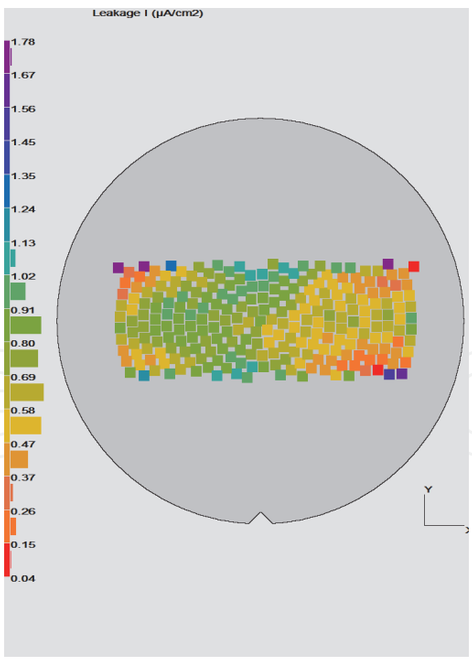

Fig. 21. RsL leakage current measurement for $C_{16}H_{10}$ co-implanted USJ shows an average of 0.7 uA/cm² in this case.

We also investigated the combination of $C_{16}H_{10}$, and $B_{18}H_{22}$ implants for USJ formation in a p-MOSFET SDE doping process for a 40nm logic device. We studied the split condition of

various energies, beam currents, and different advanced annealing schemes. The objective of this study is to use molecular carbon implant technology to supersede monomer carbon implants as a new process step in advanced CMOS device manufacturing. There are several reasons for the industry to consider molecular carbon instead of monomer carbon. First, conventional monomer carbon implant has poor implanter productivity. Secondly, carbon implants may have side effects (Mirabella, 2002), such as their competition with electrical dopant for substitutional silicon lattice sites and formation of excessive point defects, and incur penalties as well as benefits. Therefore, its adoption requires complicated integration schemes.
The purpose of this study was on developing the future USJF. Since the annealing program could be altered and the thermal budget be reduced, the focus was put on the interaction between implant and anneal. There are three different annealing programs involved in this study. The first one is a millisecond laser anneal. The second and the third programs are with spike RTP with the peak temperatures at <1000°C and >1000°C, and followed by laser anneal. We denote them as anneal "A" and anneal "B" respectively. In the blanket wafer test part, an implant and anneal matrix was designed to study the possibility of using $C_{16}H_{10}$, to replace the 2-step Ge-PAI + carbon co-implant sequence. In the device wafer test, we use the p-MOSFET of 40nm node logic, which requires high dose and low energy BF_2 implant, along with three other co-implants for the SDE doping process. In this study, the productivity of $B_{18}H_{22}$ for low energy boron implant was also evaluated. We first focus on the process matching of $B_{18}H_{22}$ to the recipe of 3keV BF_2^+ in the process of record (POR). There is also a 2-step Ge-PAI + carbon co-implant sequence precedes the BF_2 SDE implant. In the subsequent annealing process, both RTP spike and LSA annealing are applied in this case. Since there is fluorine in the BF_2 implant, which is known to affect the boron doping profile during anneal, the $B_{18}H_{22}^+$ energy may need some adjustment to reflect the difference in the boron diffusion profile from the influence of fluorine.
If the conventional co-implants were replaced by $C_{16}H_{10}$, the R_s could be further improved when millisecond laser anneal was applied. This offers the process solution to the LSA only scheme. We expect lower device leakage since Ge-PAI was eliminated. In this case, a light RTP spike anneal was applied to remove the implant damage. Although the molecular carbon implant appears to have the process equivalency as the conventional co-implants, it has lost the process advantages in R_s reduction as shown in the LSA only case. Figure 22 shows the 350eV boron post anneal dopant profile of different annealing schemes. As expected, the xj increases in accordance to RTP temperatures. LSA offers diffusionless anneal, and it only shifts the profile for no more than 2nm deeper, and gets the best sheet resistance. If the spike RTP was added prior to LSA, the profile would shift from 5 to 7nm for "A" annealing scheme and "B" annealing scheme respectively. In figure 23, the 350eV boron implant of the 2-step co-implant is compared against the $C_{16}H_{10}$ co-implant. The xj of these two implant schemes all shift 5nm after "A" annealing scheme. We can conclude that, even with the light spike RTP added in the annealing scheme, molecular carbon co-implant would behave the same as the monatomic co-implants. The reason is that millisecond anneal, although can activate boron dopant atoms effectively, it doesn't remove the excessive interstitials resulted from implant damage due to limited thermal annealing. When a spike RTP in the 1000°C regime was applied, the implant induced EOR defect damage would resolve and release the interstitials, which allows the boron TED to run out its course, due to sufficient thermal energy. Therefore, the self-amorphization property of the molecular $C_{16}H_{10}$ implant may not bring process benefits to p-type USJ formation, unless a diffusionless annealing scheme is employed.

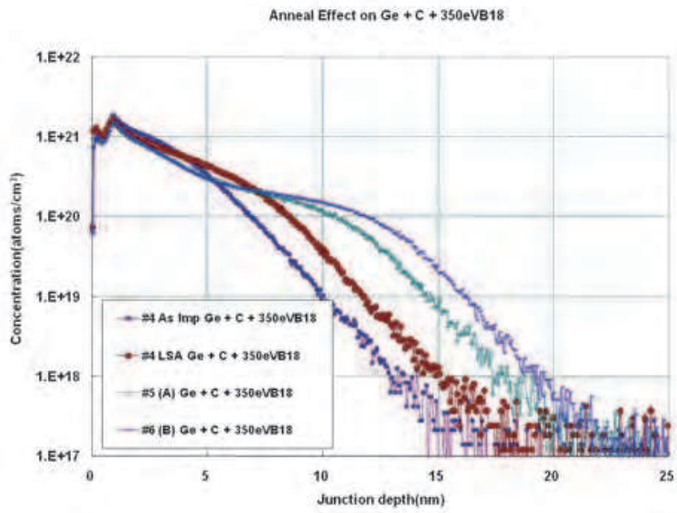

Fig. 22. The 350eV boron post anneal dopant profile of different annealing schemes. LSA is a millisecond laser anneal. Anneal "A" is a <1000°C spike RTP followed by a millisecond anneal; and anneal "B" is a >1000°C spike RTP followed by a millisecond anneal.

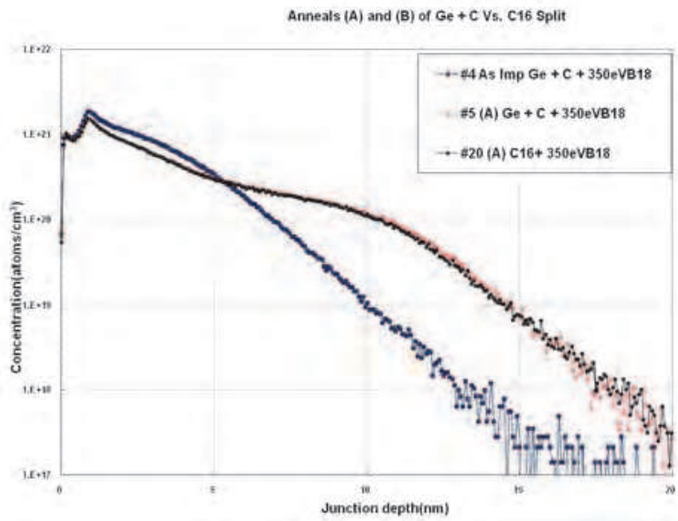

Fig. 23. The 350eV boron post anneal dopant profile of different annealing schemes, and of the Ge-PAI plus mono-atomic carbon 2-step co-implant versus the $C_{16}H_{10}$ co-implant.

Figure 24 shows the overlap capacitance of $C_{16}H_{10}$ plus $B_{18}H_{22}$ implanting into the SDE region of a 40nm logic device. In comparison to the POR implant matrix shown on the left side, $B_{18}H_{22}$ direct replacement of BF_2 as the boron dopant in the POR appears to have a much higher C_{ov}. This indicates that $B_{18}H_{22}$ diffuses faster than BF_2 in the RTP plus LSA annealing scheme. The main reason should be due to the presence of fluorine in the BF_2 implant, which also plays a role in boron TED suppression. However, if the $C_{16}H_{10}$ implant is employed instead of the conventional co-implants, the C_{ov} is restored. In short, molecular implants can at least be shown to have process equivalency even if the annealing scheme is not in favor of molecular implants. On the other hand, $C_{16}H_{10}$ has been shown as a valid

replacement for current POR co-implants for PMOS SDE. It not only can be easily integrated into the existing process nodes for Ge-PAI replacement, but also allows a smooth transition to a smaller thermal-budget or diffusionless annealing scheme in the future.

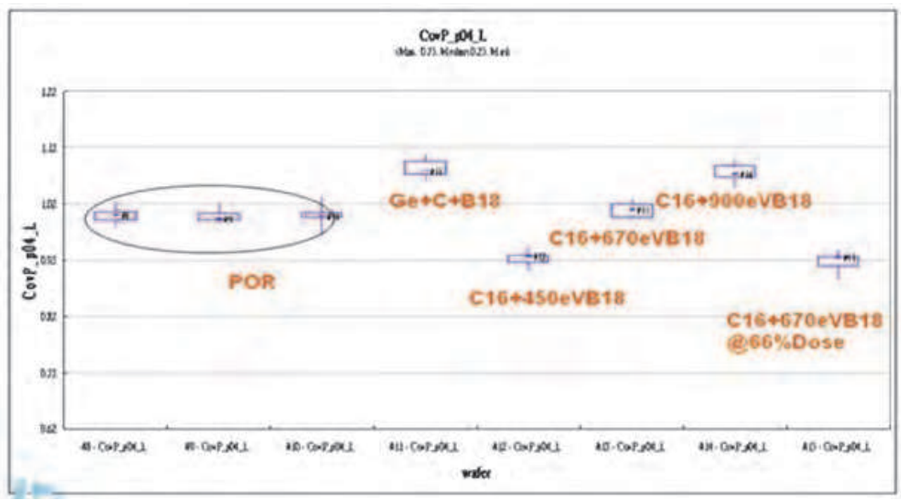

Fig. 24. Overlap capacitance of $C_{16}H_{10}$ plus $B_{18}H_{22}$. implanting into the SDE region of a 40nm logic device, where the POR is mono-atomic Ge-PAI plus C, followed by a BF2 SDE implant.

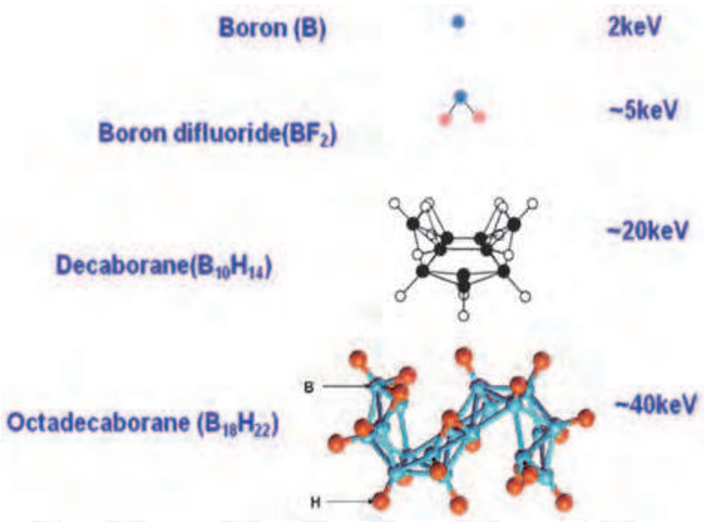

Fig. 25. The 2keV equivalent boron energy beams of BF_2, $B_{10}H_{14}$, and $B_{18}H_{22}$, could be extracted from the source and travel in the ion implanter beam line at an energy of 5keV, 20keV and ~40keV respectively.

6. Conclusion

Owing to the advent of High Mass Molecular implant technology, semiconductor manufacturing fabs now have an opportunity to leap forward in making great productivity and process improvement by utilizing its unique properties of effective beam transportation in the ion implanter beam line, and self-amorphization during process. The amorphous layer could be formed at a relatively lower dose for the HMM implant to avoid the side effects of

excessive implant damage. By proper tuning the molecular carbon implant, we can show process equivalency to conventional co-implant scheme, and utilize it for the 40nm p-MOSFET device. Should the annealing scheme be flexible, and the carbon implant only sees the LSA as the post-implant anneal, the adverse effects of carbon implant, such as its competition against boron dopant for activation, etc, can be nullified. Figure 25 shows the industrial trend in the past 40 years for choosing the primary p-type dopant. This trend is in response to the demand for low energy boron implant. Fortunately, people always find a production worthy solution when the request becomes imminent. Even though using BF_3 as the source material is problematic, the industrial people are still clinging to it due to the benefit of higher productivity than monatomic boron for low energy operation. It is authors' believe that as long as Moore's law still holds, both productivity and process issues will compel fab engineers to migrate to the next generation of p-type dopants. It would be only natural for such evolution to take place. Just as sometimes in the past, we migrated from monatomic boron to small molecular BF_2. This time we are just going from BF_2, the smaller molecule to $B_{10}H_{14}$ or $B_{18}H_{22}$, bigger molecules. For the last transition, the productivity improvement was noticeable, but not awesome, due to either boron or BF_2, only has one dopant atom in it. But for this transition, the productivity would get improved from ten to twenty times, due to the HMM $B_{10}H_{14}$ or $B_{18}H_{22}$ ions contain that many more dopant atoms. This would be more than just an evolutionary change. It is so significant a leap for the ion implantation technology so that it should to be deemed as a revolutionary change for the silicon manufacturers to make.

7. Acknowledgment

The author would like to thank Hans Cheng of TSMC, Phoenix Kuo of UMC, and Jay Huang of Rexchip for their many years of collaboration with us in the field of HMM ion implantation for DRAM and advanced logic device manufacturing. Most of all, I would like to extend my appreciation to P.S. Chen and S.H. Yang of NTC, who actually adopted $B_{18}H_{22}$ ion implantation in their 70nm DRAM production for the P+ poly implant process.

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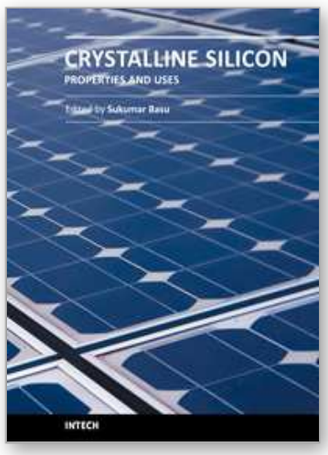

Crystalline Silicon - Properties and Uses

Edited by Prof. Sukumar Basu

ISBN 978-953-307-587-7
Hard cover, 344 pages
Publisher InTech
Published online 27, July, 2011
Published in print edition July, 2011

The exciting world of crystalline silicon is the source of the spectacular advancement of discrete electronic devices and solar cells. The exploitation of ever changing properties of crystalline silicon with dimensional transformation may indicate more innovative silicon based technologies in near future. For example, the discovery of nanocrystalline silicon has largely overcome the obstacles of using silicon as optoelectronic material. The further research and development is necessary to find out the treasures hidden within this material. The book presents different forms of silicon material, their preparation and properties. The modern techniques to study the surface and interface defect states, dislocations, and so on, in different crystalline forms have been highlighted in this book. This book presents basic and applied aspects of different crystalline forms of silicon in wide range of information from materials to devices.

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

Bill Chang and Michael Ameen (2011). High Mass Molecular Ion Implantation for Advanced Logic and Memory Devices Manufacturing, Crystalline Silicon - Properties and Uses, Prof. Sukumar Basu (Ed.), ISBN: 978-953-307-587-7, InTech, Available from: http://www.intechopen.com/books/crystalline-silicon-properties-and-uses/high-mass-molecular-ion-implantation-for-advanced-logic-and-memory-devices-manufacturing

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