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Implementation-Aware System-Level Simulations for IR-UWB Receivers: Approach and Design Methodology

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1. Introduction

Impulse-Radio Ultra-Wide Band technology (IR-UWB) allocates very large bandwidth with short duration pulses. Interest for research started in 2002 when Federal Communication Commission (FCC) normed the power spectral densities allowed for unintentional and unlicensed UWB radiators in the pre-existing full communication band 0-10 GHz FCC (2002). An ultra-wide band pulse has some unique features compared to conventional wireless signals. If on the one hand, narrowband signals envelope is close to a time unlimited continuous function, on the other hand, in a possible conception pulses can be perfect duty cycled tones having limited time support. Pulses with very short duration occupy very large bandwidth and this is in contrast to the narrowband approach, that subdivides the available spectrum into small slices for efficiently allocating radiated power. IR-UWB is then very interesting because it poses these kinds of challenges, i.e. the use of pulses and the coexistence with the existing RF systems.

The use of short duration pulses implies a physical limitation which normally narrowband RF systems are excluded from. These are multipaths, that is reflections from the objects localized in the operating environment. This has conditioned the use of IR-UWB for very high data rates applications because notwithstanding the very large theoretical channel capacity, a very high data rate communication is now almost infeasible with low complexity electronics tackling multipath diversity. IR-UWB has then been proposed for short/medium range Ultra-Low Power (ULP) communication Wireless Sensor Networks (WSN) Bielefeld et al. (2009); IEE (2007); Lecointre et al. (2010); Stoica et al. (2005); Verhelst & Dehaene (2008); Wang et al. (2011). At the transmitters very low average consumed power is possible with aggressive duty cycling, as well as in receivers even if with lower efficiency. Transmitters radiate dBm-order power signals in just 1-3 ns and receivers typically demodulate and synchronize data by detecting the presence of the UWB pulses with time domain computations.

One important key-word for understanding how IR-UWB will possibly impact on new ULP applications is "system-level". The validation of a receiver or a transmitter architecture being aware of the impact of blocks physical implementation prior to full low-level

design can possibly lead to significant performance increase and help lower complexity. Based on these considerations, this book chapter shows a methodology used for IR-UWB receivers simulation, design and conceptualization. A multi-level approach is presented and contextualized with an implementation example, that is an energy detection receiver. This design methodology has been already presented in Crepaldi et al. (2007) and extensively used in Casu et al. (2008). In this book chapter we expand it and provide more comments and considerations based on successive works dealing with IR-UWB system-level design.
Section 2 considers an Energy Detection receiver as a case study and section 3 introduces the design methodology after emphasizing its requirements. Later, section 4 applies the methodology to a specific block of the receiver and section 5 shows the obtained simulation results. Section 6 concludes the chapter.

2. A case study: the Energy Detection receiver

IR-UWB Energy Detection receivers represented mostly the number one choice for WSN and have been widely integrated and researched starting the second half of 2000-2010 decade Crepaldi et al. (2010); Daly et al. (2009); Lee & Chandrakasan (2007). Energy detection receivers are robust and of easy implementation notwithstanding being non-coherent, therefore sub-optimal. In the beginning, research was focused on conceptualized architectures that studied the communication performance of IR-UWB and attempted to solve some system-level issues. An example for non-coherent M-PPM receivers is given in Carbonelli & Mengali (2006). The proposed architectures did not deeply account for circuit-level implementation details. Starting from this first conceptualization mechanism, first energy detection receivers have been proposed Stoica et al. (2005), Lee & Chandrakasan (2007). By then all the required system-level performance figures were validated on silicon for the first time. This, and the successive receivers proposed by then, aimed towards lower energy consumption or to increase performance of some of these reference points. In this book chapter we refer to a somewhat old energy detection receiver scheme, in which an Analog-to-Digital Converter (ADC) is used for data demodulation as well the use of other blocks that differ compared to recent implementations. Here, we explicitly utilize this scheme because it represents a case study, and still, valid ideas can emerge from the analysis of this system from cross-sectional views.
A standard energy detection receiver block scheme is depicted in fig. 1. The complete transceiver is assumed to be fully implemented as a silicon System-on-Chip (SoC) and at this stage the transmitter is assumed to be only behaviorally modeled. The antenna switch commutates the wideband antenna to receiver and transmitter ends, while an external Band-Pass Filter (BPF) ensures that on-chip generated UWB pulses satisfy the FCC mask and, at the same time, filters out-of-band interference from the received ones. The energy detector, depicted in the *front-end* part is composed of a linear amplification block, the Low-Noise Amplifier (LNA), Variable Gain Amplifiers (VGA) a squaring unit and an Integrate&Dump (I&D). The receiver computes the raw pulse energy. By assuming that integration generically starts at t_a and ends at t_b, $Ar(t)$ is signal at the output of the VGA, where A is the gain of the previous blocks, the energy E at the output of the I&D is,

$$E = \int_{t_a}^{t_b} A^2 r(t)^2 dt \tag{1}$$

To run both synchronization and demodulation the receiver circuitry operates on t_a and t_b to detect for example the maximum energy peak and, for 2-PPM receivers, activate

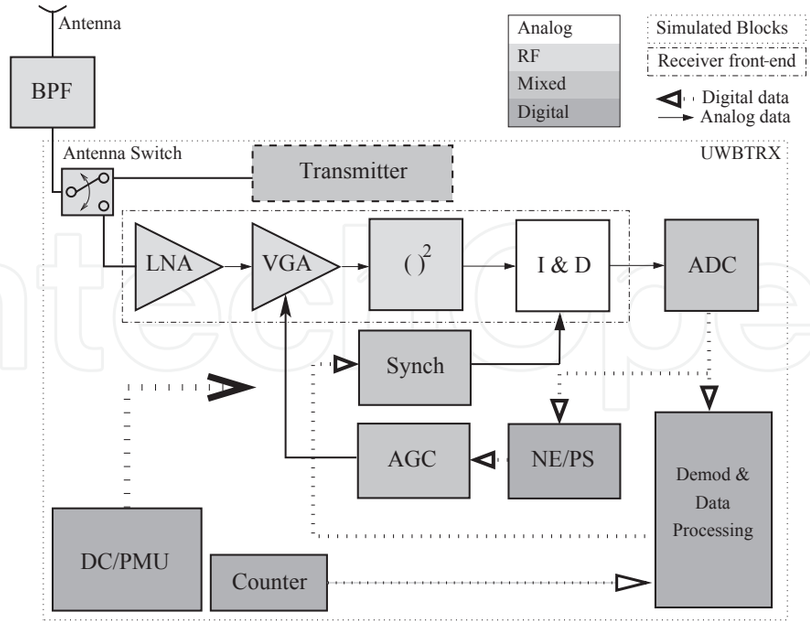

Fig. 1. Energy Detection transceiver block scheme Crepaldi et al. (2007).

integration once pulses timing is acquired at the correct '1' or '0' bins. For gain control the receiver operates on parameter A with an digital-to-analog feedback from the demodulation chain. After energy is calculated it is quantized with an ADC and then processed by the back-end that can implement a threshold based demodulation algorithm for OOK, or a relative comparison as in the case of 2-PPM. Here the receiver operates with 2-PPM modulation. The Data processing block controls also the synchronization unit, that operates similarly to a Delay-Locked-Loop (DLL) for searching the maximum energy peak within a known preamble. The Automatic Gain Control unit (AGC) automatically sets the front-end gain based on the digitized energy. The NE/PS block, namely Noise Estimation&Preamble Sensing block, helps detecting the presence of a preamble once the receiver is activated and collects energy samples from channel when no pulse is transmitted. This helps assessing the clearance of channel as soon as receiver is activated, therefore allowing system shutdown in case no packet is received. Data saved by this digital block is used for adjusting the gain of the receiver front-end for allowing the input range adaptation of the input signal for I&D and consequent A/D conversion. Note that here, receiver sensitivity is defined by the LNA, that shall have the highest gain and the lowest noise figure. The noise figure of the successive VGA units is not as influent as for the first stage because input-referred noise figure is calculated by propagating each amplifier noise figure with Friis formula. Notwithstanding this, the receiver must provide enough amplification to process the UWB pulses, overcome the non-linear law of the squaring unit and the channel path-loss that highly depends on the objects distributed in space. The Counter in the high-level architecture is useful UWB pulses Time-of-Flight calculation, in this case with a Two-Way-Ranging (TWR) packet exchange (defined in section 5). The Duty Cycling/Power Management Unit (DC/PMU) implements receiver duty cycling and deactivates the front-end units to save energy when the receiver is idle. The full implementation of this block requires the definition of the complete packet exchange mechanism as well as detailed information on each single block of the receiver.

Therefore, the complete development of the DC/PMU must be faced at the end of the design but it shall not be considered less important than the others.
It is worth mentioning that our methodological approach is devoted to system-level implications rather than being focused on circuit-level challenges. As recent research shows, we believe that one of the next steps for PHY IR-UWB systems research has to regard both decreasing energy consumption and solving problems from a more general and wide-sense system-level view Gorlatova et al. (2010).

3. The substitute-and-play design methodology

3.1 Simulator and target system

The methodology outlined here is applied on a specific simulation tool called ADVanceMS (ADMS, Mentor Graphics, now Questa ADMS) that allows multi-language descriptions with multi-resolution simulations. It supports VHDL-AMS, Verilog-AMS, VHDL, Verilog, SystemVerilog, SPICE[1] and SystemC in the same simulation environment. The Very High Speed integrated circuit Hardware Description Language (VHDL), similarly to Verilog, is widely used to logically and behaviorally describe digital circuits, modular by construction and based on a very simple math. VHDL is a concurrent language in which every described process works in parallel with the others. Communication among processes is based on events. Before evolving to the next time step, the simulator engine processes a single list in which all process events are queued. While this task is accomplished simulation time is frozen. The VHDL-AMS (AMS is for Analog and Mixed-Signal extensions) language is an extension of the common VHDL IEEE (2007) and adds directives and constructs to support at the same time both digital concurrent and simultaneous statements. These last ones, are used to allow the implementation of the continuous-time nature of analog systems. Continuous-time simulations are not based on events, but on the computation of quantities representing the solution of a continuous mathematical model. In a mixed-signal simulation the inter-communication between these two totally different worlds is ensured by the software tool that handles the different VHDL constructs depending on the cases and interfaces them to a simulation kernel, for example SystemC.
With the same continuous-time granularity the tool can include SPICE-level netlists in the description. Netlists can be directly interfaced to VHDL-AMS, therefore a block can painlessly jump from a behavioral world to the voltage and current domain of silicon devices. Also, other commercial tools such as Cadence IC provide multi-level and multi-resolution descriptions but still they are based on an analog point of view, referring to the system-level use of circuit blocks instead of exploiting the flexibility of a digital description language formalism. Another example is Advanced Design System (ADS, Agilent) that enriches its system-level design flow with low-level electro magnetic simulations. All these tools are frameworks meant to bridge multiple description languages and simulation tools transparently to the user. Here, with this methodology, we believe that that the use of a single and homogenous formalism, with possibly a single simulator, can make the difference.
The evaluation of system-level performance of an IR-UWB system in time-domain is important. As an example, let us consider Duty Cycling (DC). Ideally an IR-UWB receiver has to be kept operating for time durations on the order of few nanoseconds sufficient for receiving pulses from channel and be shut-down for the remaining time to save power

[1] In the following paragraphs we will refer to SPICE descriptions by referring to the name of the Mentor Graphics simulator, ELDO.

consumption. Typically RF front-ends have resonant loads therefore, depending on the implementation, spurious pulses can be erroneously generated whenever a hard digital activation signal operating on active amplification elements is toggled. If the RF amplifiers are simulated only in AC and integrated without a time-domain verification, at the measurements time the system performance can be seriously compromised or even the receiver cannot operate because the successive baseband and backend units are saturated. Therefore, in this methodology we stressed out the time-domain aspect of simulations and to save runtime used the multi-resolution feature to activate only the most important non-ideality required for obtaining figures as much close as possible to the physical verification. Unfortunately running time-domain simulations requires the full large signal expressions of transistors, if simulation includes circuit level blocks, or to solve differential equations whether a high-level behavioral model is conceived. The multi-resolution aspect is then fundamental for obtaining results in a reasonable time because system-level figures of IR-UWB receivers are based on iterative statistical analyses.

Implementation-aware actions on IR-UWB transceivers design require the identification of performance figures that depend on system-level constraints. The most common figures are typically related to Bit-Error-Rate (BER), for communication purposes and, in the case of IR-UWB for ranging applications, to the estimation of the Time-of-Flight (ToF). The UWB channel is statistical, therefore determining these system-level data implies randomizing different multipath realizations according to a specific operating environment, i.e. indoor office, residential, industrial, outdoor, open outdoor, and for Line-Of-Sight (LOS) or Non Line-Of-Sight (NLOS) links IEE (2004). Also, the computation of ToF with TWR schemes requires the modeling of a complete packet transmission mechanism without ideal synchronization. In communications, for bit error-rate tests large random data needs to be tested. Take for example a 10^{-6} BER: theoretically to obtain this single error-rate point at least 100 points are required for high confidence and this implies randomizing an average of 10^8 pulses. Note that from a pure communication point of view all these functionalities can be easily implemented with any high-level modeling language e.g. Matlab but this lacks of flexibility because top-down refinement of heterogeneous blocks is typically not possible. The use of a multi-description modeling tool permits an easy “context switching” between a high-level model to a circuit-level or SPICE post-layout netlists without having to interface the description. This flexibility is not relative only to the simulation tool itself but to the description language and in particular to the use of an homogeneous interface between descriptions. Let us consider an Integrate & Dump unit. Basically, the block shall have an input, an output and an integrate/dump control. Alternatively, if description is at a very high abstraction level control signal can be potentially undefined. These terminals not necessarily convey voltage or current but instead can be, if present, symbolic that only in a successive step are mapped onto a physical counterpart. The use of a priori homogeneous interfacing between different descriptions avoids burdensome conversion times and can be useful for defining electrical interconnections from early design stages.

System-level simulations aiming towards physical implementation predictions, must be enriched with many circuit-level non-ideality concerning silicon integration. Electro-Static Discharge (ESD) protection circuits, bondwire for die soldering on packages and inductive or capacitive parasitic couplings are few of the possible non-ideal effects. These, however, concern circuit-level design and at first design concept phases these can be disregarded, therefore assuming that chip-level integration countermeasures can efficiently tackle them in a next step. For example, if a cascoded tuned amplifier LNA requires a very well controlled

to-ground parasitic inductance then this aspect has to be tackled at die-level floorplanning when the number of PAD is decided, therefore at circuit-level design steps. Instead, if the boundary conditions among two or more functional units represents a critical point, this shall be included in system level models. Also, the same parasitic can play different roles if shared among other circuit blocks. For example, if parasitic inductance influences much the operation of a block, for example an UWB coherent correlator, then this shall be included in the system-level model. From this analysis we conclude that the definition of the parameters required in simulation is fundamental.

Non-ideality can depend on many different factors but a flexible high-level simulation requires that they can be effectively modeled as generic parameters. For example, based on circuit-level details, the squarer unit in energy detection receivers, if not differential, can originate additionally to the $()^2$ term a linear by-product that depends on input signal level Han & Sanchez-Sinencio (1998). A high-level parametric behavioral modeling requires the implementation of a mathematical relationship that covers, in the most general conception and with sufficient confidence, the behavior of the circuit-level unit in all the operating conditions. In a high-level methodology this is particularly important because system level simulations are not meant to be a mere verification but instead shall represent a starting point for deriving useful design constraints. The inclusion of circuit-level descriptions at system-level with a uniform and flexbile language serves as inspection and analysis. Successive chip-level integration can be then easily derived by painlessly placing and routing all the blocks at their lowest layout description level.

3.2 Methodological assumptions

Based on the previous analysis, a design methodology for electronics systems shall be referred to at least three important respects: *uniformity*, *partitioning* and *refinement*. Uniformity can be read as the requirement of having an homogeneous formalism to describe the operation of a system. Partitioning can be read as the effort a designer makes for physically mapping the conceptual operation of a system according to very well defined rules. Refinement can be read as the enrichment of physical non-ideality applied to a pure mathematical model to more precisely describe physical behavior. Take for example digital design. Hardware description language as VHDL or Verilog are uniform, because they are completely portable and allow an homogeneous description of a block. The languages permit both gate-level and behavioral-level descriptions at the same time. The logic conception of digital circuits inherently permits a partitioning, that is the identification of input and output signals. Refinement is also possible because, provided that a block has the same inputs and outputs, its description can pass from behavioral to structural, therefore getting closer to single logic gates.

With circuit-level design we have very different aspects. The basic building blocks are not logic gates but devices with a particular electrical interface. In digital domain interface comprises purely logical inputs outputs while here the same input and output terminals are enriched with continuous power by voltage and current. Parasitic are very important in RF design and the well defined input/output paradigm valid for digital circuits is compromised. In the above reading key, couplings between two near blocks on the same silicon chip can generate other inputs and outputs, even if their physical counterpart is a fF order capacitance, a pH order coupling inductance or a GΩ resistor. An RF amplifier having a single input or output, after layout can have more physical interconnections with other blocks that share the same die. In this digital-like input/output key, the effect of parasitic can be also modeled

impacting on a given electrical signal, i.e. bandwidth or gain decrease without having to map it as an additional input or output. While the modeling of parasitic effects can be more systematic in digital design (consider for example delay of logic gates), in the analog world this is more complex because it depends on physical design. Filling the modeling gap between analog and digital worlds with a uniform methodology can be possibly obtained by using a description language that forces the same partitioning as in digital domain and at the same time has enough flexibility for being used in the digital simulation domain. Description is not the only aspect that shall be considered. Attention regards also the simulator itself and therefore its inherent capability of accepting hardware described with different languages. Therefore, the design methodology presented here refers to a simulator with which multiple description languages with a uniform formalism are contemplated. Fig. 2 schematizes the interactions between simulation and hardware worlds.

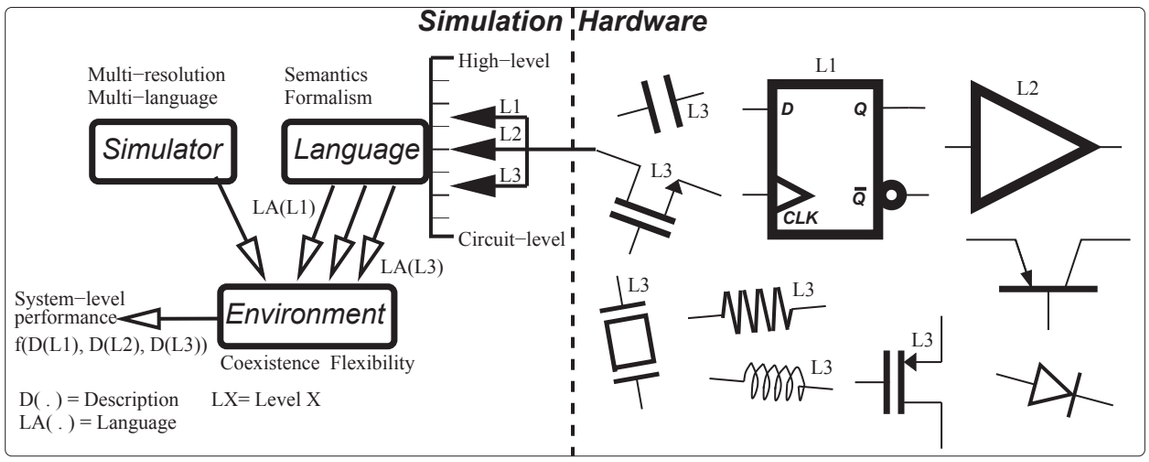

Fig. 2. Simulator and language in a multi-level description.

3.3 Design methodology

The design methodology outlined in this work is organized in four phases. During Phase-I the receiver, or generally the IR-UWB system is behaviorally defined and a first high-level model is generated. This phase is known as *conception*. In the case of our Energy Detection receiver front-end this implies behaviorally modeling e.g. LNA, squaring unit, Integrate and Dump and the Analog-to-Digital Converter (ADC). Note that in the example of figure 3 the front-end is shown but the methodology can be applied to complete systems, even including a dedicated backend for bit and symbol synchronization and demodulation, because VHDL and VHDL-AMS lie on the same domain. At this abstraction level, the description still recalls the formalism of a high-level modeling language e.g. Matlab since an electrical interface is not defined yet and the complete system is packed onto few VHDL-AMS process disregarding the complexity its implementation may imply. Figure 3 (Phase I) shows a single Entity-Architecture (E&A) couple comprising a complete energy detection receiver front-end. At this point, the model is validated by checking consistency with high-level models developed in Matlab or in other high-level languages applied on the system-level figures previously mentioned. Here, from the engineering point of view, the main effort consists of defining the system operation without forcing a design partition that is mandatory towards physical-level implementations.

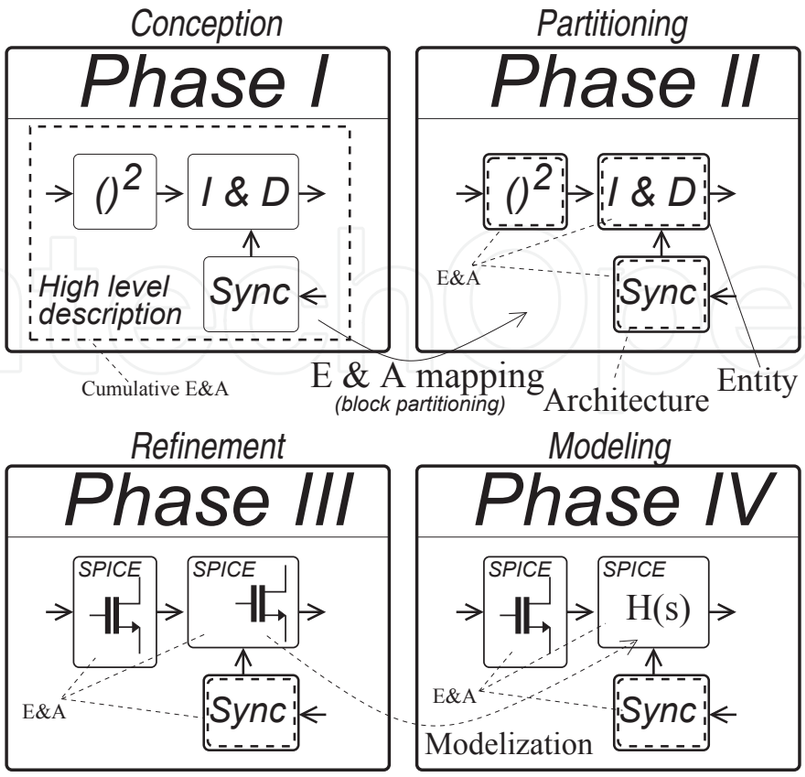

Fig. 3. Design methodology organized in 4 phases.

In Phase-II a first electrical signal definition is forced. We call this very important phase *partitioning*. This implies rearranging the description developed during Phase-I in separate E&A. Here we simply apply the modularity of the VHDL-AMS language on the design to get closer to silicon implementation. Once electrical signals are defined, successive refinement phases applied on a single block are painless provided that electrical interface is the same. Partitioning is the key for efficiently conceiving the system and the later adjustment of system partitioning can be problematic. Here, considering the importance of this phase, no non-ideality are included or modeled in the simulation. The inclusion of non-ideal effects in fact, recalls low-level implementations or, alternatively system-level parameters known to severely impact on system-level performance. The development of a new system, intended not being reported in the state of the art, implies only the partial knowledge of the exact non-ideality that may compromise performance.

The ADC quantization, the AGC look-up table as well as a DAC for AGC gain analog conversion can be all included in this phase not being properly non-ideal effects, rather fundamental circuit features included in normal operation. Bandwidth, saturation and blocks power consumption are not defined at this phase. System partitioning, i.e. electrical interconnection definition, requires the knowledge of lower circuit level constraints. Since the design is simply "rewritten", therefore differently described with the same simulation tool, the result must not change from Phase-I, but consistency with the previous phase needs to be checked. Note that in Phase-II signal electrical partitioning is possible but it is not strictly necessary, while formally only the E&A rearrangement of the conceptual operation is required. Whether this first partitioning does not comprise electrical-level terminals, it can be done in the next phase for each unit by refining each entity declaration.

Once system partitioning is complete, the electrical interface of all the blocks in the IR-UWB system are defined. We are now ready to increase the details in each block. For this reason, Phase-III is called also *refinement*. With refinement, signals partitioned in Phase-II assume a circuit-level meaning. Every important circuit-level non-ideality is modeled according to continuous time or digital statements and included in the architecture. The importance of this phase regards the identification of the non-ideal effects that impact on system-level performance, or, if the system leads the state-of-the-art, even on its basic operation. Efforts in the definition of the number of non-ideality of their description is an important trade-off because very accurate models can severely impact on simulation runtime or excessive efforts on this side can waste time and compromise the overall system-level performance inspection. For energy detection receivers for example, modeling of compression in the front-end is important e.g. for understanding the impact on interference rejection, but still, since the system computes the raw energy of the UWB pulses with a squarer, this is not extremely important. Dedicating weeks of research time on this would avoid taking important decisions next or would block the project at its beginning, while other problems may rise during circuit-level design or chip-level integration.

Phase-III is not only related to the inclusion of non-ideality to the previously idealized blocks. Provided that an homogenous electrical interface derived from Phase-II in the entity declaration of every VHDL-AMS unit is given the complete VHDL architecture can be switched. This enables the replacement of the full VHDL-AMS modeling with transistor-level SPICE models extracted from Cadence Front-end to Back-end or IC Station (Mentor Graphics) other front-end circuit design tools. The description can be also extracted from layout. This Substitute-and-Play (S&P) philosophy allows the identification of the impact of blocks refinement on system-level performance figures. This is very important because it permits architectural analyses by intelligently exploring all the possibilities without focusing on a single abstraction level. Here, a heterogeneous multi-level description can help understanding faster the problems that may arise when solid-state circuits are tested. Provided that refinement is intelligently run, performance e.g. on ranging, demodulation, synchronization, transceiver packet exchange, power consumption, can be forecasted and decision taken whether constraints are not met.

IR-UWB demands time-domain simulations and a complete refined system, even if not for all its blocks, can require very high runtimes especially when statistical tests are executed. Notwithstanding the computational power of workstation and servers keeps increasing as well as code parallelism in software, due to the short duration pulses high simulation accuracy is required and a complete 10 or 100 s packet exchange simulation can require days or even more. This applies also e.g. for PLL, where full SPICE level time-domain simulations are impractical (and in this context also inaccurate) Lai et al. (2005). Moreover, it can result that the effect of some circuit-level blocks severally impacts on system-level performance but cannot be neglected in the description. Therefore, we define a successive Phase-IV, called *modeling* or back-annotation, that aims at the inclusion of the relevant circuit-level non-ideality extracted from the transistor-level description of Phase-III. This can be accomplished in two different ways. The already modeled parameters are refined based on pure circuit level simulation, or, if the non-ideality discovered during Phase-III was not included previously the architecture is redesigned by keeping the same entity definition. The refined models can be used in Phase-III for running again simulations and obtaining further results.

The full design methodology is applied on the I&D unit of our Energy Detection receiver case study as an example. Next paragraph will focus on the design of the block and all

the hypothesis used for its conceptualization will be explained and identified in the outlined methodological key.

4. S&P contextualization: The I&D block design

Fig. 4 shows also the partitioned entity of the I&D and the entity declaration structure. At the highest abstraction level, the I&D electrical boundary is not defined and simply implements the math function $\int x(t)dt$, where $x(t)$ is input signal. $x(t)$ has not a physical counterpart nor it is single-ended or differential and integration output is a quantity that is neither voltage nor a current. A control signal is implicitly defined among the other high-level statements that control the computation of the formula. This integrator has been included in the high-level model and a first consistency check with a Matlab model has been completed. When description enters Phase-II, some circuit level properties must be considered. These are mainly related to 1) power supply, 2) control signals, 3) input and output electrical features (single-ended or differential, AC or DC coupled, current or voltage). By satisfying these constraints, valid for this specific case, the electrical interconnection boundary can be defined. The I&D is a pure analog unit, that has to cope with relatively high frequency signals[2]. Therefore, this block is not critical from the RF point of view and a single power supply and ground connection pin can be considered. Notwithstanding this, the block is critical at system-level. In the case of the LNA for example, having multiple power supplies can help reducing inductance parasitic and, depending on circuit-level design, it can be fundamental for matching. Therefore, modeling multiple power supply pins can be useful even at this abstraction level, and the problems that may arise can be directly tackled here rather than successively, when the floor plan is defined and circuit blocks placed down. A very first constraint we had in the design on the energy detection receiver was that it had to be fully differential, therefore fully differential input and outputs were assumed, in fig. 4 the couples `Inp`-`Inm` and `Out_intp`-`Out_intm`, in particular DC coupled voltage signals. For integration control signals the discussion is more complex because the use of a single ended or a differential signal (one, vs. two terminals) depends on the internal implementation of the unit. Homogeneously, we assume also perfectly differential voltage signals `Controlp`-`Controlm`. In this very first implementation we assume that integrator is the gm-C structure depicted in fig. 4. The transconductor transforms the input voltage into differential current and charges a load capacitor C. When control signal `Controlp`-`Controlm` is active integration is run, while when it toggles to '0' integration is reset. The biasing circuit is connected to V_{bias1}, V_{bias2} and to V_{bias3}, it consists of two self-biasing stages that generate the required voltages for both transconductor and Common Mode Feedback Network (CMFB), not shown here for sake of brevity. According to the state-of-the-art simpler integrator structures are possible and they can be single ended and much simpler than those depicted here Lee & Chandrakasan (2007). At this point, the target was the replacement of a BiCMOS integrator by then used in a first implementation Stoica et al. (2005) with a lower cost CMOS integrator. Note that at this point the I&D architecture boundary has been fully defined. From an electrical point of view this enables the VHDL architecture switching among different Phase-III domain models. For example, a VHDL-AMS behavioral model, with the given electrical interface can be painlessly substituted with the equivalent circuit-level or layout-description.

[2] Note that after squaring, the useful portion of the spectrum of a UWB signal of bandwidth B is at baseband, $[0, B/2]$, e.g. for a standard UWB pulse having a 500 MHz bandwidth, this corresponds to operating in the band 0-250 MHz.

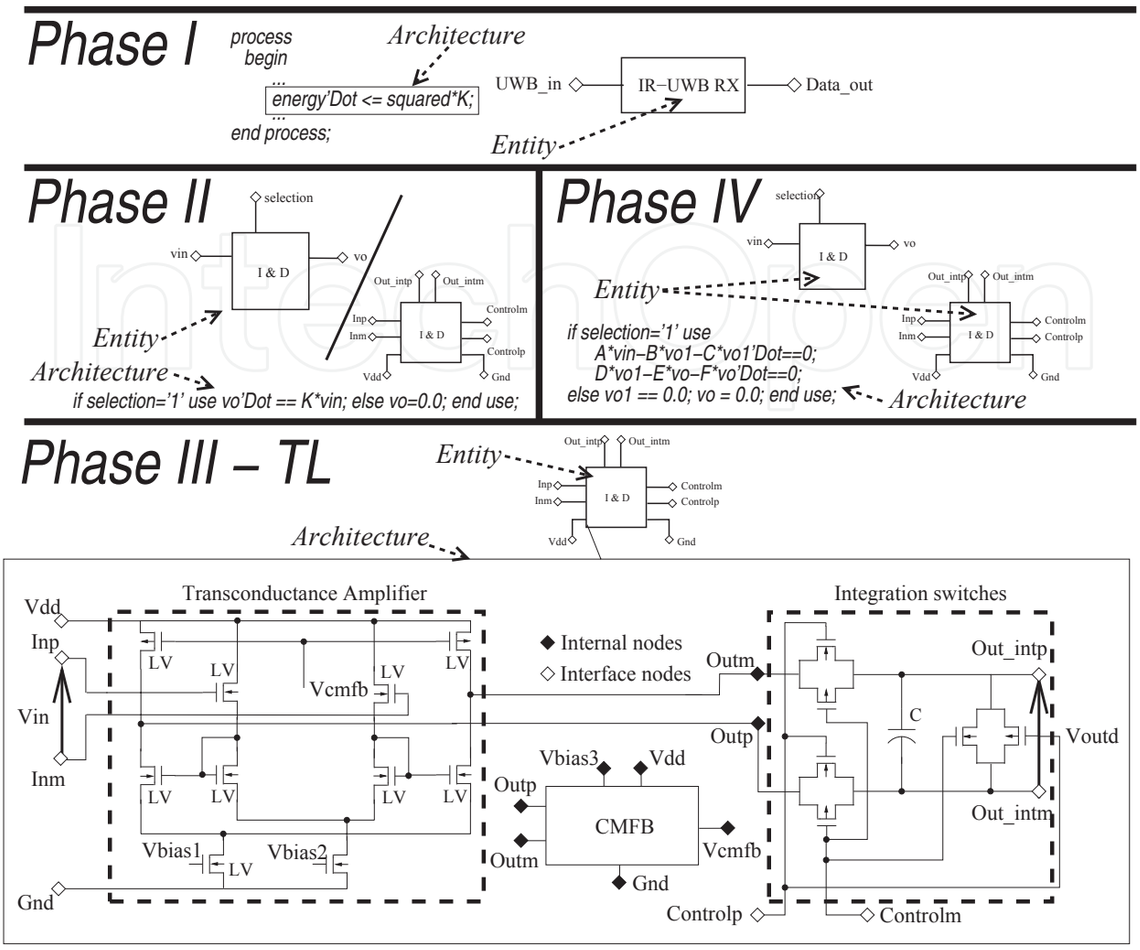

Fig. 4. I&D circuit at the circuit-level design and partitioning level.

With circuit-level simulation the AC behavior of the I&D can be easily extracted. This is reported here on fig. 5 from Crepaldi et al. (2007). The integrator operates from 1 MHz to 1 GHz, has an additional low-pass transfer function, and not ideally infinite DC gain. The second pole at high frequency is due to parasitics of the devices. Note that the useful part of the UWB signal is concentrated from 0 to 250 MHz for a 500 MHz pulse and the behavior of the integrator at very high frequency is not fundamental. The non-infinite DC gain is a loss therefore limiting the maximum length of the integration window. At this point, this AC model can be included in the Phase-III VHDL-AMS models to speed up simulation time. Note that by including the AC model only non-linearities and saturation of the transconductor are not accounted for. This is a clear example of the mandatory requirement of Phase-IV, that is an intelligent inclusion of the relevant non-ideality derived from transistor-level design. In the case the required system-level simulation explicitly requires accounting for this non-ideal effect, then, the backannotation shall be enriched, or alternatively the full circuit shall be included and other blocks non-ideality deactivated to speed-up simulation time. Before applying the substitute-and-play approach, consistency with ideal (Phase-II) and VHDL-AMS models has been checked. As shown in fig. 5, the backannotated model and the AC circuit simulation of Phase-III match.

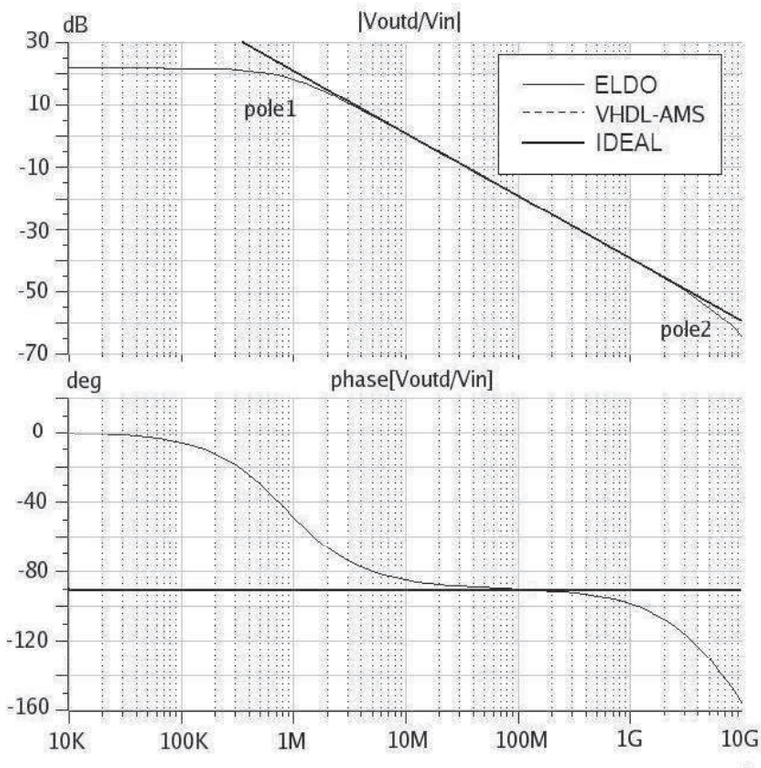

Fig. 5. AC response of the I&D circuit and Phase-II and III models Crepaldi et al. (2007). The IDEAL and VHDL-AMS models overlap.

The connection of transistor level descriptions with ideal blocks can require specific considerations, not only related to the modeling language itself but on the electrical features resulting from blocks interfacing. Take for example a fully ideal Phase-II model of the squarer. A possible VHDL-AMS description can include only the simultaneous statement `vsquare==K*vin**2.0;`, where `square` and `vin` are across quantities defined on two couples of differential terminals. If this is the case, then input and output impedance of the squarer is completely disregarded. If the squarer modeled according to this simple statement is connected to the I&D the resulting integration voltage would be compromised because common mode voltage is disregarded. Therefore, in such cases the inclusion of a boundary element is fundamental for brigding the ideal world to a full custom electrical interface. These boundary elements are inherently included in the surroundings units. In this work, proper boundary elements, operating on the DC level of `vin` have been included.
Fig.6 shows a transient simulation of the integrators during three different modeling phases II, III and IV. Notwithstanding a gain mismatch output is still energy, that is the integral of the squared signal.

5. System-level simulations and results

One very interesting feature of Impulse-Radio UWB regards the possibility of determining the pulses time of flight, that is, the distance between two transceivers. Since UWB pulses are very short, the accuracy with which distance can be estimated can be very high. For example, recent receivers are designed with fine synchronization circuits reaching accuracies of few

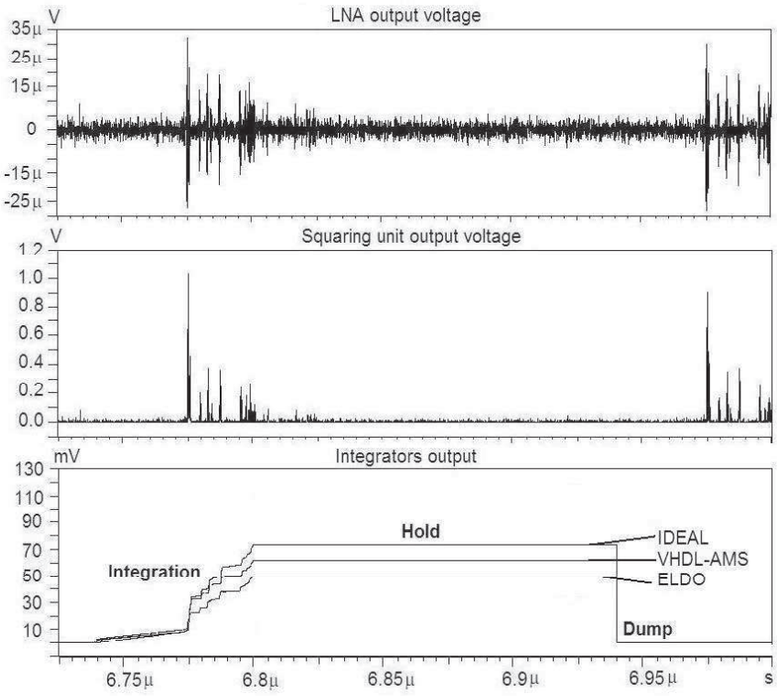

Fig. 6. Transient response of the I&D circuits obtained from different modeling phases Crepaldi et al. (2007).

millimeters Chu et al. (2011). Pulse radio was thought also to serve localization purposes even in space applications Ni et al. (2010). IR-UWB can be easily applied to biomedical devices because pulses are reflected differently depending on dielectric properties mismatches among different mediums. This enables applications in Breast Cancer Detection and wireless biometric parameters sensing. Here, we applied the methodology to Bit-Error-Rate tests for wireless link quality inspection, and to Two-Way-Ranging related to ToF estimation performance.

Figure 7 shows a graphical representation of the effect of the I&D substitution on our energy detection IR-UWB system. The figure shows also a graphical representation of the TWR mechanism implemented between two transceivers[3]. Two-Way-Ranging is a packet exchange mechanism that is based on the transmission of two packets, a request packet and an acknowledge packet between two transceivers A and B. The Time-of-Flight is calculated at the transceiver B, after having received the acknowledge packet from transceiver A. The ToF calculation is based on the determination of the exact leading edge of the UWB pulses with a proper synchronization algorithm. A very common synchronization algorithm, also called window integrator, is based on the determination of the time when the sampling of the maximum UWB energy occurs. It is based on an integration window shift within a fixed pulse repetition period. The shift is realized by a dedicated DLL and phase selector that sequentially shift the control signal of the I&D. After a full exploration within the Pulse Repetition Interval (PRI) the clock phase corresponding to maximum energy is selected. The accuracy of the algorithm depends on the integration window shift, that for coarse synchronization can be

[3] Note that other ranging schemes are possible, for example in Ni et al. (2010) Time-Difference-Of-Arrival (TDOA) is used.

on the order of 5 ns or for fine synchronization even less than 1 ns. Here we applied this windowed integrator for both coarse and fine synchronization. Transceiver B system clock phase is different with respect to transceiver A, therefore the acknowledge packet must include information on both the processing time offset of TRX A and the synchronization phase used for detecting the maximum energy. Transceiver B, processes this information and, according to its synchronization phase, calculates the ToF, therefore distance. Details about the full mechanism can be found in Casu et al. (2008).

Bit-Error-Rate is determined in presence of Additive White Gaussian Noise (AWGN). Its determination implies the inclusion of the Salleh-Valenzuela UWB channel model in the simulation environment with a VHDL-AMS formalism IEE (2004). Natively, the model is implemented in Matlab and here its VHDL-AMS description is based on text files with rendered saved data samples issued with a constant time step. Fig. 8 shows the effect of

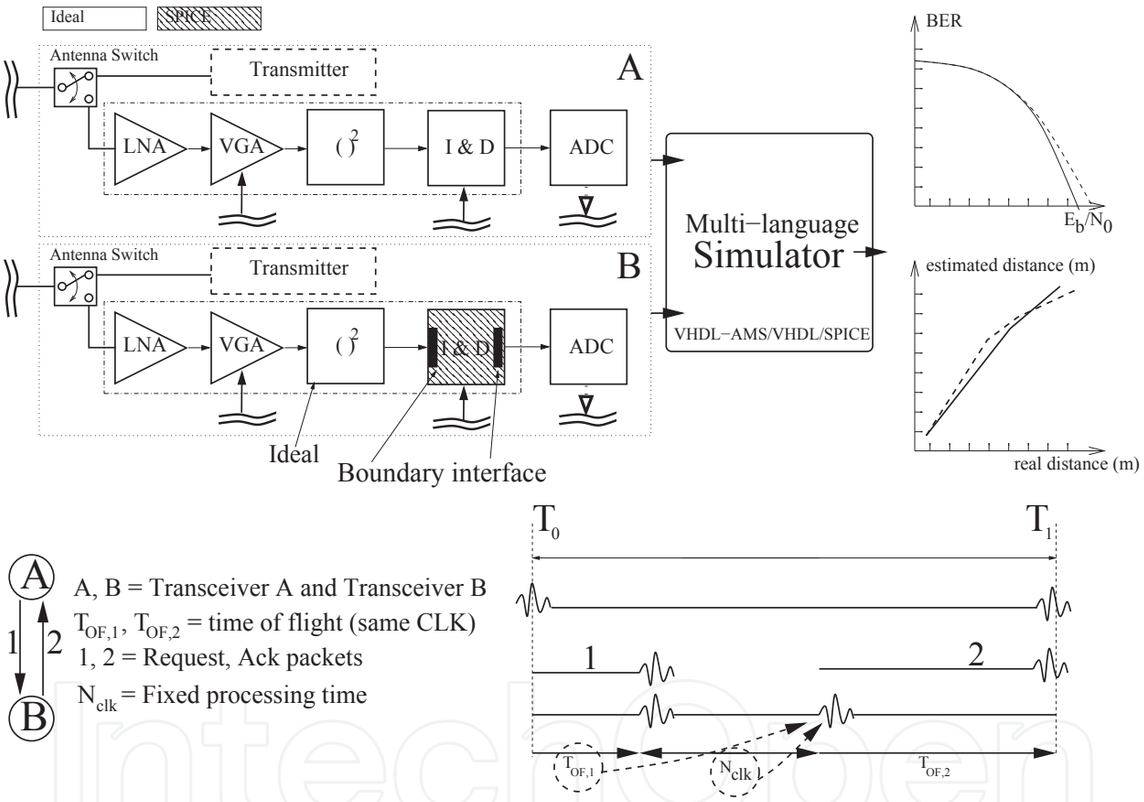

Fig. 7. Deactivation of non-ideal effects during system-level simulation and Two-Way-Ranging.

Phase-III integrator on the BER performance of the system Crepaldi et al. (2007) as a function of E_b/N_0 (proportional to Signal-to-Noise Ratio). The BER curve is slightly shifter because the *pole*2 of the integrator additionally filter input noise out of the squarer. If other blocks are implemented at transistor-level then, noise filtering increases. The results demonstrate that this design methodology permits the determination of transistor-level non-ideality at higher abstraction level.

With the Salleh-Valenzuela channel VHDL-AMS model TWR ranging simulations are also possible. Detailed TWR simulation results are reported in Casu et al. (2008). Two instances of the same IR-UWB transceiver schematized in 1 have been included in the environment

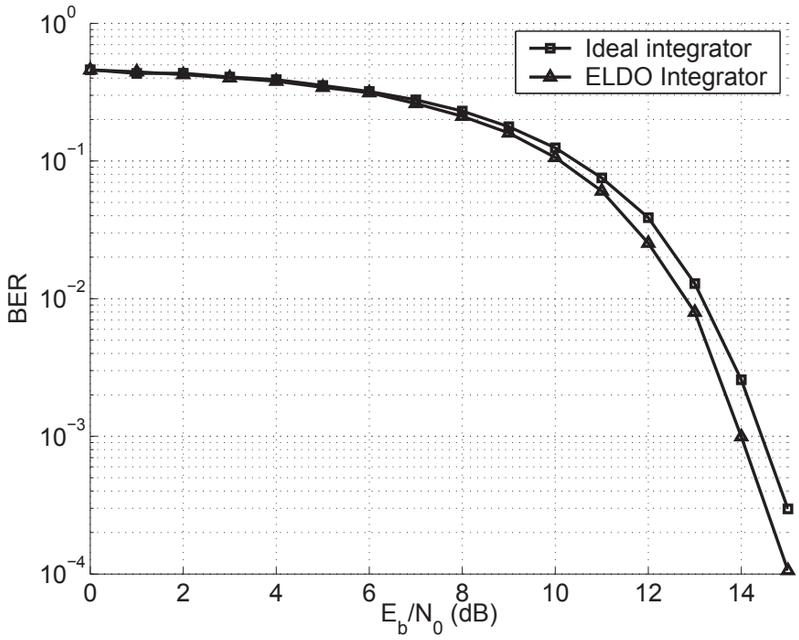

Fig. 8. Bit Error-Rate associated to the circuit-level I&D compared to the ideal system Crepaldi et al. (2007).

as well as specific scripts for enabling batch simulations execution. Channel is residential Line-Of-Sight (LOS) with the recommended path loss. The simulation environment sets its parameters with a parametric constant that models TRX distance. After 10 TWR packet exchanges we can obtain the effect of the I&D refinement on the localization performance of the system Crepaldi et al. (2007). With an ideal integrator at 9.9m distance, the estimated distance is 10.10m and 11.16m with variance 0.49m and 0.10m, for the Phase-II and transistor-level Phase-III models. Thanks to these inherent transient simulations results, the analysis of these two results permits the identification of the circuit blocks influenced in the performance loss. That is, having activated a transistor-level III description, enables the effects of other ideal blocks to influence performance. From the analysis it results that the reason for such a high variation in the estimated distance for Phase-III transistor level implementation depends on the operation of the AGC. The presence of a slightly non-ideal effect on the I&D "excites" the ideal AGC and a incorrect gain adjustment is provided. The incorrect amplification imposed by the AGC loop causes the squared signal to be out of the integrator input range and a lower output voltage is obtained. This causes the ADC quantization to be less effective and the ranging algorithm implemented in the digital back-end fails by few coarse synchronization steps.

Based on successive reasonings, other considerations are possible. The presence of a transistor-level block among other ideal blocks can lead to erroneous simulation conditions. For example, an LNA simply modeled with a perfectly linear amplifier $V_{out} = GV_{in}$, where G is voltage gain, V_{out} and V_{in} are across quantities defined on input and output terminals, does not include saturation. Due to automatic and autonomous system-level operation, an erroneous or partial modeling of some of the other blocks, can force, for example, a gain G on the LNA that leads to output voltage exceeding the allowed signal swing, e.g. 10 times bigger than supply voltage. This problem occurs mainly because the system is conceived

starting from high level models when inputs and outputs miss a physical counterpart. Note that this problem is irrelevant for high-level Matlab simulations in which idealized systems are proven. We conclude that for a consistent and correct system-level modeling, the inclusion of some fundamental circuit-level parameters such as voltage and power ranges limitations, bandwidth and power consumption dependency is extremely important.
The CPU time required to run a 30 μs simulation is an important information that justifies the presence of Phase-IV in our design methodology. As indicated in Crepaldi et al. (2007), on an IBM-Xeon server, 4GB RAM, 3.0 GHz processor with a fixed time step of 0.05 ns, an accuracy EPS=`10e-6` and the Newton/Raphson solving algorithm, the CPU time required with the SPICE netlist is 3 times larger than the time required using the backannotated VHDL-AMS model and 6 times the IDEAL Phase-II description.

6. Conclusion

We have presented a methodology that allows the exploration of the impact of refinement on system-level parameters for an IR-UWB Energy Detection system. The methodology is based on the use of the modular formalism of VHDL, working for the design of digital circuits, properly extended for use in analog continuous-time circuits with AMS extensions. The methodology is based on the use of a multi-language, multi-resolution tool and it is organized in four phases that generally define the main tasks required for a mixed-signal electronic system conception. VHDL-AMS has been conceived for use outside the field of electrical circuit, for example on fluidics, mechanics and all the possible domains governed by linear differential equations. Scientific community endeavors are focused on the efficient integration of any kind of system including MEMS even for IR-UWB Radio Frequency Tiiliharju et al. (2009), smart sensors and energy harvesting powered devices. This design methodology can be utilized also in these contexts, provided that the interface among the different domains is correctly modeled and sufficiently enriched with implementation details. IR-UWB remains, in fact, a valuable ULP wireless technology even for applications in smart sensors.
Based on these results, we believe that to merge both analog and digital design worlds, one interesting topic for successive research can regard a simple, uniform and modular mixed-signal language with a unique simulation tool for both analog and digital circuits disregarding the math they are based on. This language shall allow on-the-fly simulation accuracy directives embedded in each unit description depending on the nature of each block, digital or analog, with a similar semantics. Compared to VHDL-AMS it shall robustly fill the gap between the digital concurrent world and the analog continuous-time paradigm, instead of keeping them separated and making them coexist. In fact, AMS remains still a modeling language, therefore far from being used for automatic low-level synthesis as in digital VHDL design.

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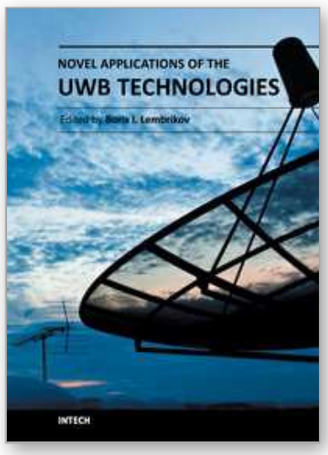

Novel Applications of the UWB Technologies

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Ultra wideband (UWB) communication systems are characterized by high data rates, low cost, multipath immunity, and low power transmission. In 2002, the Federal Communication Commission (FCC) legalized low power UWB emission between 3.1 GHz and 10.6 GHz for indoor communication devices stimulating rapid development of UWB technologies and applications. The proposed book Novel Applications of the UWB Technologies consists of 5 parts and 20 chapters concerning the general problems of UWB communication systems, and novel UWB applications in personal area networks (PANs), medicine, radars and localization systems. The book will be interesting for engineers and researchers occupied in the field of UWB technology.

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