We are IntechOpen, the world's leading publisher of Open Access books Built by scientists, for scientists

4,800
Open access books available

122,000
International authors and editors

135M
Downloads

Our authors are among the

154
Countries delivered to

TOP 1%
most cited scientists

12.2%
Contributors from top 500 universities

CLARIVATE ANALYTICS BOOK CITATION INDEX INDEXED

WEB OF SCIENCE™

Selection of our books indexed in the Book Citation Index in Web of Science™ Core Collection (BKCI)

Interested in publishing with us?
Contact book.department@intechopen.com

Numbers displayed above are based on latest data collected.
For more information visit www.intechopen.com

8

Modeling of Carbon Nanotube Field Effect Transistors

Dinh Sy Hien
HCM City University of Natural Sciences, Vietnam

1. Introduction

Since the discovery of carbon nanotubes (CNTs) by Iijima in 1991 [1], significant progress has been achieved for both understanding the fundamental properties and exploring possible engineering applications. The possible application for nanoelectronic devices has been extensively explored since the demonstration of the first carbon nanotube transistors (CNTFETs) in 1998 [2]. Carbon nanotubes are attractive for nanoelectronic applications due to its excellent electric properties. In a nanotube, low bias transport can be nearly ballistic across distances of several hundred nanometers. The conduction and valence bands are symmetric, which is advantageous for complementary applications. The bandstructure is direct, which enables optical emission, and finally, CNTs are highly resistant to electromigration.

Significant efforts have devoted to understand how a carbon nanotube transistor operates and to improve the transistor performance [3, 4]. It has been demonstrated that most CNTFETs to date operates like non-conventional Schottky barrier transistors [5, 6], which results in quite different device and scaling behaviors from the MOSFET-like transistors. Important techniques for significantly improving the transistor performance, including the aggressively scaling of the nanotube channel, integration of thin high-κ gate dielectric insulator [7], use of excellent source-drain metal contacts [8], and demonstration of the self-align techniques, have been successfully developed. Very recently, a nanotube transistor, which integrates ultra-short channel, thin high-κ top gate insulator, excellent Pd source-drain contacts is demonstrated using a self-align technique [9]. Promising transistor performance exceeding the state-of-the-art Si MOSFETs is achieved. The transistor has a near-ballistic source-drain conductance of $0.5 \times e^2 / h$ and delivers a current of 20 μA at $|V_G - V_T| \sim 1$ V. In this work, numerical simulations are developed to explain experiments, to understand how the transistor operates and what controls the performance, and to explore the approaches to improve the transistor performance. New simulation approaches are necessary for a carbon nanotube transistor because it operates quite different from Si transistors. The carbon nanotube channel is a quasi-one-dimensional conductor, which has fundamentally different carrier transport properties from the Si MOSFET channel. It has been demonstrated that treating the Schottky barriers at the metal/CNT interface and near-ballistic transport in the channel are important for correctly modeling the transistor. The CNT channel is a cylindrical semiconductor with a ~1 nm diameter, which means the electrostatic behavior of the transistor is quite different from Si MOSFETs with a 2D electron

gas. All carbon bonds are well satisfied at the carbon nanotube surface, which results in a different semiconductor/oxide interface. Furthermore, the phonon vibration modes and carrier scattering mechanisms are quite different in carbon nanotubes, which results in different roles of phonon scattering in CNTFETs. In this work, we developed physical simulation approaches to treat CNTFETs. We will show that our understanding of the carrier transport, electrostatics, and interracial properties seem to be sufficient to describe the behavior of the recently demonstrated short-channel CNTFETs.

This work is organized as follows. In section II, we start with a brief summary of progress in CNTFET technology. This discussion is intended to provide background of carbon nanotube, CNTFET technology. As our understanding of CNTFET device physics has evolved, an ability to model and simulate them has also been developed. Fabrication of CNTFET is discussed in section III. This section is intended to introduce progress in CNTFET fabrication. Section IV briefly describing the simulation approach that we use. In this section, we present non-equilibrium Green function method that commonly used for modeling and simulation in nano-scale devices. In section V, these numerical simulations are used to discuss some key issues in device physics such as ballistic transport, transport with scattering, current-voltage characteristics of CNTFET.

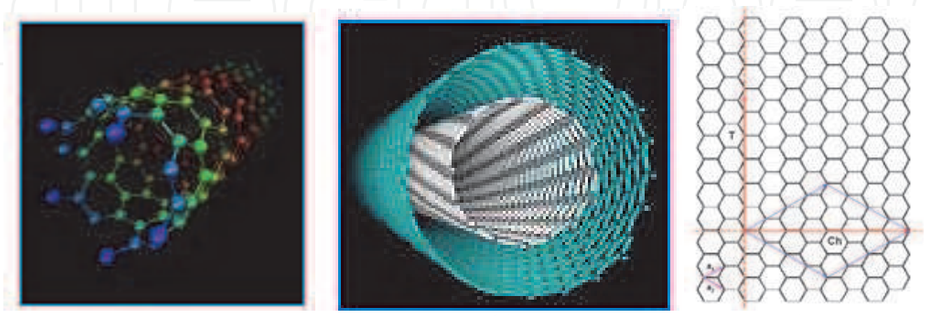
2. Carbon nanotube and CNTFET

2.1 Structure of CNT and CNTFET

Carbon nanotube (CNT) was discovered by Ijima in 1991 [1]. Since then, CNTs have been a leading candidate in continued improvement of the performance, speed and density of integrated circuits.

CNT can be viewed conceptually as graphene (a single atomic layer of graphite) sheets rolled up into concentric cylinders. The number of sheets is the number of walls and thus CNTs fall into two categories: single-wall CNTs (Figure 1a) and multi-wall CNTs (Figure 1b). There are currently three methods to synthesize CNTs: arc discharge, laser ablation and chemical vapor deposition (CVD).

The atomic structure of a single-walled CNT is conveniently explained in terms of two vectors C_h and T. T is called translational vector, it defines the direction of CNT axis. C_h is called chiral vector, representing the circumference of a CNT. Two carbon atoms crystallographically equivalent to each other were placed together according to: $C_h = n.\ \mathbf{a_1} + m.\ \mathbf{a_2}$, where $\mathbf{a_1}$ and $\mathbf{a_2}$ are the unit vectors of 2D graphene sheet (Figure 1c). (n, m) indices determine the diameter and chirality of CNTs.



(a) (b) (c)

Fig. 1. a) Single-walled carbon nanotube, b) multi-wall CNT, c) form of a single walled CNT from a graphene sheet.

Theoretical studies have shown that a single-walled CNT can be either metallic or semiconducting depending on its chirality and diameter. (n, m) nanotubes with n = m (arm-chair) are metallic; for n – m ≠ 3 × integer, the nanotubes are semiconducting with band gap proportional to 1/d. For n – m = 3 × integer, the nanotubes would be quasi-semiconducting with a small band gap proportional to $1/d^2$. The sensitivity of electrical properties on structural parameters in unique for CNTs, which opens up numerous opportunities in nanotube systems. The diameter of the zigzag nanotube, d is [7]

$$d = \frac{n\sqrt{3}a_{cc}}{\pi} \tag{1}$$

where a_{cc} = 0.142 nm is the carbon-carbon bond length in graphene. The diameter dependence on n in (16,0), (19,0), and (22,0) zigzag CNTs, which are in the experimentally useful diameter range (1.2 - 1.8 nm), can be listed in the table 1.

Type of zigzag CNTs	(16,0)	(19,0)	(22,0)
Diameter (nm)	1.25	1.50	1.70
Bandgap energy (eV)	0.67	0.56	0.49

Table 1. Parameters of semiconducting CNTs.

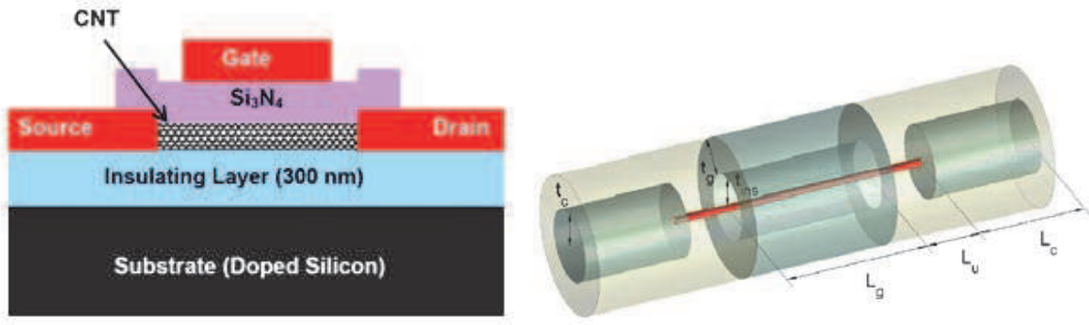
First of all, single-walled CNT are 1 D quantum systems and the two-terminal conductance is given by Landauer Buttiker formalism as: $G_c = (N.\ e^2/h) \times T$, where N is the number of conduction channels in parallel, T is transmission coefficient, and h is Plank constant, 6.625×10^{-34} J.s. For a single-walled CNT the band structure gives rise to two propagating channels and taking into account the additional spin quanta of electrons, there are four "channel" in total. Therefore, N = 4 and $G_c = (4e^2/h) \times T$, corresponding to a two-terminal resistance $R_C = 1/G_c = (h/4e^2) \times (1/T)$. In addition, the scattering of charge carriers along the length of CNTs results in a Drude-like resistance, $R_D \propto L_{CNT}$, where L_{CNT} is the length of CNT. Thus, the total resistance of a single-walled CNT contacted by metal leads on both ends is sum of these two contributions: $R_{tot} = R_C + R_D$.

If the contact is perfect (T = 1) and CNT is scattering free, charge carriers can move through the nanotube ballistically, we have $R_{tot} = R_C = h/4e^2 \approx 6.5\ k\Omega = R_0$. Usually, R_{tot} and R_C are greater than R_0 because T is less than one due to the reflection of charge carriers at the imperfect metal/CNT interface. R_{tot} even greater when there exists energy barriers at the metal/CNT interface, namely, Schottky barriers when CNTs are semiconducting. Schottky barriers have been a long standing problem for silicon and other conventional semiconductors. This problem is circumvented by replacing metal leads with heavy doping in conventional semiconductor industry. However, doping CNTs with nanoscale spatial resolution would be a formidable challenge. Recently, R_{tot} approaching R_0 has been observed for semiconducting CNT by Javey et al. at room temperature [8]. Further group reported a mobility of 79000 $cm^2/V.s$ measured from a semiconducting CNT [9]. This value exceeds those for all known semiconductors. Furthermore, the strong covalent bands give CNTs high mechanical strength and thermal stability and enormous charge carrying capacity. Current density as high as 10^9 A/cm^2 has been reported [10].

2.2 Carbon nanotube field effect transistors

CNTFET is a three-terminal device consisting of a semiconducting nanotube bringing two contacts (source and drain), and acting as a carrier channel, which is turned on or off electrically via the third contact (gate). Presently, there are several types of CNTFETs have been fabricated, but CNTFET geometries may be grouped in two major categories: planar and coaxial CNTFET, whether planar or coaxial, relies on simple principles, while being governed by additional phenomena such as 1D density of states (DOS), ballistic transport, and phonon scattering.

Planar CNTFETs (Figure 2a) constitute the majority of devices fabricated to date, mostly due to their relative simplicity and moderate compatibility with existing manufacturing technologies. The coaxial geometry (Figure 2b) maximizes the capacitive coupling between the gate electrode and the nanotube surface, thereby inducing more channel charge at a given bias than other geometries. This improved coupling is desirable in mitigating the short-channel effects that plague technologies like CMOS as they downside device features. The key device dimensions are: the gate inner radius, R_g, and thickness, t_g; the nanotube radius, R_t, and length L_t; the insulator thickness $t_{ins}= R_g-R_t$; the end-contact radius, t_c (the source and drain may sometimes be of different sizes), and length, L_c; and the gate-underlap L_u.



(a) (b)

Fig. 2. Structures of CNTFETs: a) planar, b) coaxial.

Manufacturing issues will ultimately play a decisive role in any future CNT electronic technology. Our focus here, however, is on the physics of CNT devices - specifically the CNTFET. It is still too early to tell what role CNTFETs will play in electronic systems of the future, but they provide us with a specific context in which to develop technology and understand transport, contacts, interfaces, etc.; which are likely to be important for CNT electronics in general. It is appropriate, however, to say a few words about where CNTFET technology stands today. Early CNTFETs were fabricated using nanotubes synthesized by a laser ablation process using nickel-cobalt catalysts [11]. The nanotubes were then suspended in a solvent and dispersed on an oxidized silicon wafer with predefined metal contact pads. The result was a random distribution of CNTs with some that bridged the contacts. Subsequently, catalytic chemical vapor deposition (CVD) methods were developed to grow CNTs on predefined catalyst islands [12]. The nanotubes thus fabricated are rooted in the catalyst islands and grow in random directions on the wafer with some terminating on

another island creating bridges. CVD techniques provide more control over device fabrication and have led to rapid progress in device performance.

CNTFETs are typically p-type devices that operate as so-called Schottky barrier (SB) transistors. The p-type characteristics have been attributed to the alignment of source-drain metal Fermi level near the valence band of the CNTs rather than to background doping or charges [5]. The holes in the channel are electrostatically induced by applying a negative gate voltage. Transistor action occurs because the gate modulates the SB width for hole tunneling near metal-CNT contact [5, 6]. While early transistors used gold (Au) as contact metals, significant performance improvements were obtained by using palladium contacts instead, which seem to eliminate the Schottky barrier for holes and produce near-ballistic operation [6]. However, other metals such as cobalt (Co) and titanium (Ti) are still being employed for high performance CNTFETs.

Early CNTFETs were fabricated on oxidized silicon substrates with a back-gated geometry and a thick SiO_2 layer that resulted in poor gate control of drain current [13, 14]. The use of a top-gated geometry produced immediate performance improvements [16]. Wind et al. deposited a thin dielectric layer (15-20 nm) on top of CNTs, and lithographically defined metal electrodes for gating and contacts. A transconductance ($g_m = dI_{ds}/dV_{gs}\,|_{Vds}$) of 3.25 μS and subthreshold swing ($S = ln(10)\,[dV_{gs}/d(ln(I_{ds}))]$) of 130 mV/decade were obtained, which was a significant improvement in device performance [16]. Later, the incorporation of high-κ dielectrics in a top-gated structure produced even better device characteristics [18]. Javey et al. employed a high-κ ZrO_2 (κ ~ 25) gate dielectric with a thickness of ~ 8 nm and obtained $g_m \approx 12$ μS and $S \approx 70$ mV/decade [18]. Although not always with top-gated geometry, other groups have also reported the use of high-κ dielectrics such as HfO_2 (κ ~ 11), TiO_2 (κ ~ 40-90), $SrTiO_3$ (κ ~ 175), and even electrolyte gating mechanisms for attaining improved performances [19, 20, 21, 22, 23]. In the case of electrolyte gating, Siddon et al. have reported $S \approx 62$ mV/decade which is very close to the theoretical limit of 60 mV/decade [23]. All of these devices appear to operate as CNT MSDFETs, some with essentially no barrier and others with rather large (half bandgap) barriers.

The possibility of ballistic operation of CNTFETs has been a topic of great interest. Since there are no dangling bonds in CNTs, surface scattering can be expected to be negligible. Back-scattering by acoustic phonons is suppressed by symmetry arguments related to the CNT bandstructure [24, 25] and by the reduction in phase space for one-dimensional conductors. The result is that mean-free-paths of several hundred nanometers are commonly observed [24, 26]. Under high bias, however, optical or zone boundary phonons may be emitted, and the mfps decrease substantially. Yao et al. showed that for long metallic CNTs, the current saturates at about 25 μA per nanotube [24]. They showed that the high-field current is limited by the emission of optical or zone boundary phonons with $\hbar\omega_0 \approx 200$ meV and that the high-field mfp is ~ 10 nm. Yao's results suggest that for short nanotubes, comparable in length to the mfp, the current should exceed 25 μA per nanotube. This expectation was confirmed by Park et al [27] and Javey et al, [26] who both showed that the current increases above 25 μA when the length of the nanotube is less than several mfps long. By analyzing their data, both Park and Javey extracted an mfp of ~10 – 15 nm, which was consistent with the value extracted by Yao for long nanotubes. The mfps deduced from these experiments are considerably shorter than the values of 50 nm or so, which are estimated from the expected electron-phonon coupling strength [24, 27]. Although these

results are for metallic nanotubes, similar effects are expected for semiconducting nanotubes and CNTFETs. For a tube much shorter than the mfp, carrier transport in the tube is quasi-ballistic, and the tube resistance is nearly length-independent. In contrast, a tube much longer than the mfp behaves like a classical resistor, in the sense that the resistance is proportional to the tube length.

Several recent improvements to CNTFET design collectively incorporate various techniques that have been developed during the past few years. For instance, Javey et al. reported a self-aligned top gate structure that uses the catalytic CVD method for CNT growth, a thin HfO_2 top gate dielectric ~ 50 nm in length and self-aligned palladium source-drain contacts [28]. A transconductance of 30 μS, subthreshold swing of 110 mV/decade, and a saturation current of ~25 μA at a power supply of V_{DD}~1 V were obtained [28]. Novel CNTFET device structures that enable high current operation and high integration densities have also been reported [29]. These devices are all of the metal source-drain (MSDFET) variety, but it is recognized that the use of a metal source will limit the drain current (unless the SB is sufficiently negative). Although progress in CNTFETs has been rapid, there are still many issues to address. The potential for digital logic [30, 31] was demonstrated early on. Techniques that modify the behavior of the nanotube from p-type to n-type have been implemented, which allowed their use in complementary CMOS logic. Following this, Derycke et al. demonstrated an inverter structure based on nanotubes [30]. Other nanotube based elementary digital logic gates with high gain and high I_{on}/I_{off} ratios, such as a NOR gate, a ring oscillator and an SRAM cell, have also been implemented [31].

With respect to RF performance, measurements [32, 34] and modeling [35] have both been initiated to assess performance potential. Experimental work includes that of Frank and Appenzeller, [32, 33] who developed a technique to circumvent the low-current-drive problem of CNTFETs to place a lower bound on the frequency response. Li et al. [34] measured the microwave reflection coefficient from a load comprised of a nanotube and a matching circuit and demonstrated transistor operation at 2.6 GHz. In terms of modeling, Burke [35, 36] has suggested an RF circuit model for a metallic nanotube, and emphasized the importance of both quantum capacitance and kinetic inductance. More recently, Burke used a standard formula, along with estimated and measured values for the parameters, to predict the unity-current-gain frequency (f_T) of CNTFETs, and suggested the f_T would be given by 80 GHz divided by the tube length in microns [$f_T = 80\ GHz / L(in\ \mu m)$].

A pressing issue that limits logic and RF device performance has to do with contacts. Good contacts to the valence band are achieved by using palladium. The barrier height is approximately zero for relatively large diameter nanotubes (D ~ 1.7 nm). Achieving small barrier contacts to the small diameter nanotubes that will be necessary for room temperature operation (D ~ 1 nm) is a key challenge, as is also achieving good, low barrier, contacts to the conduction band. CNT MOSFETs, however, are expected to deliver significantly better performance than MSDFETs, and recent progress on stable, heavy doping of CNTs is encouraging [37, 38]. For many applications, high currents are needed, so innovative structures that place several CNTs in parallel will be required. If these problems can be addressed, manufacturing challenges will move to the forefront. The key challenges are control of chirality and development of low temperature growth processes to allow CNTFETs to be placed at low cost on CMOS substrates.

3. Fabrication of CNTFET

Following the discussion on the properties of carbon nanotubes, we now give an overview of an important application and the topic of this work: the carbon nanotube field effect transistor. This three-terminal device consists of a semiconducting nanotube bridging two contacts (source and drain) and acting as a carrier channel, which is turned on or electrostatically via the third contact (gate). Presently, there are various groups pursuing the fabrication of such devices in several variations, achieving increasing success in pushing performance limits, while encountering myriad problems, as expected for any technology in its infancy. While the ease of manufacturing has improved significantly since their first conception in 1998, CNTFETs still have a long way to go before large-scale integration and commercial use become viable. Furthermore, as these transistors evolve at every research step, the specifics of their workings become clearer, and given that the aim of this work is to present a working model of CNTFETs, it is reassuring to see some of the findings presented herein being proven by recently released experimental data.

As regards the CNTFET's principle of operation, we briefly introduce two distinct methods by which the behavior of these devices can be explained. Primarily, the typical CNTFET is a Schottky-barrier device, *i.e.*, one whose performance is determined by contact resistance rather than channel conductance, owing to the presence of tunneling barriers at both or either of the source and drain contacts. These barriers occur due to Fermi-level alignment at the metal-semiconductor junction, and are further modulated by any band bending imposed by the gate electrostatics. Moreover, in some devices, the work-function-induced barriers at the end contacts can be made virtually transparent either by selecting an appropriate metallization or by electrostatically forcing via a separate virtual-gate terminal. These devices, sometimes labeled as bulk-modulated transistors, operate differently in that a thicker (non-tunneling) barrier, between the source contact and the mid-length region of the device, is modulated by the gate-source voltage. This operation is akin to that of a ballistic MOSFET, and effectively amounts to a channel modulation, by the gate, of a barrier to thermionically-emitted carriers, injected ballistically from the end contacts. We now provide a brief description of typical CNTFET geometries, which are grouped in two major categories, planar and coaxial. The specifics of nanotube growth and transistor fabrication issues, albeit of tremendous importance for this emerging field of nanoscale transistors, are beyond the scope of this work.

3.1 Planar devices

Planar CNTFETs constitute the majority of devices fabricated to date, mostly due to their relative simplicity and moderate compatibility with existing manufacturing technologies. The nanotube and the metallic source-drain contacts are arranged on an insulated substrate, with either the nanotube being draped over the pre-patterned contacts, or with the contacts being patterned over the nanotube. In the latter case, the nanotubes are usually dispersed in a solution and transferred to a substrate containing pre-arranged electrodes; transistors are formed by trial and error. Manipulation of an individual nanotube has also been achieved by using the tip of an atomic force microscope (AFM) to nudge it around the substrate; due to its strong, but flexible, covalent bonds, this is possible to do without damaging the molecule. In the case where the electrodes are placed over the tube, manipulation of the CNT is not required and alignment markers, pre-arranged on the substrate, allow accurate positioning of the contacts once the nanotube is located via examination by a scanning

tunneling microscope (STM). The gate electrode is almost always on the back side of the insulated substrate, or alternatively is patterned on top of an oxide-covered nanotube.
The first CNTFET devices were reported in 1998, and involved the simplest possible fabrication. They consisted of highly-doped Si back gates, coated with thick SiO_2, and patterned source-drain metal contacts, either using Au or Pt, as shown in figure 3A [13, 14]. Experimentations with different metals such as Ti, Ni, Al, and Pd have since been carried out by several groups, primarily to manipulate the work function difference between the end contacts and the nanotube. Subsequent work also produced a device that replaced the back gate with an electrode placed over the substrate, perpendicular to the source and drain contacts, as illustrated in figure 3B [15]. Here, the nanotube was separated from this gate electrode by a thin insulating layer of Al_2O_3, with the source-drain electrode strips placed over the tube ends for reduced contact resistance.

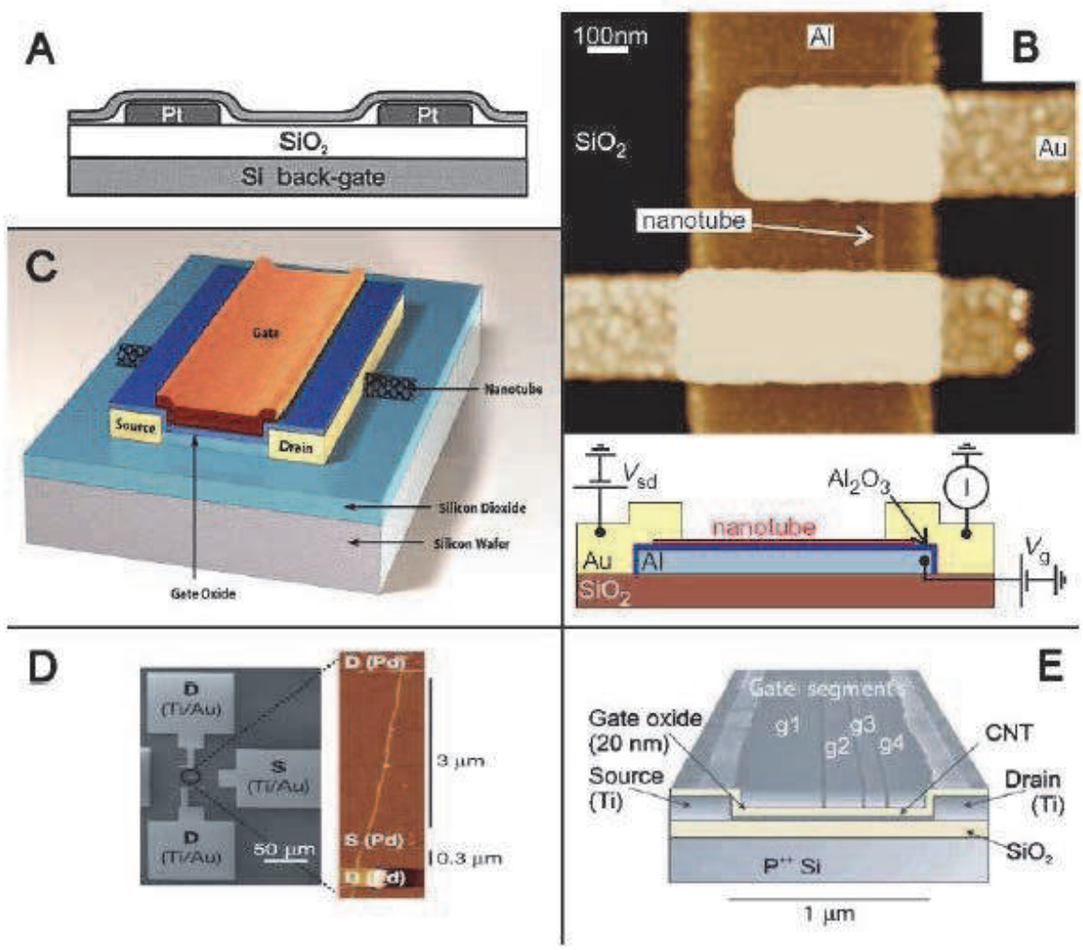


Fig. 3. Examples of planar CNTFETs: (A) Ref. [13], (B) Ref. [15], (C) Ref. [16], (D) Ref. [9], and (E) Ref. [19].

Figure 3C shows a further improvement in CNTFETs through the placement of the gate electrode over the semiconducting nanotube, thus improving the channel electrostatics via the thin gate oxide [16]. Moreover, the Ti source-drain metalizations in this device form

titanium carbide abrupt junctions with the nanotube, yielding increased conductance [17]. Another attempt to obtain better gate electrostatics involved materials with high dielectric constants, such as zirconia (ZnO_2) and hafnia (HfO_2), being used as gate insulators [18].
Figure 3D illustrates a device built with Pd source-drain contacts in order to exploit the sensitivity of this material's work function to hydrogen [9].
A multi-gate device, as shown in figure 3E, has recently been reported, whereby parallel top gates are used to independently control the electrostatics of different sections of the channel, thus facilitating a study of the transport characteristics of the nanotube channel [19]. More recently, a device with excellent DC characteristics was fabricated with Pd end contacts, Al gate, and hafnia for the insulator [10].
Most recently, a local gated carbon nanotube field effect transistor, as shown in figure 4, has been reported [42]. The approach is based on directed assembly of individual single wall carbon nanotube from dichloroethane via AC dielectrophoresis onto pre-patterned source and drain electrodes with a local aluminium gate in the middle. Local gated CNTFET devices display superior performance compared to global back gate with on-off ratios greater than 10^4 and maximum subthreshold swings of 170 mV/decade.

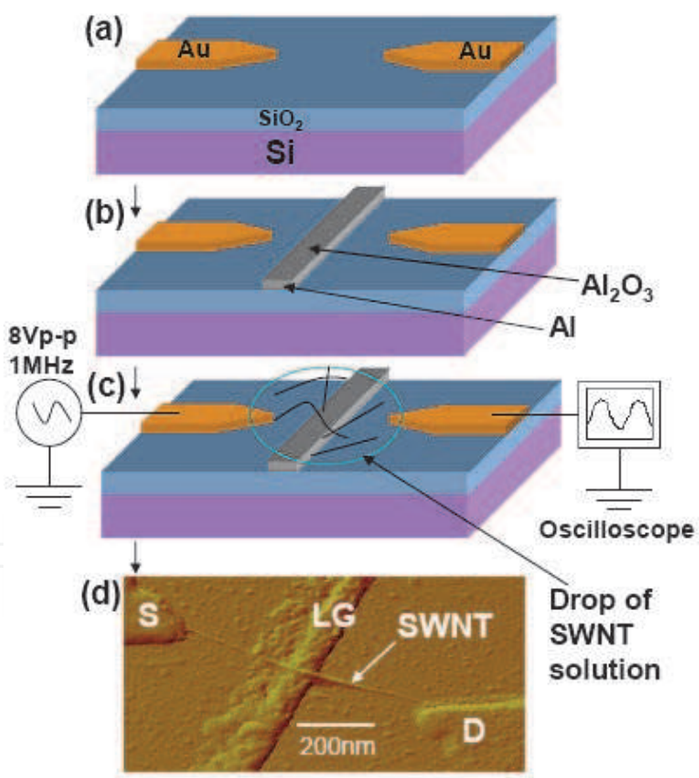


Fig. 4. Fabrication of local gated CNTFET: a) Source-Drain electrodes of 1 μm separation are patterned on heavily doped Si/SiO_2 substrates (250 nm thick oxide layer), b) Local Al gate electrodes are patterned using EBL and a 2-3 nm thick Al_2O_3 is created by oxygen plasma treatment, c) DEP assembly of CNT. An AC voltage of 8 Vp-p is applied for 1-2 seconds to the source electrode with a function generator, d) resulting AFM image of a device showing nanotubes are assembled at the tips [42].

3.2 Coaxial devices

Although yet to be fabricated in its ideal form, coaxial devices are of special interest because their geometry allows for better electrostatics than their planar counterparts. Capitalizing on the inherent cylindrical shape of nanotubes, these devices would exhibit wrap-around gates that maximize capacitive coupling between the gate electrode and the nanotube channel.

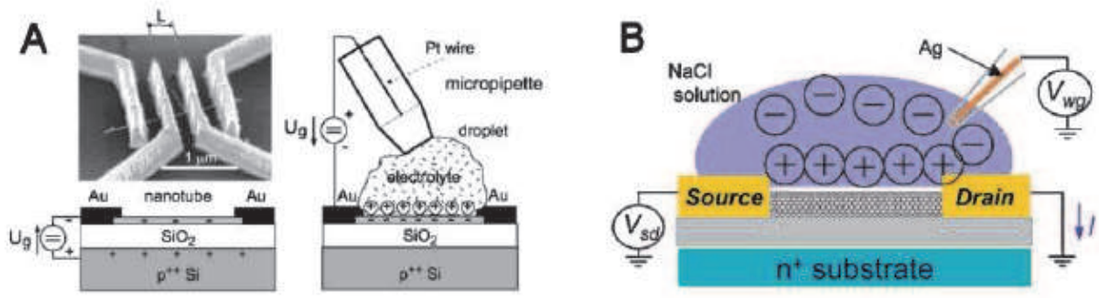


Fig. 5. Examples of electrolyte-gated CNTFETs: (A) Ref. [39], (B) Ref. [40].

Presently, the closest approximation to this geometry has been the development of electrolyte-gated devices. Kruger et al. reported the first such device, shown in figure 5A, using a multi-wall nanotube for the channel [39]. Two gates can be activated: a highly-doped Si back gate similar to planar devices; and an electrolyte gate, formed by a droplet of $LiClO_4$ electrolyte contacted by a thin platinum wire.

Figure 5B illustrates an improved version of this device, this time using single-wall carbon nanotubes and NaCl for the electrolyte, and yielding current-voltage characteristics that match those of modern Si MOSFETs [40]. Alternative structures for CNT devices that place the tube vertically with respect to the substrate have already been used for field-emission applications. Coaxial CNTFETs could perhaps be fashioned by placing nanotubes inside the cavities of a porous material such as alumina, surrounding them by an electrolyte solution for gating of individual devices.

Carbon nanotube transistors are not, however, the only devices in which an increased channel coupling is being sought. Other Si technologies, such as the FinFET and the tri-gate MOSFET are presently attempting to do this, and "wrap-gated" InAs-nanowire transistors have already been successfully prototyped [41].

Before we describe simulations and device physics of CNTFETs, we examine a key issue, numerical simulation technique that commonly used in modeling of nanoscale devices, non-equilibrium Green function method (NEGF).

4. Non-equilibrium Green function method

A number of groups have reported modeling and simulation studies of CNTFETs [43-48]. Our intent in this section is not to review that works. Instead, we briefly describe the techniques we currently use to simulate CNTFETs, because the results of our simulations will be used in section V to illustrate key features of CNTFET device physics.

Detailed treatment of carbon nanotube electronics requires an atomistic description of the nanotube along with a quantum-mechanical treatment of electron transport. For ballistic transport, we self-consistently solve the Poisson and Schrödinger equations using the non-equilibrium Green's function (NEGF) formalism [49]. Electron-phonon scattering does occur

under modest bias [26] and can be simulated by semi-classical, so-called Monte Carlo techniques, but scattering has a rather small role on the dc performance of CNTFETs with a channel length less than 100 nm.

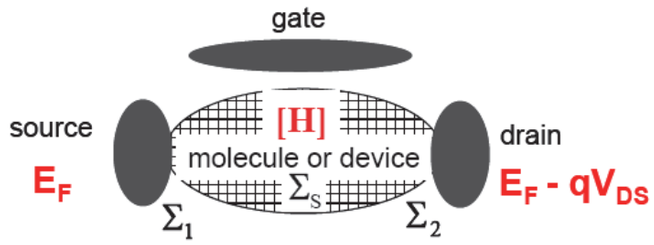


Fig. 6. A generic transistor comprised of a device channel connected to source and drain contacts. The source-drain current is modulated by a third electrode, the gate. The quantities involved in NEGF formalism are also shown.

To correctly treat transport in carbon nanotube transistors, we need to include quantum mechanical tunneling through the Schottky barriers at the metal-nanotube contacts, and quantum tunneling and reflection at the barriers within the nanotube channel. The non-equilibrium Green's function (NEGF) formalism provides a sound approach to describe ballistic and dissipative quantum transport. Figure 6 describes the essence of the technique and the key parameters of the formalism. We describe the device by using an effective mass Hamiltonian $H = -\left(\hbar^2 / 2m^*\right)\nabla^2 + U(r)$ and using the method of finite differences. The approach begins by identifying a suitable basis set and Hamiltonian matrix for the isolated channel. The self-consistent potential, which is a part of the Hamiltonian matrix, is included in the diagonal components of **H**, which is an N x N matrix where N is the total number of orbitals in the simulation domain (i.e. the number per carbon atom times the number of carbon atoms in the channel). The second step is to compute the so-called self-energy matrices, Σ_1, Σ_2, and Σ_S, which describe how the channel couples to the source and drain contacts, and to the scattering process. For example, only ballistic transport is treated, we assume that $\Sigma_S = 0$, while transport with scattering, $\Sigma_S \neq 0$. The third step is to compute the retarded Green's function. The retarded Green's function for the device in matrix form is given by

$$G(E) = [(E + i\eta^+)I - H - \Sigma(E)]^{-1} \tag{2}$$

where η^+ is an infinitesimal positive value, and I is the identity matrix.
The self-energy contains contributions from all mechanisms of relaxation, which are the source and drain electrodes, and from scattering:

$$\Sigma(E) = \Sigma_1(E) + \Sigma_2(E) + \Sigma_S(E) \tag{3}$$

Note that, in (2), the self-energy functions are, in general, energy dependent. The density matrix given by

$$[\rho] = \int_{-\infty}^{+\infty} \frac{dE}{2\pi} \left\{ \left[A_1(E) \right] f_1(E) + \left[A_2(E) \right] f_2(E) \right\} \tag{4}$$

where $A_{1,2}(E)$ are spectrum functions given by

$$A_1(E) = G\Gamma_1 G^+, A_2(E) = G\Gamma_2 G^+ \tag{5}$$

where level broadening can be defined as follows:

$$G_{1,2}(E) = i[S(E) - S^+(E)] \tag{6}$$

where $\Sigma^+(E)$ represents the Hermitian conjugate of $\Sigma(E)$ matrix defined by (2).
$f_{1,2}(E)$ are the Fermi distribution functions in the source and drain contacts, respectively. The Fermi distribution functions are given by

$$f_{1,2}(E) = \frac{1}{1 + \exp(E - \mu_{1,2}) / kT} \tag{7}$$

Once we apply a drain-source bias, V_{DS}, the Fermi energies in the source and drain contacts denoted by μ_1 and μ_2 will separate as follows

$$\mu_1 = E_f + (eV_{DS} / 2) \text{ and } \mu_2 = E_f - (eV_{DS} / 2) \tag{8}$$

The current flows from source to drain can be defined by

$$I = \frac{4e}{\hbar} \int_{-\infty}^{+\infty} \frac{dE}{2\pi} T(E)[f_1(E) - f_2(E)] \tag{9}$$

With the transmission coefficient T(E) given by

$$T(E) = \text{Trace}\,[G_1(E)G(E)G_2G^+(E)] \tag{10}$$

In the next section, we will use numerical simulations to discuss the physics of CNTFETs.

5. Simulations of CNTFET

In this section we summarize versions of simulators on nanoelectronics devices such as NEMO-VN1, and NEMO-VN2 that are developed by our research group for demonstrations. Especially, here we have focused on simulation results of CNTFETs. The reader can refer to [50, 51] for more detail.

5.1 NEMO-VN1 [52]

The dimensional scaling of CMOS device and process technology will become much more difficult as the industry approaches 10 nm around year 2020 and will eventually reach asymptotic end according to the International Technology Roadmap for Semiconductor for emerging research devices (2005). Beyond this period of traditional CMOS it may be possible to continue functional scaling by integrating an alternative electronic device on to a silicon platform. These alternative electronic devices in the future include 1D structures (such as CNTs and compound semiconductor nanowires), RTDs, SET, molecular and spin devices, all of which are discussed in ref. [52].

Despite these exciting possibilities, nanoelectronic devices are still in their relative infancy. The expense and difficulty of device fabrication precludes simply building and testing vast arrays of quantum devices. To focus efficiently on the best design, engineers need a tool that predicts electronic characteristics as a function of the device geometry and composition. In the more scientific mode, such a simulator would greatly enhance the understanding of quantum effects that drive the transport process and provide a means to investigate new device concepts.
Even conventional devices require a correction for quantum effects associated with the smaller device features. MOS devices, for example, exhibit electron confinement effects in the inversion layer. This phenomenon is a function of decreasing oxide thickness rather than the overall size of the device. Quantum effects become important as the oxide layer thickness decreases below 2 nm, which will soon be a standard for manufactured integrated circuits. Problems of this nature will become more prevalent as device geometries continue to shrink.
Nanoelectronic device modeling requires a fundamental quantum-mechanical approach. Many forms of quantum correction to classical electronic device models have been proposed or implemented. These include MOSFET-specific quantum corrections and generic quantum corrections to the drift-diffusion, hydrodynamic, and Boltzmann transport equation models. Therefore, the semiconductor industry needs a new fully quantum-mechanically based TCAD (technology computer aided design) tool [52].
To address this problem, we developed a general purpose quantum device simulator called NEMO-VN1 (NanoElectronic MOdeling in Vietnam). NEMO-VN1 can simulate a wide variety of nanoelectronic devices, including Quantum Dot (QD), Resonant Tunneling Diode (RTD), Resonant Tunneling Transistor (RTT), Single Electron Transistor (SET), Molecular FET (MFET), Carbon Nanotube Field Effect Transistor (CNTFET), Spin FET (SPINFET). It has a collection of models that allow user to trade off between calculation speed and accuracy. NEMO-VN1 also includes a graphic user interface (GUI) of Matlab that enables parameter entry, calculation control, display of calculation results, and in-situ data analysis methods.
In the next section, we review the capabilities of NEMO-VN1 and give example of typical NEMO-VN1 simulations.

5.1.1 NEMO-VN1 GUI

Another important goal of the NEMO-VN1 project was to make a user-friendly simulator that provides as much control as possible over every aspect of the simulation. Flexibility and ease of use are difficult to achieve simultaneously, but given the complexity of quantum device simulations became clear that both criteria were vital to program success. Consequently, graphic user interface (GUI) development was major part of the NEMO-VN1 program.

5.1.2 Main screen

NEMO-VN1 has a rich variety of simulation models, while this provides the maximum flexibility in term of applicability to different types of devices and test conditions. The problem is that NEMO-VN1 requires over 100 simulation parameters. Traditional device simulators force the users to familiarize themselves with all available simulation parameters and ensure that they are set correctly. To minimize this burden for the users, NEMO-VN1 uses a hierarchical approach to input and displays simulation parameter values. The top level of this hierarchy specifies the highest level option (type of device). Subsequent levels contain more detailed options such as current-voltage characteristics of devices, types of material, size of devices, size of barriers, temperature, colors, etc.

The main screen shown in Figure 7a is the central location where the user controls the NEMO-VN1 simulation. From Main Screen, the user can choose various types of quantum device simulations by clicking the mouse pointer on component items (left top corner). In this manner, the user can quickly enter the device list with minimum of typing. Double clicking the left mouse pointer on each item in the device list initiates the selection of models which is used to calculate the current voltage characteristics (Figure 7b).

(a) (b)

Fig. 7. a) The NEMO-VN1 main screen. File of components contains a device list. b) Pressing left mouse pointer on "components" displays a list of simulation quantum devices.

5.1.3 NEMO-VN1 simulation

In the course of the NEMO-VN1 program, we have simulated QD, QWi, QWe, RTD, RTT, SET, CNTFET, MFET, and SPINFET. As example, in the following sections, we consider current voltage characteristics of CNTFET.

5.1.4 CNTFET's simulation

The algorithm for the calculation of drain current in the model can be described as follows. Because of the small size of these devices, and the near one-dimensional nature of charge transport within them, CNTFET's modeling demands a rigorous quantum-mechanical basis. This is achieved in this model by using non-equilibrium Green's function method to compute transport of the electron and hole charges in nanotubes, and by using the Landauer Equation to compute the drain current. The model of CNTFET is displayed in Figure 8a. Current voltage characteristics are shown in Figure 8b.

The current voltage curve can be divided into two regions: linear and saturation. Drain current in the linear region of planar CNTFET can be described as follows:

$$I_d = \frac{W}{L}\mu C_{ox}[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}] \tag{11}$$

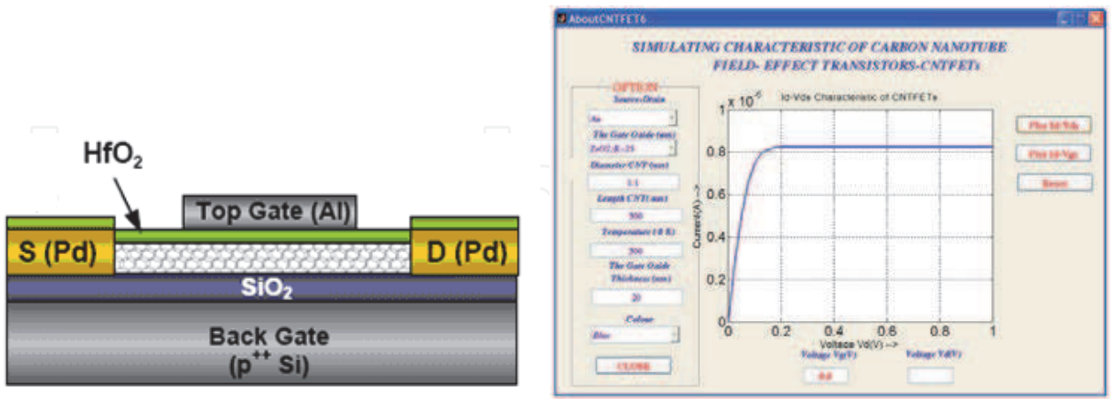
or

$$I_d = K_n\left[2\left(V_{gs} - V_T\right)V_{ds} - V_{ds}^2\right] \tag{12}$$

where K_n is conductance of CNTFET, W is the width of CNTFET, L is the length of CNTFET, μ is mobility of carriers, C_{ox} is oxide gate capacitance.

We can also obtain saturation current of CNTFET by replacing $V_{ds(sat)} = V_{gs} - V_T$. Then the expression of saturation current of CNTFET can be written:

$$I_{d(sat)} = K_n\left(V_{gs} - V_T\right)^2 \tag{13}$$



(a) (b)

Fig. 8. a) The model of CNTFET, b) NEMO-VN1 plots current voltage characteristics for CNTFET. Current is measured as a function of drain voltage at 300 K. For this device, source-drain of CNTFET is made of Au, the diameter of CNT is 1.1 nm, the length of CNT is 300 nm, the gate thickness is 20 nm

The drain I-V characteristics in 3D are shown in Figure 9. The parameters used in 3D simulation are drain current-voltage characteristics and temperature. Drain I-V characteristics exhibited dependence of saturation drain current (ON-current) on temperature. When CNTFET is cooled, drain saturation currents were lightly decreased.

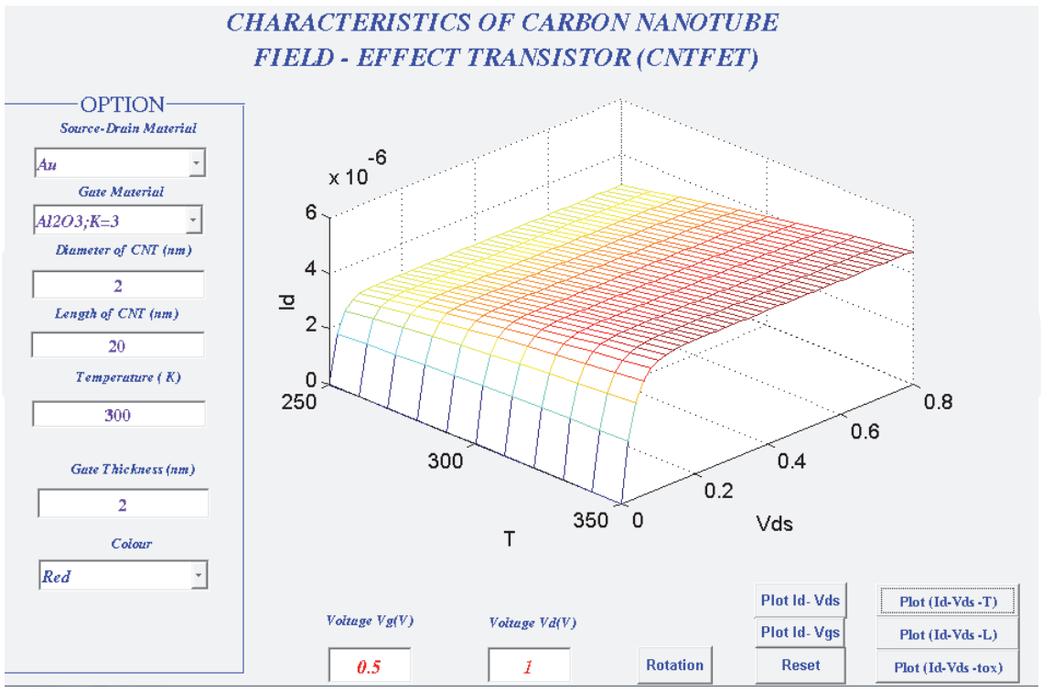


Fig. 9. Drain current-voltage characteristics in 3D. When CNTFET is cooled, its saturation drain currents are lightly decreased.

Drain current-voltage characteristics in 3D exhibited dependence of saturation currents on CNTFET length, L are shown in figure 10. Tendency of saturation currents is decreased, when CNTFET length is increased. We found that in the range of CNTFET length from 10 nm to 15 nm, ON-currents lightly changed.

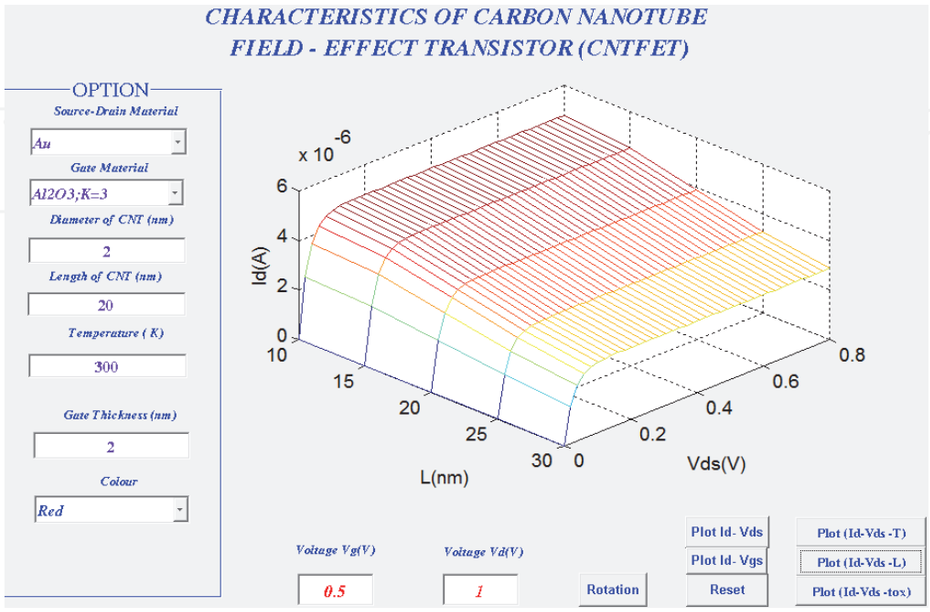


Fig. 10. Drain current-voltage characteristics in 3D exhibited dependence of saturation drain currents on CNTFET length.

Drain current-voltage characteristics in 3D exhibited dependence of saturation current on the gate thickness of CNTFET, t_{ox} are shown in figure 11.

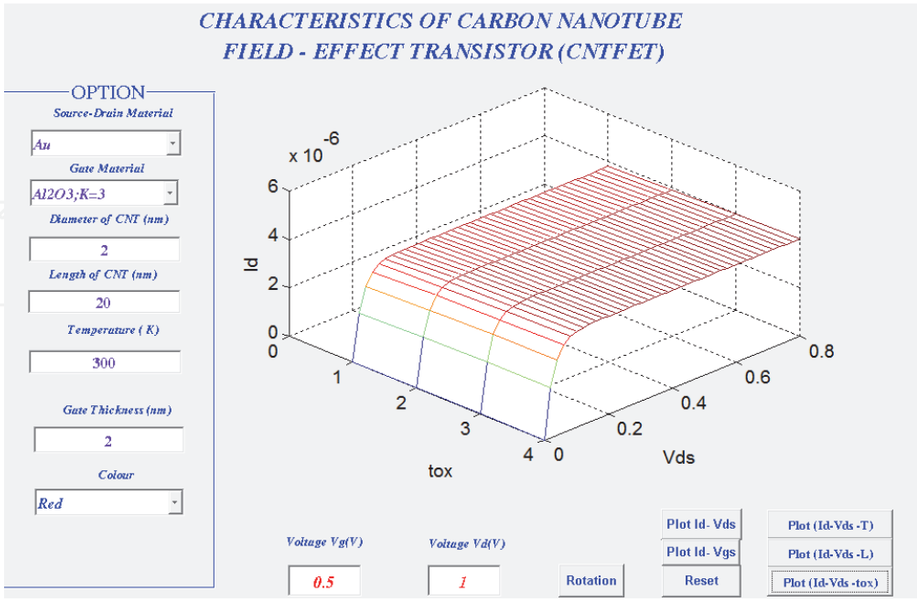


Fig. 11. Drain current-voltage characteristics in 3D exhibited dependence of saturation drain currents on the gate thickness of CNTFET.

The current voltage curve can be divided into two regions: linear and saturation. Drain current in the linear region of coaxial CNTFET can be described as follows:

$$I_d = \mu C_{ox}[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}] \tag{14}$$

or

$$I_d = K_n\left[2\left(V_{gs} - V_T\right)V_{ds} - V_{ds}^2\right] \tag{15}$$

where K_n is conductance of CNTFET, μ is mobility of carriers, C_{ox} is gate capacitance.
In the coaxial CNTFET,

$$C_{ox} = 2\pi R_g L_g k\varepsilon_0 \left(\lg\frac{R_g}{R_t}\right)^{-1} \tag{16}$$

where k is relative dielectric constant, ε_0 is dielectric constant in vacuum, 8.85×10^{-14}Fcm^{-2}.
We can also obtain saturation current of coaxial CNTFET by replacing $V_{ds(sat)} = V_{gs} - V_T$. Then the expression of saturation current of CNTFET can be written:

$$I_{d(sat)} = K_n\left(V_{gs} - V_T\right)^2 \tag{17}$$

The drain I-V characteristics in 2D are shown in figure 12. The saturation current at V_{GS} = 0.5 V is around 6 μA.

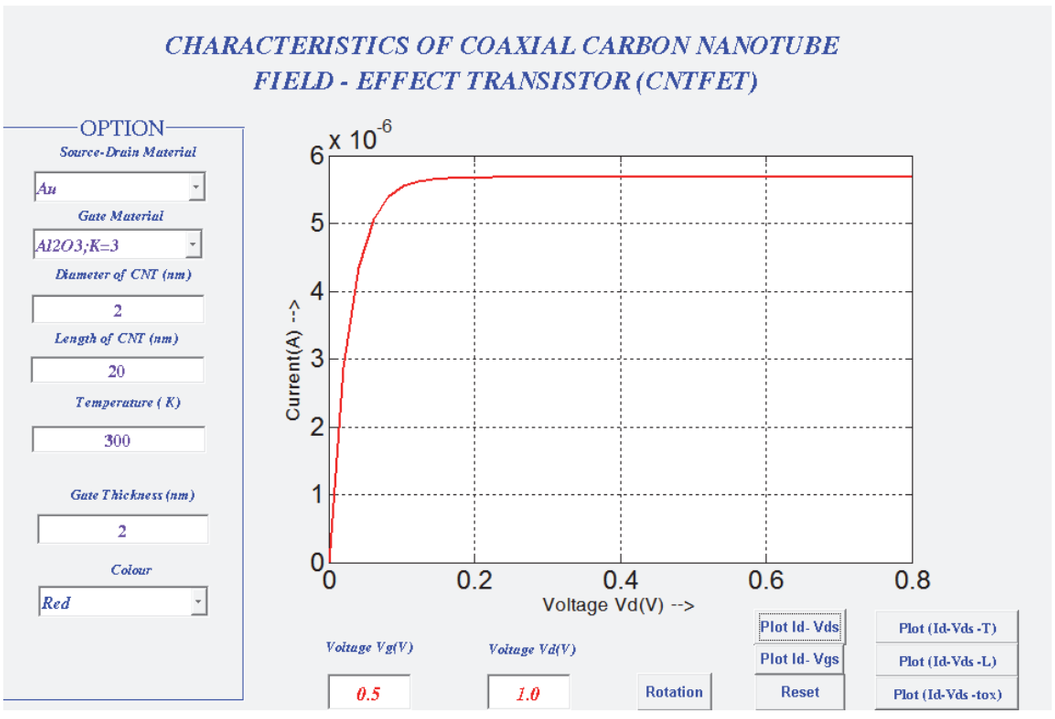


Fig. 12. Drain current-voltage characteristics of coaxial CNTFET.

The drain I-V characteristics in 3D are shown in figure 13. The parameters used in 3D simulation were drain current-voltage characteristics and temperature. Drain I-V characteristics exhibited dependence of saturation drain current on temperature. When CNTFET is cooled, saturation currents were lightly decreased.

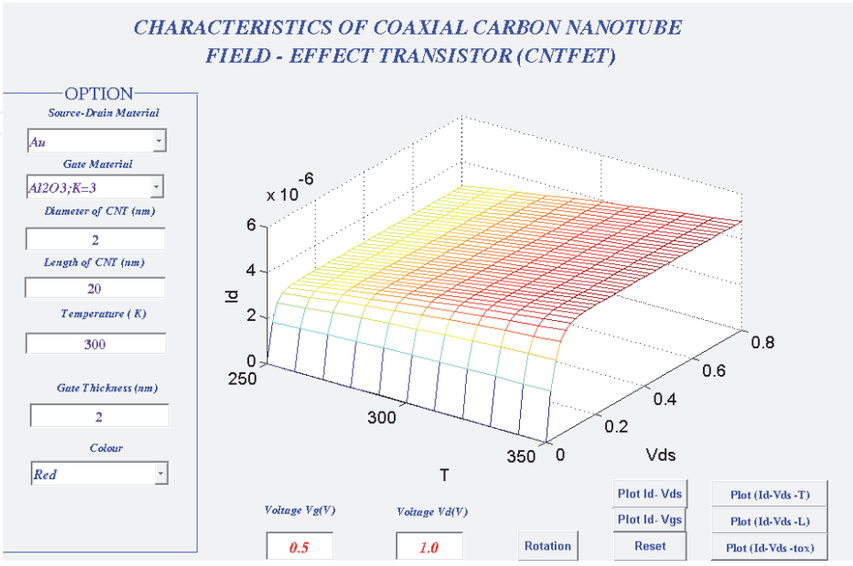


Fig. 13. Drain current-voltage characteristics in 3D. When CNTFET is cooled, its saturation drain currents were lightly decreased.

Drain current-voltage characteristics in 3D exhibited dependence of saturation currents on CNTFET length, L are shown in figure 14. Tendency of saturation currents is decreased, when CNTFET length is increased. We have also found that in the case of coaxial CNTFET, ON-currents in the range of the length, L from 10 nm to 15 nm is lightly decreased.

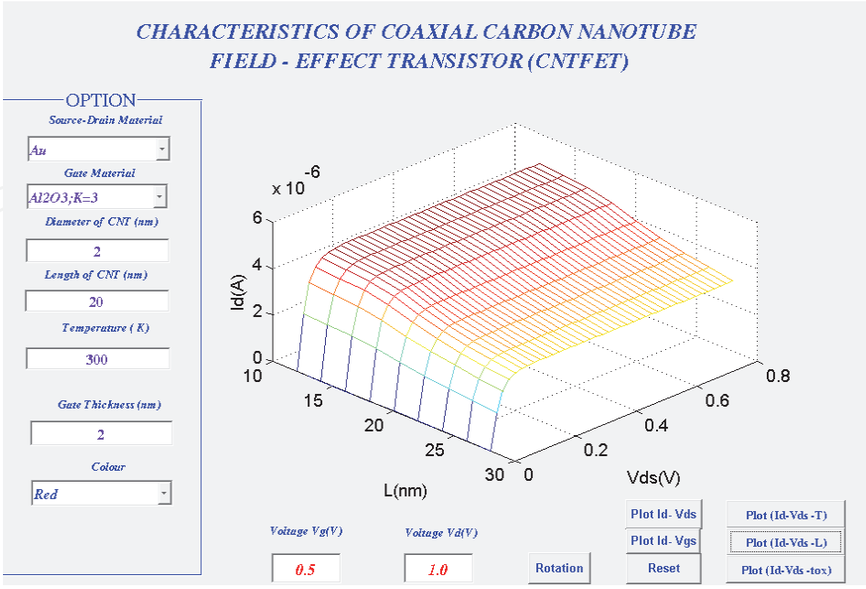


Fig. 14. Drain current-voltage characteristics in 3D exhibited dependence of saturation drain currents on CNTFET length.

5.2 NEMO-VN2 [53]

The quantum device simulator – NEMO-VN2 focuses on carbon nanotube FET (CNTFET). CNTFETs have been studied in recent years as potential alternatives to CMOS devices because of their compelling properties. Studies of phonon scattering in CNTs and its influence in CNTFET have focused on metallic tubes or on long semiconducting tubes. Phonon scattering in short channel CNTFETs, which is important for nanoelectronic applications, remains unexplored. In this work the non-equilibrium Green's function (NEGF) is used to perform a comprehensive study of CNT transistors. The program has been written by using graphic user interface (GUI) of Matlab. We find that the effect of scattering on current-voltage characteristics of CNTFET is significant. The degradation of drain current due to scattering has been observed. Some typical simulation results have been presented for illustration.

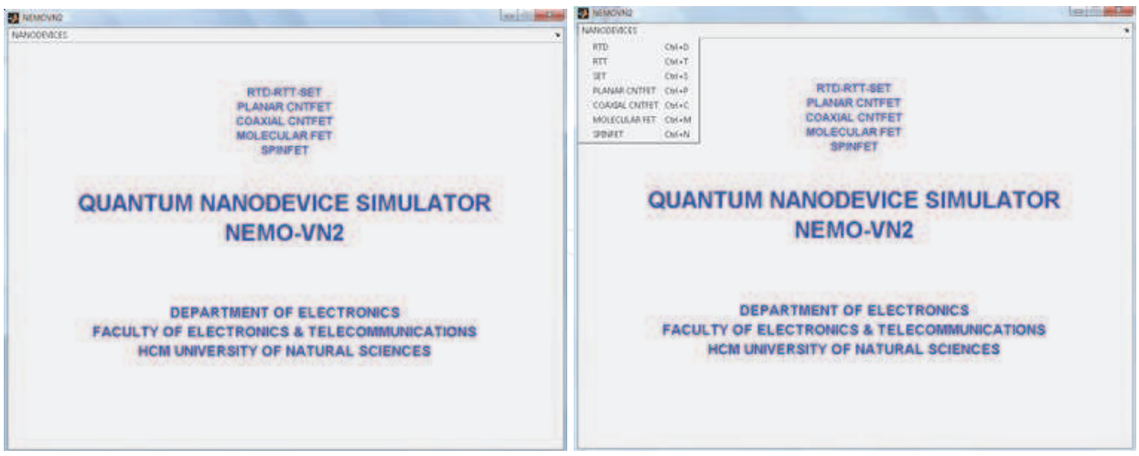
5.2.1 Simulation results of CNTFETs

The main goal of the NEMO-VN2 project was to make a user-friendly simulator that provides as much control as possible over every aspect of the simulation. Flexibility and ease of use are difficult to achieve simultaneously, but given the complexity of quantum device simulations became clear that both criteria were vital to program success. Consequently, graphic user interface (GUI) development was major part of the NEMO-VN2 program.

NEMO-VN2 has a rich variety of simulation models, while this provides the maximum flexibility in term of applicability to types of different devices and test conditions. The problem is that NEMO-VN2 requires over 100 simulation parameters. Traditional device simulators force the users to familiarize themselves with all available simulation parameters and ensure that they are set correctly. To minimize this burden for the users, NEMO-VN2 uses a hierarchical approach to input and displays simulation parameter values. The top level of this hierarchy specifies the highest level option (nanodevices). Subsequent levels contain more detailed options such as current-voltage characteristics of devices, types of material, size of devices, size of barriers, temperature, colours, etc.

The main screen shown in figure 15a is the central location where the user controls the NEMO-VN2 simulation. From main screen, the user can choose various types of quantum device simulations by clicking the left mouse pointer on the submenu of nanodevices (in the left top corner). In this manner, the user can quickly enter the device list and hot keys with minimum of typing. Clicking the left mouse pointer on each item in the device list or using hot keys initiates the selection of models which is used to calculate the current voltage characteristics (figure 15b).

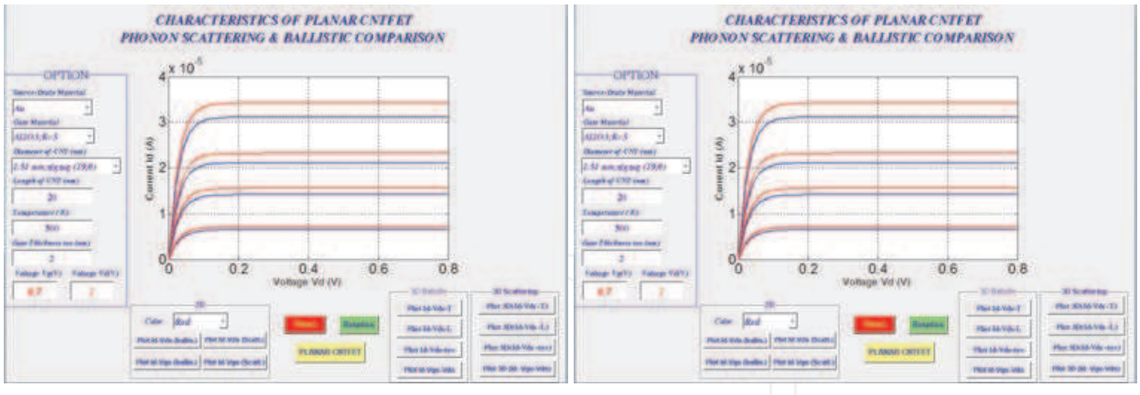
In the course of the NEMO-VN2 program, we have simulated all of emerging nanodevices such as RTD, RTT, SET, planar CNTFET, coaxial CNTFET, molecular FET, and SPINFET. Here, as an example, we study the effects of phonon scattering on the planar and coaxial CNTFET characteristics. We compare their characteristics under ballistic and that with phonon scattering. The device parameters are used for the simulations are as follows: source-drain material of Au, length of CNTFET, L = 20 nm, diameter of CNT, d = 1.5 nm, zigzag, gate material of Al_2O_3, gate thickness, t_{ox} = 2 nm, temperature under simulation, T = 300 K.



(a) (b)

Fig. 15. a) The NEMO-VN2 main screen, b) pressing left mouse pointer on "NANODEVICES" displays a list of simulation quantum devices.

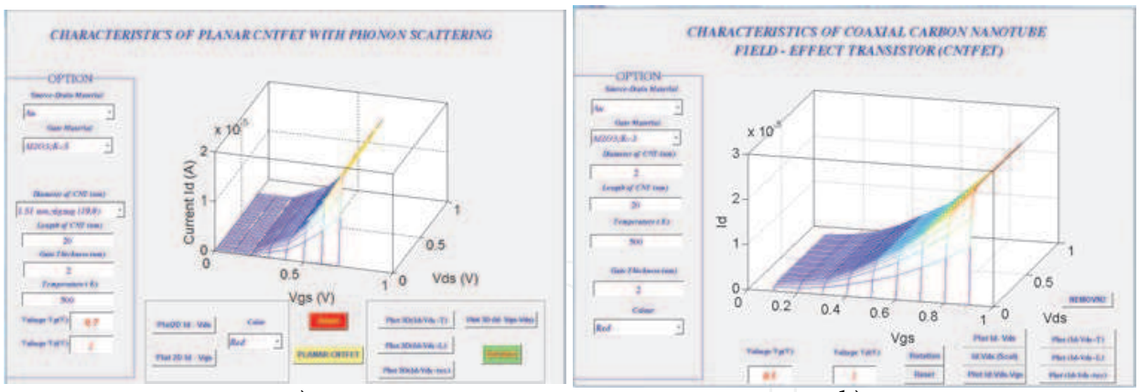
Figure 16 compares the I_{DS}-V_{DS} results for two types of planar and coaxial CNTFETs having the length of 20 nm under ballistic transport and that with phonon scattering. It is shown that scattering can have an appreciable affect on the ON-current. At V_{GS} = 0.7 V, in the planar and coaxial CNTFETs, the ON-current is reduced by 9% due to the phonon scattering. It can be noted that when the gate voltage is increased the saturated drain current gradually increased.



a) b)

Fig. 16. I_{DS}-V_{DS} characteristics of a) planar and b) coaxial CNTFETs having the length of 20 nm under ballistic transport (red colour), with scattering (green colour) at various gate biases in the range from 0.4 to 0.7 V in the step of 0.1 V. The bottom and top curves are at the gate voltages of 0.4 V and 0.7 V, respectively.

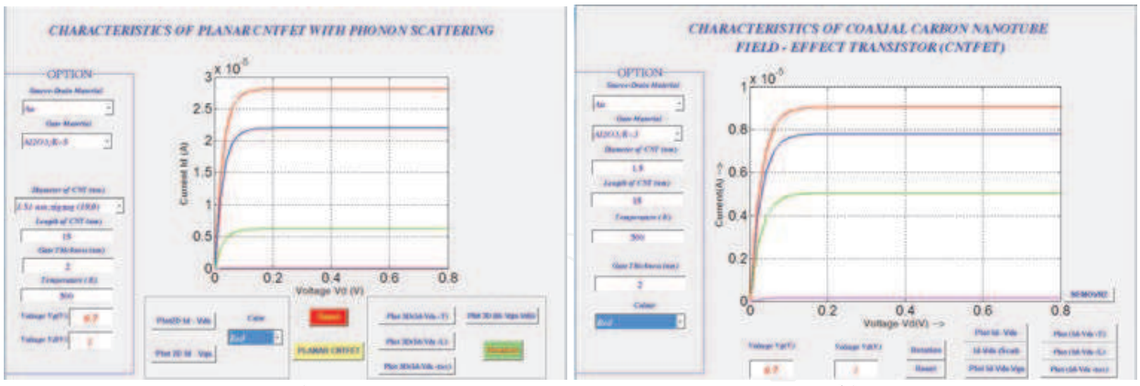
Figure 17 shows I_{DS}-V_{GS} characteristics of planar and coaxial CNTFETs. When the gate voltage is small, the drain current is gradually increased. When the gate voltage is greater than V_{GS} = 0.3 V, the drain current is exponentially increased.



a) b)

Fig. 17. Three dimensional simulations of I_{DS}-V_{GS} characteristics of CNTFETs having the length of 20 nm: a) planar, b) coaxial.

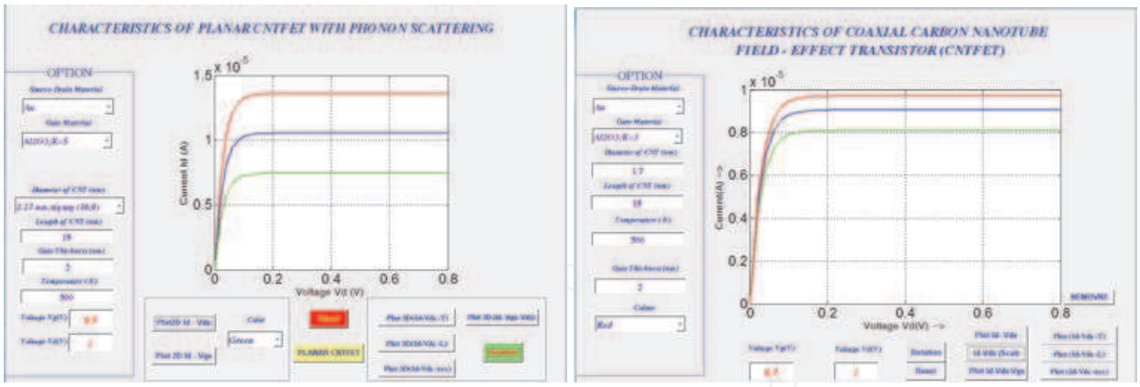
Figure 18 compares the length dependence of I_{DS}-V_{DS} results for the (19,0) CNTFETs under phonon scattering. The ON-current at V_{GS} = 0.7 V is reduced when the length is changed by 15, 10, 5, 2.5 nm. In figure 18a, it is also shown that the impact of phonon scattering in planar CNTFET increases for shorter length tubes at high voltage bias. It should be noted that ON-current strongly depends on reducing the length of CNTFET. At high gate voltage bias ON-current of CNTFET having length of 15 nm is by 30 μA, when length of CNTFET reduced to 2.5 nm ON-current is by 8 pA. In figure 18b, it is also shown that the impact of phonon scattering in coaxial CNTFET. ON - current increases for shorter length tubes at high voltage bias. It should be noted that ON-current strongly depends on reducing the length of CNTFET. At high gate voltage bias ON-current of the coaxial CNTFET having length of 15 nm is by 9 μA, when length of CNTFET reduced to 2.5 nm ON-current is by 150 nA.



a) b)

Fig. 18. The length dependence of I_{DS}-V_{DS} results for the (19,0) CNTFETs under phonon scattering: a) planar CNTFETs; b) coaxial CNTFETs. The lengths of CNTFETs are of 15, 10, 5, 2.5 nm from top to bottom curves.

Figure 19a compares the diameter dependence of the I_{DS}-V_{DS} results of the impact of phonon scattering in planar CNTFET having the length of 15 nm. It is shown that ON-currents at V_{GS} = 0.7 V increase by 8, 11, 14 μA when diameters of CNT increase by 1.25, 1.5, 1.7 nm, respectively. In figure 19a, it notes that the impact of phonon scattering in CNTFET decreases for larger diameter tubes.



a) b)

Fig. 19. The diameter dependence of I_{DS}-V_{DS} characteristics at V_{GS} = 0.7 V in CNTFET having the length of 15 nm under scattering: a) in planar CNTFET ON-current increase by 8, 11, 14 μA when diameters of CNT increase by 1.25, 1.5, 1.7 nm, respectively, b) in coaxial CNTFET under scattering, ON-currents increase by 8.0, 9.0, 9.5 μA when diameters of CNT increase by 1.25, 1.5, 1.7 nm, respectively.

Figure 19b compares the diameter dependence of the I_{DS}-V_{DS} results of the impact of phonon scattering in coaxial CNTFET of 15 nm length. It is shown that I_{DS}-V_{DS} results at V_{GS} = 0.7 V increase by 8.0, 9.0, 9.5 μA when diameters of CNT increase by 1.25, 1.5, 1.7 nm, respectively. In figure 19b, it is also shown that the impact of phonon scattering in CNTFET decreases for larger diameter tubes.

6. Conclusion

Carbon nanotube field-effect transistors are interesting devices with potentially important applications in nanoelectronics. In this work, we have summarized the current status of the field in terms of fabrication technology and device physics. The rate of progress in CNTFET technology and in the understanding of their device physics has been very rapid. Although uncertainties remain, the dc performance of field-effect transistors can now be explained. During the next few years, we expect to see increased work on other devices, for example, high-speed transistors, optoelectronics devices, and bio-sensors. We are sure to learn a good deal of interesting new device physics in the process and may even discover important technological applications.

7. References

[1] S. Iijima, Helical Microtubules of Graphitic Carbon, *Nature*, Vol. 354, pp. 56-58, 1991.
[2] S. J. Tans, A. R. M. Verschueren, and C. Dekker, Room-temperature transistor based on a single carbon nanotube, *Nature*, Vol. 393, pp. 49-52, 1998.
[3] P. Avouris, J. Appenzeller, R. Martel, and S. J. Wind, Carbon nanotube electronics, *Proceedings of the IEEE*, Vol. 91, pp. 1772-1784, 2003.
[4] P. L. McEuen, M. S. Fuhrer, and H. K. Park, Single-walled carbon nanotube electronics, *IEEE Transactions on Nanotechnology*, Vol. 1, pp. 78-85, 2002.

[5] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and P. Avouris, Carbon nanotubes as Schottky barrier transistors, *Physical Review Letters*, Vol. 89, pp.106801.1-106801.4, 2002.

[6] J. Guo, S. Datta, and M. Lundstrom, A numerical study of scaling issues for Schottky-Barrier carbon nanotube transistors, *IEEE Transactions on Electron Devices*, Vol. 51, pp. 172-177, 2004.

[7] R. Saito, G. Dresselhaus, and M. S. Dresselhau, *Physical Property of Carbon Nanotubes*, Imperial Colledge Press, London, U.K, 1998.

[8] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and P. Avouris, Fabrication and electrical characterization of top gate single-wall carbon nanotube field-effect transistors, *Journal of Vacuum Science & Technology B*, Vol. 20, pp. 2798-2801, 2002.

[9] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. J. Dai, Ballistic carbon nanotube field-effect transistors, *Nature*, Vol. 424, pp. 654-657, 2003.

[10] A. Javey, J. Guo, D. B. Farmer, Q. Wang, E. Yenilmez, R. G. Gordon, M. Lundstrom, and H. Dai, Self-aligned ballistic molecular transistors and parallel nanotube arrays, *Nano. Lett.*, Vol. 4, No. 7, pp. 1319-1320, 2004.

[11] A. Thess, R. Lee, P. Nikolaev, H. Dai, P. Petit, J. Robert, C. Xu, Y. H. Lee, S. G. Kim, A. G. Rinzler, D. T. Colbert, G. E. Scuseria, D. Tomanek, J. E. Fischer, and R. E. Smalley, Crystalline ropes of metallic carbon nanotubes, *Science*, Vol. 273, pp. 483-487, 1996.

[12] J. Kong, H. T. Soh, A. M. Cassell, C. F. Quate, and H. Dai, Synthesis of individual single-walled carbon nanotubes on patterned silicon wafers, *Nature*, Vol. 395, pp. 878-881, 1998.

[13] Sander J. Tans, Alwin R. M. Verschueren, and Cees Dekker, Room-temperature transistor based on a single carbon nanotube, *Nature*, Vol. 393, pp. 49-52, 1998.

[14] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris, Single- and multi-wall carbon nanotube field-effect transistors, *Appl. Phys. Lett.*, Vol. 73, No. 17, pp. 2447-2449, 1998.

[15] Adrian Bachtold, Peter Hadley, Takeshi Nakanishi, and Cees Dekker, "Logic circuits with carbon nanotube transistors," *Science*, Vol. 294, pp. 1317-1320, 2001.

[16] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and Ph. Avouris, Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes, *Appl. Phys. Lett.*, Vol. 80, No. 20, pp. 3817-3819, 2002.

[17] R. Martel, V. Derycke, C. Lavoie, J. Appenzeller, K. K. Chan, J. Tersof, and Ph. Avouris, Ambipolar electrical transport in semiconducting single-wall carbon nanotubes, *Phys. Rev. Lett.*, Vol. 87, No. 25, pp. 256805-1-256805-4, 2001.

[18] Ali Javey, Hyoungsub Kim, Markus Brink, QianWang, Ant Ural, Jing Guo, Paul McIntyre, Paul McEuen, Mark Lundstrom, and Hongjie Dai, High-k dielectrics for advanced carbon-nanotube transistors and logic gates, *Nature Mater.*, Vol. 1, pp. 241-246, 2002.

[19] S. J. Wind, J. Appenzeller, and Ph. Avouris, Lateral scaling in carbon-nanotube field-effect transistors, *Phys. Rev. Lett.*, Vol. 91, No. 5, 058301-1-058301-4, 2003.

[20] J. Appenzeller, J. Knoch, V. Derycke, R. Martel, S. Wind, and P. Avouris, Field-modulated carrier transport in carbon nanotube transistors, *Physical Review Letters*, Vol. 89, No. 12, 126801, 2002.

[21] B. M. Kim, T. Brintlinger, E. Cobas, M. S. Fuhrer, H. M. Zheng, Z. Yu, R. Droopad, J. Ramdani, and K. Eisenbeiser, High-performance carbon nanotube transistors on $SrTiO_3$/Si substrates, *Applied Physics Letters*, Vol. 84, pp. 1946-1948, 2004.

[22] S. Rosenblatt, Y. Yaish, J. Park, J. Gore, V. Sazonova, and P. L. McEuen, High performance electrolyte gated carbon nanotube transistors, *Nano Letters*, Vol. 2, pp. 869-872, 2002.

[23] G. P. Siddons, D. Merchin, J. H. Back, J. K. Jeong, and M. Shim, Highly efficient Gating and doping of carbon nanotubes with polymer electrolytes, *Nano Letters*, Vol. 4, pp. 927-931, 2004.

[24] Z. Yao, C. L. Kane, and C. Dekker, High-field electrical transport in single-wall carbon nanotubes, *Physical Review Letters*, Vol. 84, pp. 2941-2944, 2000.

[25] T. Ando, H. Matsumura, and T. Nakanishi, Theory of ballistic transport in Carbon Nanotubes, *Physica B*, Vol. 323, pp. 44, 2002.

[26] A. Javey, J. Guo, M. Paulsson, Q. Wang, D. Mann, M. Lundstrom, and H. J. Dai, High-field quasiballistic transport in short carbon nanotubes, *Physical Review Letters*, Vol. 92, 106804, 2004.

[27] J. Y. Park, S. Rosenblatt, Y. Yaish, V. Sazonova, H. Ustunel, S. Braig, T. A. Arias, P. W. Brouwer, and P. L. McEuen, Electron-phonon scattering in metallic single-walled carbon nanotubes, *Nano Letters*, Vol. 4, pp. 517-520, 2004.

[28] A. Javey, J. Guo, D. B. Farmer, Q. Wang, E. Yenilmez, R. G. Gordon, M. Lundstrom, and H. Dai, Self-aligned ballistic molecular transistors and parallel nanotube arrays, *Nano Letters*, Vol. 4, pp. 1319-1322, 2004.

[29] R. Seidel, A. P. Graham, E. Unger, G. S. Duesberg, M. Liebau, W. Steinhoegl, F. Kreupl, and W. Hoenlein, High-current nanotube transistors, *Nano Letters*, Vol. 4, pp. 831-834, 2004.

[30] V. Derycke, R. Martel, J. Appenzeller, and P. Avouris, Carbon nanotube inter- and intramolecular logic gates, *Nano Letters*, Vol. 1, pp. 453-456, 2001.

[31] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, Logic circuits with carbon nanotube transistors, *Science*, Vol. 294, pp. 1317-1320, 2001.

[32] D. J. Frank and J. Appenzeller, High-frequency response in carbon nanotube field-effect transistors, *IEEE Electron Device Letters*, Vol. 25, pp. 34-36, January 2004.

[43] J. Appenzeller and D. J. Frank, Frequency dependent characterization of transport properties in carbon nanotube transistors, *Applied Physics Letters*, Vol. 84, pp. 1771-1773, 2004.

[34] S. D. Li, Z. Yu, S. F. Yen, W. C. Tang, and P. J. Burke, Carbon nanotube transistor operation at 2.6 GHz, *Nano Letters*, Vol. 4, pp. 753-756, 2004.

[35] P.J. Burke, Luttinger Liquid theory as a model of the gigahertz electrical properties of carbon nanotubes, *IEEE Transactions on Nanotechnology,* Vol.2, No.1, pp. 129-144, Sept. 2002.

[36] P.J. Burke, An RF circuit model for carbon nanotubes, *IEEE Transactions on Nanotechnology,* Vol.2, No.1, pp. 55-58, March. 2003.

[37] M. Radosavljevic, J. Appenzeller, Ph. Avouris, and J. Knoch, High performance of potassium n-doped carbon nanotube field-effect transistor, *Applied Physics Letters*, Vol. 84, No. 18, pp. 3693-3695, 2004.

[38] A. Javey, R. Tu, D. B. Farmer, J. Guo, R. G. Gordon, and H. Dai, High performance n-type carbon nanotube field-effect transistors with chemically doped contacts, *Nano Letters*, Vol.5, No. 2, pp.345-348, 2005.

[39] M. Kruger, M. R. Buitelaar, T. Nussbaumer, C. Schonenberger, and L. Forro, Electrochemical carbon nanotube field-effect transistor, *Appl. Phys. Lett.*, Vol. 78, No. 9, 1291-1293, 2001.

[40] Sami Rosenblatt, Yuval Yaish, Jiwoong Park, Jeff Gore, Vera Sazonova, and Paul L. McEuen, High performance electrolyte gated carbon nanotube transistors, *Nano Lett.*, Vol. 2, No. 8, pp. 869-872, 2002.

[41] Lars-Erik Wernersson, Tomas Bryllert, Erik Lund, and Lars Samuelson, Wrap-gated InAs nanowire field-effect transistor, *IEDM Tech. Digest*, 273-276, 2005.

[42] Paul Stokes and Saiful I. Khondaker, Local gated single-walled carbon nanotube field effect transistors assembled by AC dielectrophoresis, *Nanotechnology*, Vol. 49, 175202, 2008.

[43] D.L. John, L.C. Castro, J.P. Clifford and D.L. Pulfrey, Electrostatics of coaxial schottky-barrier nanotube field-effect transistors, *IEEE Trans. Nanotech.*, Vol. 2, 175-180, 2003.

[44] G. Pennington and N. Goldsman, Semi-classical transport and phonon scattering on electrons in semiconducting carbon nanotubes, Phys. Rev. B, 68, 045426, 2003.

[45] K. Alam and R. Lake, Performance of 2 nm gate length carbon nanotube field-effect transistors with source-drain underlaps, *Appl. Phys. Lett.*, Vol. 87, pp. 073104, 2005.

[46] A. Verma, M. Z. Kauser, and P. P. Ruden, Ensemble Monte Carlo transport simulations for semiconducting carbon nanotubes, *J. Appl. Phys.*, Vol. 97, pp. 114319, 2005.

[47] T. S. Xia, L. R. Register, and S. K. Banerjee, Calculations and applications of the complex band structure for carbon nanotube field-effect transistors, *Phys. Rev. B*, Vol. 70, pp. 045332, 2004.

[48] A. Svizhenko and M. P. Anantram, Effect of scattering and contacts on current and electrostatics in carbon nanotubes, *Phys. Rev. B.*, Vol. 72, pp. 085430, 2005.

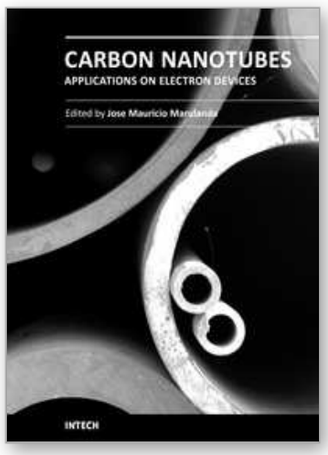
[49] S. Datta, Q*uantum transport: atom to transistor*, Cambridge University Press, Cambridge, UK, 2005.

[50] Dinh Sy Hien, Dinh Viet Nga, Nguyen Thi Luong, Thi Tran Anh Tuan, Modeling of planar carbon nanotube field effect transistor and three dimensional simulations of current-voltage characteristics, *Journal of Physics*, Vol. 187, 012049, UK (8pp), 2009.

[51] Dinh Sy Hien, Nguyen Thi Luong, Thi Tran Anh Tuan, 3D simulation of coaxial carbon nanotube field effect transistor, *Journal of Physics*, Vol. 187, 012061, UK (8pp), 2009.

[52] Dinh Sy Hien, Nguyen Thi Luong, Le Hoang Minh, Tran Tien Phuc, Pham Thanh Trung, Bui An Dong, Huynh Lam Thu Thao, Nguyen Van Le Thanh, Thi Tran Anh Tuan, Huynh Hoang Trung, Nguyen Thi Thanh Nhan, Dinh Viet Nga, Development of quantum device simulator, NEMO-VN1, *Journal of Physics*, Vol. 187, 012088, 2009.

[53] Dinh Sy Hien, Development of quantum device simulator, NEMO-VN2, *Proceedings of fifth IEEE international symposium on electronic design, test and applications, DELTA 2010*, 13-15 January 2010, Ho Chi Minh City, pp. 170-173, 2010.



Carbon Nanotubes Applications on Electron Devices

Edited by Prof. Jose Mauricio Marulanda

ISBN 978-953-307-496-2
Hard cover, 556 pages
Publisher InTech
Published online 01, August, 2011
Published in print edition August, 2011

Carbon nanotubes (CNTs), discovered in 1991, have been a subject of intensive research for a wide range of applications. In the past decades, although carbon nanotubes have undergone massive research, considering the success of silicon, it has, nonetheless, been difficult to appreciate the potential influence of carbon nanotubes in current technology. The main objective of this book is therefore to give a wide variety of possible applications of carbon nanotubes in many industries related to electron device technology. This should allow the user to better appreciate the potential of these innovating nanometer sized materials. Readers of this book should have a good background on electron devices and semiconductor device physics as this book presents excellent results on possible device applications of carbon nanotubes. This book begins with an analysis on fabrication techniques, followed by a study on current models, and it presents a significant amount of work on different devices and applications available to current technology.

INTECH
open science | open minds

InTech Europe
University Campus STeP Ri
Slavka Krautzeka 83/A
51000 Rijeka, Croatia
Phone: +385 (51) 770 447
Fax: +385 (51) 686 166
www.intechopen.com

InTech China
Unit 405, Office Block, Hotel Equatorial Shanghai
No.65, Yan An Road (West), Shanghai, 200040, China
中国上海市延安西路65号上海国际贵都大饭店办公楼405单元
Phone: +86-21-62489820
Fax: +86-21-62489821

IntechOpen