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Bandwidth Extension for Transimpedance Amplifiers

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1. Introduction

This chapter aims to introduce optical receivers in general and application of electronic circuits in these receivers then some important parts of these electronic circuits which are the amplifiers are discussed. An attempt has been made in this chapter to provide some useful information about different aspects of the optical communication in our life and the importance of high speed wideband aspects in such systems. Eventually the role of transimpedance amplifiers in a typical optical communication receiver is discussed.

1.1 Role of fiber optic systems in present-day communication

By growing the number of Internet nodes, the volume of the data transported on the backbone has increased. The load of the global Internet backbone will increase to tens of terabits per second very soon. This indicates that the backbone bandwidth will increase by a factor of 100. Handling of such volumes of data requires suitable media with low loss and high bandwidth. Among the available transmission media, Optical fibers have the best performance for loss and bandwidth. High speed data can be transported over hundreds of fiber without significant loss in signal integrity. These fibers benefit from reduction of cost and performance. The number of the Internet nodes increase with a fast pace, leading to bit rate of a few terabits per second. The bandwidth requirements are growing with fast pace. Applications such as virtual reality will require data rates that are 10,000 times higher than currently available ones [1].

The arrival of cheaper and more powerful personal computers has not only expanded the user base but also created a demand for greater transmission capacity among the telecom networks. In state-of-the-art technology, fiber optic devices and systems are widely employed to satisfy this need for more data throughput economically [2]. Fiber optic communication is an economic solution because its physical nature lets network providers broaden capacity by increasing the transmission bit rate.

Because fiber optics are only communication medium capable of handling such high data rates, there is a widespread demand for high-speed optical and electronic devices, circuits, and systems.

Today possibility of high levels of integration on a single chip enables higher performance. VLSI technologies such as CMOS can now take over the territories of GaAs and InP devices.

1.2 Review of some important optical communication systems

In the past two decades, CMOS technology has dominated the analog integrated circuit design arena, providing low-cost, high performance solutions and. Around 90% of the analog and mixed-signal products in today's semiconductor industry are designed and fabricated in CMOS technologies [1].

Use of CMOS process for fabrication of the electronic system in the optical system lets integration of high-speed front-end circuits and low-speed framers on the same chip. This integration can reduce the package count, board size, and cost of the system.

The two widely accepted commercial systems, SONET OC-192 and OC-768, operate at 10 and 40 Gb/s. The 10-Gb/s CMOS transceiver has already been introduced by a few companies and an extensive amount of research has been performed to improve the design of these systems. However, implementations of the 40- Gb/s CMOS transceivers is behind the 10 Gb/s receivers by a few years because these systems have only become realizable in relatively advanced technologies. In modern fiber optic transmission system, the synchronous optical network (SONET) and synchronous digital hierarchy (SDH) standard define a technology for carrying many signals of different capacities. The basic transmission bit rate is OC-1 at 51.8Mbit/s, and higher bit rates offered by SONET/SDH are summarized in Table 1.1 [2].

SONET	SDH	Bit Rate
OC-1	-	51.84 Mbit/s
OC-3	STM-1	155.52 Mbit/s
OC-12	STM-4	622.08 Mbit/s
OC-48	STM-16	2.4883 Gbit/s
OC-192	STM-64	9.9533 Gbit/s
OC-768	STM-196	39.8131 Gbit/s

Table 1. 1-standard bit rates for optical communication

1.3 A typical optical communication system

Optical communication systems become more important because of the increasing demands for high-speed and large-capacity data communication. The Fig 1.1 and 1.2 show the block diagram of the optical transmitter and receiver system. In this system data are received in the digital form in the optical transmitter side and should be delivered in the digital form in the receiver side. In general in the transmitter data are converted to light using the Laser Diode and delivered to the Optical fiber and in the receiver the data coming from the optical fiber are converted to the electrical signal (current) using the Photo Diode (PD) and amplified using the amplifiers in the receiver.

The transimpedance amplifier (TIA) which converts the photodiode current into a voltage requires high gain, wide bandwidth, low noise and low input impedance with low power consumption.

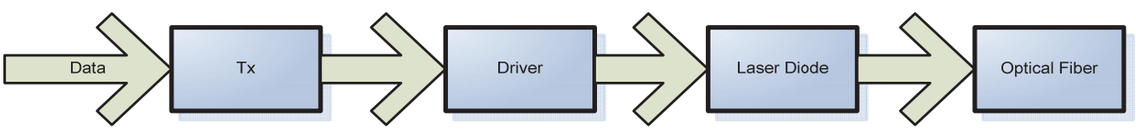

Fig. 1.1 Optical Transmitter Block Diagram

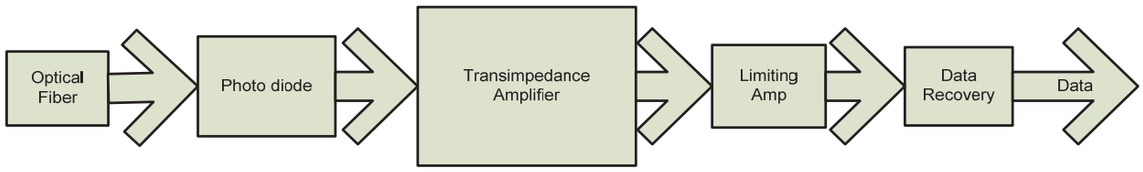

Fig. 1.2 Optical Receiver Block Diagram

An optical receiver must convert a μ A–input current into a digital signal. Furthermore the receiver should use a standard commercial digital CMOS process with little external overhead. In this way the optical receiver can be integrated with a DSP into a single VLSI device. An optical receiver can not be characterized only by its maximum bit rate. The transimpedance of the first stage is an important parameter as well. A high gain transimpedance is necessary when low input currents (a few μ A) must be detected. This is necessary to achieve a high output voltage in the first stage in order to reject noise from sources, such as the digital environment integrated on the same IC [2].

Transimpedance amplifiers play a vital role in optical receivers. Trade-offs between speed, gain, noise and supply voltage exist in TIA design. As TIAs experience a tighter performance envelope with technology scaling at the device level and speed scaling at the system level, it becomes necessary to design the cascade of the TIA, the limiter, and the decision circuit concurrently [1].

As the gain bandwidth product is a measure of both amplification and bandwidth for opamps, the product of the transimpedance (Z) and the bandwidth (BW) should be taken into account in comparison of transimpedance amplifiers. As transimpedance can be exchanged for bandwidth to some extent, a transimpedance-bandwidth-product (ZBW) can be defined for optical receivers.

The transmission of optical data via fiber cables involves electrical-to-optical conversion at the transmission end and optical-to-electrical at the receiving end. These conversion processes are handled by optoelectronic transceiver units that contain electronic devices and semiconductor optical components.

1.4 Transmitting and receiving requirements

In the receiver which is shown in Fig 1.2, the PD converts the received light to a signal current, and the signal swing is amplified to logic levels. Subsequently, the Data Recovery part performs timing and amplitude-level decisions on the incoming signal, which leads to a time- and amplitude-regenerated data stream. The result is then de-multiplexed, thereby reproducing the original channels.

The light-wave traveling through the fiber usually goes under considerable attenuation before reaching the PD. This attenuation requires a subsequent stage to detect and amplify the signal at an acceptable rate. Hence the TIA, the first stage of amplification, should provide wide-band amplification and low input referred noise. To provide the high input sensitivity necessary to receive optical signals weakened by transmitter, the TIA noise must be reduced to a minimum. On the other hand, a high overload tolerance is required to avoid bit errors caused by distortion in the presence of strong optical signals. Furthermore, to ensure stable operation and the required bandwidth, gain can be optimized only within a narrow range. This limitation sometimes causes the output voltage that results from low-power optical signals to be insufficient for further processing. Therefore, the LA often follows to amplify small TIA voltages.

1.5 Technological implementation

In optical communication systems, the front-end of the receiver has a PD and a TIA. Because of the performance requirements for the TIA, the front-end circuit has traditionally used III-V compound semiconductor technologies. On the other hand, their CMOS counterparts, despite having such advantages as low power consumption, high yield that lowers the cost of fabrication, and higher degree of integration, have not performed well enough to survive in such a noisy environment without sacrificing other important attributes. This performance shortcoming is mainly due to the nature of silicon CMOS devices that have limited gain, limited bandwidth. The low voltage headroom in submicron CMOS technologies also is an obstacle to the implementation of broadband amplifiers.

The optical front-end can be realized with monolithic optoelectronic integrated circuits (OEIC) that have all the components in a single chip. In these products, the PDs and circuits are individually optimized, fabricated and packaged in separate processes and connected by external wires. However, the interconnections may cause unwanted parasitic feedback that degrades overall system performance.

1.6 Some important parameters in optical receivers

An optical receiver front-end consists of two major parts, a semiconductor Photo Diode (PD) followed by an electronic signal amplifier. Light traveling through the fiber is attenuated before reaching the PD, thus requiring a highly sensitive receiver to detect the signal. Hence the performance of the receiver is often characterized by the input sensitivity, bandwidth, and gain in the receiver. This sensitivity can be expressed in terms of mean optical input power or root-mean–square (RMS) input-referred noise. Bandwidth is usually determined by the total capacitance contributed by the PD, the preamplifier and other parasitic elements present at the optical front-end.

The fundamental behind the optical to electrical signal conversion is optical absorption. In the operation of the PD, absorbing the incident radiation and in turn generating electron-hole pairs that drift to the metal contacts to generate a current in the external circuit. An equivalent circuit model of the PD is often represented by a current source with a shunt capacitance [2].

Common types of the Photodiode (PD) are p-i-n and avalanche PDs with the types defined based on the photo detection process.

First, the p-i-n consists of a highly resistive middle layer between p and n sections to create a wide depletion region in which a large electric field exists. Most of the incident is absorbed inside i-region thus the drift component of the photocurrent dominates over the slow diffusion component that can distort the temporal response of the PD.

Second, the PD uses an impact ionization mechanism in which an additional multiplication layer is introduced to generate secondary electron-hole pairs that result in an internal current gain. An avalanche PD is often used when the amount of optical power that can come from the receiver is limited, however the avalanche process has major drawbacks in its high noise contribution and in the trade-off between gain and bandwidth.

1.7 Characteristics of transimpedance amplifier

The small photo current generated by the PD must be converted, to a usable voltage signal for further processing. Therefore a preamplifier is used as the first stage and has great

impact on determining the overall data rate and sensitivity that can be achieved in an optical communication system. Typically the preamplifier is required to be able to accommodate wide-band data extending from dc to high frequencies to avoid inter-symbol interference (ISI). These are some parameters which show the performance of the preamplifier and in here we are going to learn about them:

1. Bandwidth
2. Gain
3. Noise
4. Sensitivity
5. BER

As a rule of thumb the amount of BW required for the amplifiers in the receiver side should be 70 percent of the bit rate (BR). For example for an optical receiver to be employed in a 10Gb/s bit-rate system we need to at least have 7GHz bandwidth for the preamplifier.

The Gain required for the preamplifier (TIA) is not defined as a specific value to be mentioned and in the literature, there are a lot of different values achieved for the gain of the TIA but because TIA needs to deliver the voltage to the main amplifier (LA), the input sensitivity of the main amplifier should be satisfied ,therefore normally we need to achieve at least a few mili-volts at the output of the TIA and because we have the amount of the input current as tens or hundreds of micro ampere at the input of the TIA (depend on the optical system) we need to achieve the gain of a few hundreds at least to satisfy the conditions. Normally in the literature the gain of between 40dB-Ohms and 60dB-Ohms has been reported for the recent TIAs.

The sensitivity and noise are related to each other. Since the TIA needs to sense a very small amount of current at the input, the amount of input referred noise should be very low so the amplifier can have a high sensitivity which can sense the very small amount of current.

BER normally in the optical system the amount of BER should be less than 10^{-12} .The definition of BER is the ratio of the number of errors received to the total number of bits. There are some mathematical relations between BER and the BW of the amplifiers in the receiver side which shows if the rule of thumb mentioned above is achieved for the amplifiers in the receiver side the amount of BER will be satisfied.

2. Background and literature review

2.1 Overview

The aim of this chapter is to review some of the previous works which have been done in the TIA area. We aim to discuss the BW extension and review some of the techniques which have been done in the literature to improve the performance of the TIAs.

2.2 BW extension in the TIA design

The general structure for the feedback TIA is shown in the figure below in which we can see that a voltage amplifier with a resistive feedback can be converted to a Transimpedance amplifier [3]. As we can see the light is converted to current using the Photodiode (PD) and then this current is amplified using the TIA and then the voltage signal will be delivered to the main amplifier (Limiting Amplifier).

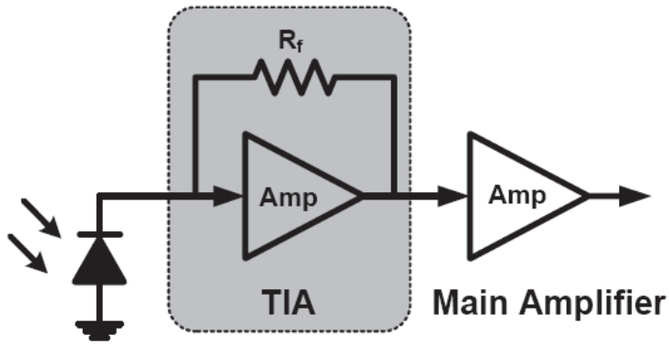

Fig. 2.1 PD, TIA and LA

Now according to the discussion here, there are several obstacles to extend the Bandwidth of a TIA:

1. Photodiode Capacitance (CPD)
2. Inherent parasitic capacitance of the MOS Transistor
3. Loading Capacitance (input capacitance of the main amplifier)

The methods normally we see in the literature on the topic of bandwidth extension are dealing with either of these issues and try to defeat them in some respects and hence extend the Bandwidth of the TIA .There are several bandwidth extension techniques for the TIAs in the literature and in this part we need to discuss these techniques.

For the matter of this discussion we need to define the word bandwidth .The bandwidth is defined as the lowest frequency at which the TIA gain drops by $\sqrt{2}$ or 3dB. Accordingly this bandwidth is often called the 3-dB bandwidth [4].

Some of the techniques which have been done previously in the literature are summarized below.

1. Shunt peaking
2. Series peaking
3. PIP technique
4. Inductor between the stages

2.2.1 Shunt peaking

Shunt peaking is the traditional way to enhance the bandwidth in wideband amplifiers. It uses a resonant peaking at the output of the circuit. It improves the BW by adding an inductor to the output load. It introduces a resonant peaking at the output as the amplitude starts to roll off at high frequencies. Basically what it does is that, it increases the effective load impedance as the capacitive reactance drops at high frequencies [4].

The model for a common source amplifier with shunt peaking is shown in the figure below [5], [16]. As we can see an inductor is added in series with the resistive load and establishes a resonance circuit and reduces the effect of the output capacitance which in this figure consists of all the parasitic capacitances of the drain of the transistor and the loading capacitance of the next stage.

Kromer [7] has used inductive peaking technique in all the 3 stages of the TIA, The main stage is CG but it uses 2 boosting stages in the path of the signal. He could achieve the transresistance gain of 52dB ohms and -3dB BW of 13GHz, although he worked with the technology of 80nm.The amount of Photodiode capacitance he used is 220fF.

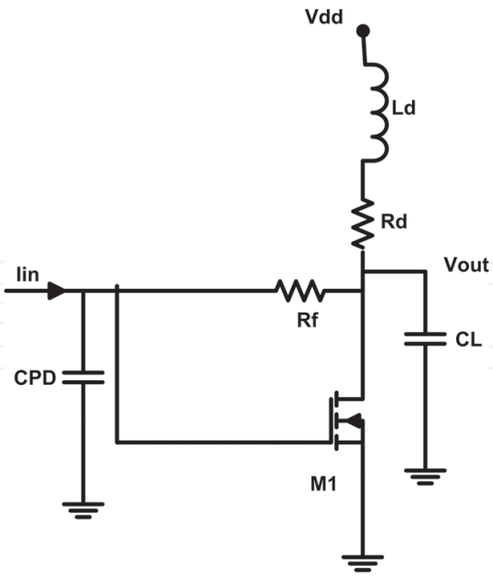

Fig. 2.2 Shunt peaking

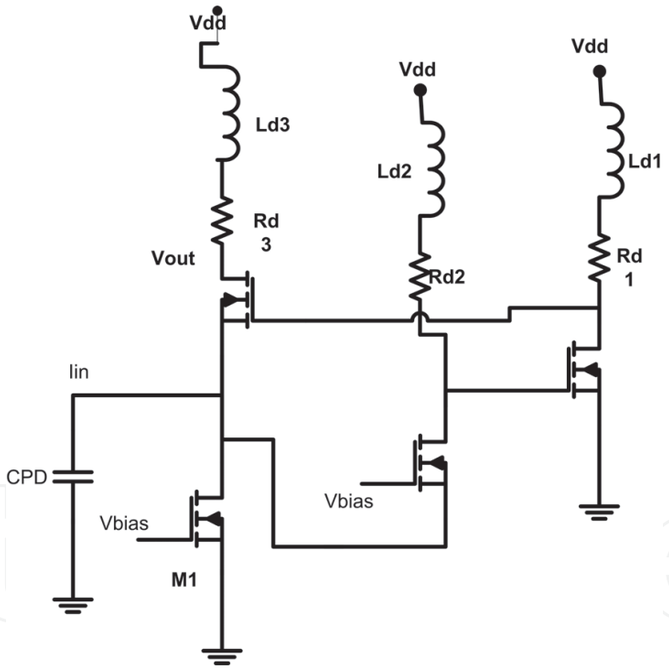

Fig. 2.3 Shunt peaking technique by Kromer

2.2.2 Series peaking

Wu [8] has presented this technique. This technique mitigates the deteriorated parasitic capacitances in CMOS technology. Because the inductor is inserted in series with all the stages in the signal path, it is called series peaking technique. As we can see in the Fig 2.4 the structure of the circuit shows that inductors are used to reduce the effect of the parasitic capacitances in the different stages of the amplifier. As we can see without inductors, amplifier bandwidth is mainly determined by RC time constants of every node.

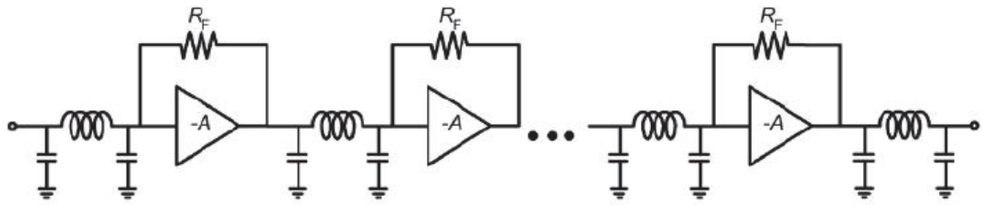

Fig. 2.4 Series peaking technique

This work was done in 0.18um CMOS technology and achieves a gain of 61dB-Ohms and BW of around 7GHz. The amount of PD capacitance in this work is 250fF.

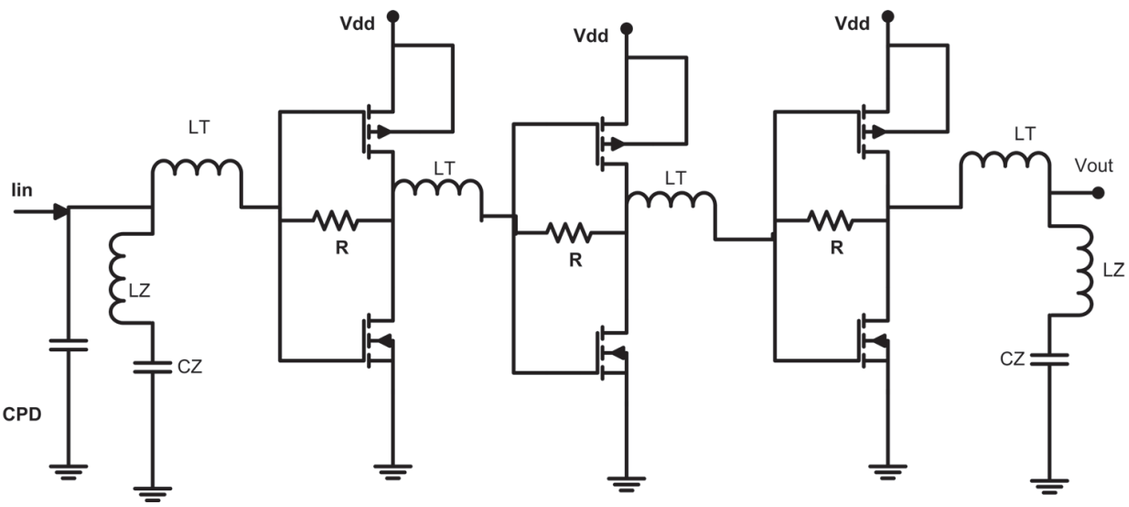

Fig. 2.5 Circuit implemented by Wu

2.2.3 PIP technique

Jin and HSu [9] have proposed this technique to defeat the parasitic capacitances using the combination of several inductors. The combination of the inductors shapes a Π and hence they call it a Pi-type Inductor Peaking (PIP). The Fig 2.6 shows how the combination of 3 inductors in a common source amplifier constructs the PIP technique.

This technique improves the BW of the TIA by resonating with the intrinsic capacitances of the devices. The actual implemented circuit by them is shown in the figure below.

This circuit is done in 0.18 CMOS technology and achieves around 30GHz BW and 51dB-Ohms gain. The amount of PD capacitance in this circuit is the lowest used in the literature and it is 50fF.

2.2.4 Matching inductor between the stages

Analui [10] has mentioned a technique to isolate the effect of parasitic capacitance of different stages to each other. It uses a passive network (inductor) to isolate the effect of capacitors. It has claimed this passive network absorbs the effect of parasitic capacitor of the transistor. This passive network mainly can be an inductor and it can form a ladder filter with the parasitic capacitances of the devices.

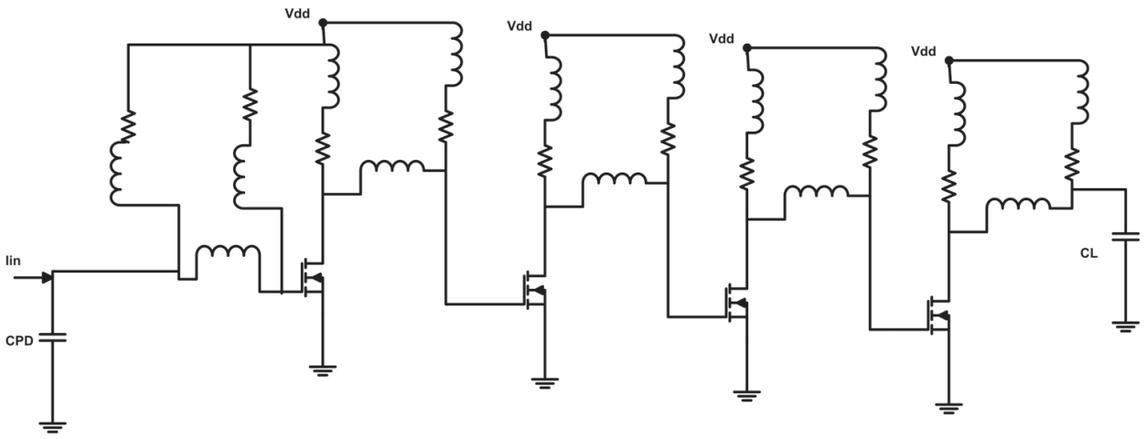

Fig 2.6 Circuit implemented by Jin and HSu

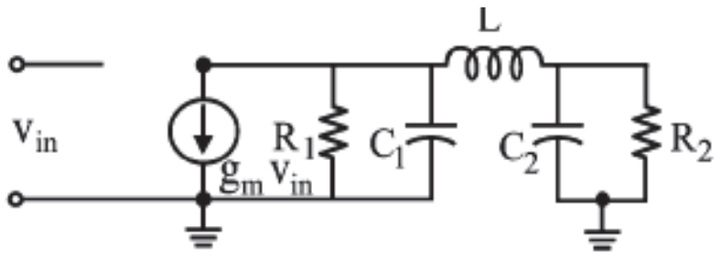

Fig 2.7 Inductor between the stages

The circuit was implemented by Analui. The parasitic capacitances of the devices are shown in the circuit which can form the ladder structure with the deliberately added inductor
He has achieved the gain of 54dB and 3dB BW of 9.2GHz and this work was done in 0.18um BICMOS process using CMOS transistors. The amount of PD in this circuit is 500fF.

2.3 Conclusion

In this chapter we reviewed some of the BW extension techniques available in the literature in the field of TIA design. In general inductive techniques are quite common to extend the BW in the TIAs and researchers have accepted the fact that in order to have wide band circuits. It is worth losing some area in the chip and instead have a better circuit in order to build optical receivers for higher data-rates but still it is a challenge that although it is acceptable to build wideband circuits using spiral inductors, we need to have circuits with fewer number of inductors to have low cost chips.

3. Three stage low power transimpedance amplifier

In this chapter a three-stage Transimpedance Amplifier based on inductive feedback technique and building block of cmos inverter TIA has been proposed. The effects of parasitic capacitances of the MOS transistors and the photodiode capacitance have been mitigated in this circuit [11], [12]. The process of zero-pole cancellation in inductive feedback to extend the BW of the amplifier has been reviewed. To demonstrate the feasibility of the technique the new three stage transimpedance amplifier has been simulated

in a well-known CMOS technology (i.e. 90nm STMicroelectronics). It achieves a 3-dB bandwidth [13] of more than 30GHz in the presence of a 150fF photodiode capacitance and 5fF loading capacitance while only dissipating 6.6mW.

3.1 Introduction

Optical receivers are important in today's high data rate (Gb/s) wireline data communication systems. The requirement for the amplifiers is to be wideband to be able to handle the data. Transimpedance amplifiers (TIAs) at the frontend of the optical receivers do an important job which is the amplification of the current received from the photodiode (PD) to an acceptable level of voltage for the next stage. The bandwidth of CMOS TIAs can be limited by the photodiode (PD) capacitance and parasitic capacitances of the MOS transistors. Bandwidth extension technique essentially is a technique to mitigate the effect of these capacitances in high frequencies when the TIA gain (ratio of the output voltage to input current) starts to roll off. Different circuit techniques for TIAs have been proposed in the past. Shunt peaking is the most well-known technique to enhance the bandwidth of the amplifiers [22]. Multiple inductive series peaking is also a proposed technique for BW extension in the amplifiers [23]. Putting matching networks (inductor) between the stages of the amplifier has been proposed [4]. A Π-type inductor peaking (PIP) technique to enhance the bandwidth of TIAs was recently proposed [24]. Inductive feedback technique [19], [25] has also been applied to extend the BW of TIAs.

The remainder of this chapter is organized as follows: Section 3.2 reviews the inductive feedback technique and the theory of zero pole cancellation for the conventional inverter based TIA [19]. In Section 3.3 the proposed three-stage TIA is introduced. To show the validity of the design simulation results of the circuit and a comparison with other works are shown in Section 3.4. In Section 3.5, conclusions are given.

3.2 Bandwidth extension using inductive feedback technique

This part has been discussed in the previous publication [19] and is reviewed in this paper as the basis for the extension of the work which is discussed in part 3.4 of this paper. The objective of using inductive feedback is to extend the BW of the TIA by deliberately adding a zero to the transfer function of the TIA and hence cancel the dominant pole of the amplifier thereby extending the BW. This can be done by adding an inductor to the feedback path of the TIA. The newly introduced inductor in the feedback path (inductive feedback) adds one zero and one pole to the transfer function of the TIA and by an appropriate design the newly added zero can cancel the dominant pole of the amplifier and hence extend the BW [19]. In order to discuss the technique in detail we consider two TIAs shown in Figures 3.1 and 3.2. In this paper we refer to the circuit in Fig. 3.1 as the TIA with resistive feedback and the circuit in Fig. 3.2 as the TIA with inductive feedback. Fig. 3.3 shows the small signal model of the TIA.

In the small signal model for the TIA we have these definitions:

$$G_m = g_{m1} + g_{m2}\ ,\ r_o = (r_{ds1} \,||\, r_{ds2})$$

$$c_i = c_{gs1} + c_{gs2} + c_{PD}\ ,\ c_f = c_{gd1} + c_{gd2}$$

$$c_o = c_{db1} + c_{db2} + c_L$$

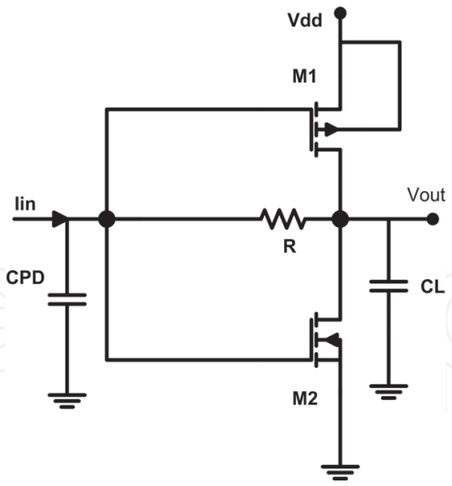

Fig. 3.1 TIA with resistive feedback

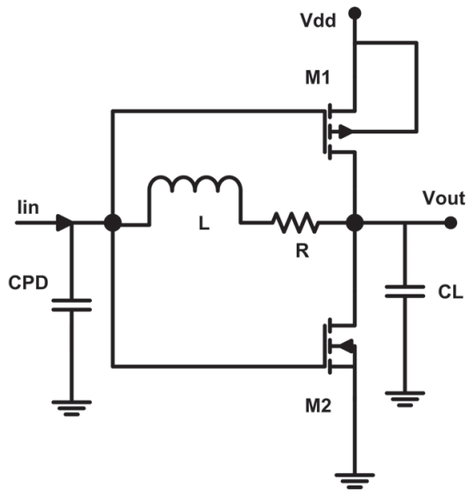

Fig. 3.2 TIA with inductive feedback

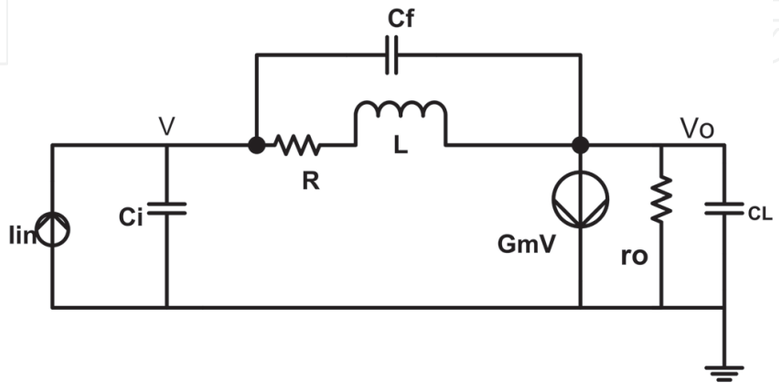

Fig. 3.3 Small signal model of the TIA with inductive feedback

And the transfer function of this circuit is:

$$Z(s) = \frac{as^2 + bs + c}{As^3 + Bs^2 + Cs + D} \tag{1}$$

In which for the case of the Fig. 3.1 (L=0) the coefficients are shown with the index 1 and we have:

$$a_1 = 0\ ,\ b_1 = Rc_f\ ,\ c_1 = 1 - G_m R$$

$$A_1 = 0\ ,\ B_1 = R(c_i c_o + c_f c_o + c_i c_f)$$

$$C_1 = c_i + c_o + R(c_i g_o + c_f g_o + c_f G_m)$$

$$D_1 = g_o + G_m$$

For the case of the circuit in Fig. 3.2 we have the coefficients as (shown with the index 2):

$$a_2 = Lc_f\ , b_2 = R_{c_f} - LG_m\ , c_2 = 1 - G_m R$$

$$A_2 = L(c_i c_o + c_f c_o + c_i c_f)$$

$$B_2 = R(c_i c_o + c_f c_o + c_i c_f) + L(c_i g_o + c_f g_o + c_f G_m)$$

$$C_2 = c_i + c_o + R(c_i g_o + c_f g_o + c_f G_m)$$

$$D_2 = g_o + G_m$$

Now considering the transfer function of the system in Fig. 3.1, the dominant pole of the system (-3db BW) can be approximately calculated as D_1 / C_1.

$$P = \frac{g_o + G_m}{C_i + C_o + R(C_i g_o + C_f g_o + C_f G_m)} \tag{2}$$

In the proposed approach, the dominant pole is cancelled by adding a zero. This can be achieved by adding an inductor in the feedback path of the amplifier giving the circuit in Fig 3.2. As we can see adding an inductor to the feedback path adds one pole and one zero to the transfer function and the newly added zero is approximately:

$$Z = \frac{R}{L} \tag{3}$$

By a judicial choice of the inductance we can cancel the dominant pole of the circuit in Fig. 3.1 which determines the -3db BW and hence extend the BW. An approximate value for the amount of the inductor can be calculated by solving the equation P=Z, giving

$$L = \frac{R(C_i + C_o) + R^2(C_i g_o + C_f G_m)}{g_o + G_m} \tag{4}$$

3.3 Zero-pole cancellation process

The zero-pole analysis in this part has been taken from the previous publication [19] and is reviewed to show the theory for the extension of the work in part 3.4. The circuit has been simulated using a well-known sub-micron CMOS technology (i.e. 90nm CMOS STMicroelectronics). Simulations are done with a single supply (i.e. Vdd=1.2 V) and in the presence of a 150fF photodiode capacitance and 5fF loading capacitance. The pole-zero analysis outlined here was done using the schematic of the circuit with ideal inductor values to show the process of zero-pole cancellation more clearly. Based on the pole-zero analysis for TIA with resistive feedback the circuit has two poles and one zero. The poles are located in the LHP of the s-plane which shows the circuit is stable. The TIA with inductive feedback will have two zeros and three poles. By choosing the inductor according to (4) we can cancel the dominant pole leaving a pair of complex conjugate poles in the circuit. The circuit after having cancelled the single dominant pole will have two complex conjugate poles with a damping factor and natural frequency which can be designed for the desired frequency response. The zero-pole cancellation process has been shown and we can see that by changing the value of the inductor in the circuit the newly added zero is moving towards the dominant pole of the circuit. In the end it reaches to that pole and cancels it and hence this zero can extend the -3dB BW. We can also see that the positions of the complex conjugate poles [14] are changing by sweeping the value of the inductor. The actual values of the poles and zeros extracted from the simulation are shown in Table I.

L(nH)	Zeros (GHz)	Poles (GHz)
0	192.2	-12.7 -22
2	-27.3 223.4	-14.6 -17±17.9j
2.5	-21.8 224.2	-14.9 -13.6±17j
3	-18.1 224.8	-15.2 -11.4±16j
3.5	-15.5 225.2	-15.5 -9.8±15j

Table 3.1 Pole -Zero analysis for the circuit

3.4 Proposed three-stage TIA using the inductive feedback technique

In this part the new proposed TIA is discussed. Cascaded amplifiers are one of the ways to widen the bandwidth of the amplifiers [3], [17] and therefore, we can cascade the previously

discussed single stage transimpedance amplifier to get more Gain*Bandwidth from the amplifier. In this part we introduce the new three stage cascaded TIA using inverter based TIA with inductive feedback. In Figure 3.4 the new transimpedance amplifier has been shown.

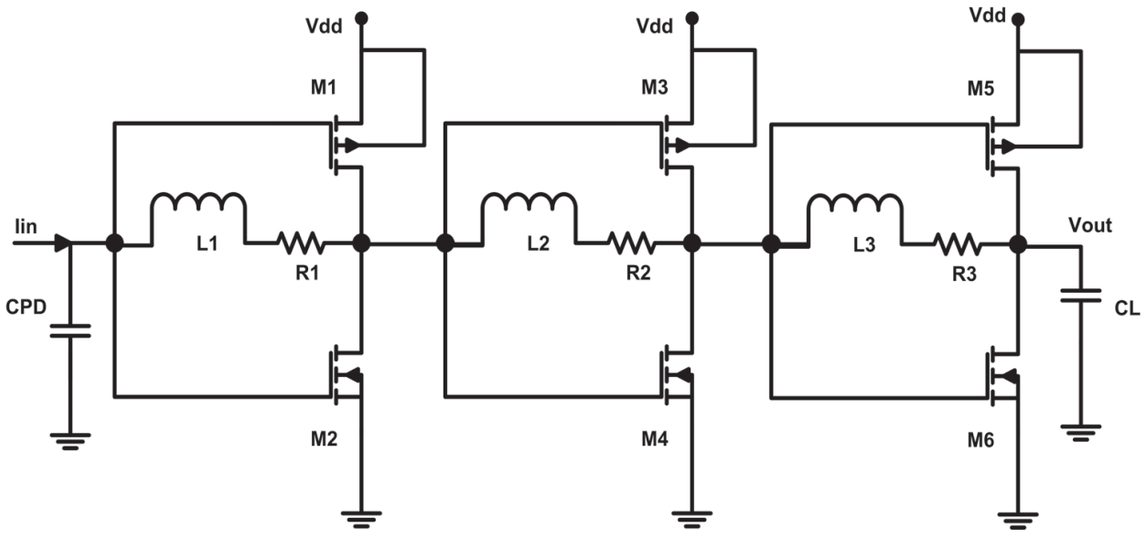

Fig. 3.4 Three stage inverter based TIA with inducitve feedback

In Figure 3.5 the simulation results based on different values of the inductors have been shown. The frequency response of the three-stage TIA has been summarized in table 3.2 as well. In order to fabricate the circuit in sub-micron CMOS spiral inductors are needed [15].In the table the size of the transistors are all 12/0.1(um/um) and the resistor in the feedback path is 400Ohms. The frequency response of the three stage transimpedance circuit for different values of the inductor has been shown in Figure 3.5.

The frequency response of the three-stage transimpedance amplifier has been summarized in table 3.2. For different values of the three inductors for each stage in the table the amounts of the -3dB Bandwidth and gain peaking have been shown. Table 3.3 gives a comparison of this work with other previously published works using other techniques and the new Transimpedance amplifier simulation results together with the other works in the literature has been summarized. As we can see the advantage of this work is to offer high bandwidth consuming very low power consumption in comparison with other previously published works.

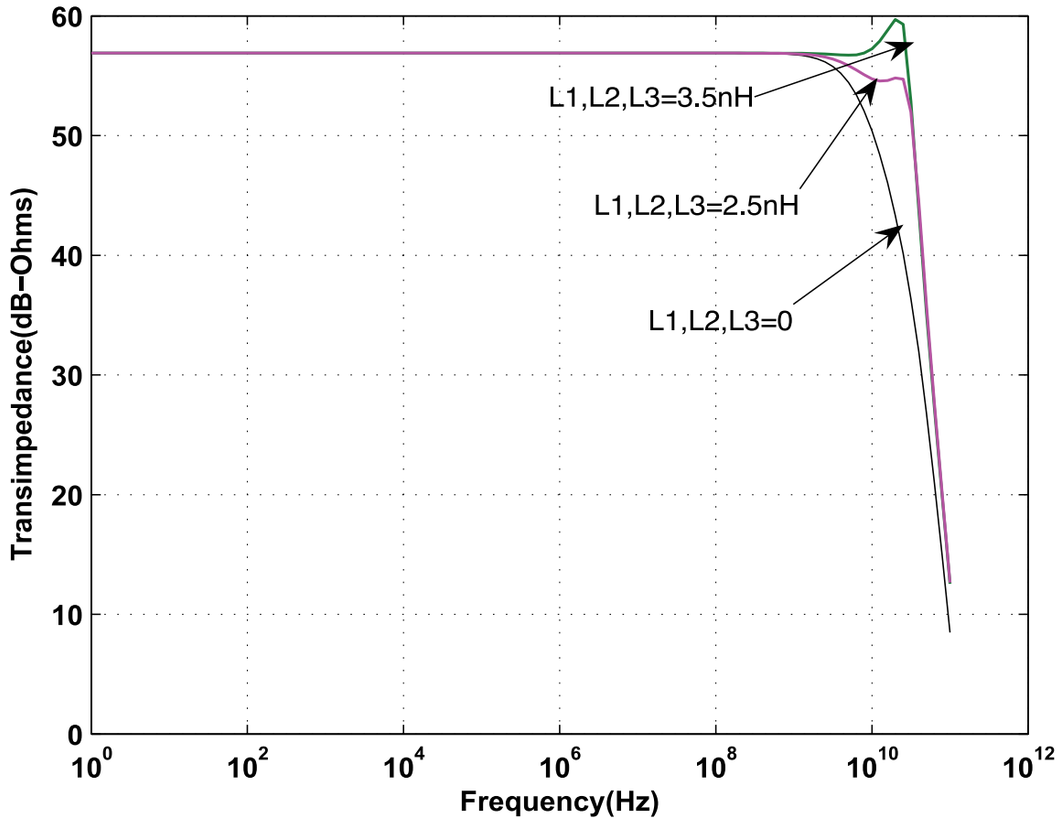

Fig. 3.5 Frequency response of the three stage TIA

Transistor size (um/um)	Resistors(Ohms) R1,R2,R3	Inductors(nH) L1, L2, L3	TIA-Gain (dB-Ohms)	-3dB BW (GHz)	Peaking (dB)
12/0.1	400	0	56.89	5.6	0
12/0.1	400	2.5nH	56.89	27.2	0
12/0.1	400	3.5nH	56.89	30.5	2.4

Table 3.2 Frequency response of the three stage TIA with PD=150fF

	Technology	TIA Gain (dB-Ohm)	-3 dB BW(GHz)	$i_{n,in}$ (pA/√Hz)	Power (mW)	Number of Inductors	PD Cap (fF)
This work	90nm- CMOS	56.8	30.5	36.4	6.6	3	150
Design[5]	90nm- CMOS	50.8	16.7	16.9	2.2	1	150
Design[2]	180nm-CMOS	61	7.2	8.2	70.2	9	250
Design[3]	180nm-BiCMOS	54	9.2	17	137.5	4	500
Design[4]	180nm-CMOS	51	30.5	34.3	60.1	15	50
Design[6]	65nm-CMOS	8	29	N/A	6	1	N/A
Design[7]	80nm-CMOS	52.8	13.4	28	2.2	3	220
Design[8]	180nm-CMOS	62.3	9.0	N/A	108.0	2	150

Table 3.3 Performance of the new TIA and comparison with state of the art

3.5 Conclusion

In this chapter we briefly reviewed bandwidth extension techniques for TIAs and the single stage inverter based transimpedance amplifier using inductive feedback technique has been discussed. The new three stage inverter based TIA using inductive feedback was introduced and the simulation results for the new TIA have been discussed in detail and comparison with the other previously published works has been done.

3.6 Acknowledgements

The tools and design kits were provided by CMC Mircosystems in Concordia University.

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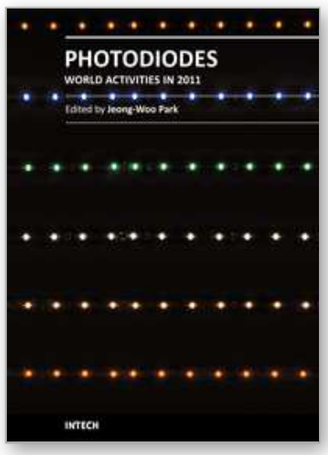

Photodiodes - World Activities in 2011

Edited by Prof. Jeong Woo Park

ISBN 978-953-307-530-3
Hard cover, 400 pages
Publisher InTech
Published online 29, July, 2011
Published in print edition July, 2011

Photodiodes or photodetectors are in one boat with our human race. Efforts of people in related fields are contained in this book. This book would be valuable to those who want to obtain knowledge and inspiration in the related area.

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

Omidreza Ghasemi (2011). Bandwidth Extension for Transimpedance Amplifiers, Photodiodes - World Activities in 2011, Prof. Jeong Woo Park (Ed.), ISBN: 978-953-307-530-3, InTech, Available from: http://www.intechopen.com/books/photodiodes-world-activities-in-2011/bandwidth-extension-for-transimpedance-amplifiers

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