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Active Pixel Sensor CMOS Operating Multi - Sampled in Time Domain

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1. Introduction

CMOS image systems have receiving great attention from industry and academy due to the growing demand for compact and low power image systems. Compared to charge-couple device CCD, CMOS image sensors presents as advantage higher integration capability. In general, CCD achieve better performance due to its particular fabrication process, however, they require high operation voltage and cannot be easy integrated with CMOS circuits that compound cameras. In last decades, the CMOS imager sensor technology has been improving and they are being used in several applications as multimedia and biomedicine (Fossum, 1997, Hosticka, 2003, Sandage, 1995).

Dynamic range is one of the most important merit figure of image sensors. It is defined as the ratio between the maximum and minimum signal acquired. External scenes present dynamic range higher than 100dB but conventional CMOS image sensors and CCDs shows dynamic range about 60dB. Therefore, they are not able to capture properly external images. However, several researchers proposed different CMOS image sensors architectures with high dynamic range (>80 dB) (Stoppa, 2002, Trepanier, 2002, Yadid-Pecht, 2003, Yang, 2002, Yasuda, 2003, Saffih, 2007).

An attractive high dynamic range architecture approach is the digital pixel sensor (DPS) (Kleinfielder, 2001). This architecture is composed by a ramp digital converter and an 8 bit memory integrated per pixel. The main advantage of this approach is the high frame rate operation however, it presents as disadvantage low fill factor. Different architectures based on DPS were proposed (Doge, 2002, Kitchen, 2004, Qi, 2004). Time-domain DPS were proposed in (Bermak, 2006) and (Chen, 2006). They are characterized by the measurement of fall time of photodiode´s voltage. In general, time-domain DPS architectures integrate a comparator and a 8 bit counter in each pixel. The main disadvantage of this approach is the low fill-factor due to the great number of transistors integrated per pixel. A time-domain imager with only 10 transistors per pixel was proposed in (Lai, 2006). A pipeline operation is proposed in order to achieve high dynamic range. However this approach requires the use of two ramp, one at beginning and other at the end of the integration time reducing the sensitivity at middle range of illumination.

A sampled time-domain CMOS imager was proposed in (Campos, 2008). This pixel architecture is composed by a clocked comparator and a dynamic D flip-flop integrated per pixel. The number of transistor integrated per pixel is still significantly and the fill-factor is low. However the sampling in time-domain concept proposed suggest that the comparison

can be performed outside pixel lowering at maximum the number of transistors integrated per pixel. In this chapter the multisampling time-domain CMOS imager is described.

2. Principle of operation

Most of CMOS imagers operate in voltage domain. However, one disadvantage of this operation mode is that the dynamic range small (<60dB). In this operation mode, the photodiode is charge reversely to V_{dd} voltage by controlling a reset transistor as shown in Fig. . This operation is called reset. After the reset time, the reset transistor "open" and the photodiode, in high impedance, starts to discharged. The period of discharge is called integration time. After certain integration time the photodiode´s voltage is sampled and digitalized.

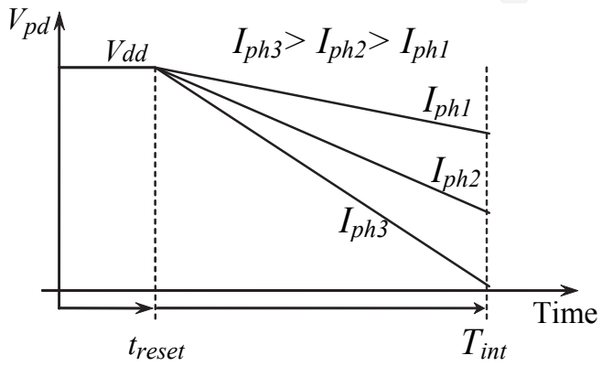


Fig. 1. Photodiode operating in integration mode

During the integration time, the photodiode´s voltage is usually linearized and given by

$$V_{pd} = V_{reset} - S \cdot L_I \cdot t \tag{1}$$

where V_{pd} is the photodiode voltage, V_{reset} is the initial reverse voltage, S is the sensitivity, L_I is the light intensity and t is time.

Time-domain CMOS imagers were proposed as a technique to obtain a CMOS imager with high dynamic range. Time-domain operation is based on fall time of photodiode voltage. The photodiode voltage is compared to a reference constant voltage and the fall time is measured from integration time beginning to the instant of comparison as shown in Fig. 2a. Each fall time is related to a different light intensity.

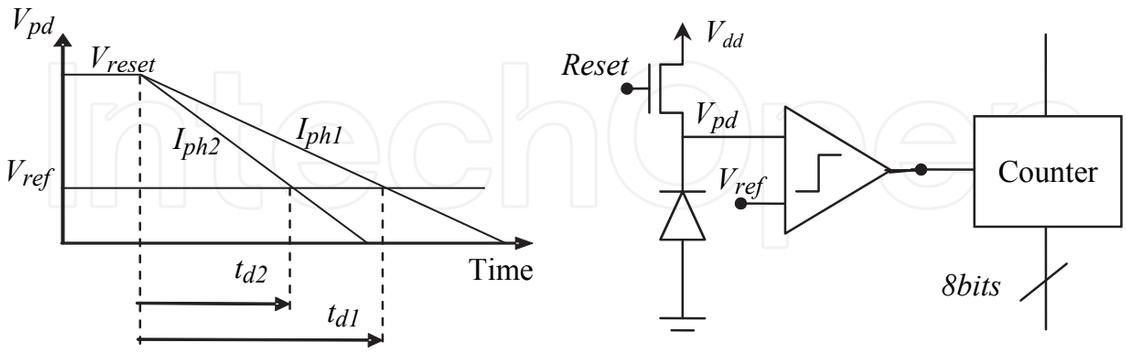
Fig. 2b shows typical pixel architecture of time-domain imagers. A comparator and a counter are integrated per pixel. The counter starts the count in the beginning of integration time. The comparator output signal goes high in the comparison instant stopping the counting. Assuming that the photodiode voltage decrease linearly, the instant of comparison or comparison time is given by

$$t_d = \frac{V_{reset} - V_{ref}}{S \cdot L_I} \tag{2}$$

where V_{reset} is the initial photodiode voltage, V_{ref} is the reference constant voltage, S is the sensitivity and L_I is the light intensity.

In time-domain the dynamic range is given by

$$. DR = 20log\left(\frac{L_{Imax}}{L_{Imin}}\right) = 20log\left(\frac{t_{dmax}}{t_{dmin}}\right) \quad (3)$$



(a) (b)

Fig. 2. Time-domain imager (a) main signals and (b) typical pixel architecture

According equation (3), operation with high dynamic range (>100dB) requires long maximum integration time (t_{dmax}) leading to low frame rates. In order to reduce the maximum time it has been proposed to vary the reference voltage, usually as a ramp voltage (Fig. 3). As one can see in Fig. 3 the comparison time is reduced when the reference voltage is varied as a ramp.

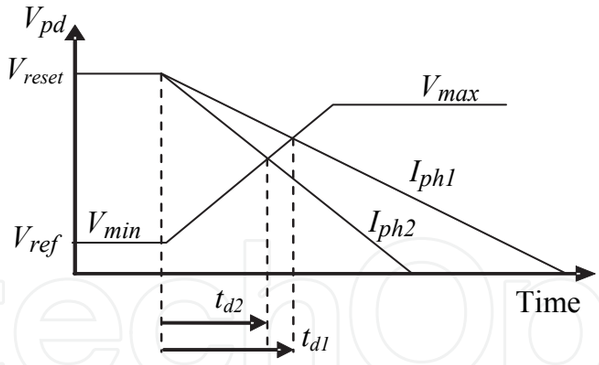


Fig. 3. Time-domain imager main signals using ramp reference

For ramp voltage reference the discharge time is given by

$$t_d = \frac{\left(V_{reset} - V_{min}\right) \cdot T_{int}}{\left(V_{max} - V_{min}\right) + S \cdot L_I \cdot T_{int}} \quad (4)$$

Fig. 4 shows the transfer curve td versus L_I for constant reference voltage and ramp reference voltage. It was assumed V_{reset}=3.3, V_{ref}=1.5, S=3.6·10^{+6}, V_{max}=3V,V_{min}=0.3V and T_{int}=1s. One can see that the ramp reference voltage reduce the time discharge at lower light intensities. However, the compression becomes higher at low light intensities making difficult to discrete.

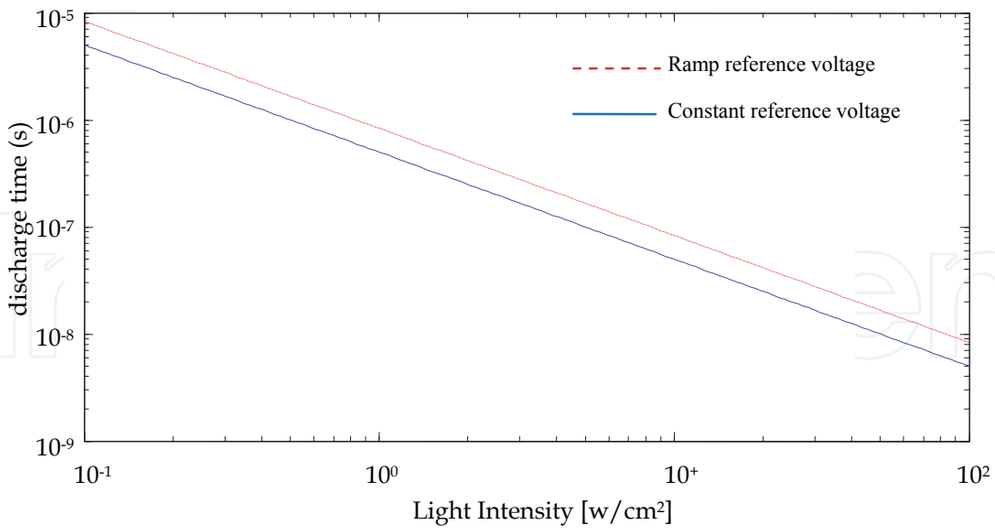


Fig. 4. Discharge time characteristic

Multisampled time-domain CMOS imagers are time-domain imagers in which the comparison result is sampled. The comparison result is sampled where each instant of sample is coded. The first time in which the sample indicated that a comparison occurs determines the code related to that comparison time or light intensity incident. Fig. 5(a) shows the main signals for regular interval sampling time T_i. For a given integration time T_{int} the regular interval sampling time is given by $\Delta T_s = T_{int}/2^N$ where N is the total number of bits.

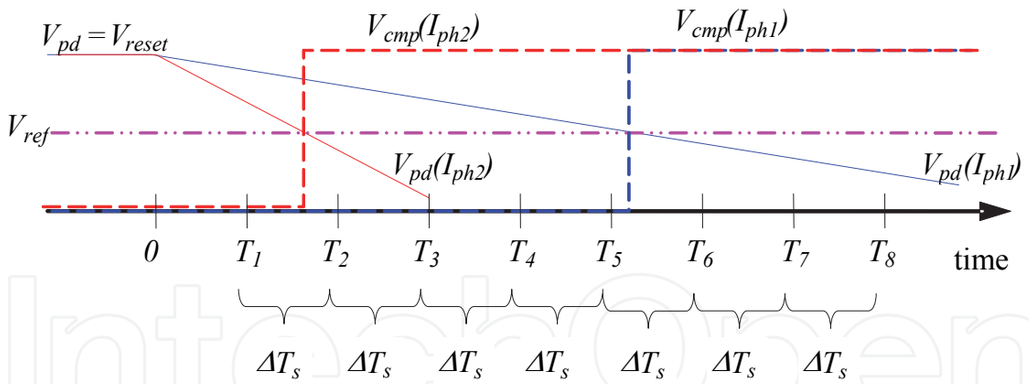


Fig. 5. Sampling in regular interval time.

In this case the dynamic range is given by

$$DR = 20log\left(2^N\right) \tag{5}$$

In this case the dynamic range for N=8 is 48.16dB, for N=10 is 60 dB and for N=12 is 72dB. As one can see, in order to achieve high dynamic range (100dB) is needed more than 16 bits. Therefore, the high number of the bits required by this approach is a disadvantage. However, the sampling can be non linear as shown in Fig. 6. The interval time can be varied logarithmic (Fig. 6a) or a combination of linear and log (Fig. 6b). The number of bits required can be reduced applying non-linear sampling intervals.

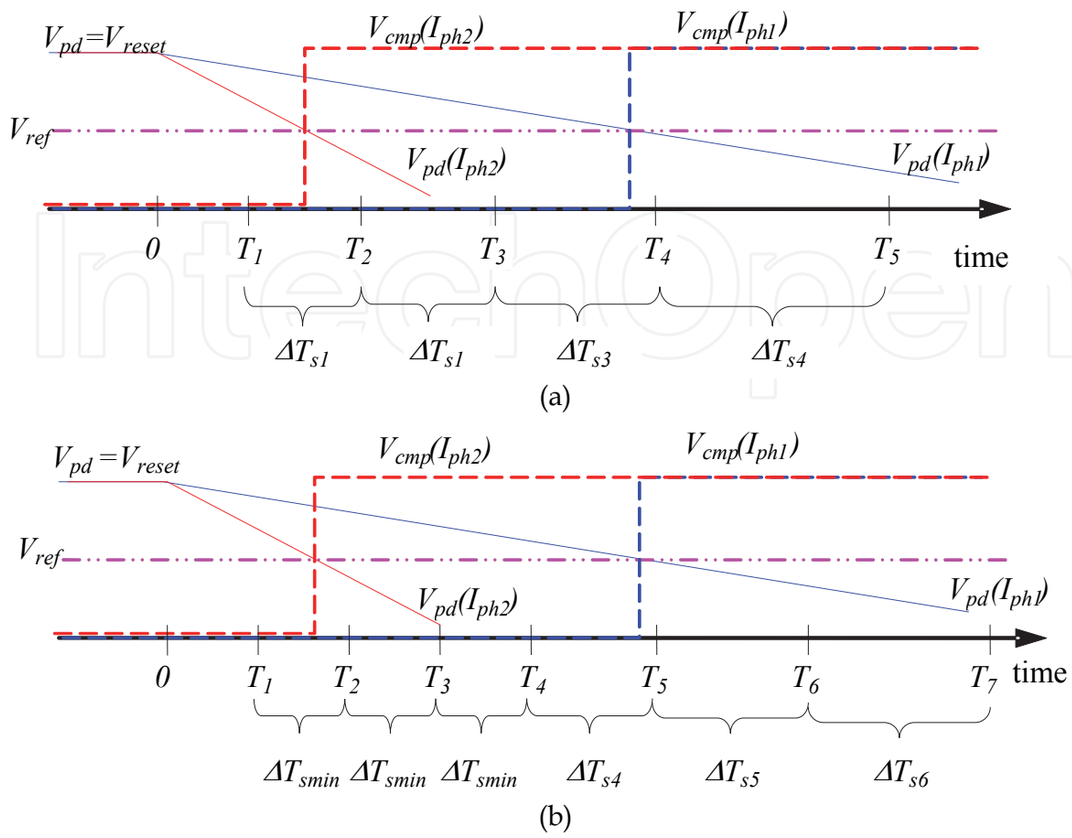


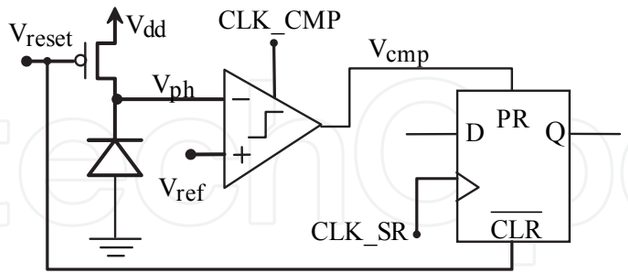
Fig. 6. Sampling in (a) logarithmic interval times (b) linear-logarithmic interval times

3. Pixel architecture

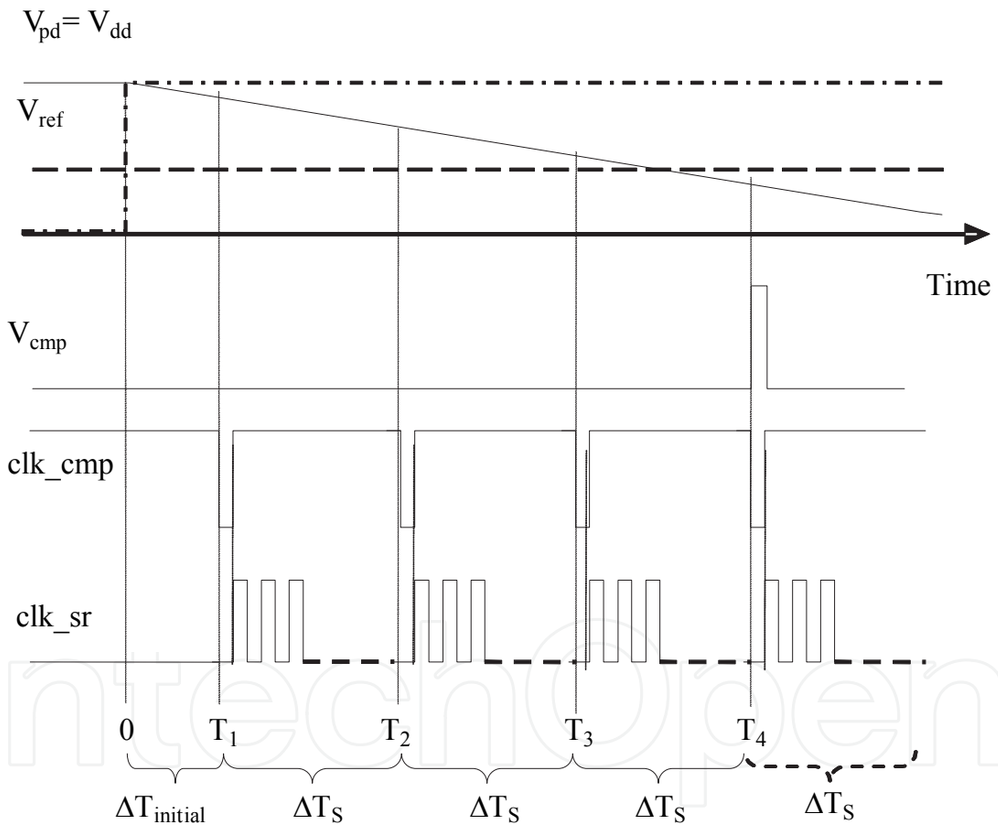
Fig. 7a shows the block diagram of the pixel architecture proposed in (Campos 2008). The pixel is composed of a photodiode, the reset transistor, a comparator type of clocked flip-flop and a D-type with asynchronous inputs (PR and CLR). The clocked comparator type offers operating speed and timing between the pixels of the array. The D-type flip-flop are used to store the comparison result and they are connected together forming a shift register for serial line per row. The serial shift register allows reading outside of the comparison result by means of shifting the data using the clock signal (clk_sr) of the shift register. Fig. 7b shows the timing diagram of the main control signals of the system. The reset signal is responsible for activating the reset transistor and loading the initial photodiode voltage V_{reset} and simultaneously activates the CLR input initializing the flip-flop with Q = 0. The clock signal (clk_cmp) of the comparator determines the moment of performing the comparison, while the sampling interval (T_s). Note that the comparison occurs simultaneously in all pixels in the array.

In the sampling instants (T_s) in which $V_{fd} < V_{ref}$, the output signal of the comparator (V_{cmp}) normally remains low and the value in the flip-flop remains at 0 because in this case PR = 0. In the sampling instants in which $V_{fd} < V_{ref}$, the output signal of the comparator (V_{cmp}) determines PR = 1 and hence the state in the flip-flop to go high (Q = 1). Thus, as a result of the comparison, the state Q = 0 indicates $V_{fd} \geq V_{ref}$ while the state Q = 1 indicates $V_{fd} \leq V_{ref}$.

The D flip-flops of the pixels on each row are connected together to form a shift register on line. The shift register for serial line allows you to read outside of the comparison results by means of shifting the data using the clock signal (clk_sr) of the shift register.



(a)



(b)

Fig. 7. Architecture´s (a) block diagram and (b) control signals

Fig. 8 shows the block diagram of the system architecture proposed for an imaging system in which the sampling results and subsequently its encoding is performed externally. The data from the shift registers are provided in the input multiplexer whose number of output bits is PO.

The discharge time of the voltage signal from the photodetector is associated with the first moment of the comparison sample (T_S) at which the comparison result is positive (Q = 1). Offering only a memory 1bit per pixel, the array reading should be performed after each sample without exceeding the time interval between samples (ΔT_S). Whereas the operating frequency of the multiplexer ($1/T_{mux}$) is greater than the operating frequency of shift registers, the total time for reading the array (T_m) can be defining as:

$$T_m = T_{clk\_cmp} + \left(\frac{n_L \cdot n_C}{PO} \right) \cdot T_{mux} \tag{6}$$

where $n_L x n_C$ is the dimension of the array of pixels, PO is the number of bits in the output of the multiplexer, T_{clk_cmp} is the time to compare and t_{mux} is the period of operation of the multiplexer.

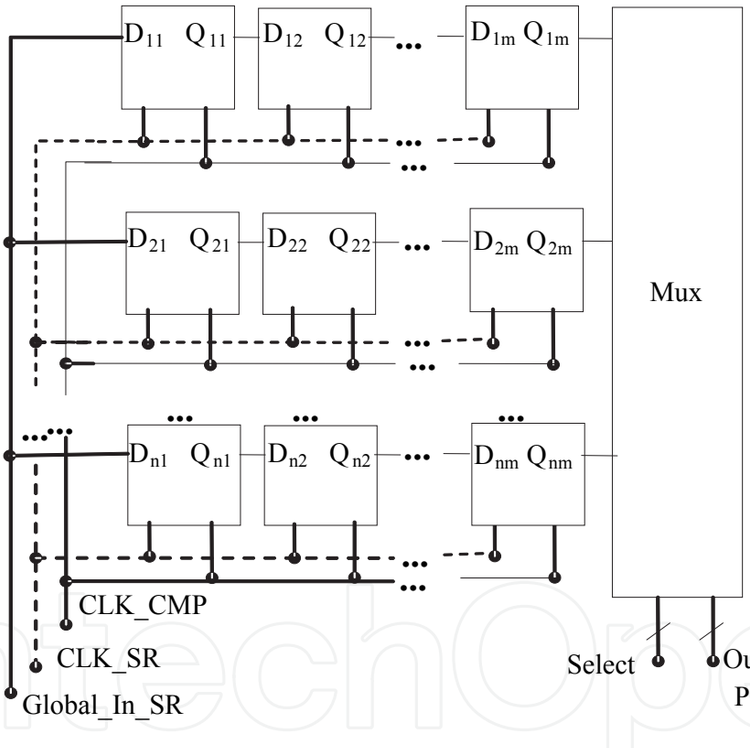


Fig. 8. Array block diagram

The total read time of the matrix (T_m) must be less than the intervals between samples (ΔT_S). The dimensions of the matrix and the operation speed of the circuit determine the array time reading. Thus, the limit of operation of the system depends on the size of the array, the speed of circuit operation, the number of bits that determines the time interval between samples (number of bits of the image) and the number of bits read in parallel at the output multiplexer. Assuming that sampling is performed at regular intervals, the interval between samples will be $T_{int}/2^N$ where T_{int} is the maximum integration time and N is the number of

bits of the image. Fig. 9 shows the total time given by equation (6) depending on the size of a square matrix DXD for different number of output PO, considering typical times of 100ns to 5ns and operating times of the comparator (T_{clk_cmp}) and multiplexer (t_{mux}) respectively. Fig. 9 also shows the intervals between sampling (ΔT_S) for 8-bit image and 10bits. It can be seen in Fig. 9 the maximum dimensions of the matrix in which to operate within the limit $T_m < \Delta T_S$.

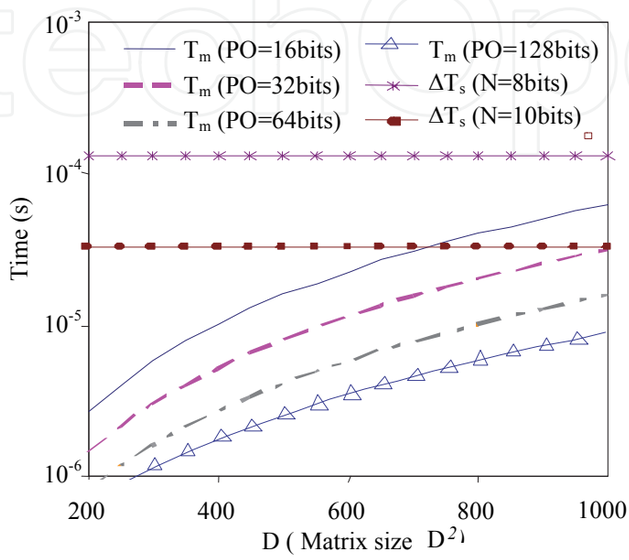


Fig. 9. Time Reading

Assuming operation rate of 30 frames/second or a total time of integration (T_{int}) of 33.33 ms, the interval between samples of linear $\Delta Ts = T_{int}/2^N$ is approximately 130 μ s for 8 bit images and 32 μ s for 10bits images. Note that once defined the technology and dimensions of the array of pixels, the choice of the number of output bits (DB) has a fundamental role in limiting the maximum frame rate. The CMOS imaging system proposed could be constructed with VGA resolution (580x640) capturing images of 10 bits considering output of 16bit. However in order to achieve dynamic range higher than 90dB it is need operates with images of 16bits or higher.

4. Fill-factor

Fig. 10 shows the comparator topology. The comparator is a typical clocked comparator composed by a low gain first stage followed by a decision circuit as a second stage. The clocked comparator make possible to sample the comparison result at sampling instant.
There are two stages of operation, the track and latch phases. In track stage, the switch M13 is closed and the output has low gain. The role circuit operates as a differential gain stage. Fig. 11 shows simulations results of the output voltage (drain of M09 and M10) as a differential voltage is applied to input. As one can see, the resolution is about 2mV and the maximum differential output voltage is about 0.6V. Simulations were performed using model of 0.35 um technology. The transistors sizes are show in table 1.

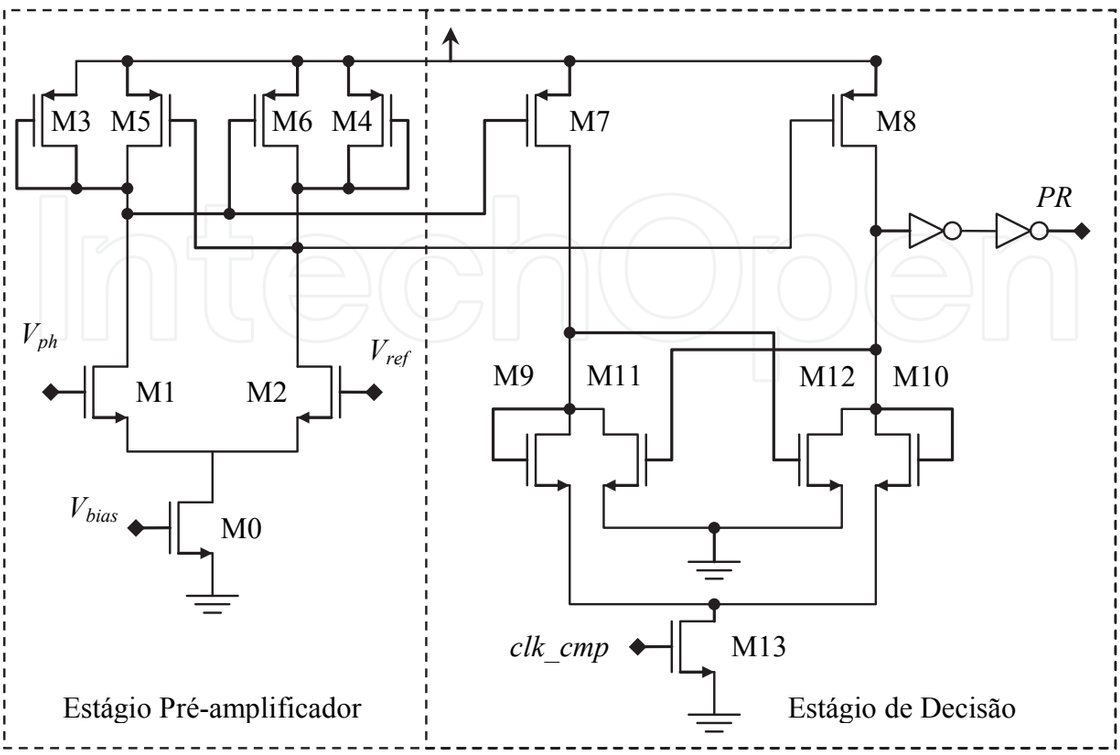


Fig. 10. Topology of clocked comparator

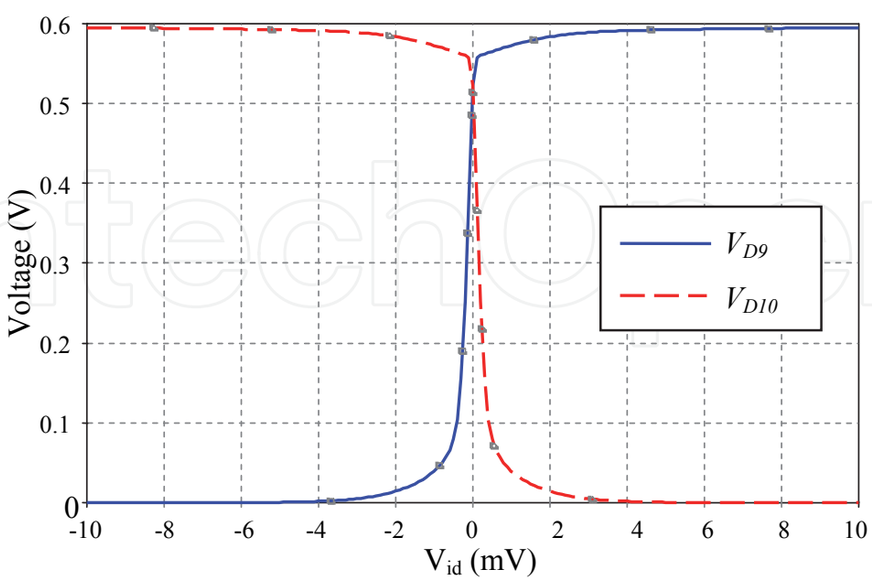


Fig. 11. Output voltage of comparator in track stage.

M0	2μm/2μm
M1= M2	2μm/1μm
M3=M4=M5=M6=M7=M8	0,8μm/0,4μm
M9=M10=M11=M12=M13	0,4μm/0,35μm

Table 1. Transistors sizes used in simulations.

After the track stage, the M13 operating as switch is opened beginning the latch stage. In latch stage M9 and M10 are disconnected and M7, M8, M11 and M12 compose a latch circuit. The initial differential voltage (0,6V on Fig. 11) is then amplified by latch circuit to logic voltage levels. Two inverters were used at output to ensure logic levels even during track stage.

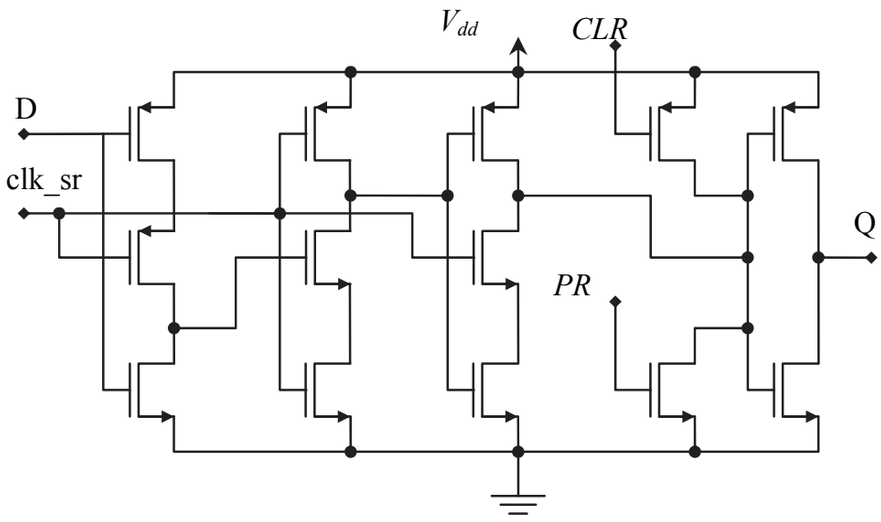


Fig. 12. Topology of dynamic D flip-flop with preset and clear

Fig. 12 shows the D flip-flop topology. The D flip-flop topology is a dynamic flip-flop with preset and clear. The dynamic topology was chosen instead the static topology in order to reduce the total number of transistor required. Simulations results in Fig. 13 show the main propagation delays using load of 50fF. All transistor of D flip-flop are minimum sizes.

As one can see there are 22 transistors integrated per pixel (Figs. 7(a), 10 and 12). The prototype presented in (Campos, 2008) shows only 16% of fill-factor. However, it is possible to implement other pixel architecture using the multisampling in time-domain technique in order to reduce the number of transistor integrated per pixel and to increase the fill-factor.

The pixel architecture showed in Fig. 14 is proposed here as an alternative to pixel architecture showed previously proposed in (Campos, 2008). The pixel is the typical 3T architecture. It is composed by a buffer (source follower) between the photodetector and the transistor select. The transistor select isolates the pixel from bus column and make possible to select the pixel line that must be read outside matrix. Also, there is a reset transistor. The comparator is integrated per column outside pixel. In this case the fill-factor becomes maximized.

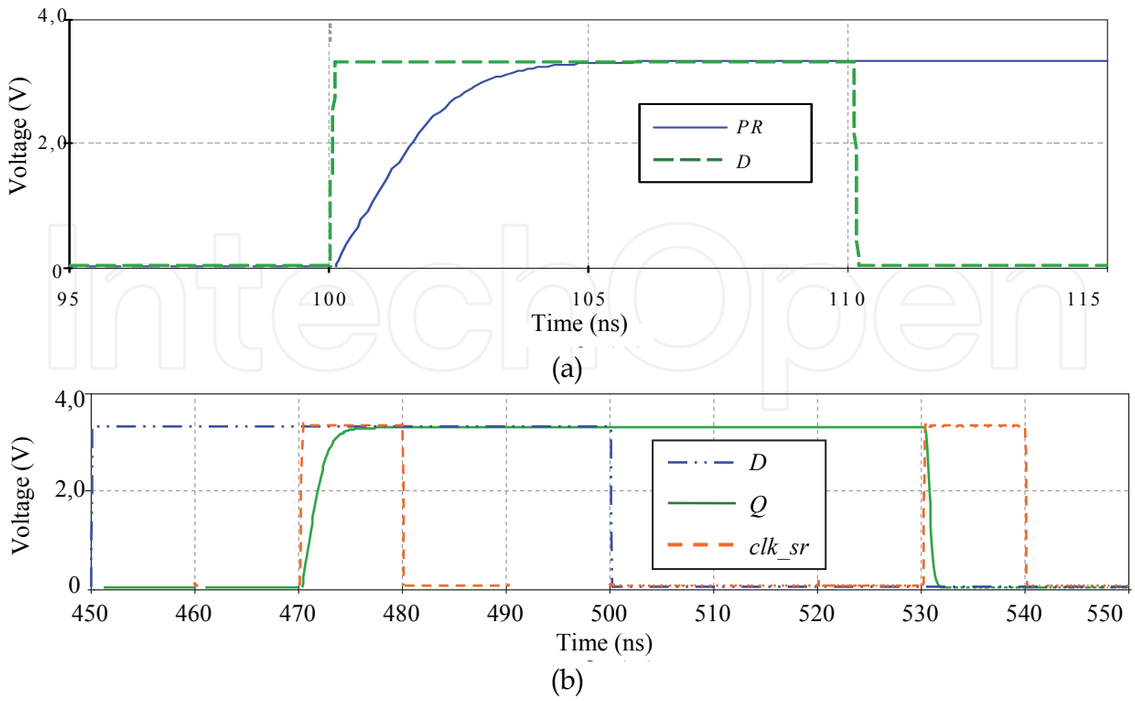


Fig. 13. D flip-flop propagation delays with 50fF load (a) related to the preset (PR) and (b) related to the input (D)

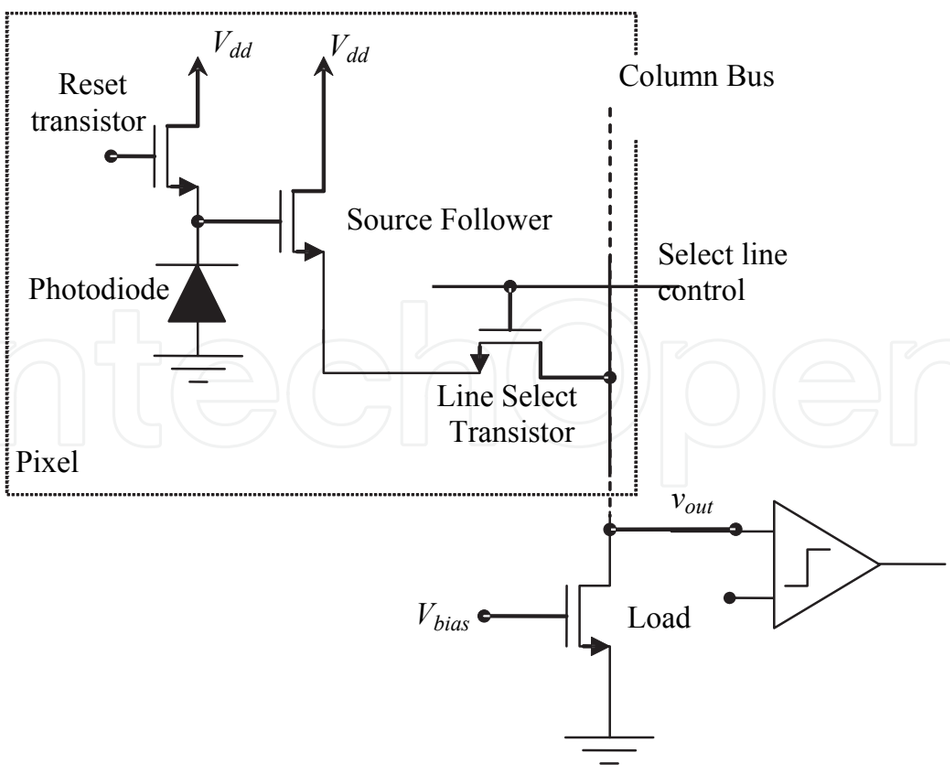


Fig. 14. A different architecture with high fill-factor for multisampling in time technique.

5. Fixed-pattern noise

The fixed pattern noise (FPN) is defined as the non-uniformity resulting from the image signal variation from pixel to pixel when a beam of light intensity is applied uniformly. The FPN in CMOS imaging systems is a major disadvantage compared to CCDs. Two major sources contribute to FPN in CMOS imaging systems in time domain: (i) the variation of initial voltage (V_{reset}) and (ii) the variation of the offset voltage of the comparator. Pixels in which the reset transistor is NMOS type, the maximum initial voltage is V_{dd}-V_{thn}. Different values of the threshold voltage cause different initial voltage (reset voltage) from pixel to pixel introducing non-uniformity at image. The conventional method to eliminate non-uniformity due to the reset transistor is using as reset transistor PMOS type MOSFET which provides maximum initial voltage V_{dd} regardless of the value of the threshold voltage.
The offset voltage of the comparator is modeled as a voltage source in series with inputs of the comparator. Considering the offset voltage as a voltage source in series with the reference voltage, the equations of discharge time (2) and (4) can be rewritten as

$$t_{dct} = \frac{(V_{dd} - V_{refct} \pm V_{offset})}{S \cdot I_L} \tag{7}$$

$$t_{drp} = \frac{(V_{máx} - V_{mín} \pm V_{offset}) \cdot T_{\text{int}}}{(V_{máx} - V_{mín}) + S \cdot I_L \cdot T_{\text{int}}} \tag{8}$$

where t_{dct} and t_{drp} are the time of discharge using a constant reference voltage and a ramp reference voltage respectively. Manipulating equations (7) and (8), we obtain the absolute error in the time of discharge using a constant reference voltage and a ramp respectively as:

$$Absolute\ error = \pm \frac{V_{offset}}{S \cdot I_L} \tag{9}$$

$$Absolute\ error = \pm \frac{V_{offset} \cdot T_{\text{int}}}{(V_{\max} - V_{\min}) + S \cdot I_L \cdot T_{\text{int}}} \tag{10}$$

According to the equations (9) and (10), the absolute error in the time of discharge varies with the incident light intensity. Manipulating equations (7), (8), (9) and (10), the relative error is given by:

$$Relative\ error = \pm \frac{V_{offset}}{(V_{dd} - V_{ref})} \text{ for constant reference voltage} \tag{11}$$

$$Relative\ error = \pm \frac{V_{offset}}{(V_{dd} - V_{mín})} \text{ for ramp reference voltage} \tag{12}$$

The results of equations (11) and (12) suggest that it is possible to implement methods of correcting the error introduced by the offset voltage using multiplicative factors. Error introduced by the offset voltage can be graphically interpreted as a steady shift in the t_d

photoresponse features shown in Fig. 4. Fig. 15 show the relative error given by equation (11) as function of reference voltage (V_{ref}) for V_{offset}=50mV and V_{dd}=3.3V. The relative error is lower for lower values of reference voltage and it is constant and independent of light intensity.

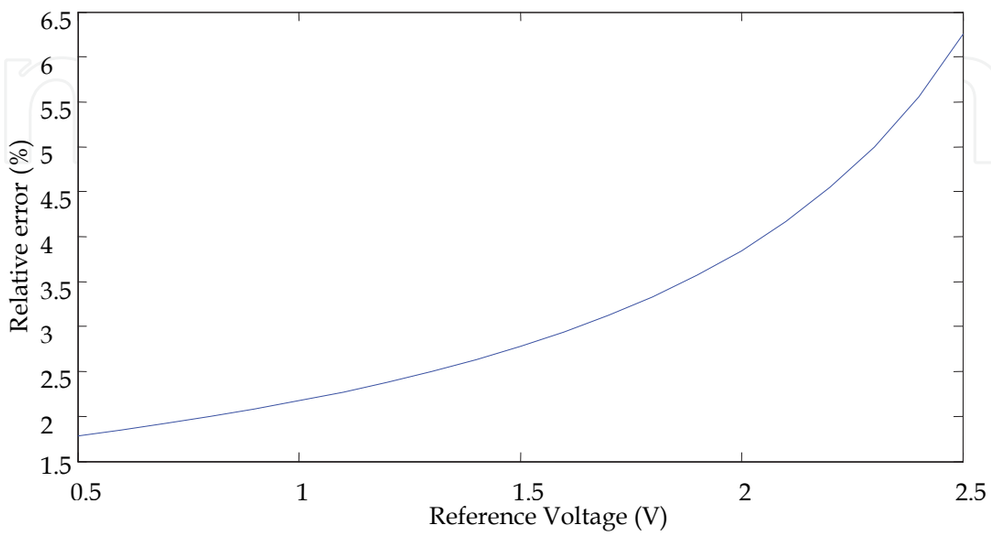


Fig. 15. Relative error introduced by offset voltage of comparator.

6. Experimental results

This section presents the measurements results reported in (Campos, 2008). The prototype integrated circuit containing an array of size 32x32 pixels was fabricated in 0.35 μ m CMOS standard process of C35O Austriamicrosystems. A Xenon lamp type with a peak luminous intensity at 830 nm and an optical filter of 825nm were used to perform the measurements of the discharge time. All measurements were performed using the nominal supply voltage of 3.3 V and bias voltage of the differential pair comparator fixed at 0.7 V. Fig. 16 shows the result of measuring the photoresponse td versus light intensity when the pixel operates with constant reference voltage of 1.5 V. The points in Fig. 16 represent the average discharge time measured for the same light intensity and the continuous curve corresponds to the mean curve fitted. According to the result of curve fitting the photodiode has a sensitivity of 3.4 μV-cm²/s-W. The measurements showed that the discharge time of darkness is 37segundos.

Fig. 17 shows three different photoresponse in time domain resulting from the use of three different ramp reference voltages. Reducing the integration time of the ramp the time discharge time is reduced. By comparing the discharge times (time comparison) using a constant reference voltage and the ramp one can see that there is a reduction in discharge time at lower light intensities when a ramp reference voltage is used. Note that the photoresponse is approximately flat in the range of irradiation below 10^{-1} (μ W/cm²) (Fig. 17). In this region the discharge time becomes almost constant becoming harder to indentify the light intensity.

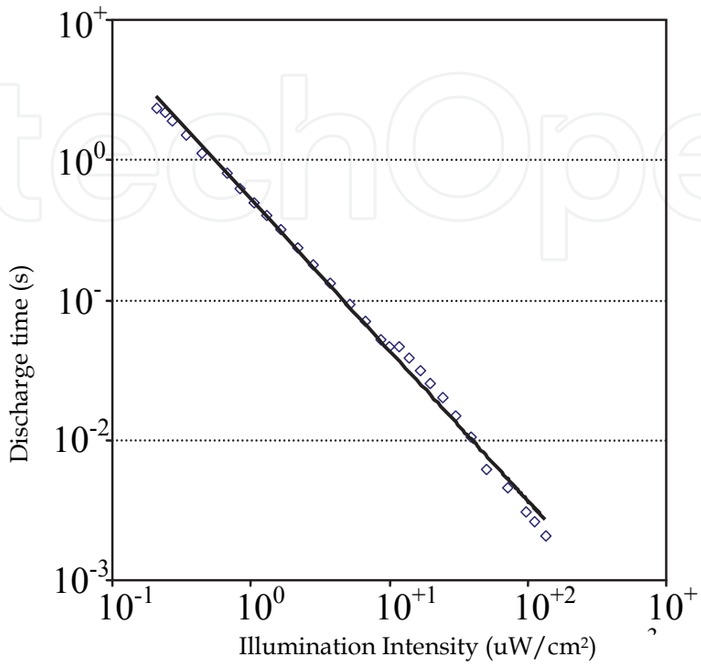


Fig. 16. Time discharge characteristic for constant reference voltage

The experimental measure of the normalized spectral response is shown in Fig. 18. The wide range in which the response will be approximately constant due to the fact that although the junction depth is shallow, low doping concentration of the substrate causes the width of the depletion region extends significantly into the substrate (greater depth). Documents supplied by the factory also report approximately flat spectral response in most of the visible spectrum.

Fig. 19 shows the relationship obtained from SNR measurements as a function of light irradiation. The ratio remains constant SNR value of 54dB in most of the range of irradiation showing good agreement with the theoretical analysis presented in subsection 3.2.5 (Figure 3.25). The theoretical results indicate that using the constant reference voltage SNR is constant throughout the range of light irradiation. It is considered that the discrepancy observed in the SNR measured in the upper level of irradiation was due to the process of determining the average using the oscilloscope. At the time of the measurements was not obtained proper adjustment of the oscilloscope to perform the average. A constant feature of the SNR shows very attractive and important when compared to the results reported in the literature so far. The results reported in other studies shows that the SNR varies from 0 to 54dB, where 54 dB is suggested as a maximum.

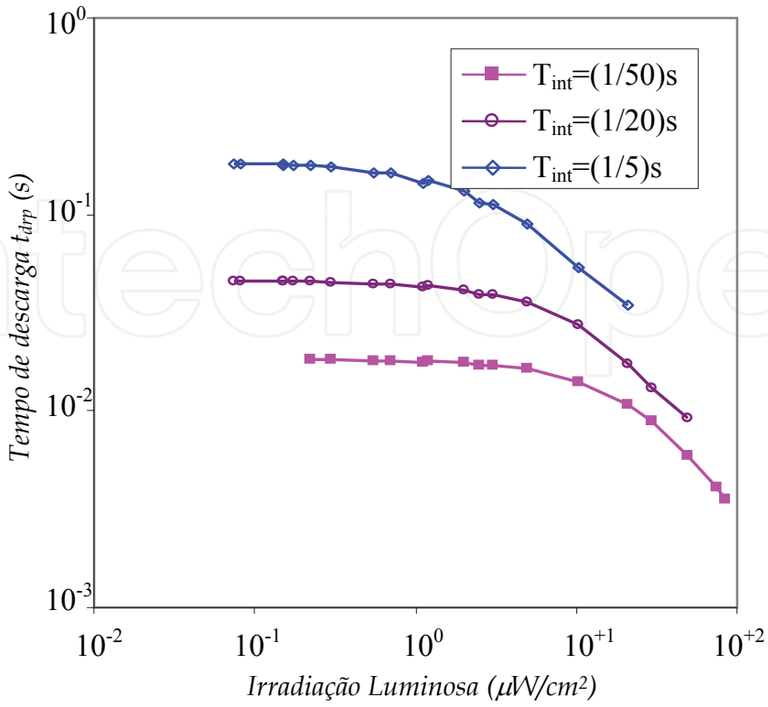


Fig. 17. Spectral photoresponse in time-domain using constant reference voltage

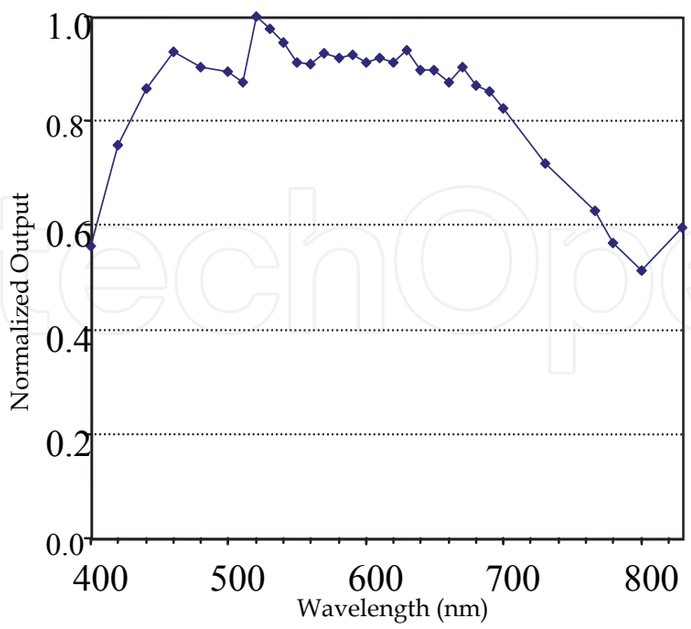


Fig. 18. Spectral photoresponse in time-domain using constant reference voltage

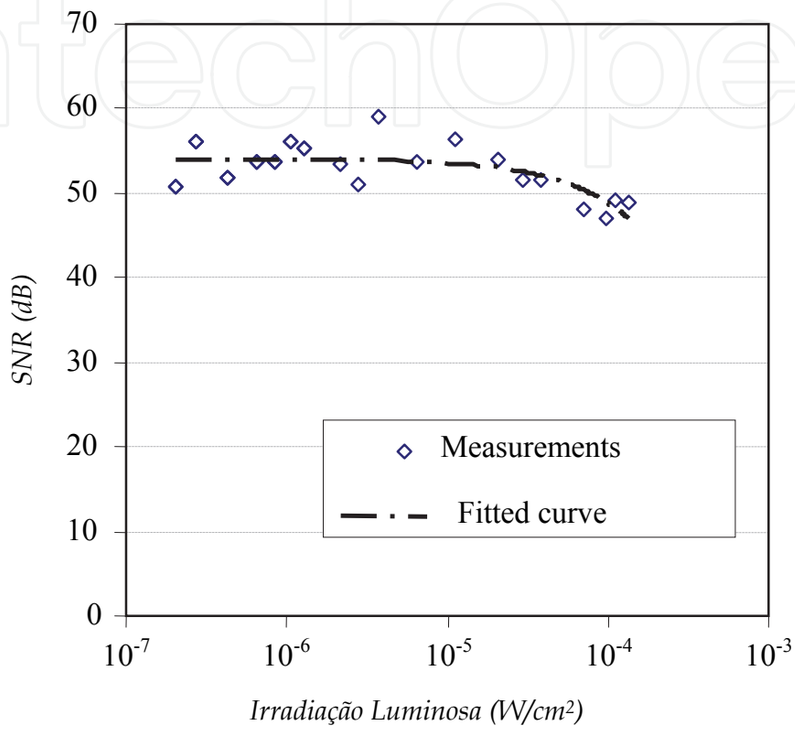


Fig. 19. Noise in time-domain for constant reference voltage (V_{ref}=1.5V)

7. Conclusions

Multisampling time-domain CMOS imagers were presented. Sampling can be linear, logarithmic and linear-logarithmic. Pixel architecture is composed only by a comparator and a D flip-flop reducing the total transistors integrated per pixel compared to others approach. Analysis shows that the matrix size limits the total bit number that represents the image. High dynamic range is achieve only for operation in which the image representation is higher or equal to 16 bits. The FPN introduced by voltage offset of comparator presents constant relative error. This constant relative error might be particularly interesting for lower light intensities.

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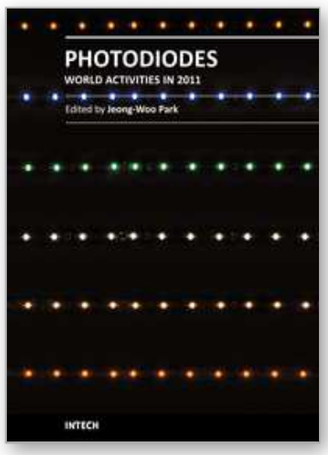

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Photodiodes or photodetectors are in one boat with our human race. Efforts of people in related fields are contained in this book. This book would be valuable to those who want to obtain knowledge and inspiration in the related area.

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