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CMOS, Delta-Sigma pH-to-Digital Converter as New Integrated Device for Potentiometric Biosensors Applications

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1. Introduction

The explosive growth in the healthcare and lifestyle application has fueled recent research efforts to increase both integration and adaptability in biosensor readout design. Potentiometric sensor is emerging as important sensing devices in the areas of biomedical applications since the pioneer work on pH sensor has been introduced (Bergveld, 1970). It has appreciable advantages over traditional glass-electrode sensors on the basis of its small size, robustness, simplicity in fabrication and low cost (Yin et al., 1999). Moreover, many research works have exploited different circuit architectures of readout circuits, which usually play the role in translating the values to voltage domain presentation, with the goal to obtain good sensitivity as well as linearity (Chan et al., 2007). However, the conventional readout circuitry of pH sensor comprises multiple chips and discrete components which are fabricated in different technologies. The goal of this research is to propose a novel pH sensor readout circuitry onto a single chip in standard CMOS technology. Such fully integrated solution results in pH sensor readout devices with lower cost and higher performance.

New architectures and circuit techniques need to be explored in the design of fully integrated potentiometric sensor readout circuit. The wide dynamic range and low power are necessitated by the elimination of discrete high Q filters in traditional potentiometric sensor readout channel. In addition, readout circuits need to adapt to the different dynamic range, linearity, and signal bandwidth requirements of multiple potentiometric sensors. This programmability can be easily achieved by performing signal processing in the digital domain. Moreover, the reliability of signal processing in digital form can readily permit sensor systems to combine with other instruments.

In moving the signal response of pH sensor to the digital domain, a high dynamic range, low power analog-to-digital converter (ADC) is needed to quantize a small desired signal. Delta-sigma modulators are uniquely suited to this application because the high pass shaped quantization noise falls into the same band as the environment noise (Kuo et al., 2001). This implies that a single programmable digital decimation filter following the delta-sigma analog-to-digital modulator can attenuate both the quantization and environment noise.

2. Delta-Sigma pH-to-digital converter

The delta-sigma modulator is an attractive candidate for the sensor applications due to its robust capability to process variations and high-resolution performance (Lemkin et al., 1999). Furthermore, delta-sigma modulator can trade time for improvements of the resolution and signal to noise ratio.

Direct sensor signal-to-digital converter provides digital output without the need for its intermediate processing circuit. Direct capacitance-to-digital converters (Petkov et al., 2005) and magnetic-to-digital converters (Kuo et al., 2001), based on the principles of the delta-sigma technique, are suitable for sensors signal processing. In this study, direct pH-to-digital converter based on delta-sigma modulator in fully integrated pH sensor readout circuitry is proposed.

2.1 Conventional pH sensor readout system

The sensor readout system shown in Fig. 1 is the conventional approach to pH sensor receiver architecture. With high Q off-chip filters (shaded in Fig. 1), this conventional architecture is not amenable to a highly integrated solution. The off chip filters also must be specific to a particular sensor.

Consider the propagation of a desired pH sensor signal through the readout path as shown in the frequency plan. The pH sensor signal at the sensing membrane passes through an off-chip filter and is amplified by the pre-amplifier or low-noise amplifier (LNA). Amplification of the pH sensor signal is required to achieve adequate sensitivity by reducing the noise contributions of environment noise in the receive path. After the pre-amplifier or LNA, the sensor signal goes off-chip through the filter. The combination of the pH sensor signal and filters rejects environment noise which is out off pH sensor signal bandwidth that must be attenuated prior to offset cancellation circuit. The offset cancellation circuit is constructed by a digital-to-analog converter and a differential amplifier with low gain. The general correction method used in readout channel is successive approximation. The variable gain amplifier (VGA) is used to reduce the dynamic range (DR) requirement of subsequent stages. The most important design factor of variable gain amplifier is the total harmonic distortion (THD). The variable gain amplifier must amplify the sensor signal without distortion. Finally, anti-aliasing and analog-to-digital conversion (ADC) are performed. ADC is required so that output bits can be recovered in the digital domain. The filter can be performed in the analog domain using either continuous time or discrete time (switched-capacitor) filters or in the digital domain. The choice of analog or digital selection impacts the dynamic range requirements of the ADC and the programmability of the sensor readout system.

Analog filter in front of the ADC must band-limit the incoming signal with enough stop band rejection to remove the environment noise prior to sampling by the ADC. In alternate way, the ADC must oversample enough so that the environment noise does not alias into the desired frequency band and can be removed by a subsequent digital filter. Thus, from the ADC design view, the bandwidth selection of sensor signal reduces to providing adequate anti-aliasing in either the analog or digital domain. The analog filter must have enough dynamic range and linearity to select the desired bandwidth in the presence of pH sensor signal. Since all bandwidth select filtering is performed prior to the ADC, only a low resolution ADC with enough bandwidth to digitize the desired bandwidth is required. One implementation of the pass band processing block would employ a continuous time low

pass analog filter in front of the ADC. This filter would be implemented by switched-capacitor technology since the pH sensor signal is DC-like signal. Linearity considerations dictate the signal-handling capability of the filter. Moreover, bandwidth selection can be performed in the digital domain using an oversampled delta-sigma modulator followed by a digital decimation filter.
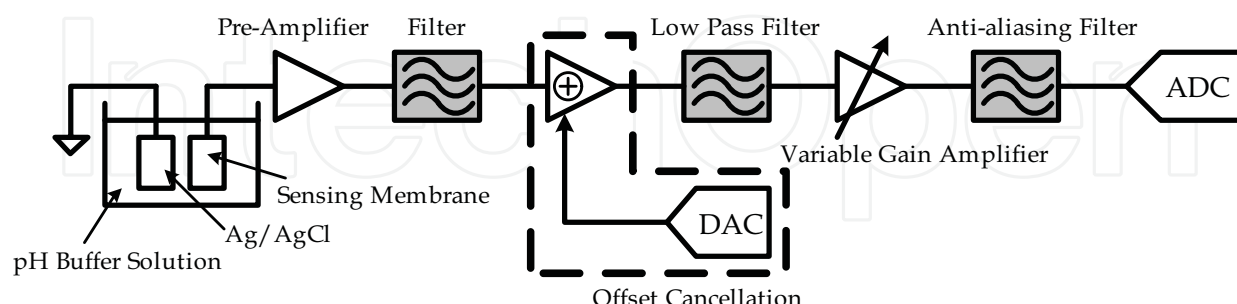

Fig. 1. Block diagram of conventional pH sensor readout circuit

2.2 EGFET-operational amplifier

Ion sensitive field effect transistors (ISFETs) are emerging as important sensing devices in the areas of environmental monitoring applications and biomedical applications (Bergveld, 1970). The ISFET used as a pH sensor is an integrated device composed of a conventional ion selective membrane and a metal oxide semiconductor field effect transistor (MOSFET). Extended gate field effect transistor (EGFET) is another structure to isolate field effect transistor (FET) from chemical environment, in which a sensitive membrane is fabricated on the end of the signal line extended from the gate electrode of FET (Spiegel et al., 1983). EGFET has advantages over ISFET such as low cost, simple structure and ease to package (Chin et al., 2001). Behavior of surface ion adsorption effect of the ISFET and EGFET are the same (Chou et al., 2009). The much difference between ISFET and EGFET is the impedance of sensing film. The gate electrode of EGFET must be high conductivity material to be a sensing electrode that can transmit sensing signals easily.

The EGFET can be represented by a model as depicted in Fig. 2. It consists of a chemical part and an MOS transistor part. In chemical part, two series capacitances and represent the equivalent Gouy-Chapman and Helmholtz capacitance (Grattarola et al., 1992), which has been developed by site-binding model and the electrical double-layer theory (Fung et al., 1986). Two voltage sources and are connected in series to denote the voltage components of chemical threshold voltage of EGFET. The chemical threshold voltage consists of two potentials $-\Psi_{eo}+\chi^{sol}$, χ^{sol} in which is a constant with respect to the pH value, and Ψ_{eo} is the only chemical parameter that is responsible for pH sensitivity of EGFET. χ^{sol}, with a typical value of 50 mV, is the surface dipole potential of the solvent being independent of pH (Chan et al., 2007). The sensitivity of Ψ_{eo} , which is defined as the change of Ψ_{eo} with respect to a change of the pH value of the solution $\Delta\Psi_{eo}/\Delta pH$, has already been explained by the Hal and Eijkel's theory (Van Hal et al., 1995). This is elaborated by using the general accepted site-binding model and the Gouy-Chapman-Stern model to yield on:

$$\frac{\Delta\Psi_{eo}}{\Delta pH} = -2.303 \cdot \frac{KT}{q} \cdot \alpha \tag{1}$$

where K is the Boltzmann constant, T is the absolute temperature, q is the magnitude of the electron charge, α is a dimensionless sensitivity parameter, with the value ranging between 0 and 1.
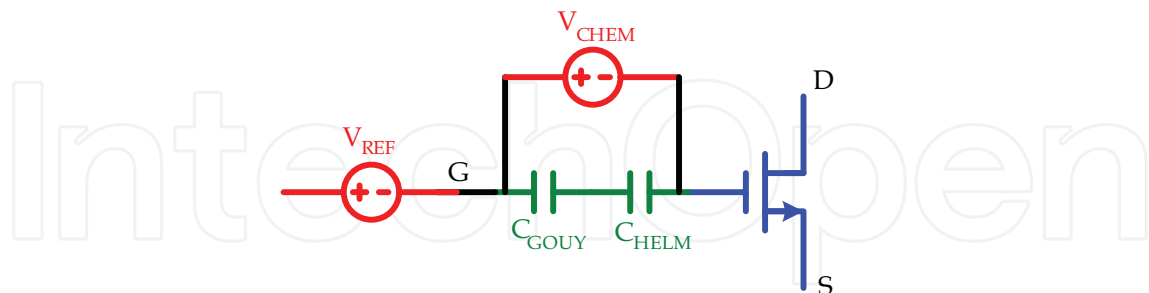

Fig. 2. EGFET modeling components

The other physical constants have their usual meanings. Therefore, the voltage source becomes:

$$V_{CHEM} = 2.303 \frac{KT}{q} \alpha \cdot pH + (\chi^{sol} - C)$$ (2)

where the first term is pH-dependent and the constant terms in the parentheses are pH-independent.

Like the standard MOSFET, for a long-channel EGFET operating in a saturation region, the drain current can be expressed as

$$I_{DS} = \frac{1}{2} \frac{W}{L} \mu C_{OX} \left(V_{GS} - V_{TH(EGFET)} \right)^2$$ (3)

where μC_{ox} is the process transconductance parameter, W/L is the aspect ratio. Moreover, the EGFET threshold voltage combined with the MOS transistor counterpart which includes body effect in a four-terminal device can be unified as

$$V_{TH(EGFET)} = V_{CHEM} + V_{TH}$$ (4)

where V_{TH} is the threshold voltage of the MOS transistor.

As this potential is pH-independent, it can be viewed as a common-mode input signal for an EGFET interface circuit in any pH buffer solution and can be nullified during system calibration and measurement procedures. The SnO₂/ITO glass, fabricated by sputtering SnO₂ on the conductive ITO glass, was used as a pH-sensitive membrane of EGFET-operational amplifier. The SnO₂ thin films were formed by the radio frequency sputtering system at a substrate temperature of 150°C. Mixed sputtering gases included O₂ and Ar. Thickness of the SnO₂ thin film was about 2000 Å. The ITO glasses were supplied by the Wintek corporation. The coating thickness of ITO was about 230 Å. The sheet resistance of ITO is 50-100 Ω/□. The conducting line was bound from the ITO layer and packaged by epoxy after the thin film was deposited. The commercial buffer solutions were used as the test solutions. The micro slide glass and corning 7059 glass were purchased from Kimax Glass Instrument and Tekstarter corporation. The deposition parameters are summarized as follows:

1. Deposition rate is 20 Å/s.
2. Deposition pressure is 20 e-3 Torr.
3. Background pressure is 2×e-6 Torr.
4. The Ar/O_2 ratio is 4:1.
5. Substrate temperature is 150°C.

The fabrication processes of sensing structure were summarized as follows and its cross-section is shown in Fig. 3.

1. Clean the silicon substrate.
2. SnO_2 was deposited on ITO about 3000Å by sputtering method.
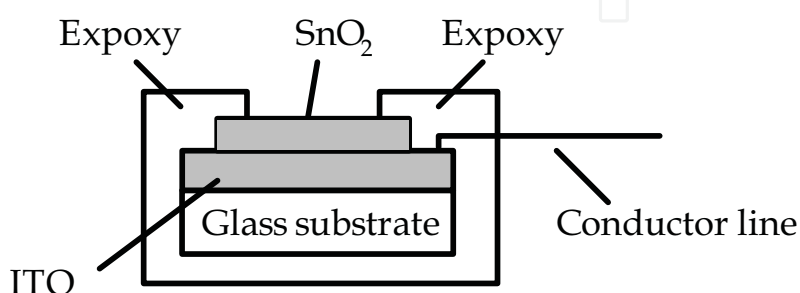3. Bounding and packaging by epoxy.

Fig. 3. Cross-section of SnO2/ITO glass sensing membrane

The operation of the extended-gate field effect transistor is very similar to that of a conventional MOS, except that an additional sensing structure is dipped in the buffer solution. In the study of pH sensitivity of the SnO_2/ITO glass, the SnO_2/ITO glass sensing membrane was connected to an instrumentation amplifier (Yin et al., 2000). The instrumentation amplifier was used to measure output response of the SnO_2/ITO glass in the pH buffer solutions, and the result shows that the sensing membrane, SnO_2/ITO glass, has a linear pH sensitivity of approximately 59.3mV/pH in the ion concentration ranging between pH 2 and 10. To evaluate the hysteresis characteristic of the SnO_2/ITO glass sensing membrane, we measured the output offset voltage after solution change such as pH7→pH4→pH7 and pH 7→pH10→pH7. The results show that the hysteresis of the SnO_2/ITO glass sensing membrane is about 4.2mV. For the sensor signal measurement, we need an interface circuit that tracks the threshold voltage (or the flat-band voltage) of the EGFET as the electrolyte pH is varied. A more practical solution to monitor the sensor signal with electronics is to view the EGFET as a circuit component in an integrated circuit rather than as an add-on sensor whose output signal is further processed. In this work, we adapt the EGFET-operational amplifier approach of utilizing the EGFET as one of the input transistors in the differential stage of an operational amplifier shown as in Fig. 4.

Circuit functions of the EGFET-operational amplifier as follows: when the EGFET-operational amplifier is configured as a voltage follower (β=1), the output voltage is equal to the input voltage; any difference in threshold voltages and bias currents between the two input transistors at the differential input stage will also appear at the output. Writing out the terms of the threshold voltages of the MOSFET and the EGFET explicitly, the output of the EGFET-operational amplifier is as followings:
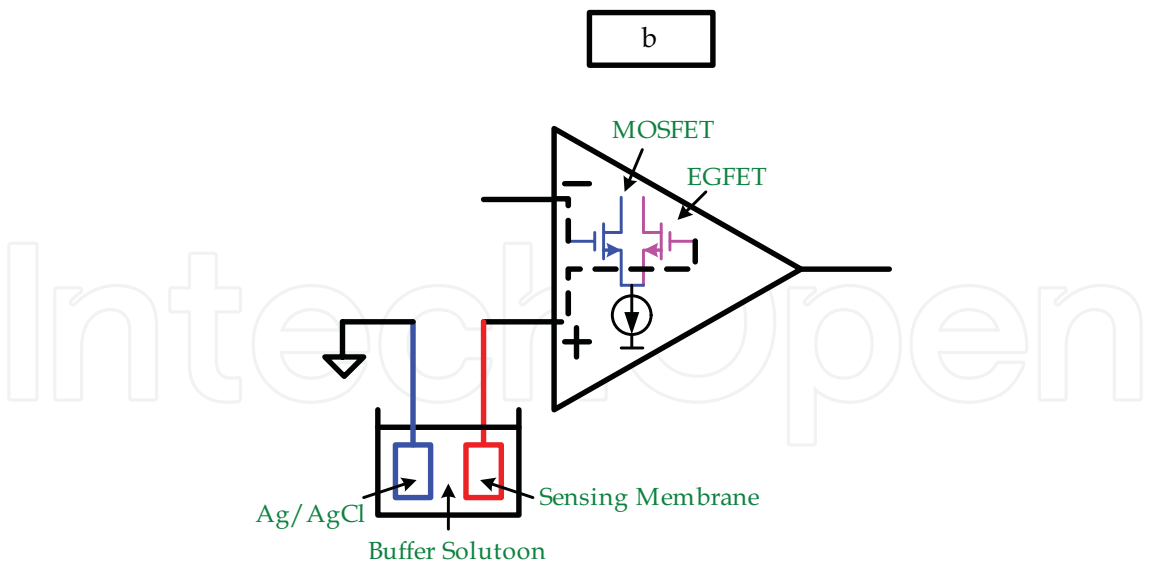
$$V_{OUT} = \Delta V_{TH} = V_{CHEM} \tag{5}$$

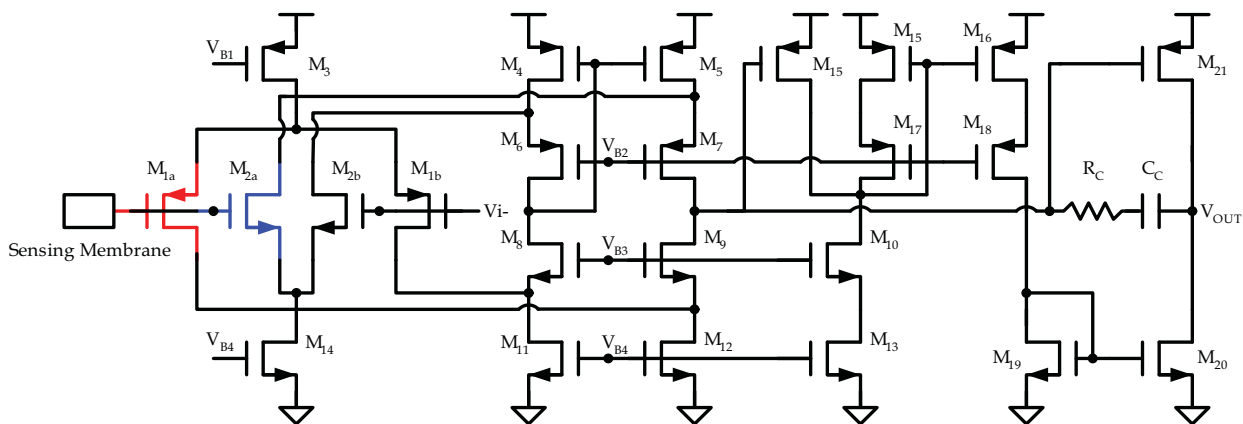Fig. 4. Block diagram of the EGFET modeling components

Fig. 5. EGFET operational amplifier

For the realization of pH sensor readout systems, low power and high dynamic range interface circuits are indispensable building blocks. EGFET operational amplifier shown in Fig. 5 is investigated to track the output response caused by the H^+ ion concentration. To improve the input dynamic range, the n-p complementary EGFETs differential stage was adopted as the input stage of the EGFET operational amplifier. The EGFETs were biased in the suitable operating point by the reference electrode. It is important to keep the total transconductance variation small if n-p complementary differential input stage of the amplifier was adopted. The gain of the amplifier used in the negative feedback must be large enough to keep the transconductance variation small instead of adding compensation structure. For this purpose, the voltage gain of the amplifier was chosen to be higher than 75 dB for 12-bits application. The first stage of the EGFET-operational amplifier is a folded cascode structure which provides most of the overall DC gain. The second stage is a slew rate enhancement circuit to provide a high driving capability. The output stage senses the PMOS driver current of the first stage and subtracts this current from a reference current source M_{13}. The difference is then mirrored to the NMOS output device M_{20}. Thus, the output stage works in a push-pull fashion and results in significantly improved slew rate

performance. This output stage must be able to drive loads up to 2pF for the discrete time pH-to-digital converter application. Moreover, the MOSFETs of the EGFET-operational amplifier were integrated in one process to enable a more stable operation. A nulling resistor R_C in series with the compensation capacitor C_C was inserted to move the right half-plane zero into the left half-plane to improve the phase margin of the amplifier.

Fig. 6. Bias network for EGFET operational amplifier

Fig. 6 shows the biasing scheme for the prototype chip. High-swing cascade biasing circuit is generated by stacking a number of triode-region devices. The PMOS portion of the biasing is slaved off the NMOS portion for better matching and tolerance toward process shifts. To provide good isolation between circuits on the chip, the EGFET operational amplifier (where performance is the most critical) has its own bias network while the other three amplifiers designed for reference regulator share another bias network. The master bias currents shown in Fig. 6 are generated on chip by mirroring the current from an external master current source, as shown in Fig. 7. The master bias is distributed to local bias networks as a current so that IR drops in routing do not affect the biasing.

Fig. 7. Master bias circuit

2.3 Direct pH-to-digital converter

Delta-sigma analog-to-digital converter is another important sensor readout technology. Modern sensor instrumentation systems become favorable in digital form due to its excellent user interface and anti-noise performance (Ezekwe et al., 2008). Moreover, digital signal processing can readily permit sensor systems to combine with other instruments. Delta-sigma converters achieve high resolution by transferring the quantization noise into high frequency and removing it with a digital filter. Fig. 8 shows the block diagram of a delta-sigma analog-to-digital modulator.
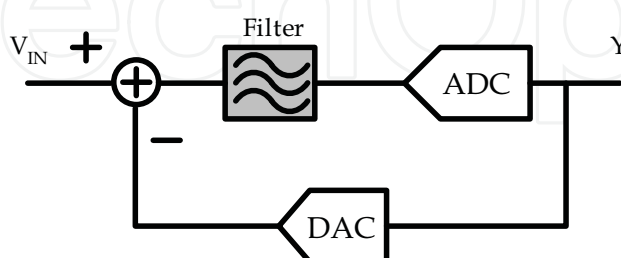
Fig. 8. Block diagram of delta-sigma analog-to-digital modulator

Intuitively, the negative feedback loop causes the output of the DAC to on average equal the input voltage V_{IN} (Ezekwe et al., 2008). Therefore the output bits of the ADC are a rough, low frequency representation of the analog input V_{IN}. If the signal bandwidth is sufficiently smaller than the sampling frequency then the high frequency quantization noise can then be digitally separated and removed with a low pass filter to yield the final digital output signal Y. The transfer function from V_{IN} to Y is a pure delay. If the quantizer is modeled as white quantization noise, the converter can be treated as a linear system. Now the transfer function of the quantization noise Q to the output Y is a high-pass (Boser et al., 1988). Thus the quantization noise at low-frequencies is suppressed as shown in Fig. 9. The remaining high-frequency quantization noise can then be removed with the digital low-pass filter. From equation (6), the power of quantization noise is independent of the sampling rate. And the quantization noise power in oversampled converters is the same as that for Nyquist rate converters, but is now distributed over a wider band (Norsworthy et al., 1997).

$$P_{Q,Oversampled} = \int_{-f_{BW}}^{f_{BW}} \frac{\Delta^2}{12} \cdot \frac{1}{f_S} df = \frac{P_{Q,Nyquist}}{\frac{f_S}{2f_{BW}}} = \frac{P_{Q,Nyquist}}{M} \tag{6}$$

where oversampling ratio, $M = f_S / 2f_{BW}$

Increasing the sampling rate therefore reduces the quantization noise power by a fraction M, which is the oversampling ratio. Let $Z = e^{jwT} = e^{jw/f_S}$ and rewrite the noise transfer function as following (Johns et al., 1997)

$$N_{TF}(f) = 1 - e^{-jw/f_S} = \sin\left(\frac{\pi f}{f_S}\right) \cdot 2j \cdot e^{-j\pi f/f_S} \tag{7}$$

Assuming the maximum signal power is the same as the quantization noise of Nyquist rate converters, the maximum SNR for the first order sigma-delta modulator is given by

$$SNR_{MAX} = 6.02N + 1.76 - 5.17 + 30\log(M) \tag{8}$$

The benefits increase as the sampling rate is increased relative to the input signal bandwidth. The ideal output SNR increases 9dB per octave in oversampling ratio (Johns et al., 1997). Thus, delta-sigma converters can achieve very high resolution for small signal bandwidths, such as bio-sensor and audio applications. By using a high oversampling ratio, an inherently linear, single-bit quantizer can be used which is beneficial because it does not require any precision, matched components. Finally a high oversampling ratio is also an advantage because it relaxes the roll-off characteristics of the anti-alias filter preceding the ADC. Furthermore, more integrators may be added to increase the noise-shaping characteristics of the system. This dramatically reduces the in-band quantization noise. Adding too many integrators, however, introduces loop stability problems. Delta-sigma applications usually make heavy use of switched-capacitor circuits. Switched-capacitor integrators usually used in the forward path, and switched capacitor comparators and DACs are also used in the loop. It is the settling time of the integrators, however, that typically limits the sampling rate of the system.

By oversampling the input and then averaging the output, we can predict the input signal. The signal transfer function, $S_{TF}(Z)$, and noise transfer function, $N_{TF}(Z)$, can be derived as following (Norsworthy et al., 1997)

$$S_{TF}(Z) = \frac{Y(Z)}{V_{IN}(Z)} = \frac{H(Z)}{1 + H(Z)} \tag{9}$$

$$N_{TF}(Z) = \frac{Y(Z)}{E(Z)} = \frac{1}{1 + H(Z)} \tag{10}$$

where $H(z)=1/(Z-1)$

The output signal function can be derived by the combination of the input signal and the noise signal. The transfer function is given by

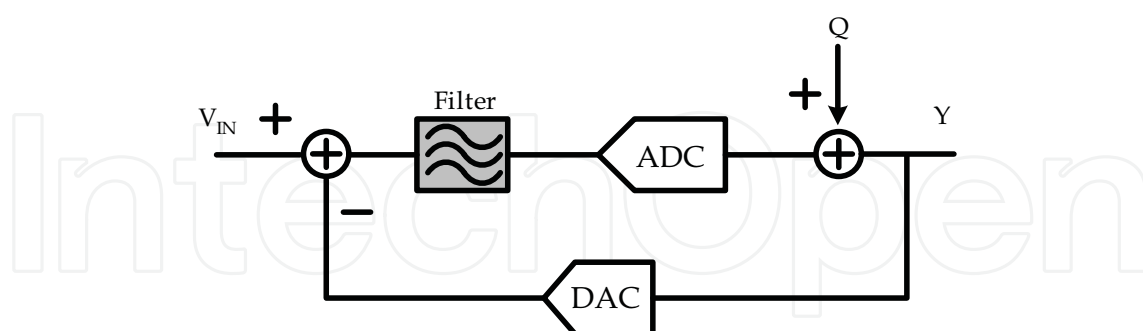$$Y(Z) = S_{TF}(Z) \cdot V_{IN}(Z) + N_{TF}(Z) \cdot E(Z) \tag{11}$$

Fig. 9. Quantization noise model

The signal transfer function is simply a delay. Since the transfer function from the quantization error source to the output is given by $(1-Z^{-1})$ the noise is shaped by a high-pass characteristic. The switched-capacitor (SC) technique is used to realize the first-order delta-sigma modulator. A first-order modulator where a 1-bit quantizer is used in the feedback loop is shown in Fig. 10. The delta-sigma modulator consists of both analog and digital circuitry. The integrator of delta-sigma modulator needs a two-phase non-overlapping clock (with delays) to minimize signal-dependent charge-injection errors. Shown in Fig. 11 is the

waveform of the two-phase clock. $\Phi1d$ are the delayed versions of $\Phi1$. The rising edges of the delayed clocks should be lined up with the rising edges of the non-delayed versions to increase the amount of available settling time for the integrator. A simple dynamic comparator shown in Fig. 12 is used to perform a single bit conversion.

Fig. 10. First-order delta-sigma modulator

Fig. 11. Clock timing for the first time delta-sigma modulator

Fig. 12. Dynamic comparator circuit

The dynamic comparator in Fig. 12 is simplified to perform a comparison with zero standby current (Kuo et al., 2001). The differential signal varies the resistance of triode region devices M_{C1} and M_{C2}. When the latch signal (Φ_{1d}) is low, the comparator output is pre-charged to positive power by devices M_{C7} and M_{C10}. On the rising edge of the latch signal, the outputs of the cross-coupled inverters formed by M_{C3}, M_{C4}, M_{C7} and M_{C8} flip in the appropriate direction based on the differential resistance of the triode region input devices.
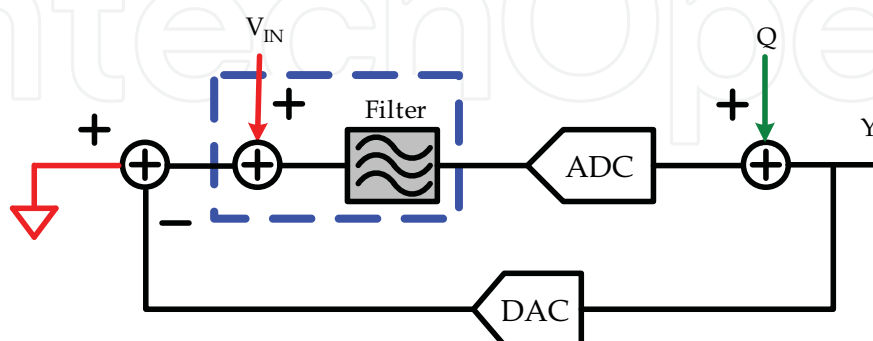
Fig. 13. Modified delta-sigma modulator

Adding analog ground in the input stage of the delta-sigma modulator will not affect the behavior function of original delta-sigma modulator. Redrawing the linear model shown in Fig. 13, we can transfer the location of the input signal into the filter block without changing the system behavior. The redrawing block diagram is shown in Fig. 14. Integrator can be used to replace the filter if the behavior of filter type is low pass filter. In other words, we can implant a direct pH-to-digital modulator based on delta-sigma technology if we can design an integrator and its output is dependent on the pH value. The direct pH-to-digital modulator is shown in Fig. 15. Following the modulator, a simple digital low pass filter can be used to remove the quantization and environment noise. For integrated pH sensor, the extended-gate field effect transistor (EGFET) operational amplifier was investigated to track the threshold voltage of the EGFET. The sensing part used in EGFET operational amplifier (EGFET-OP) is SnO_2/ITO glass. The commercial buffer solutions were used as the test solutions. First order switched capacitor low pass delta-sigma modulator constructed using EGFET-OP, shown in Fig. 15, was used to transfer the pH signal into digital. The H^+-ion induced voltage V_{pH} can be regarded as the voltage difference between two input nodes of the EGFET-OP in the switched-capacitor integrator.
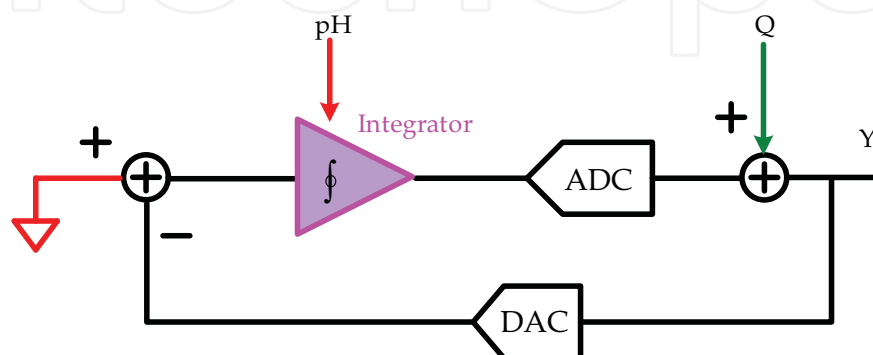

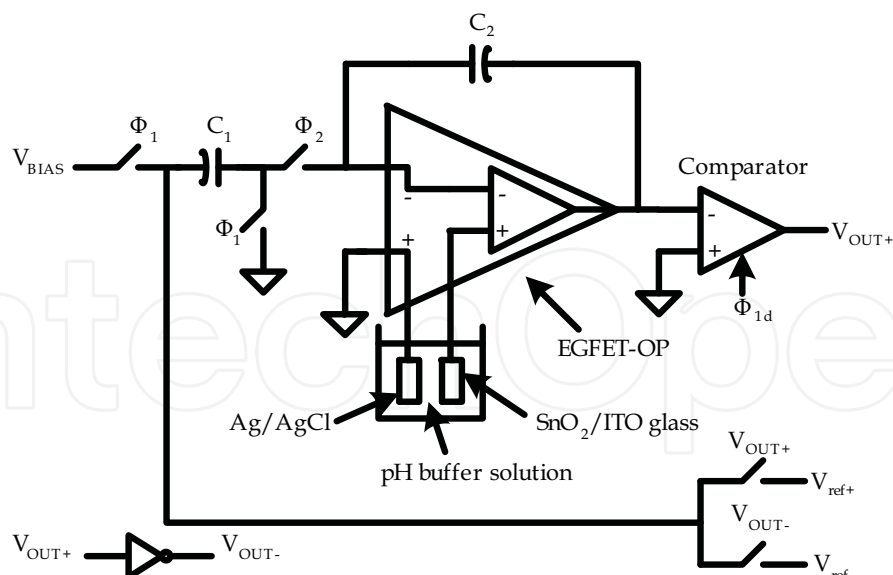Fig. 14. Direct pH-to-digital modulator

Fig. 15. Implementation of the pH-to-digital modulator

The transfer function of the pH-to-digital converter can be derived as follows:

$$Y = \left(1 + \frac{C_1}{C_2}\right) \cdot V_{pH} + \frac{1 - z^{-1}}{1 + \left(\frac{C_1}{C_2} - 1\right)z^{-1}} \cdot E \qquad (12)$$

where Y denotes the average digital output of the quantizer, and E indicates the quantization noise. When choosing $C_1 = C_2$, the expression will be simplified to:

$$Y = 2 \cdot V_{pH} + (1 - z^{-1}) \cdot E \qquad (13)$$

Furthermore, the quantization noise is first-order shaped as expected. Through an on-chip simple digital filter realized by 14-bits up-down counter, the digital average value of the comparator was obtained after shifting the bits of the output code depending on the sampled numbers. The high frequency quantization noise was filtered out. The general regenerative latch comparator shown in Fig. 12 was employed as the quantizer in the delta-sigma modulator.

The direct pH-to-digital converter derived is used to measure the pH response. The chip has been encapsulated in a standard dual inline package. The sensing art has been exposed to test solutions in the ion concentration range between pH 2 and 12. The measurements were performed under a 1.8V power supply, and the sampling frequency of the converter was 6.25 MHz. Through an on-chip simple digital filter realized by 14-bits up-down counter, the digital average value of the comparator was obtained after shifting the bits of the output code depending on the sampled numbers. Layout microphotograph of the pH-to-digital converter circuit is shown in Fig. 16. The circuit (without pad) occupied an area of 0.66mm × 0.43mm. The input range of the delta-sigma modulator is 1.2V since the positive and negative reference voltages of the delta-sigma modulator are 0.3V and 1.5V, respectively. The sensitivity of the pH-to-digital converter is 197 digital counts/pH. The plot of the digital output versus pH value is shown in Fig. 17. Deviation between measured points and the linear regression line of sensitivity shown in Fig. 18 is under ±0.02pH. The performance of this pH-to-digital converter was summarized in Table 1.
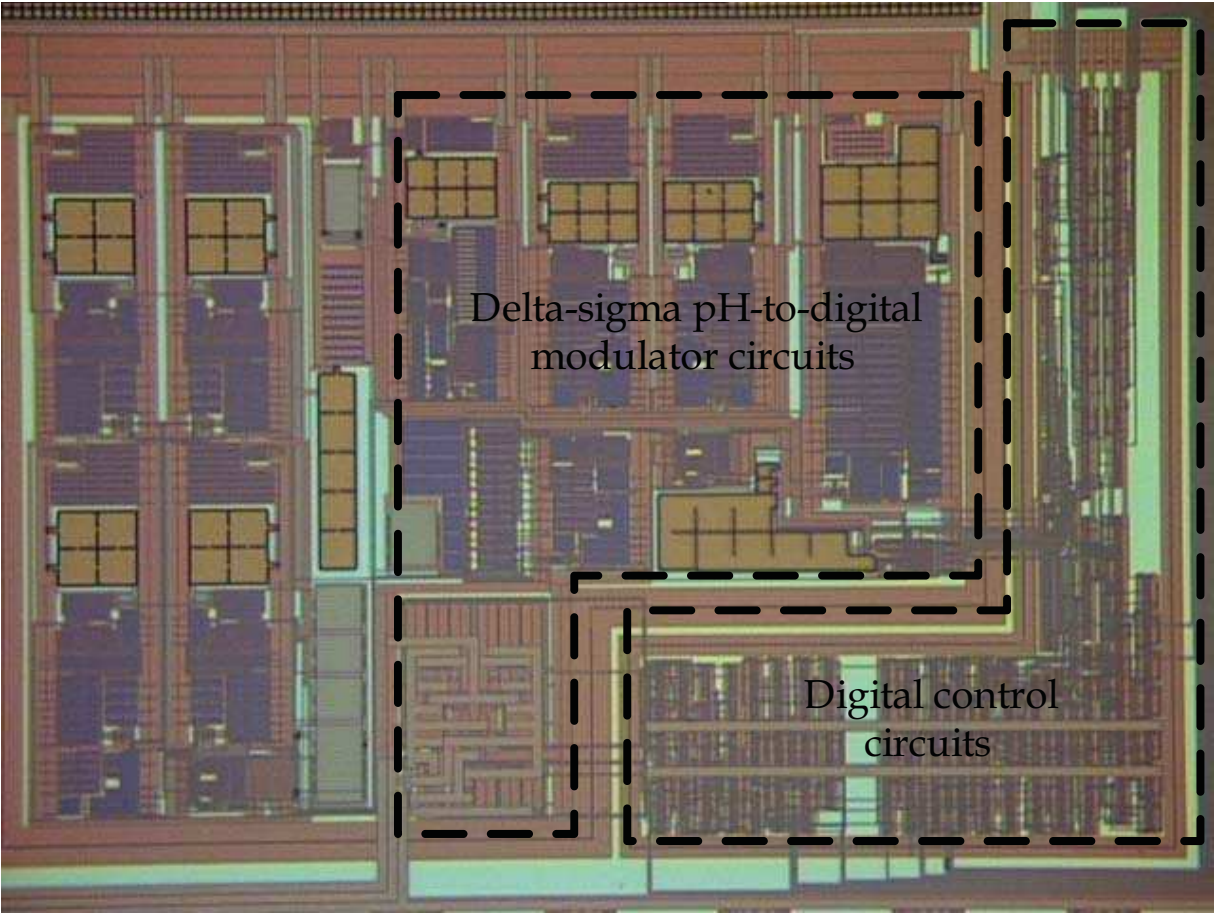
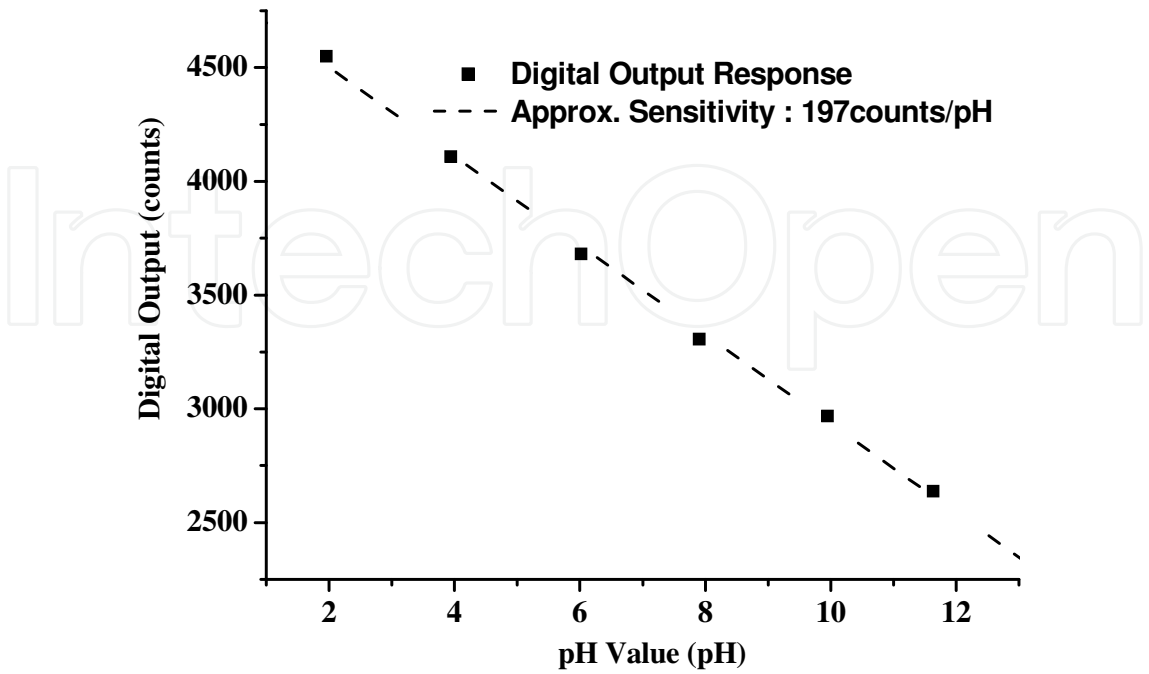Fig. 16. Layout microphotograph of the pH-to-digital converter circuit

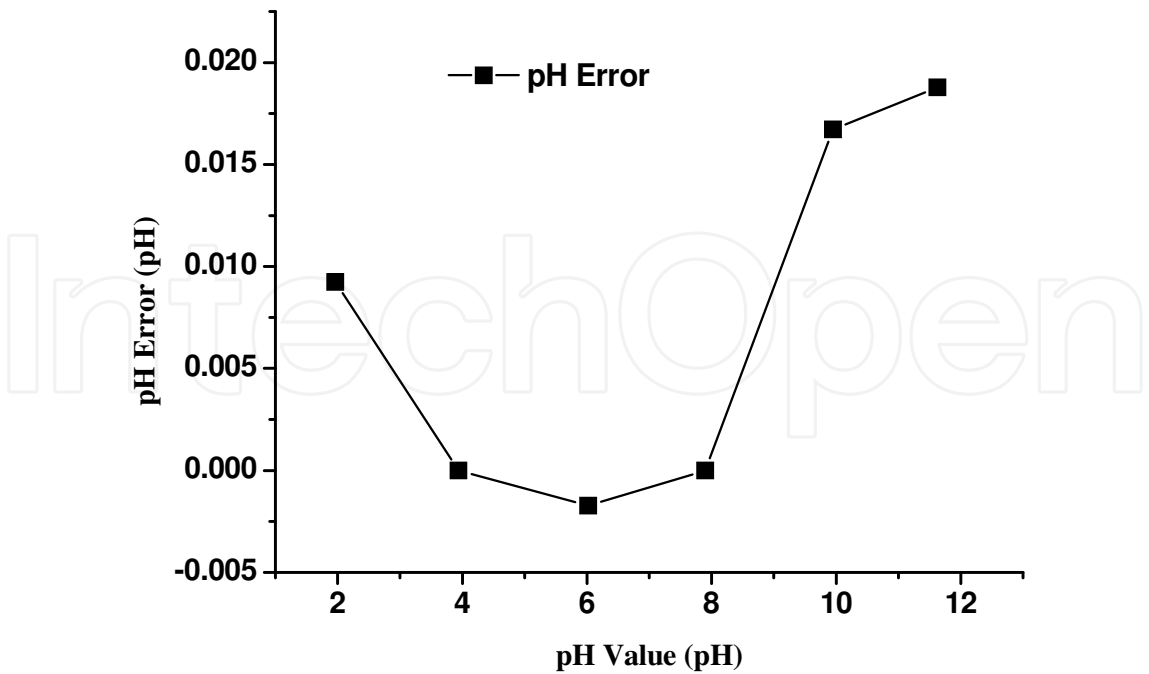Fig. 17. Plot of the digital output versus pH value

Fig. 18. pH error of the proposed pH-to-digital converter

Parameter	pH-to-Digital Converter
Supply Voltage	1.8V
Power Consumption	9.8mW
Dynamic Range	pH2 - pH12
Sensitivity	197 digital counts/pH
Gain Error	2%
pH Error	±0.02pH
Sampling Frequency	6.25MHz

Table 1. Performance summary

3. Conclusion

A CMOS ΣΔ pH-to-digital converter has been developed for continuous monitoring of H⁺-ion concentrations in this research. The ΣΔ pH-to-digital converter, constructed using EGFET-OP to realize switched-capacitor (SC) ΣΔ converter, converted directly the H⁺-ion concentration into digital form. First order low pass ΣΔ modulator constructed using EGFET-OP was used to transfer the signal into digital. Through an on-chip simple digital filter realized by 14-bits up-down counter, the digital average value of the comparator was obtained after shifting the bits of the output code depending on the sampled numbers. The high frequency quantization noise was filtered out. The circuit (without pad) occupied an area of 0.66mm × 0.43mm. The sensitivity of the pH-to-digital converter is about 197 digital counts/pH. This chip, fabricated in a 0.18-um CMOS 1P6M process, operated at a 1.8V supply voltage and normal sampling rate of 6.25MHz. The linearity errors of the converter in the H⁺-ion concentration range between pH 2 and pH 10 is less than 2%, and the minimum detectable pH value can reach as small as ±0.02pH.

4. Acknowledgment

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