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2

Main RF Structures

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1. Introduction

The low noise amplifiers – LNA and the mixers are among the most used structures used in RF integrated circuits. Therefore the goal of this chapter is to present an analysis overview of them as well as the main considerations of their design. Nevertheless, since their interconnections play an important role on performance and noise isolation, this chapter will also describe their AC and DC coupling.

2. Inter-connection

Consider initially a simple common source amplifier stage, with the load impedance Z_L, as given in Fig. 1. Consider also the simplified transistor model as shown in Fig. 2.

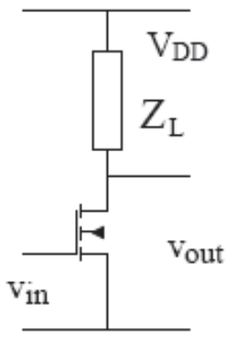

Fig. 1. Simple common source stage.

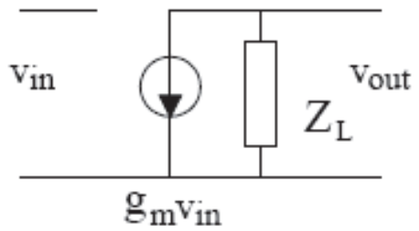

Fig. 2. Simplified circuit model of Fig. 1.

The gain of this stage can be easily calculated as below.

$$A_v = \frac{V_{out}}{V_{in}} = -g_m Z_L \tag{1}$$

Assume this common source stage drives the gate of the following circuit. This next stage needs proper biasing. Usually the DC bias of one stage does not interfere with the bias of another stage, thus the output of the common source stage and the input of the following stage are separated by a DC block capacitor as indicated in Fig. 3. Usually, the biasing resistor R_{bias} is large enough to prevent RF or analog signal from flowing into a bias source.

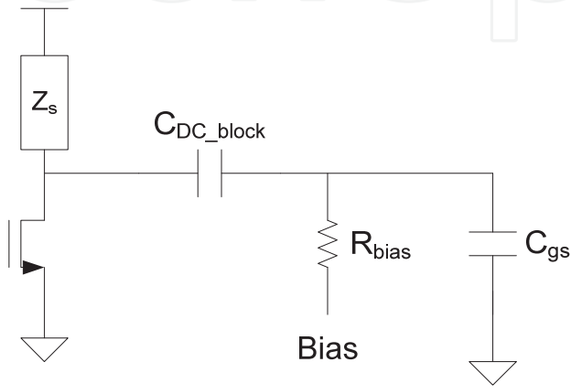

Fig. 3. AC coupling with DC block capacitor.

At high frequency, the effect of the DC block capacitor is negligible, since the DC block capacitor is virtually short. The effect of the large biasing is also negligible since it is connected in parallel with the drain resistor of the first stage. The simplified circuit model is presented in Fig. 4.

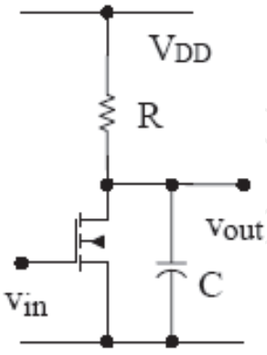

Fig. 4. Common-source stage with RC-load.

When no inductor is used, the only available load is RC-load, thus the load amplifier becomes:

$$Z_L = \frac{R}{1 + RCs} \tag{1}$$

The circuit topology of Fig. 4 is well known and corresponds to a low pass filter configuration. The frequency response of this filter is shown in Fig. 5 and its gain is given by:

$$A_v = -\frac{g_m R}{1 + RC} \tag{2}$$

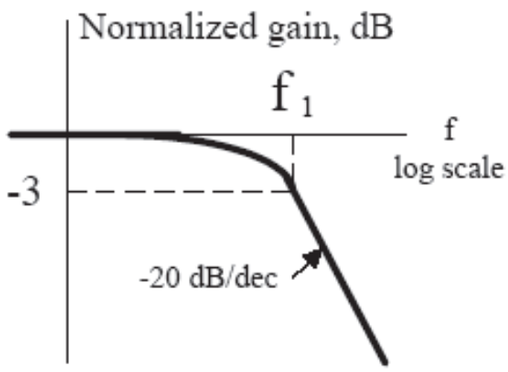

Fig. 5. Frequency response of Fig. 4.

Hence, the DC gain is $-g_m R$ and the bandwidth is $\omega_1 = 1/RC$. The frequency ω_1 is called "uncompensated bandwidth". After frequency ω_1 the gain decreases at the rate of -20dB/dec.

Unfortunately, at low frequency, the effects of DC block capacitor and the bias resistor are more severe, since the equivalent circuit, at low frequency, is a high pass filter.

Therefore, one can expect huge loss of information at very low frequencies for some applications such as Direct-Conversion transceiver, which carries information around DC. Even for DC-free applications, the cutoff frequency should be considered for the high pass filter. Since the 3dB cutoff frequency is defined as 1/RC, one can increase resistance and capacitance. However the capacitor normally occupies more space in integrated circuit than a resistance. Therefore, only the resistance should be increased, only up to few Mega ohms, so that a smaller capacitance can be used.

2.1 DC coupling

As reviewed in previous section, the AC coupling is suitable for RF circuitry, but may present DC blocking problems for baseband analog circuitry. Thus, if information around DC is concerned, one should integrate blocks with DC coupling. The DC coupling consists of combining two blocks so that the DC output voltage level of the previous block is same as the DC input bias voltage of the following block, and thus there is no reason to insert a DC block capacitor between them. The DC coupling is certainly advantageous at low frequency, and since the common-source stage model of Fig. 4 is valid for both low and high frequency, it is also suitable for high frequencies; nevertheless it may restrict the freedom of biasing.

Since the modern integrated technology allows construction of inductors, the designer should know the advantages the inductor can add in the circuit design. This section shows how to enhance the bandwidth using the 'shunt-peaking' technique. It consists of adding an inductor in series with the resistor, as shown in Fig. 6.

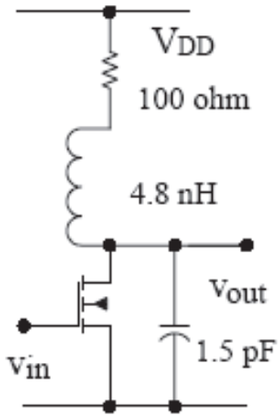

Fig. 6. Common-source stage with RLC-load.

The load impedance for this case becomes:

$$Z_L = (R + Ls) \,||\, \frac{1}{Cs} = \frac{R + Ls}{(R + Ls)Cs + 1} \tag{3}$$

And, substituting this value in (2), one can find that:

$$A_v = -\frac{g_m(R + Ls)}{(R + Ls)Cs + 1} = -\frac{g_m R\left[s(L/R) + 1\right]}{s^2 LC + sRC + 1} \tag{4}$$

Observe that the inductor added a zero, which always increases the bandwidth, and also two poles. These poles can be complex conjugate, and this also can increase bandwidth, yet they introduce peaking, hence the name of the method. On the other side, the difference between the number of finite poles and finite zeros is still one. This means that the asymptotic decrease of gain is the same as in the previous circuit, –20 dB/dec. Thus the inductor allows modifying the gain locally, in the vicinity of the frequency ω_1, and the designer should use this possibility to his/her advantage.
Consider the amplitude of the frequency response for this circuit, given as

$$\left|A_v(j\omega)\right| = g_m R \sqrt{\frac{(\omega L/R)^2 + 1}{\left(1 - \omega^2 LC\right)^2 + (\omega RC)^2}} \tag{5}$$

To facilitate subsequent derivations, it is introduced a factor *m*, defined as the ratio of the *RC* and $\tau = L/R$ time constants,

$$m = \frac{RC}{L/R} = \frac{R^2}{L/C} = \frac{R^2}{\rho^2} \tag{6}$$

Here $\rho = \sqrt{L/C}$ is the wave resistance of the load. This allows writing two more useful relationships, namely, $\tau^2 m = \frac{L^2}{R^2}\frac{R^2}{L/C} = LC$ and $\tau m = \frac{L}{R}\frac{R^2}{L/C} = RC$. Using these relationships (5) can be written as:

$$\frac{A_v(j\omega)}{g_m R} = \sqrt{\frac{(\omega\tau)^2 + 1}{\left(1 - \omega^2\tau^2 m\right)^2 + (\omega\tau m)^2}} \tag{7}$$

The right side of (7) is considered the normalized gain.
First, the bandwidth will be maximized without any consideration regarding the behavior to the gain in the bandwidth. The frequency where the right side equals $1/\sqrt{2}$ is denoted as ω_{-3dB}. Considering a new parameter defined as $x = \omega_{-3dB}\,\tau$, then one has the equation:

$$2\left(x^2 + 1\right) = \left(1 - x^2 m\right)^2 + (xm)^2 \tag{8}$$

or

$$x^4 m^2 + x^2\left(m^2 - m - 2\right) - 1 = 0 \tag{9}$$

From this equation one can find that:

$$x^2 m^2 = -\frac{m^2}{2} + m + 1 + \sqrt{\left(-\frac{m^2}{2} + m + 1\right)^2 + m^2} \tag{10}$$

But:

$$x^2 m^2 = \omega_{-3dB}{}^2\tau^2 m^2 = \omega_{-3dB}{}^2 (RC)^2 = \left(\frac{\omega_{-3dB}}{\omega_1}\right)^2 \tag{11}$$

And maximizing the right side of (10) by proper choice of m one can find the maximum available bandwidth, given as:

$$f_{-3dB}(m) = \sqrt{\left(m^2 - 2m - 2\right)^2 + 4m^2} - m^2 + 2m \tag{12}$$

Differentiating and equating the derivative of (12) to zero, one can obtain:

$$\left(m^2 - 2m - 2\right)(m - 1) + 2m = (m - 1)\sqrt{\left(m^2 - 2m - 2\right)^2 + 4m^2} \tag{13}$$

Squaring both sides of this equation, then:

$$(m - 1)\left(m^2 - 2m - 2\right) = m\left[(m - 1)^2 - 1\right] \tag{14}$$

And from this equation one finally finds that the required value of m is $\sqrt{2}$.
Substituting this value of m in the right side of (10), then:

$$\left(\omega_{-3dB}/\omega_1\right)\Big|_{\max} = \sqrt{\sqrt{2} + 2} = 1.847 \tag{15}$$

Hence the bandwidth is improved nearly two times as shown in Fig. 7. Consider as an example improving the bandwidth from 1 GHz to 1.85 GHz. This is tremendous improvement with the addition of just one inductor.

Unfortunately, however, this choice of m leads to nearly 20% peaking. Indeed, with this choice of m:

$$\left|\frac{A_v(j\omega)}{g_m R}\right|^2 = \frac{x^2+1}{\left(1-x^2\sqrt{2}\right)^2+\left(x\sqrt{2}\right)^2} = \frac{y+1}{2y^2-2\left(\sqrt{2}-1\right)y+1} \tag{16}$$

Where $x=\omega\tau$, and $y = x^2$. Differentiating the right side of (16) and equating the derivative to zero, one obtains that the maximal value of the right side occurs at y obtained from the equation:

$$2y^2+4y-\left(2\sqrt{2}-1\right)=0 \tag{17}$$

The solution of this equation gives y=0.3836, i.e. $x=\sqrt{y}=0.6193=(\omega\tau)\big|_{peaking}$. Therefore:

$$\omega_{peaking}=\frac{0.693}{\tau}=\frac{0.693m}{RC}=\frac{0.693\sqrt{2}}{RC}=0.98\omega_1\approx\omega_1 \tag{18}$$

And the normalized amplitude frequency response has the value of:

$$\left|\frac{A_v(j\omega_{peaking})}{g_m R}\right|^2 = \frac{0.3836+1}{2\cdot 0.3836^2-2\left(\sqrt{2}-1\right)\cdot 0.3836+1}=\left(1.1904\right)^2 \tag{19}$$

This corresponds to a peaking about 1.5dB, as shown in Fig. 7.

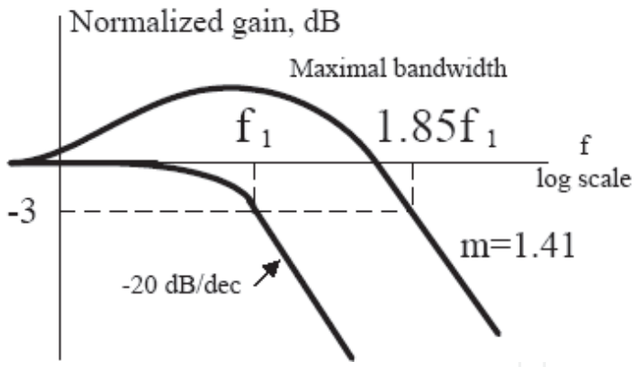

Fig. 7. Frequency enhancement by Fig. 6.

However, there are many applications where the frequency response should be completely free of peaking. Therefore, consider again:

$$\left|\frac{A_v(j\omega)}{g_m R}\right|^2 = \frac{x^2+1}{\left(1-x^2m\right)^2+\left(xm\right)^2} \tag{20}$$

Where $x=\omega$, as it was before, and require that the right side does not have any other maximums, except x = 0. The search of maximum leads to:

$$\begin{aligned} &2x\left(1-2x^2m+x^2m^2+x^4m^2\right) \\ &=\left(x^2+1\right)\left(-4xm+2x^3m^2+2xm^2\right) \end{aligned} \tag{21}$$

One of possible solutions of this equation is $x = 0$. Other solutions can be obtained from the equation:

$$2x^2m+m^2-2m-1=0 \tag{22}$$

One can see that two other solutions will be at $x = 0$ as well, if:

$$m^2-2m-1=0 \tag{23}$$

This gives:

$$m=1+\sqrt{2}=2.414 \tag{24}$$

Direct calculation using (10) shows that this value of m leads to a bandwidth:

$$\omega_{-3dB}/\omega_1=1.707 \tag{25}$$

The corresponding amplitude frequency response is shown in Fig. 8.

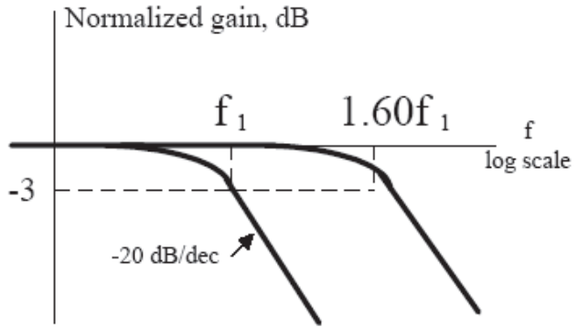

Fig. 8. Maximally flat frequency response.

For this choice of m, both the first and second derivatives of the right side of (20) equal zero at $x = 0$. This amplitude frequency response can be considered as maximally flat. For this reason this choice of m is also very frequently used.

In other situations, there may be a specification on the time response of the amplifier, rather than on frequency response. The amplifier must not only amplify uniformly the various spectral components of the signal over as large a bandwidth as practical, but the phase relationships among its Fourier components must be preserved as well. If all frequencies are delayed by an equal amount of time, then this fixed amount of time delay must represent a linearly increasing amount of phase shift as frequency increases. Phase distortion will be minimized if the deviation from this ideal linear phase shift is minimized. Evidently, then, the delay as the function of frequency must be examined. If this delay is the same for all frequencies, there will be no phase distortion. The delay is defined as

$$T_D(\omega)=-\frac{d\phi}{d\omega} \tag{26}$$

Where ϕ is the phase shift of the amplifier at frequency ω.
Using (4), then:

$$\frac{A_v(j\omega)}{g_m R} = -\frac{1+j\omega\tau}{1-\omega^2\tau^2 m + j\omega\tau m} \tag{27}$$

And from this expression, one can find that:

$$\phi(\omega) = -\tan^{-1}\omega\tau + \tan^{-1}\left(\frac{\omega\tau m}{1-\omega^2\tau^2 m}\right) \tag{28}$$

It is impossible for this amplifier to provide a constant time delay over an infinite bandwidth. It is reasonable to provide, then, with an approximation to a constant delay over some finite bandwidth. A maximally flat time delay will result the number of derivatives of $T_D(\omega)$, whose value is zero at DC, is maximized.
This derivation is rather complicated. Ultimately, however, on may derive the following cubic equation for *m* as:

$$m^3 - 3m - 1 = 0 \tag{29}$$

whose relevant root is:

$$m = 1 + \left(\frac{3+\sqrt{5}}{2}\right)^{1/3} + \left(\frac{3-\sqrt{5}}{2}\right)^{1/3} \approx 3.104 \tag{30}$$

which is corresponding to a bandwidth improvement factor a little bit less than 1.6.
Since the conditions for maximally flat amplitude frequency response and maximally flat time delay do not coincide, one can compromise. Depending on requirements, there is a range of useful inductance value. A larger *L* (smaller *m*) gives the bandwidth extension but poorer phase linearity, whereas a smaller *L* yields less bandwidth improvement but better phase linearity. All considered cases are summarized in Table 1.

Condition	m=R2C/L	Normalized bandwidth	Normalized peak frequency response
Maximum bandwidth	1.414	1.85	1.19
Maximally flat bandwidth	2.414	1.707	1
Maximally flat time delay	3.104	1.6	1
No shunt peaking	∞	1	1

Table 1. Shunt peaking design summary.

3. Low noise amplifier

Low noise amplifier – LNA is the most critical block in the receiver signal chain, since it determines the overall noise Fig. of the received signal, so that it determines the quality of communication system.
There are several issues on LNA design for UWB applications. First, it must provide wideband impedance matching for both optimal power transfer and noise characteristic. Second, it should be a low power implementation with high power gain. According to the

802.13a specification [1] [2], it is required a power gain of at least 15dB with less than 3dB noise Fig. Since, one of the biggest applications of UWB systems is low-power implementation, the LNA should be able to operate in low supply voltage. The third issue is gain flatness to avoid any signal distortion over such a wide bandwidth.
In terms of wideband impedance matching, the most popular methods are the feedback topology, the distributed impedance matching, the BPF configuration matching network, and the common-gate topology. Nevertheless, each method has advantages and disadvantages, so it is difficult to select one single method for UWB LNA design. For example, feedback topology has good noise and impedance matching performance, but degrades the achievable power gain. The other side, BPF configuration matching is able to achieve high power gain with spurious impedance matching performance in addition to great frequency selection characteristics, while increasing noise Fig. with more passive components used to implement the filter.
This section discussed a unique UWB CMOS LNA, which utilizes both feedback, and BPF configuration method, as presented in [3].

3.1 LNA circuit synthesis

In general, it is very difficult to establish a systematic method for LNA design with satisfying simultaneously low noise factor, impedance matching, and high gain. The major difficulty comes from the fact that the optimal source impedance for optimal noise is different from the matching condition for maximum power delivery. So it is very important to confirm initial design decisions of circuit parameters because two matching conditions are highly related. Also, too simplified circuit model forces trial-and-error strategy for optimizing the circuit. Therefore, accurate circuit evaluation is required to avoid the tedious effort for circuit optimization. Thus, the accurate Miller effect of source degenerative topology with cascode topology, and a methodology to utilize the Miller effect for the input matching network implementation are presented in this section.
The overall LNA schematic, including input and output impedance matching network, is shown in Fig. 9. The LNA looks like a simple conventional narrowband LNA with one gate

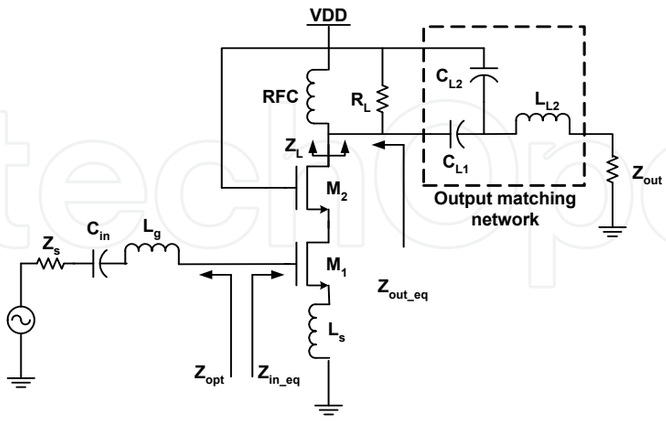

Fig. 9. Overall LNA architecture.

inductor. However, the LNA can achieve wideband input matching by using Miller effect as explained later. Also, the UWB LNA architecture does not make use of a source follower for output matching, but has passive output matching network, which consists of bandpass filter and impedance inverting scheme.

3.2 Transistor sizing and bias condition

Since the size of transistors and their bias condition determine power dissipation, it is often recommended to establish them under a certain power budget. However, the size of transistor versus its bias condition should be evaluated carefully, because they are also related to impedance seen by input gate. Thus, the best choice is to determine the size and bias condition to satisfy both impedance matching and noise matching with limited bias current. In fact, there is no much freedom for this choice technically. According to the MOSFET noise analysis [4], the generator admittance for optimal noise performance is known as (31) and (32).

$$G_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}\left(1-|c|^2\right)} \tag{31}$$

$$B_{opt} = -\omega C_{gs}\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{32}$$

where $\alpha = g_m/g_{d0}$, the parameters δ and γ are given in Chapter 3, and c is defined as the correlation between the drain noise i_{nd} and the gate noise i_{ng} currents, given as:

$$c = \frac{\overline{i_{ng}.i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}.\overline{i_{nd}^2}}} \tag{33}$$

For the sake of simplicity, initially the correlation of noise can be ignored, so that c has to be 0. Therefore, (31) and (32) can be simplified as:

$$R_{opt} \approx \frac{1}{\alpha\omega C_{gs}}\sqrt{\frac{5\gamma}{\delta}} \tag{34}$$

$$X_{opt} \approx \frac{1}{\omega C_{gs}} \tag{35}$$

Furthermore, (35) can be modified to (36) in order to take account of the degenerative inductor at the source-end.

$$X_{opt} \approx \frac{1}{\omega C_{gs}} - \omega L_s \tag{36}$$

Note that expressions (34) and (35) represent real and imaginary terms of impedance, while (31) and (32) presents admittance expressions.

Observe from expression (36) that the imaginary term of the optimal noise generator impedance is inversely proportional to the gate-source capacitance. Since the gate-source capacitance is always positive, than noise matching can be achieved with inductive generator impedance. However, increasing L_s will reduce the gain, but at the same time, the inductive term of generator impedance (L_g) can be decreased. According to the above observation, it is clear that optimal noise condition and maximum power transfer are obtained simultaneously when $Z_{opt} = Z_{in\_eq}^*$, where Z_{in_eq} is the equivalent input impedance seen by input gate of amplifying transistor given as:

$$Z_{in\_eq} = R_{in\_eq} + jX_{in\_eq} = \frac{g_m L_s}{C_{gs}} + j\left(\omega L_s - \frac{1}{\omega C_{gs}}\right) \tag{37}$$

However, it is not easy to make both Z_{opt} and $Z_{in\_eq}^{*}$ to have same value. Nevertheless, high gain can be achieved if the inequality shown in (38) is satisfied. Obviously, smaller resistive term of input impedance seen by gate-end leads higher gain.

$$R_{in\_eq} \le R_{opt} \le Z_s \tag{38}$$

where Z_s is the source impedance.
Since the reactance term of Z_{opt} and $Z_{in\_eq}^{*}$ are almost always matched according to (36) and (37), inequality (38) will force Z_{in_eq} to be positioned in outer side of Z_{opt} in Smith chart until the frequency exceeds the desired frequency range.
As mentioned already, the bias condition should be achieved under a limited current, thus I_{DS} is a limited value. For the sake of simple procedure, assumed the g_m and C_{gs} are given as (39) and (40), which ignore overlapped channel length L_{ov}, The initial value of V_{eff} is given by (40).

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{eff} \tag{39}$$

$$C_{gs} = \frac{2}{3} WLC_{ox} \tag{40}$$

$$V_{eff} \le \frac{2Z_s L^2}{3L_s \mu_n} \tag{41}$$

Note that considers minimum channel length L. Once V_{eff} is obtained, then the minimum value of g_m is:

$$g_m \ge \frac{2I_{DS}}{V_{eff\_\max}} \tag{42}$$

where V_{eff_max} is the maximum effective voltage.
Assume, roughly, that $\gamma \approx 2$, $\delta \approx 4$ and $\alpha \approx 5$, since $g_{ds} \approx 0.2 g_m$ in active region, so that (34) can be simplified even more as:

$$R_{opt} \approx \frac{1}{\sqrt{10}\omega C_{gs}} \tag{43}$$

Finally, the minimum channel width W given in (44), is based on (38), (40) and (43):

$$W \ge \frac{3}{2\sqrt{10}\omega Z_s L C_{ox}} \tag{44}$$

Again, minimum channel length is assumed and the results are roughly selected so that they must be optimized later. The obtained Z_{opt} and Z_{in_eq} are shown in Fig. 10 over the frequency range of 100MHz to 20GHz, and one can notice that $Z_{in\_eq}^{*}$ is almost matched to Z_{opt}. $Z_{in\_eq}^{*}$

remains positioned in outer circle of Z_{opt} in Smith chart up to $6GHz$, which is higher than the desired frequency range.

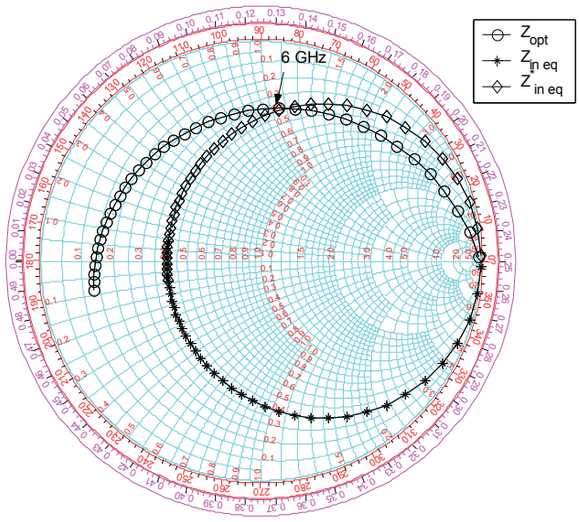

Fig. 10. Zopt, Zin_eq, and Zin_eq*.

The obtained condition so far should be applied to M_1 in Fig. 9.

3.3 Miller effect in cascode topology

The Miller effect implies that the effective capacitance is increased by negative voltage gain between input and output. However, since the input impedance of the cascode device M_2 is capacitive, the voltage gain is high in low frequency and low in high frequency, which implies the effective Miller capacitance will be high in low frequency and low in high frequency. Therefore, it explains that the Miller effect creates not only a single capacitor, but also an inductor in parallel with the Miller capacitor.

The input impedance Z_{Load} of the cascode device M_2 seen at the source of M_2 is described as

$$Z_{Load} = \frac{R_{ds2} + Z_L}{1 + g_{m2}R_{ds2} + sC_{gs2}\left(R_{ds2} + Z_L\right)} \tag{45}$$

where Z_L is the output load connected to drain of M_2, and this is assumed as pure resistor over the frequency of interest, for simplicity.

The load impedance of the cascode device, therefore, can be expressed as R and C parallel circuit as shown in Fig 11, whose values are:

$$C_{Load} = C_{gs2} \tag{46}$$

$$R_{Load} = \frac{R_{ds2} + Z_L}{1 + g_{m2}R_{ds2}} \tag{47}$$

The resistance term of the cascode load is equal to $1/g_{m2}$, when R_{ds2} is infinite. Note that the R_{ds2} is relatively large for low power design due to the relation $R_{ds} = 1/\lambda I_{DS}$, where λ is the depletion length coefficient (channel length modulation), and I_{DS} is the bias DC current, which is small for low power design.

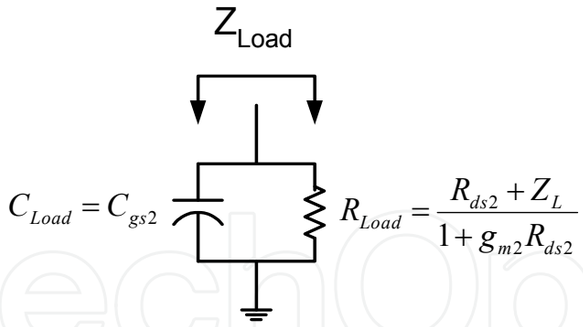

Fig. 11. Input impedance of cascode device M_2.

The effective transconductance for source degenerative topology can be obtained as:

$$G_m = \frac{g_{m1}}{1 + g_{m1}L_s s + C_{gs1}L_s s^2} \tag{48}$$

Thus, the overall open voltage gain A_{vo} is:

$$A_{vo} = -G_m Z_{Load} = \frac{-g_{m1}(R_{ds2} + Z_L)}{\left(1 + g_{m1}L_s s + C_{gs1}L_s s^2\right)\left(1 + g_{m2}R_{ds2} + C_{gs2}(R_{ds2} + Z_L)s\right)} \tag{49}$$

According to the non-flat open voltage gain between gate and drain of M_1, the Miller capacitor is not a simple capacitor anymore, but an RLC combination circuit.
The Miller capacitance C_{mil} is:

$$C_{mil} = (1 - A_{vo})C_{gd1} == \left(1 + \frac{g_{m1}(R_{ds2} + Z_L)}{\left(1 + g_{m1}L_s s + C_{gs1}L_s s^2\right)\left(1 + g_{m2}R_{ds2} + C_{gs2}\left(R_{ds2} + Z_L\right)s\right)}\right)C_{gd1} \tag{50}$$

Finally, the overall Miller impedance caused by the non-flat voltage gain is:

$$Z_{mil} = \frac{1}{sC_{mil}} \approx \frac{s^2 L_s(C_{gs1}g_{m2} + C_{gs2}g_{m1}) + s(C_{gs2} + L_s g_{m1}g_{m2}) + g_{m2}}{s^3 C_{gd1}L_s(C_{gs1}g_{m2} + C_{gs2}g_{m1}) + s^2 C_{gd1}(C_{gs2} + L_s g_{m1}g_{m2}) + sC_{gd1}(g_{m1} + g_{m2})} \tag{51}$$

Note that non dominant terms are eliminated for the sake of simplicity.
The equivalent impedance given by Miller effect is indicated in Fig. 12, whose values of individual components are:

$$C_{mil1} = \frac{C_{gd1}(g_{m1} + \alpha)}{\alpha} \tag{52}$$

$$C_{mil2} = \frac{C_{gd1}(g_{m1} + \alpha)}{g_{m1}} \tag{53}$$

$$L_{mil1} = \frac{L_s g_{m1}(C_{gs1}\alpha + C_{gs2}g_{m1})}{\alpha(g_{m1} + \alpha)} \tag{54}$$

$$R_{mil1} = \frac{g_{m1}(C_{gs2} + L_s g_{m1}\alpha)}{C_{gd1}(g_{m1} + \alpha)^2} \tag{55}$$

where $\alpha=1/R_{Load}$.
Note that the resistive term R_{mil1} is related to the quality factor of the inductive term L_{mil1}, and it is relative small enough to be ignored.

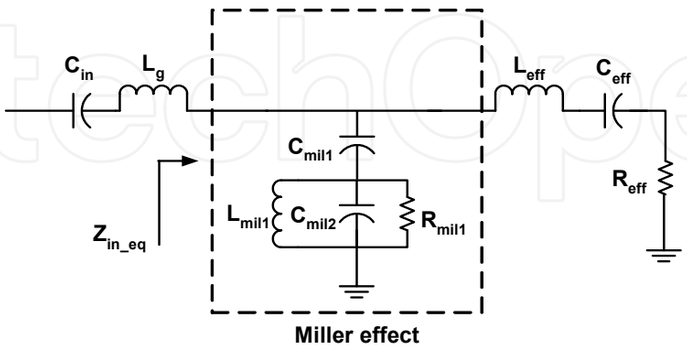

Fig. 12. Equivalent input circuit.

3.4 Modified input impedance by feedback

Now, the input impedance of the inductive degenerative topology including Miller effect must be re-evaluated.
The input impedance of the open circuit is well known as RLC series circuit, given as:

$$Z_{ino} = sL_s + \frac{1}{sC_{gs1}} + \frac{g_{m1}L_s}{C_{gs1}} \tag{56}$$

From the feedback system, the modified input impedance of the feedback system, as shown in Fig. 13, is given by:

$$Z_{inc} = \frac{Z_{ino}(Z_f + Z_{load})}{Z_{ino}(1 + G_m) + Z_L + Z_f} \tag{57}$$

Note that the close loop input impedance includes the Miller effect.
The feedback impedance Z_f is $(1/sC_{gd1})$, which is the gate-to-drain capacitor. By using the effective transconductance and load impedance as obtained above, the overall expression of the input admittance Y_{inc} of the close loop circuit after simplification is:

$$Y_{inc} = Y_{mil} + \frac{1}{\frac{1}{R_{eff}} + sC_{eff} + \frac{1}{sL_{eff}}} \tag{58}$$

where Y_{mil} is $1/Z_{mil}$, the admittance of the equivalent Miller circuit, and:

$$R_{eff} = \frac{g_{m1}L_s}{C_{gs1}}\left(1 + \frac{C_{gd1}R_{ds2} + 2C_{gs2}R_{ds2}}{g_{m1}L_s(1 + g_{m2}R_{ds2})}\right) \tag{59}$$

$$C_{eff} = C_{gs1} \tag{60}$$

$$L_{eff} = L_s + \beta \tag{61}$$

$$\beta = \frac{(R_{ds2} + Z_L)\left(C_{gd1}\left(g_{m1}\left(L_s + g_{m2}L_sR_{ds2}\right) + C_{gs2}\left(R_{ds2} + Z_L\right)\right) + C_{gs2}\left(2g_{m1}\left(L_s + g_{m2}L_sR_{ds2}\right) + C_{gs2}\left(R_{ds2} + Z_L\right)\right)\right)}{C_{gs1}\left(1 + g_{m2}R_{ds2}\right)^2} \tag{62}$$

Thus, the actual RLC series circuit is changed by the feedback effect. The feedback effect effectively increases the inductive term L_{eff} and resistive term R_{eff} from the original open circuit input impedance Z_{ino}.

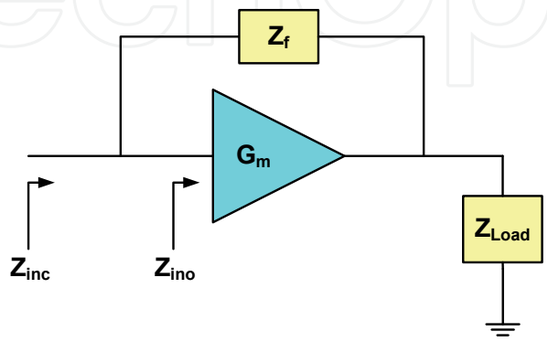

Fig. 13. Feedback system with effective transconductance.

For large R_{ds2}, the equivalent circuit can be further simplified as:

$$R_{eff} \approx \frac{g_{m1}L_s}{C_{gs1}}\left(1 + \frac{C_{gd1} + 2C_{gs2}}{g_{m2}}\right) \tag{63}$$

$$L_{eff} \approx L_s + \frac{C_{gd1}C_{gs2} + {C_{gs2}}^2 + C_{gd1}g_{m1}g_{m2}L_s + 2C_{gs2}g_{m1}g_{m2}L_s}{C_{gs1}{g_{m2}}^2} \tag{64}$$

Therefore, overall input impedance can be expressed as Fig. 12.
Note that the C_{mil1} can be ignored in high frequency and R_{mil1} also can be ignored due to its small value, so that the overall circuit can be considered as the combination of parallel LC and series LC circuits. The circuit also can be considered as a part of bandpass filter.

4. Mixer

Mixers are non-linear devices used in systems to translate from one frequency to another. All mixer types work on the principle that a large Local Oscillator – LO drive will cause switching/modulating the incoming RF into an Intermediate Frequency – IF, or in opposite direction.
There are two types of mixer, passive and active. Generally the passive types have better IM3 performance, but present higher conversion losses and hence higher noise Fig.s than active mixers.
Additionally, mixers can also be classified as single balanced mixers and double balanced mixers. Single balanced mixers are much less complex, but have inferior performance in terms of RF to IF and LO to IF rejection, compared to double balanced mixers.
The advantages of double balanced mixers are:

a. Both LO and input signals are balanced, providing both LO and input rejection at the output.
b. All ports of the mixer are inherently isolated from each other.
c. Higher linearity, compared to singly balanced.
d. Improved suppression of spurious products (all even order products of the LO and/or the input are suppressed).
e. Higher intercept points.
f. Less susceptible to supply voltage noise due to differential topology.

The disadvantages are:

a. Require a higher LO drive level.
b. Require differential input and LO signal.
c. Ports are highly sensitive to reactive terminations.

The Gilbert double-balanced mixer configuration is widely used in RFIC applications because of its compact layout and moderately high performance. This section will walk through the design of a CMOS Gilbert mixer focusing on the parameters that influence the linearity of the signal path, the noise, and therefore the spurious-free dynamic range of the mixer. Finally, some techniques to enhance the bandwidth of the Gilbert mixer will be also presented, so to be suitable for UWB applications.

4.1 Design guidelines

Depending on the application, the mixer may be designed with a low Single Side Band – SSB noise Fig., a particular gain or a high linearity. A good starting point is to use the differential LNA and add the switching transistors with the same W/L ratios.

As in the case of LNA design, the linearity of the mixer source can be increased by adding degeneration resistors (or inductors). As an example consider Z_S inserted in the sources of M_1 and M_2 in the circuit of Fig. 14.

There are several parameters to be achieved during the design process, such as device width, biasing, linearity of transconductance amplifier (input circuit), stability, input matching network, gain compression, Inter Modulation Distortion – IMD, noise Fig. and spurious free dynamic range.

Though the design method introduced here emphasizes the distortion-limited (large-signal) performance over noise-limited (small-signal) performance, there are many design choices possible. In Fig. 14, one may have to decide proper bias current and device width W_1, and W_2. Proper selection of W_1 should provide high g_m, saturation at low V_{DS} (for low power supply operation) and low noise. Large widths are preferred for noise, but the optimum width for both noise and power constraints can be estimated from the MOS device parameter [1]. Large widths also require large bias currents to obtain high g_m. Choosing $W_1 = W_2$ is typically the best approach.

The minimum current required to keep all devices in saturation must also be considered. Additionally, once the bias is determined, the linearity of signal path must be verified. The signal path from the transconductance amplifier through the source resistance and inductance is the dominant for the sake of linearization. As the resistance increases the linearity also increases, but the conversion gain also decreases to some degree. Source inductance is used mainly to guarantee stability by forcing a positive real component into the input impedance. This also helps to make the input impedance easier to match.

4.2 Device width and bias current

From Fig. 14, the voltage gain of the mixer with source degeneration is given by:

$$\frac{V_{out}}{V_{in}} \approx \frac{2}{\pi}\left(\frac{Z_L}{Z_s + \frac{1}{g_m}}\right) \tag{65}$$

This equation implies lower conversion gain with larger impedance at the source of M_1 and M_2, as expected. However, this equation does not provide a clue to determine the device width.
From the analysis of noise optimization, the optimal width can be found as [4]:

$$W_{opt} = \frac{1}{3\omega L C_{ox} R_{gen}} \tag{66}$$

where R_{gen} is the resistance of the source connected to the mixer input, typically 50 Ω, but sometimes determined by LNA output impedance.
For this width, I_{DS} must be large enough to saturate the MOSFET ($V_{DS} > V_{dsat}$). At the same time, large V_{DS} is undesirable, specially for low V_{DD} operation. Finally, large V_{DS} will increase hot electron effects at the drain, thereby increasing noise.

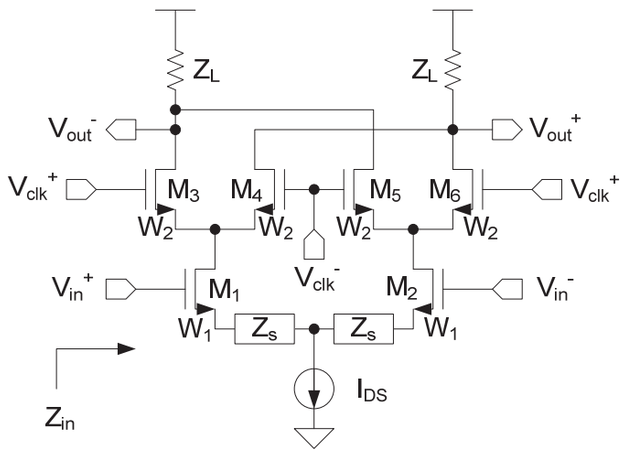

Fig. 14. Basic circuit of the Gilbert Cell Double Balanced (DB) Mixer.

4.3 Linearity of signal path

In order to investigate the linearity of the signal path, a transfer characteristic can be simulated by sweeping the input DC voltage. Consider the example given in Fig. 15. Note that the DC input voltage V_{Din} is $V_{in} - V_{ref}$.
It is expected that by increasing the resistance R_s, which increases negative feedback, the transfer characteristic would be linearized, by exchanging gain for linearity. In the simulation shown in Fig. 16, it can be seen that the gain (slope) becomes more linear over a wider input voltage range as R_s is increased.
A popular technique in low voltage RFIC design is to substitute resistors by inductors. This has the advantages that the ideal inductor does not add noise to the circuit, and it reduces the supply voltage requirement for the circuit. The effectiveness of this approach is somewhat frequency dependent. At low frequency, the gain degeneration and linearity improvement for reasonable sized inductors is limited, but it becomes more effective at higher frequencies.

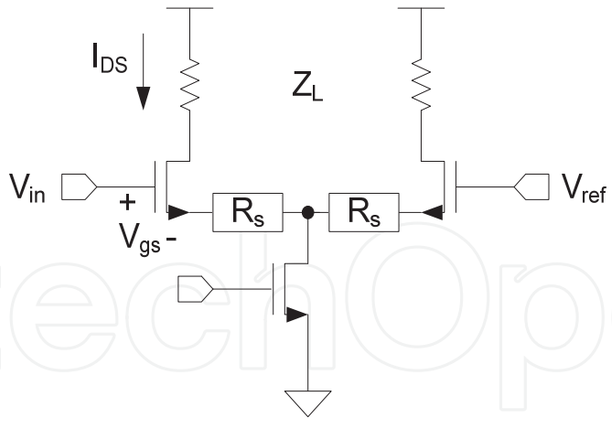

Fig. 15. Setup for transfer characteristic simulation.

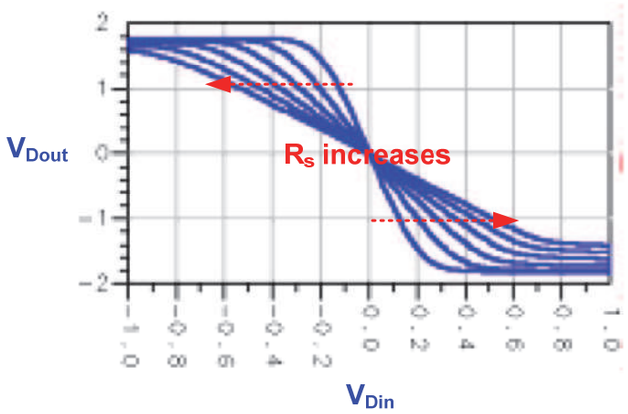

Fig. 16. DC input voltage sweeping for linearity simulation.

Also, inductors on Si substrates have low Q, on the order of 2 to 3. For a Q of 2.5, for example, a 5 nH inductor at 4GHz would have a series resistance of about 50Ω, thus, in fact both resistance and inductance are being added to the circuit. Therefore, it is valuable to investigate the effect of both inductor and resistor as Z_s.

4.4 Input impedance and stability

As explained earlier, the input impedance seen at gate of source degenerative topology with impedance Z_s is:

$$Z_{in}(j\omega) = \frac{1}{j\omega C_{gs}} + Z_s + \frac{\omega_T Z_s}{j\omega} \tag{67}$$

where $\omega_T = g_m / C_{gs}$.

Expression (67) was derived from a simple small-signal analysis; it neglected C_{gd} and assumed that the node between the source resistors is at virtual ground. As summarized in Table 2, if the source noise impedance Z_s is purely resistive, it is equivalent to an R and two series capacitors. If R is large, the equivalent input series capacitive reactance is large and has a large effect on Z_{in}. The real part is clearly positive.

Similarly, a series inductance L produces a non-frequency dependent positive real part and a series LC resonant network. Only the capacitor produces a negative resistance, a condition desirable for oscillators, not mixers, and with unusual frequency dependence. Therefore, negative input resistance can be avoided eliminating the possibility of using a capacitor.

Z_s	$\mathrm{Re}[Z_{in}] + \mathrm{Im}[Z_{in}]$
R	$R + \left(\frac{\omega_T R}{j\omega} + \frac{1}{j\omega C_{gs}} \right)$
L	$\omega_T L + \left(\frac{1}{j\omega C_{gs}} + j\omega L \right)$
C	$-\frac{\omega_T}{\omega^2 C} + \left(\frac{1}{j\omega C_{gs}} + \frac{1}{j\omega C} \right)$

Table 2. Summary of input impedance according to impedance at source.

Unfortunately, however, there is some parasitic capacitance between source and bulk of the transistors, as indicated in Fig. 17. Therefore, as R_s increases, the shunt C_{SB} effect on the source impedance increases, thus driving the input impedance negatively. If $\omega_T R_s C_{SB} > 1$, a negative real Z_{in} will show up. For this reason, it may be necessary to add some series inductance to compensate the negative resistance.
Expression (68) describes the resistive input impedance by considering the presence of C_{SB}.

$$\mathrm{Re}\{Z_{in}\} = \frac{R_s\left(1 - \omega_T R_s C_{SB}\right)}{1 - \omega^2 {R_s}^2 {C_{SB}}^2} \tag{68}$$

An extrapolation of i_D - v_{DS} intercepts the v_{DS} axis at $v_{DS} = -V_A$, known as Early voltage. For a given process, V_A is proportional to L, selected by the designer. Typically, VA is in the range of 5 V/μm to 50 V/μm.

4.5 Output resistance

So far, only inside of Gilbert cell mixer has been discussed. In fact, signal bandwidth at both input and output is another critical problem for UWB mixer. Therefore, input and output bandwidth enhancements are also necessary.
For integrated circuits, there is no restriction of intermediate impedance between blocks. In fact, the shunt-peaking method is widely used for bandwidth enhancement and interconnection between blocks. However, it is sometimes necessary to provide a specific impedance value for both input and output (in many cases 50 Ω), thus the wideband impedance matching methods can be applied. The applicable methods for bandwidth enhancement are:

a. *Shunt-peaking: suitable* for conjugate matching with non-standard intermediate impedance.
b. *Wideband matching method*: suitable for both conjugate matching and standard impedance matching, but requires more passive components.
c. *Cascode topology*: applicable for both previous methods, in addition by reducing RC constant time.

Since cascode topology reduces voltage gain between gate and drain of transconductance amplifier, it reduces the effect of the gate-drain capacitance, the so called Miller effect. However, if cascode topology is applied to reduce Miller effect, one have to consider reduced overhead voltage by voltage drop through drain to source of the cascode device.

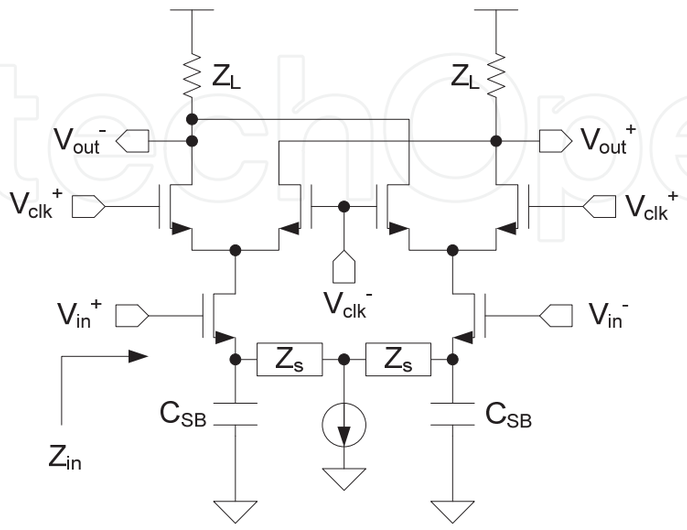

Fig. 17. Gilbert cell mixer with source to bulk capacitance.

5. Conclusions

This chapter provided the background foundations for the analysis and design of low noise amplifiers and mixers, along with their interconnections to other structures. Low noise amplifiers and mixers are among the most used structures in RF IC.

The performance of them may be compromised without proper interconnection. This chapter also presented the approaches to implement AC and DC coupling to interconnect structures, by taking into account performance and noise isolation.

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