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Energy Dissipation Minimization in Superconducting Circuits

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1. Introduction

Low energy dissipation and ability to operate at low temperatures provide for Josephson junction circuits a niche as a support for low temperature devices. With high speed operation (Chen W. et al., 1999) capability the Josephson junction circuits make a prime candidate for applications which are difficult to engineer with existing CMOS technology. The development of Josephson junction technology took a major turn for the better with the invention of the Rapid-Single-Flux-Quantum (RSFQ) devices (Likharev K.K. et al., 1991), an improvement over voltage biased Josephson Junctions logic which were plagued with the junction switching and reset problems. The modern applications of SFQ circuits extend to a larger range of temperature operation and the applications vary from low temperature magnetic sensor, to high speed mixed signal circuits, voltage and current standards (Turner C.W. et al., 1998), and auxiliary components for quantum computing circuits. Most of the SFQ circuits are fabricated with Niobium, but Aluminum based circuits are being used for quantum gates (Nielsen M.A. et al., 2000) and qubit operations. SFQ circuits based on Magnesium di-Boride junctions are being developed for higher temperature operations (Tahara S. et al., 2004). Predominantly most of the Josephson junction circuits today are operated at around 4K. All the circuits are optimized usually for liquid helium temperatures, so the circuits operated in helium bath Dewars or cryostat's do not experience any temperature gradients or drift effects which can affect the operating margins.

With the improvement in the fabrication technology and soft-wares for SFQ circuit technology, the designing complex circuits have become easier. Complex Circuits with over 20K junctions such digital synthesizer and digital RF Trans-receiver have already been demonstrated (Oleg M.A. et al., 2011). Development of circuits over 100K junctions are actively under progress. However, with enormously large circuits, power requirements also increase.

Looking at the range of applications and complexity of the problems of energy minimization, we try to look at the problem in two approaches. One for large complex circuits, we try to reduce the power bias itself, or the overall load of current that is supplied

to the chip. And secondly, we try to improve the operation of the circuit blocks by designing components that can be operated in power independent mode.

The proposals made here should be applicable to all operations to make the maximum benefit of the advantage of the design. To operate at lower temperatures such as in milli-Kelvin ranges, required for quantum computing, the junctions and circuit components have to be scaled. The cells, modules or blocks used in design of building larger parts of circuits, are modified in a way such that the cells are capable of maintaining the state of the logic even when the power bias is switched off.

The second and larger energy dissipation source, which can be directly, reduced by lowering the bias current supply. One of the simplest methods of reducing the DC bias current is recycling the bias from one part of the circuit to bias the other parts. This technique called current recycling is a method for serially biasing the circuits. Small scale demonstrations of the technique have been demonstrated a few years ago (Johnson M.W. et al., 2003). We present here some of the results for techniques for over 1k junctions in a single chip and also discuss some of the limitations of these techniques.

2. Background and related work

The problem of power dissipation has been attempted by several groups over the last two decades and the problem has gained more attention based on the new developments of applications into quantum computing technology and wireless technology applications (Tahara S. et al., 2004, Narayana S. 2011). If Josephson SFQ technology has to be extended to quantum computers, which require far fewer junctions but must be operated at much lower temperatures to maintain longer quantum coherence, the issue of power dissipation comes to the forefront.

Despite the numerous advantages, over its semiconductor counterparts, the power dissipation is high in the conventional digital Josephson technology. If the application revolves around quantum computation, the size of circuit is small but power dissipation could seriously disrupt the quantum operations. On the other hand, if the circuits being designed are large power dissipation in the bias lines could be larger by several orders of magnitude compared to the power dissipation in single block or cell.

Early efforts of reducing power dissipation were using large inductances connected to the bias resistors. This method was demonstrated for moderate size circuits in (Yoshikawa N. et al., 2001), but operating margins were reported to be reduced at higher frequencies due limitation of L/R time constant compared to the switching frequency. But reducing R also reduces the maximum clock frequency, which limits the high circuit design.

Static power dissipation, largest source of power dissipation, was eliminated by eliminating resistive biasing elements in circuit design (Polonsky S. 1999). An effort to mimic CMOS logic, also to eliminate static power dissipation was presented by (Silver A.H. et al., 2001), but was harder to integrate into SFQ circuits. But the method successfully was designed for high speed circuits. A new RQL logic has been presented which involves multi phase AC bias, which has been known to cause AC crosstalk (Silver A.H. et al., 2006). Another method for static power dissipation was presented in (Kirichenko D.E. et al., 2011), where the JTL is used to a digital controller to supply bias current to the circuits under operation.

3. Power dissipation in RSFQ circuits

Before we go into methods and experiments results, we can go to present a simplified model as which are well studied in Detail (Rylyakov A. 1997). We will just recap some of the main purpose with a numerical example so as to provide a continuation and feel for the value of method presented. Let us begin with a simple model as to get an idea of the power estimated without going into detailed mathematical models. The most power is dissipated in the bias resistors and second source of power dissipation is the shunt resistors in the junctions when junctions are in the resistive state.

If the clock operation has a frequency f , the power dissipation due to the switching of the Josephson junction is

$$P = FE = f\Phi_0 I_C \quad (1)$$

Where, E is the total energy dissipated, I_C is the critical current of the junction and Φ_0 is the quantum flux constant. Now for a critical current of $100\mu\text{A}$, and the clock frequency of 50GHz the power dissipated for a single junction by switching is 10 nW .

Now let us look at the second source of power dissipation, in figure 1, is a Josephson junction network, the junctions are usually biased to a lower value than I_C , about $0.7 I_C$, the junction can switch when a correct SFQ pulse arrives.

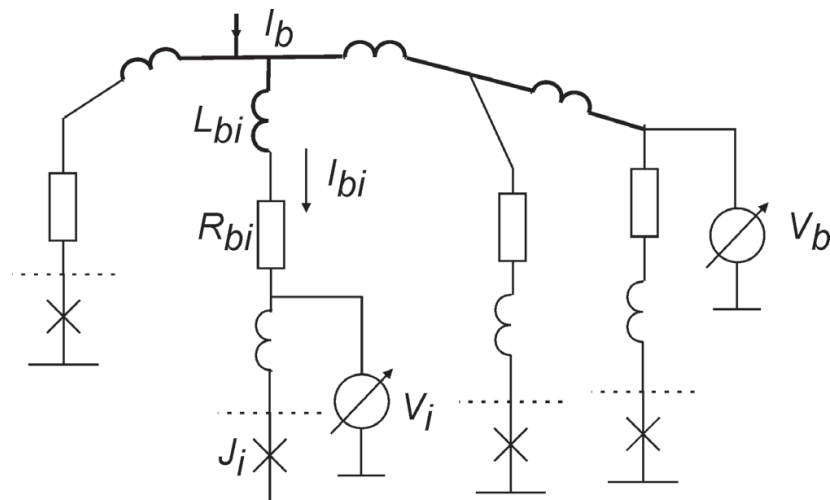


Fig. 1. Josephson junction network

The inductances can L_{bi} and L_{ij} ratios influences the order of switching events and the effects have been studied well in (Chen W. et al., 1999 and references therein) power dissipation. So for a typical power dissipation based on $V = 2.6\text{mv}$, which is the sub band gap of the niobium superconductors, and critical current $100\mu\text{A}$. The power dissipation is $P = VI$, so the power dissipation is $P = 260\text{nW}$, which is nearly 25 times higher in the bias resistors compared to the junctions. In broader context, one can say that, the power dissipation is at least one order of magnitude higher in bias resistors.

3.1 Temperature scaling

With the growing interest in quantum computing and the favorable choice of single flux quantum circuits for its application, we do have to modify a few parameters for better design. Since most of the quantum computing circuits are operate in milli- Kelvin range, we

present a simple scaling method to avoid errors in design of SFQ circuits. The resistance of the shunt resistance (R_{sh}) and the sub-band gap resistance of the junction is R_m , and both the resistances can be seen in parallel and can be calculated as in equation 2.

$$R = \frac{R_m.R_{sh}}{R_m + R_{sh}} \quad (2)$$

The principle governing factors for the Josephson junction with the combined resistance R is such that disparity must be avoided so the scaling of resistance should avoid errors due to quantum fluctuations and these quantum fluctuations must be smaller than the thermal fluctuations. So, the ratio of resistances must be smaller to the ratio of thermal noise and critical current contributions and resistance scaling must be smaller. So for scaling conditions to be satisfied we must have,

$$\frac{I_T}{I_C} > \frac{R}{R_Q} \quad (3)$$

Where $R_Q = \frac{\pi T}{e^2}$, I_C is the critical current, I_T is the thermal noise. Bias voltage cannot be scaled similarly as resistance. However, for all conventional reasons the bias voltage is fairly independent of temperature. But in reduction to the crosstalk reductions and circuit designs specifics, the bias voltage can be reduced by a factor of 2 to 5 (Narayana S. 2011, Salvin A. et al., 2006).

4. Power independent RSFQ logic

Superconducting structures have been known to keep circulating currents for unlimited time. If this current or magnetic field caused by this persistent current then one can use this phenomenon to perform useful functions without any energy dissipation. Unfortunately, the list of such functions is quite small (Tahara S. et al., 2004). This are because most of functions or blocks using the persistent currents such as RSFQ cells/latches lose their state when the power is turned off. However, below we would like to show that RSFQ cells could be modified for Power Independent (PI) operation. Let us remind that power independence means an ability of circuits to be un-powered without any loss of stored information. As a result, power independent circuits should be powered only when logic operations should be performed.

The simplest power independent circuit with memory is a well-known single junction SQUID as shown in figure 2a. The single junction SQUID is a superconducting loop with sufficiently large loop inductance L interrupted by a single Josephson junction. The dynamics of single Josephson junction SQUID has been well known for many years now and will not be discussed in detail here. But, it may be sufficient to recap the flux modulation as a function of the bias current to the SQUID as shown in figure 2b. From the figure 2b we can see that, we can write "1" or "0" by applying large enough positive ($I_b > I_{th1}$) or negative ($I_b < I_{th0}$) bias current I_b .

The device continues to remember any of these states if bias current is switched off ($I_b = 0$) as there is no dissipation in the superconducting loop.

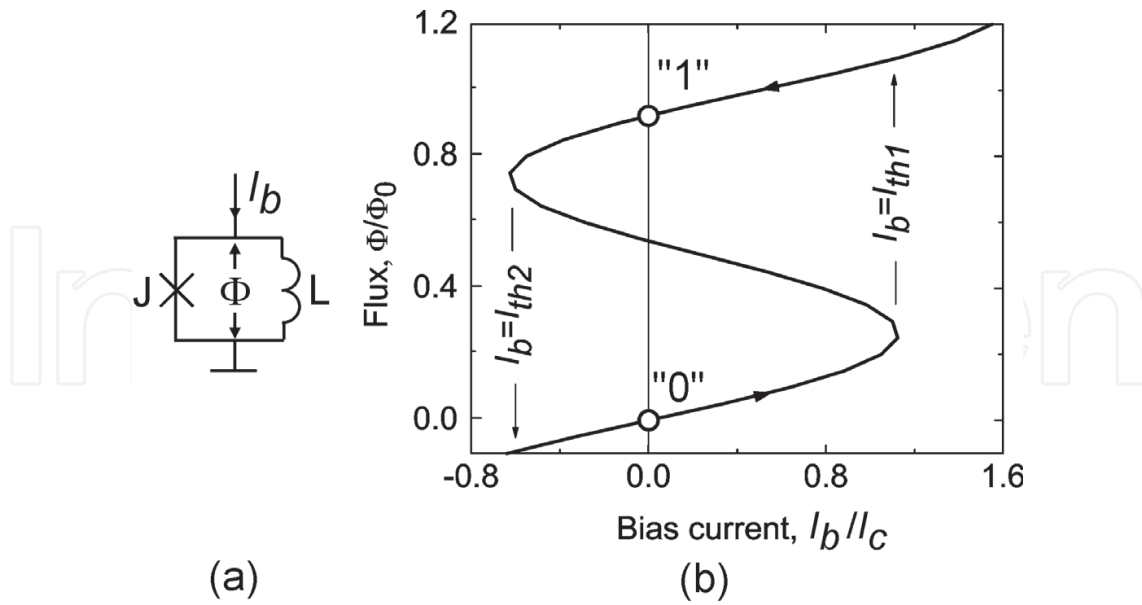


Fig. 2. (a) Single Junction SQUID ;(b) Current vs Flux characteristics. A single junction SQUID as the simplest power independent cell.

The introduced memory cell of single junction SQUID could be incorporated into RSFQ flip-flops and logic gates. The construction of power independent RS flip flop is presented in the next section.

4.1 Power Independent RSFQ RS flip-flop

The transformation of the RSFQ cell into Power Independent RSFQ cell is explained here. In the case of regular RSFQ RS Flip Flop (Turner C.W. et al., 1998), as shown in figure 3a, the Josephson junctions J3, J4 and loop inductance L, form a two junction interferometer with $I_C L = 1.25\Phi_0$, so that a flux quantum can be stored in it. The current in the loop can be expressed as the sum of the bias current equally divided between the two junctions and circulating current $I_p = \pm\Phi / 2L$. Initially, the circulating current is counterclockwise, representing a stored "0". The currents when the bias is applied are $I_{J3} = (I_b / 2) + I_p$ and $I_{J4} = (I_b / 2) - I_p$.

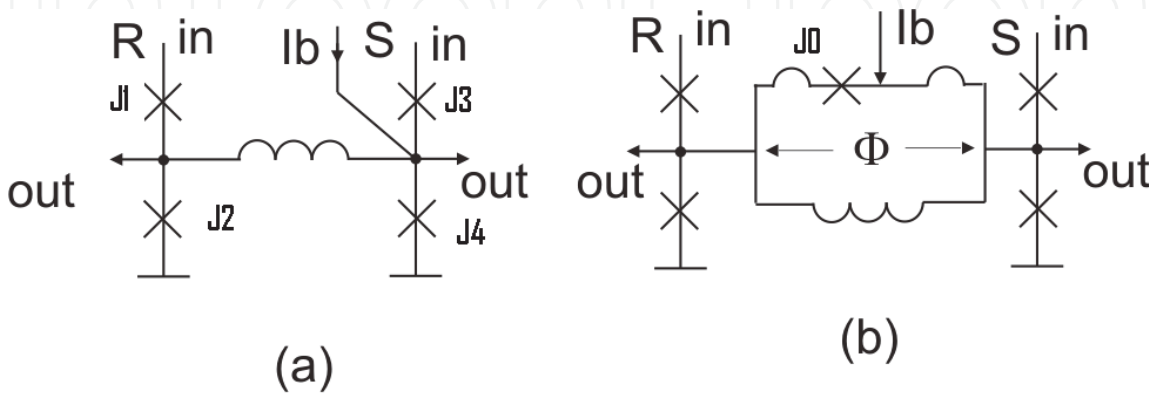


Fig. 3. (a) RSFQ RS- Flip Flop (b) RSFQ Power Independent Flip Flop. Transformation of a conventional RSFQ RS Flip flop into power independent RSFQ RS Flip flop.

When input pulses are applied to the input (set) and clock (reset) terminals, this causes circulating current to reverse polarity. When pulse arrives on the input, its current passes through the J2 (nearly biased at $\Phi = 0$) and causes J3 to switch and the circulating current is transferred to J4. The clockwise circulating current is representative of a stored "1". Then, when a clock pulse (reset) is applied, it passes through L1 and J1 and into J4, thus causing it to switch. The voltage pulse developed during the switching reverses the circulating current, so again a "0" is stored in the loop; it simultaneously applies this SFQ voltage pulse to the output inductor L3.

The junctions J1 and J2 have lower critical currents than J3 and J4 and to protect the inputs from back reaction of the interferometer if pulses come under the wrong circumstances.

In the RSFQ RS Flip Flop cell as shown in figure 3a, the magnetic bias is created by asymmetrically applying bias current I_b . This magnetic bias disappears if the bias current is switched off. As a result the circuit keeps its internal state only as long as the bias current remains applied.

In figure 3b the transformation for the RS flip-flop into Power Independent cell is shown. The operation of the Power independent RS flip flop operates in the similar manner as the conventional RSFQ RS flip flop, the junction and inductance parameters have to be adjusted accordingly. In contrast PI cell (Figure 3b) holds its magnetic bias inside its SQUID, instead of a single quantizing inductance L. To activate the SQUID and the circuit one should apply large enough bias current I_b . (Note that this "activating" current is slightly greater than its nominal value for regular logic operation.) Being activated the circuit remains magnetically biased (presumably by flux about $\Phi_0/2$) even if bias current is off. Note that even power independent circuits should be powered to perform logic operations, in order to provide the needed additional magnetic flux bias.

4.2 Investigations of power independent circuits

In order to investigate the power independent RSFQ flip flop we simulated the RSFQ flip flop. The clocked RS flip flop, where the reset terminal used as the clock terminal can be used as the RSFQ D flip-flop. The circuits were designed based on the simulations to be fabricated for Hypres 1KA/cm² Nb trilayer technology.

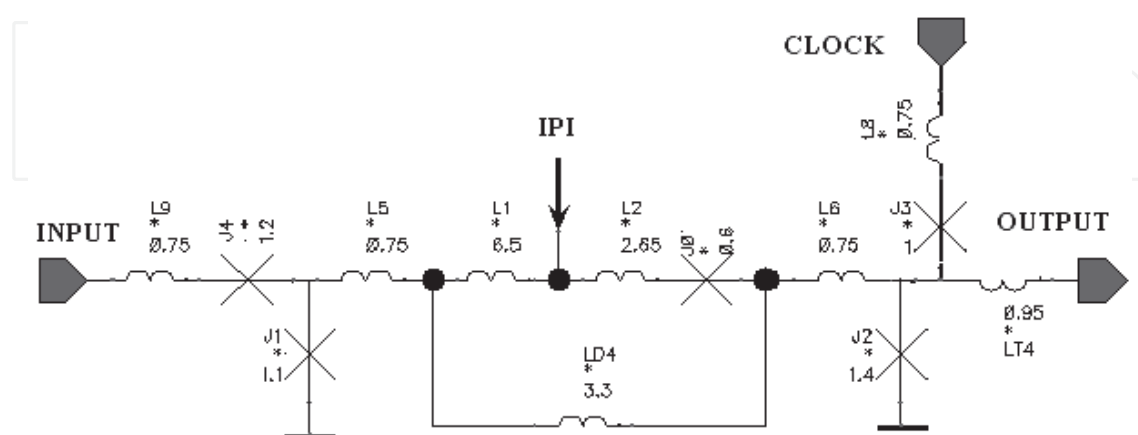


Fig. 4. Power independent D flip-flop(Clocked RS Flip-flop). Bias current IPI does 2 things: it "activates" the SQUID with junction J0 and the power the cell during normal operation. Values of paramerters are shown in dimensionless 'PSCAN' units (Polonsky S. et al., 1991).

4.3 Design of 6-bit shift register with PI cells

Figure 4 shows schematics of a D flip-flop (Clocked RS Flip flop), re-optimized for operation in power independent mode at 4 K. The power independent D flip-flop has the single junction interferometer that can be identified by schematic components L1, L2, LD4 and J0.

The interferometer is biased by current IPI. The components in the figure 4 are represented by dimensionless PSCAN units, which are easier for computation.

Figure 5 illustrate current and input data patterns used for a numerical circuit optimization with PSCAN software package. The new feature of the simulation is a more complex shape of applied bias current IPI. During the simulation it was required that junction J0 is switched only one time and when IPI current it applied for the first time. No other junctions switched when bias current goes down.

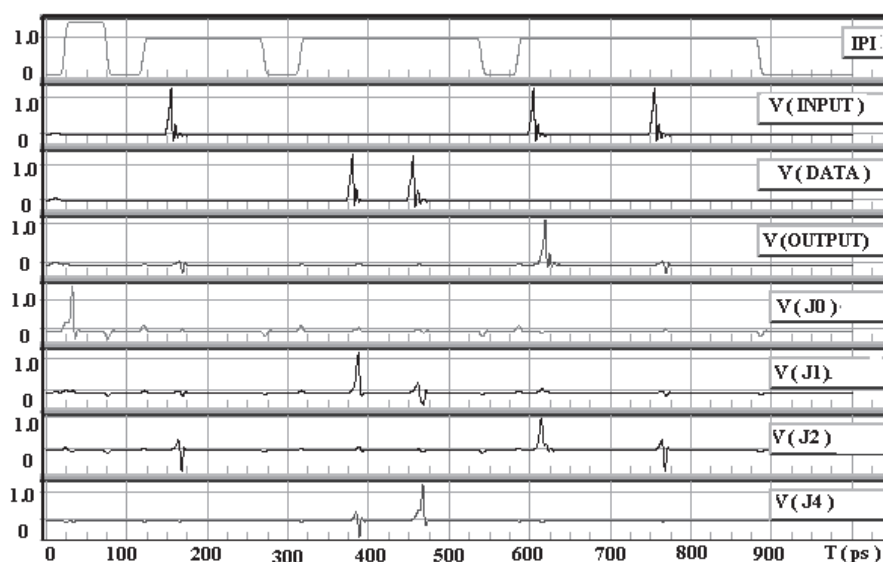


Fig. 5. Current (upper trace) and voltage waveforms illustrating the power independent operation of D cell. Note that the initial “activation” procedure could require larger current IPI than those during the regular circuit operation

A 6-bit shift register with PI D cells has been designed and laid out for HYPRES fabrication technology. The shift register has been incorporated into a benchmark test chip developed for a comparative study of flux trapping sensitivities (Polyakov Y.A. et al., 2007) of different D cells. (The earlier revisions of the test circuits are documented in Narayana S. 2011.)

Figure 6 shows a microphotograph of a fully operational circuit (as shown in Figure 4) fabricated at HYPRES (1 KA/cm² technology). Bias current margins ($\pm 16\%$) for the only measured chip are about 2 times below our numerical estimations (35%). The figure 7 the shift register was tested with Octupux (Zinoviev D. et al.,) setup where the low speed testing was use to confirm the correct operation of the shift registers. Since the shift register is a counter shift register, the clock and the data pulses travel in the opposite direction and this can be confirmed by the traces in figure 5. The chip was not tested for high speed operation

These measurements show a complete operation of the circuit but with about $\pm 16\%$ bias current margins that are more than 2 times below of our numerical estimations (35%). We believe that the discrepancy is mostly because of the large number (over a dozen) of corners in the SQUID loop. This is because we believe that the inductances for the corners in the loop have been overestimated (Narayana S 2011).

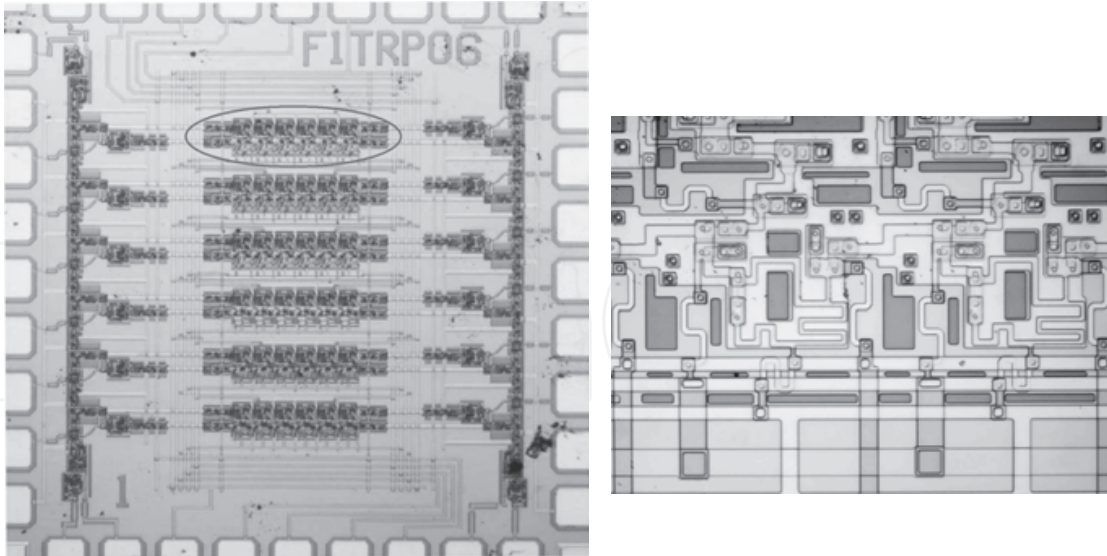


Fig. 6. The microphotographs of the chip and 2 cell fragment of the shift register (encircled on the left) consisting of power independent RSFQ D cells. Horizontal pitch of the 2 cells is $270\mu\text{m}$.

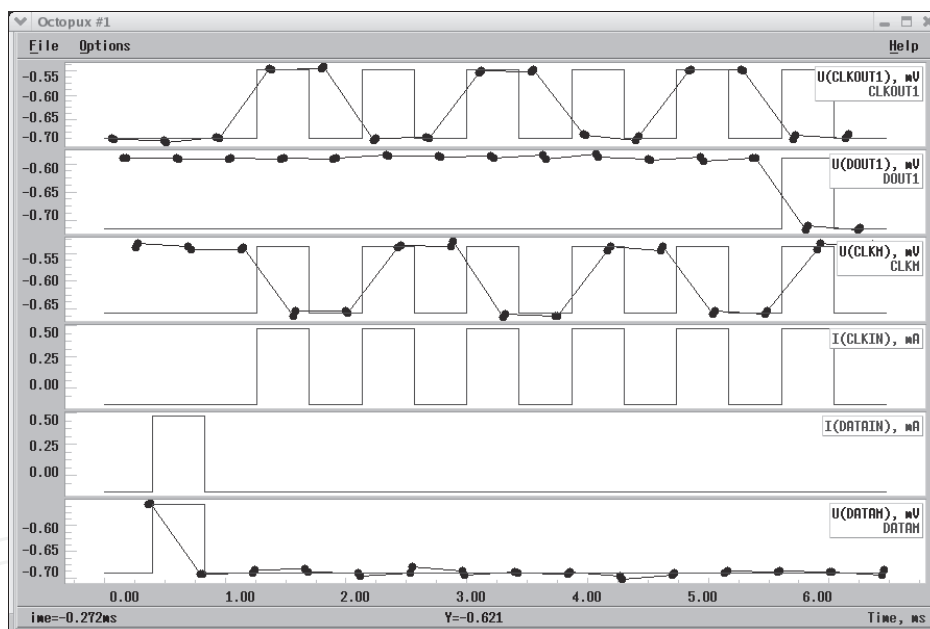


Fig. 7. The low frequency operation of counter flow shift register. The traces 3(clock), 5(data) are the inputs and 1, 2 are the clock and data output traces respectively.

5. Current recycling

One of the main advantages of RSFQ circuit is that only dc bias is needed. It eliminates the cross-talk problems caused by ac biasing and makes designing larger circuits easier. However, in larger circuits the total dc bias current could add up to a few amperes and such large bias currents cause large heat dissipation, which is not preferred (for larger modular designs the bias currents could add up several amperes). One of the techniques that has been proposed (Kang J.H. 2003) is biasing the circuits serially otherwise commonly known as

'current recycling'. Biasing large circuit blocks in series (referred to as current recycling or current re-use) will essentially reduce the total current supply for the superconducting IC to a manageable value. Both capacitive (Teh C.K., et al., 2004) and inductive methods (Kang J.H., et al., 2003) of coupling for current recycling have been demonstrated at a small scale. It is difficult to estimate the impact of the technique based on single gate operation as in (Johnson MW et al, 2003). Current recycling becomes easier at higher current density of the superconducting IC (Narayana S 2011). Current recycling however has its limitations; it does not reduce the on-chip static power dissipation by the circuit blocks and also due to additional structures, the area occupied by the circuit increases.

To demonstrate the method of current recycling, we have designed a Josephson junction transmission line (JTL) as shown in figure 8, which represents one module. The module consists of three parts, the driver, receiver and the payload. The payload is usually the circuit block that is used for operation, in this case to keep matters simple a JTL has been used, as its operating margins are very high. The payload can otherwise be replaced by flip-flops, filters, or logic gates.

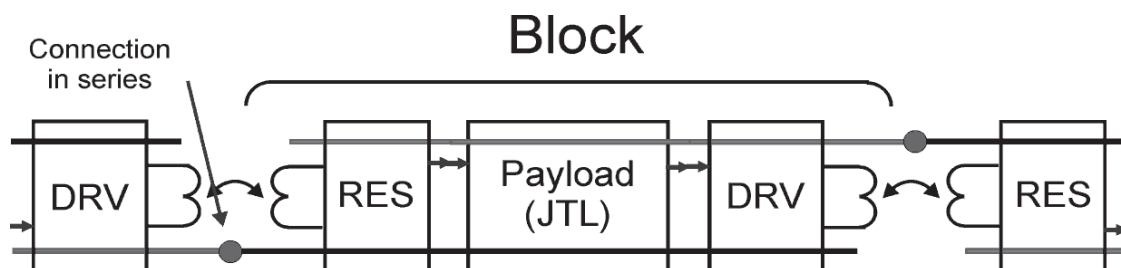


Fig. 8. Block diagram of current recycling digital transmission line

Before we explain the operation of the driver-receiver circuit, it is important to remember a few thumb rules for the current recycling design. For current recycling, the ground planes under adjacent circuit blocks must be separated and subsequent blocks biased in series. It will also be necessary to isolate SFQ transients between adjacent blocks. This may be achieved by low pass filters, but will need to avoid power dissipation in the filters. Series inductance could provide high frequency isolation; the inductors could be damped by shunting with suitable resistance, such that there is no large DC power dissipation. Capacitive coupling between adjacent blocks can be used for current recycling however they are not discussed here and also capacitors (Teh C.K., et al, 2004) used for this method also occupy larger space compared to the inductive filtering method.

5.1 Current recycling basics

The fundamental requirement for serial biasing of circuits is that current drawn from (supplied to) each circuit must be equal and the input/output must not add current to the serially biased circuits. The inputs and outputs are connected via galvanic connection to satisfy the above requirements.

In figure 9, the complete schematic of the driver- receiver is shown. The driver and receiver circuits are completely different electrical grounds. An inductor connecting two Josephson junctions momentarily stores a single flux quantum while an SFQ pulse propagates from one junction to another. Typically, this duration time is about 5picoseconds, depending on the circuit parameters. Between the time when J13 and J14 generate a voltage pulse, the magnetic flux stored in the inductor that connects J13 and J14 induces a current in the inductor, $L1u$,

connecting J1 and J2. With proper circuit parameters, this induced current causes a voltage pulse to be created on J1 and this pulse then propagates through J2 to be further processed. In this way, an SFQ signal pulse is transferred from one ground to another plane.

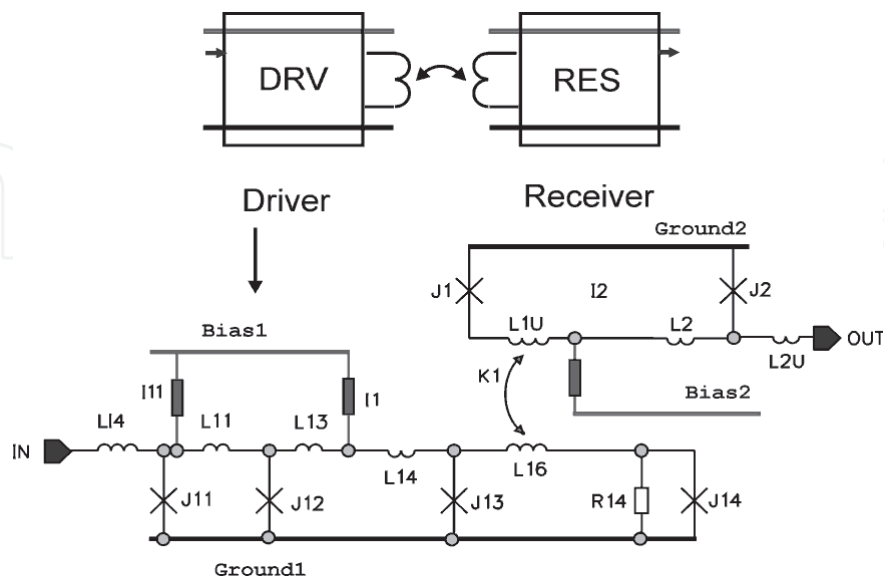


Fig. 9. Circuit schematic for magnetic coupled SFQ pulse transfer between driver and receiver

5.2 Current recycling experimental demonstration

The complete block diagram for the circuit is shown in figure 11a along with the connection scheme for the 80 blocks to be biased serially. Figure 11b shows the microphotograph of the chip which was fabricated for the circuit schematics discussed in of figure 8 and 9. The bias Current for the junction on the input side is passed to one ground plane while the ground for the junctions on the output side is isolated from the other ground by a ground plane moat. The Josephson junction J13 and J14 are damped more heavily than other junctions to guarantee that minimum reflections take place at the end of the input JTL. Tight magnetic coupling is required between the pulse transmitting the JTL and the pulse receiving JTL to obtain a robust circuit with excellent operational margins. To ensure higher coupling holes were opened in both the upper and lower ground planes as shown in figure 10.

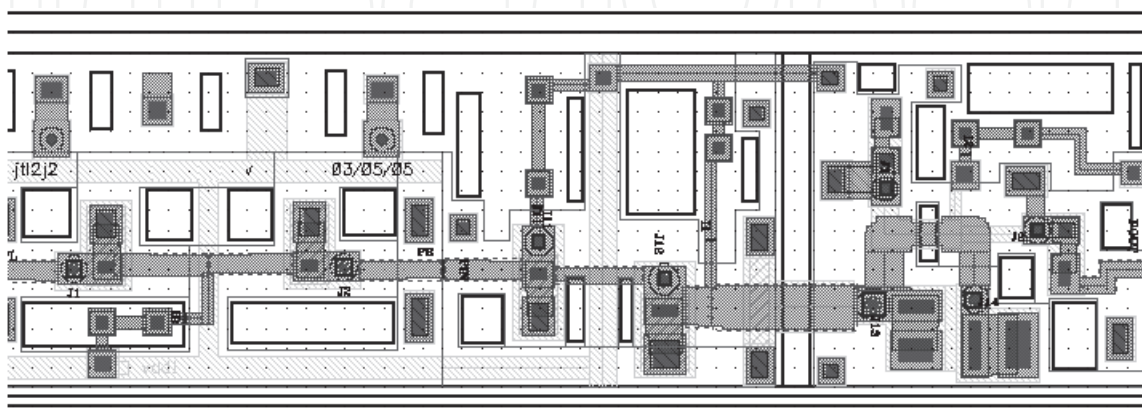


Fig. 10. The layout showing the JTL-driver-receiver connections is shown.

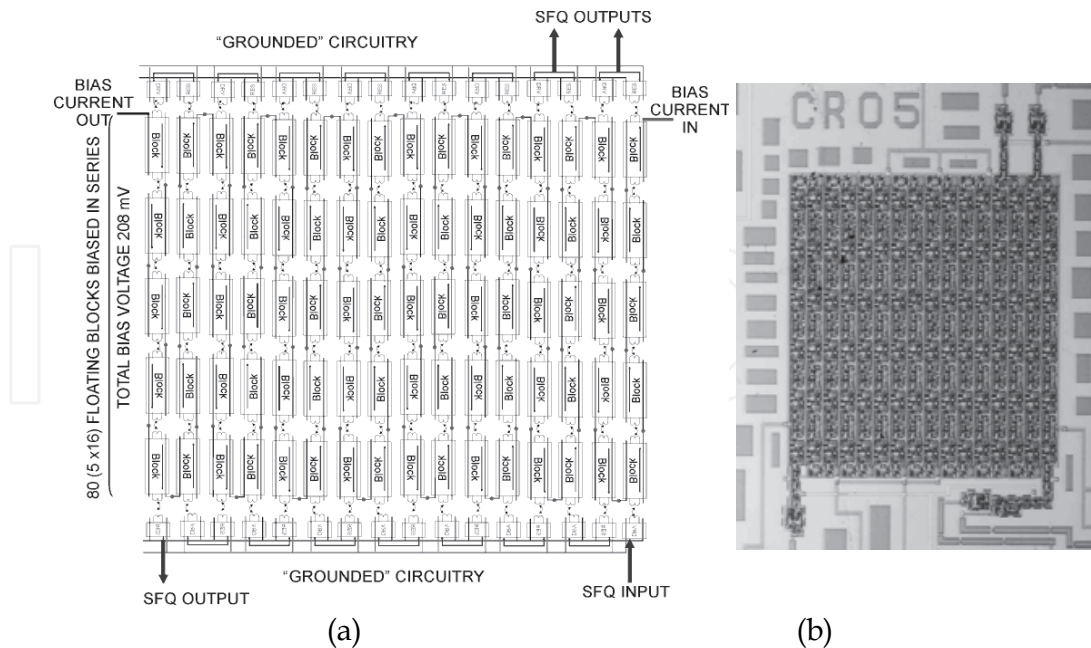


Fig. 11. (a) The block diagram for serial biasing. (b) The microphotograph of the chip for demonstrating current recycling.

The digital traces for the correct operation of the circuit are shown in figure 12. The measurements were carried out at low frequency using Octupux setup (Zinoviev 1997). The circuit tested used the standard I/O blocks of SFQ/DC converters to measure the operating margins of the circuits. The circuits were fabricated for both 1kA and 4.5KA/cm² Hypres tri-layer Niobium technology. The circuit has margins of $\pm 15\%$. The bias current to obtain correct operation was reduced to 1.7mA by current recycling method; otherwise the operation of 80 blocks with parallel biasing would require nearly 200mA.

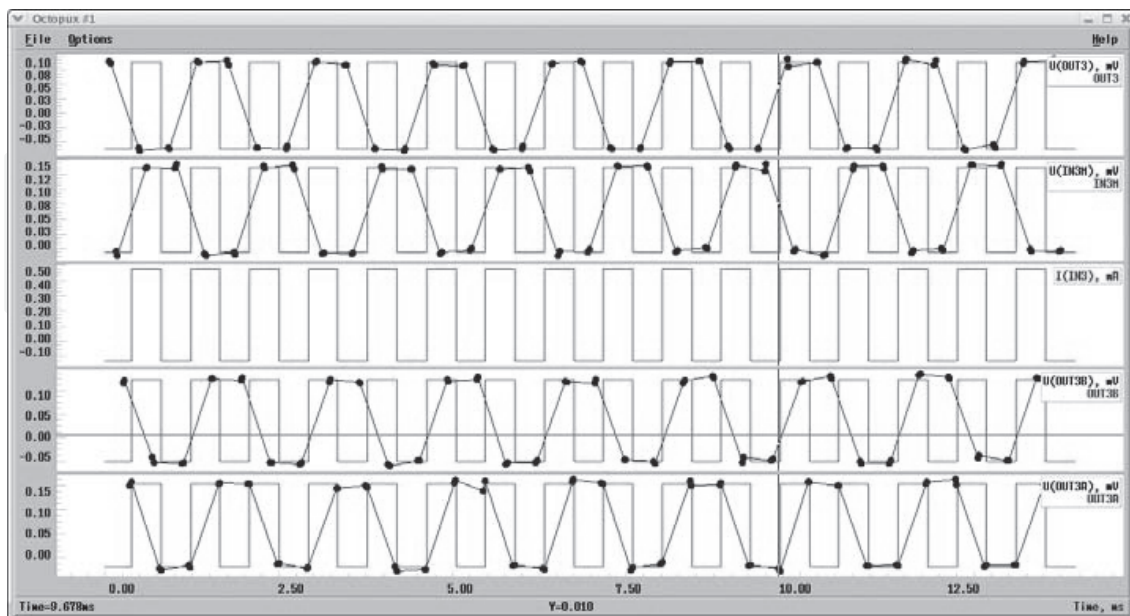


Fig. 12. The digital waveform of the input and three outputs as shown in figure 5.4. The traces 1,3,5 are the outputs and 2 is the input trace

6. Discussions and summary

In sections 4 and 5, we have demonstrated the operation of power independent RSFQ cell and current recycling technique for over 1k junctions in a single chip.. Now let us consider the latter case. If N blocks were parallel biased (that is individually biased), the power dissipated would be

$$P_p = \sum_{i=1}^N I_{b_i}^2 \cdot R_b \quad (4)$$

For the serially biased case

$$P_s = I_b^2 \cdot R \cdot N \quad (5)$$

Comparing the two cases for N uniform cells, the ratio of P_p/P_s is N. So essentially, one can reduce the bias current by maximum of N times by serial biasing scheme. However, one should note that, this scheme cannot reduce the on chip power dissipation but only reduce the total bias current load, which could prove very significant in designing large circuits.

In the power independent mode the cells can be turned on only when the cells have to be operated and can be turned off, rest of the time. Also they retain the logic state of the circuit, when they are switched off so one can eliminate static power dissipation by this method. In both the schemes discussed, we note that there is a significant increase in area overhead (about 30%).

In this chapter, we have presented solutions for energy minimization in single flux quantum circuits. We have also presented a method for scaling resistances to modify existing SFQ based circuits to fit designs for quantum computation. We have also presented some of the short comings of the proposed methods, giving us an avenue for further research in the areas to make the proposed methods more widely acceptable for application in quantum computing and high performance mixed signal circuits.

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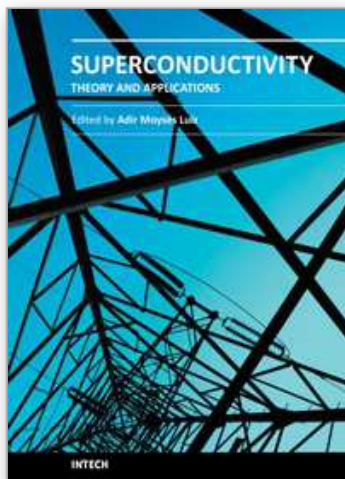
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Superconductivity was discovered in 1911 by Kamerlingh Onnes. Since the discovery of an oxide superconductor with critical temperature (T_c) approximately equal to 35 K (by Bednorz and Müller 1986), there are a great number of laboratories all over the world involved in research of superconductors with high T_c values, the so-called “High- T_c superconductors”. This book contains 15 chapters reporting about interesting research about theoretical and experimental aspects of superconductivity. You will find here a great number of works about theories and properties of High- T_c superconductors (materials with $T_c > 30$ K). In a few chapters there are also discussions concerning low- T_c superconductors ($T_c < 30$ K). This book will certainly encourage further experimental and theoretical research in new theories and new superconducting materials.

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