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Graphene Transistors

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1. Introduction

The recent discovery of graphene (Novoselov et al., 2004), a single atomic sheet of graphite, has ignited intense research activities to explore the electronic properties of this novel two-dimensional (2D) electronic system. Charge transport in graphene differs from that in conventional 2D electronic systems as a consequence of the conical energy dispersion relation near the charge neutrality (Dirac) point in the electronic band structure (Zhang et al., 2005). Field-effect mobility as high as 15 000 $cm^2/V{\cdot}s$ and a Fermi velocity of ~10^8 cm/s have been demonstrated at room temperature (Geim & Novoselov 2007). These properties make graphene a possible candidate for electronic devices in the future.

The major benefit of graphene frequently quoted is superior electron/hole mobility compared to other semiconductors, but as Fig. 1 shows, this is not experimentally the case *yet* when compared to narrow bandgap III-V semiconductors for comparable carrier densities. In addition, the lack of a bandgap limits the usage of two dimensional graphene for digital switching, where high on/off ratios are necessary. However, several potential advantages may be listed: the perfect 2D confinement of carriers, electron/hole symmetry originating from a conical bandstructure, and the possibility of opening bandgaps lithographically by fabricating graphene nanoribbons (GNRs). In Section 2, high field characteristics of 2D exfoliated graphene are reported on both short-channel and long-channel back gated field effect transistors (FETs). We will elaborate on the problem of metal contact formation and high field transport of 2D graphene. The comparison of fabricated devices based on exfoliated, epitaxial and chemical vapour deposited (CVD) graphene will follow. The large area graphene opens the possibility to make 2D graphene devices for RF/analog amplification (Lin et al., 2010). Superior frequency performance of such devices makes it a promising application of 2D graphene FETs.

The real advantage of graphene, however, can be highlighted from a novel proposed device architecture that is yet to be demonstrated (Zhang et al., 2008). If GNRs are made by lithographic patterning, and are either chemically or electrostatically doped into GNR p-n junctions, then the planar form yields to a tunnelling field-effect transistor (TFET). Towards the realization of the GNR TFET we designed a single but tuneable junction structure to demonstrate the operational principle. We discuss these GNR p-n junction transistors in Section 3 along with the developed analytical and device models used to explain the measured transistor characteristics.

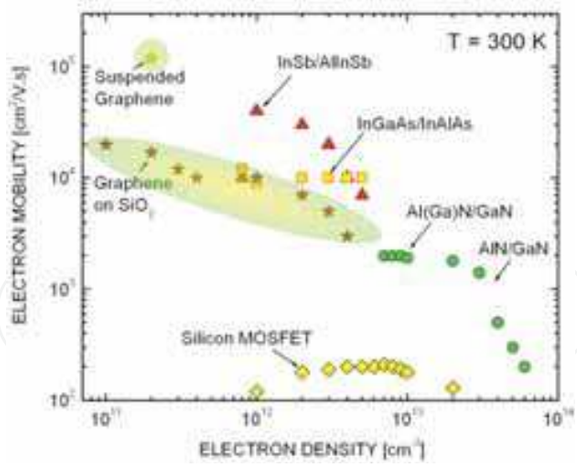


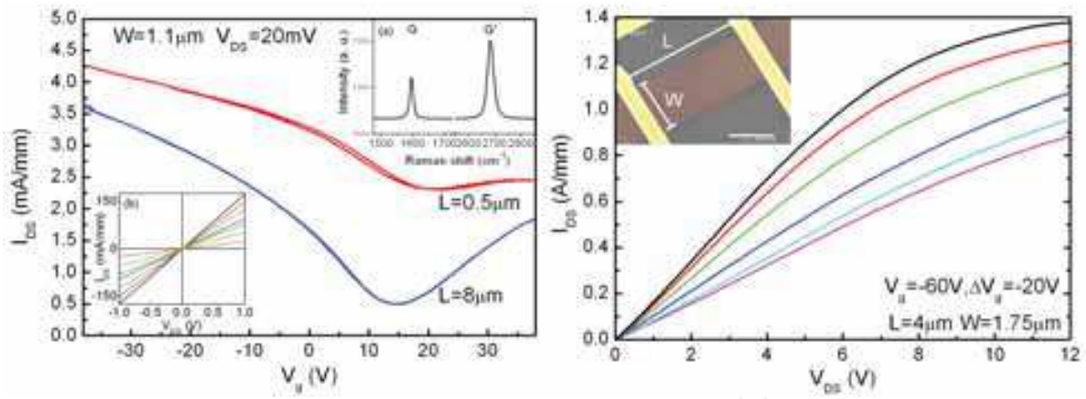
Fig. 1. 300 K electron mobility vs. 2DEG density for various semiconductor materials.

2. 2D graphene transistors

2.1 Device fabrication and characteristics of 2D exfoliated graphene transistors

Graphene offers advantages for interconnects due to high current carrying capacity despite its single layer nature (Murali et al., 2009) but more often graphene is being considered as a possible channel material for transistor technology. So far, graphene has been studied mostly at low biases, but for the application in practical devices, it is essential to investigate the high-field transport properties. High current drives were measured by pushing the devices up to breakdown. The saturation current density for many samples has been measured to be in the 1.5 – 2 A/mm range. Gate modulation of the drain current is found to depend strongly on the channel length. For comparable 2D carrier concentrations, saturation currents in 2D graphene are found to be higher than Si MOSFETs and III-V Nitride HEMTs – a feature that is attractive for various applications.

We first discuss 2D graphene FETs fabricated from exfoliated graphene and later we compare the results to graphene devices made of catalyzed CVD or epitaxial graphene. Exfoliated graphene flakes on heavily n-type doped silicon wafers with t_{ox} = 300 nm thick thermal oxide from Graphene Industries (for preparation of samples, see: Novoselov et al., 2004) were used for the experiments. Single layer graphene flakes were identified by Raman spectroscopy (inset of Fig. 2 (a)). The wafers were backside-metalized after oxide removal in HF to form back-gate contacts. E-beam evaporated Cr/Au (2/200 nm) was used to define the drain and source contacts, which were patterned by e-beam lithography. The source-drain separations ranged from L = 250 nm - 8 µm. After metal deposition and lift-off, the samples were annealed in forming gas at ~650 K for ~2 hours to remove the e-beam resist residue. The graphene flakes were then patterned by O_2 plasma reactive ion etch with PMMA masks to widths ranging from W = 1 - 10 µm. The SEM image (inset of Fig. 2 (b)) shows a typical FET. High current annealing was performed to drive off impurities for some FETs to recover their intrinsic performance. The devices were measured using a semiconductor parameter analyzer in ambient environment and in vacuum, at room temperature and at 77 K. The drain currents of the FETs were first measured at a low bias of V_{DS} = 20 mV, while the gate voltage was varied over a wide range. The gate leakage current was many orders of magnitude lower than the drain current.



(a) (b)

Fig. 2. (a) I_{DS} as a function of V_G at V_{DS} = 20 mV for short-channel (0.5 μm) and long-channel (8 μm) back-gated graphene FETs. Inset (a) Raman spectrum of single layer graphene. Inset (b) Low field I-V curves of long-channel FETs with V_G = -35 V, ΔV_G = +10 V. (b) I-V curves of a long-channel FETs. Inset is a SEM image of this FET. The scale bar is 1.5 μm.

Fig. 2 (a) shows the representative transfer characteristics of a long- and a short-channel FET. Over the same range of gate overdrives, the long channel FET was observed to exhibit higher gate modulation (~8x) than the short-channel FETs (~2x). The field-effect mobilities were calculated to be ~2000 – 4000 $cm^2/V{\cdot}s$ for long-channel FET and ~200 $cm^2/V{\cdot}s$ for short-channel FET respectively. These characteristics remained similar at different pressures, as well as at lower temperature.

Recently, saturation of drain current at high source-drain biases has been reported, and theory of optical phonon emission limited saturation current has been proposed (Meric et al., 2008; Luo et al., 2008). In particular, back- and top-gated 2D graphene FETs showed saturation current densities in the 0.5 – 0.7 A/mm range as reported by Meric et al., 2008. In Fig. 2 (b), the high bias characteristics of a back-gated FET (W/L = 1.75/4 μm) are shown. A saturation current of 1.38 A/mm is measured for this device. Saturation current densities in the 1.5 – 2.0 A/mm range were measured on a number of devices, in agreement with another earlier report for back-gated devices (Luo et al., 2008). This is ~2x higher than the reported saturation current densities for dual-gate devices, indicating that the top-gate high-κ oxide lowers the current drive through graphene. The effective 2D carrier densities were in the $2 - 4{\cdot}10^{12}$ cm^{-2} range, as estimated from the effective gate voltage. The ~0.5 - 0.7 A/mm saturation current reported earlier has been attributed to substrate-induced optical phonon scattering. However the ~2x higher current drives measured here on SiO_2 substrates indicate that the lower current drives are due to the top gate high-κ oxide rather than the SiO_2 substrate. This conjecture will be discussed in detail in the next Section.

Such current drives can be obtained in Si MOSFETs and III-V HEMTs, but only with a) high 2DEG densities (>10^{13} cm^{-2}), and/or b) very short channel lengths taking advantage of ballistic transport. Our measurements show that graphene FETs are able to achieve these high current densities without these criteria, implying that even higher current drives are possible when they are met in the future. For a rough comparison, a carbon nanotube with diameter ~2 nm and a saturation current ~25 μA has an effective current per the circumferential width ~4 A/mm (Chen & Fuhrer, 2005), much higher than either graphene or other semiconductors. At high drain biases, the current saturates at more than 1 A/mm,

but with weak gate modulation. Graphene carries over the high current carrying capacity of carbon nanotubes, but the absence of an energy bandgap hampers the modulation of this high current density.

2.2 Graphene on high-κ dielectrics

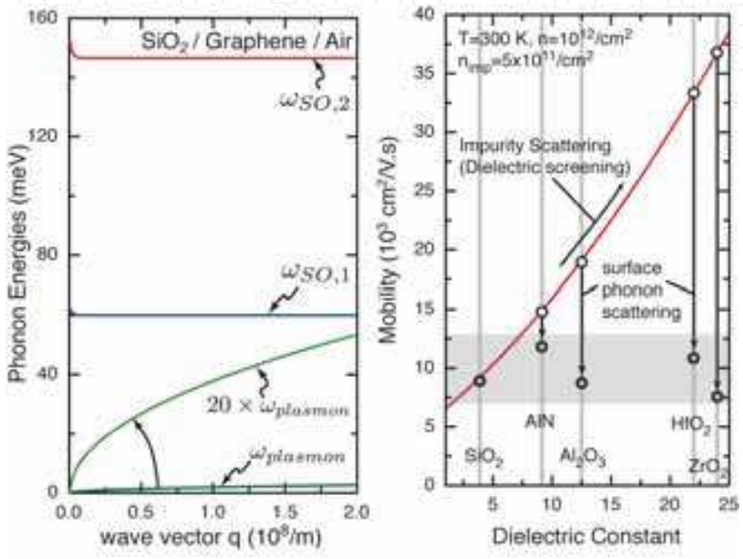
In the last section, we discussed carrier mobility and current drive of graphene on SiO_2. Low-field mobility values for graphene on SiO_2 was 4000 $cm^2/V{\cdot}s$ at room temperature and the highest reported value at $>10^{13}$ cm^{-2} carrier concentration is around 9000 $cm^2/V{\cdot}s$ in literature (Novoselov et al., 2004). It is widely believed that ionized charged impurities at the graphene-oxide interface (Hwang et al., 2007) limits the carrier mobility in graphene. As electron-ionized charged impurity interaction $v_{cou} \approx \kappa^{-2}$, where κ is the average dielectric constant of graphene's environment, it seems that use of very high-κ substrate instead of SiO_2 can improve the carrier mobility of graphene at low fields. But use of high-κ dielectrics for graphene transistors comes with an extra scattering mechanism—the remote interface-phonon or surface optical phonon (SO) scattering. Most of the high-κ materials are polar in nature because of large difference in electronegativity of constituent atoms. At room temperature, the vibrating dipoles of the high-κ dielectric material create an electric field, which decays exponentially away from the graphene-dielectric interface. Due to the fact that graphene is an atomically thin (0.3 - 0.4 nm) membrane, the decaying polarization field (also known as surface-phonon field) can scatter the carriers in the graphene channel and limit the low-field mobility. The surface phonon energies can be calculated by solving Maxwell's equation in the dielectric continuum model.

	SiO_2	AlN	Al_2O_3	HfO_2	ZrO_2	SiC
κ^0_{ox}	3.9	9.14	12.53	22.0	24.0	9.7
κ^∞_{ox}	2.5	4.8	3.2	5.03	4.0	6.5
$\omega_{TO,1}$	55.6	81.4	48.18	12.4	16.67	-
$\omega_{TO,2}$	138.1	88.5	71.41	48.35	57.7	-
$\omega_{SO,1}$	59.98	83.60	55.01	19.42	25.02	116.0
$\omega_{SO,2}$	146.51	104.96	94.29	52.87	70.80	167.58

Table 1. Surface phonon energies of graphene/dielectric/air system for various dielectric materials.

In Table 1, we present the calculated values of surface-phonon energies for commonly used dielectrics in device-physics. Most binary dielectric compounds exhibit two surface-phonon modes corresponding to two bulk transverse phonon (TO) modes. It should be noted that, high-κ dielectric materials such as HfO_2 and ZrO_2 exhibit very low- energy SO modes. The surface-phonon modes are optical-like (dispersionless) as shown in Fig. 3 and cause inelastic scattering of carrier electrons in graphene. The electron-SO phonon scattering rates are calculated using second order perturbation theory and transport coefficient such as electron mobility have been calculated using the Boltzmann transport equation under the relaxation time approximation. When ionized impurity scattering is combined with SO-phonon scattering, a comprehensive picture of charge transport emerges. At low temperature, when SO-phonons are frozen, indeed electron mobility can be enhanced by a

factor of 3-4 by using ZrO_2 as the gate dielectric, but at room temperature, this dielectric enhancement is washed out by strong electron-SO phonon scattering. Fig. 3 (b) provides a relative assessment of electron mobility on different dielectrics. The curve represents the expected mobility enhancement by high-κ dielectrics, whereas the dots represent the effective mobility after inclusion of SO-phonon scattering rates. It is seen that there is not much room for improving carrier mobility with commonly available high-κ dielectrics at room temperature. In the future, high-κ dielectrics with high SO-phonon energies should be sought to achieve high mobility and speed in graphene.



(a) (b)

Fig. 3. (a) Dispersion of SO phonon and (b) mobility of graphene on common dielectrics.

2.3 Short channel and contact effects

The dependence of high bias drain currents and their modulation efficiency with the back-gate is observed to depend strongly on the channel length of graphene. In Fig. 4, the FET characteristics are shown for four different channel lengths, ranging from 0.5 to 8 μm. Two features are observed – a) for the same channel length, the gate modulation at higher drain biases is lower, as is expected from the saturation of the current, and b) for the same bias voltages (or fields), the gate modulation efficiency decreases sharply as the channel length reduces. As shown in Fig. 4, the gate modulation reduces from ~7 to ~1.4 as the source-drain separation is scaled from 8 μm to 0.5 μm.

Due to the absence of a bandgap in graphene, charge exchange is expected at the metal-graphene source/drain contacts owing to the work function differences. Considering the work function of Cr (W_{Cr} ~4.5 eV), and that of pristine graphene (W_{Gr} ~4.5 eV) one would expect them to form a flat-band (or 'neutral') contact without any charge transfer. However, recent calculations have shown that the necessary condition for the formation of a neutral contact with a metal (work function W_M) in intimate contact with graphene is $W_M - W_{Gr}$ ~0.9eV (Giovannetti et al., 2008). Therefore, we expect that the graphene region adjacent to the Cr contact pad is effectively doped with excess carriers. The excess charge region extends over an effective Debye length from each contact resulting in source/drain extension regions. Quantitative modelling of this interesting phenomenon will be presented in detail in Section

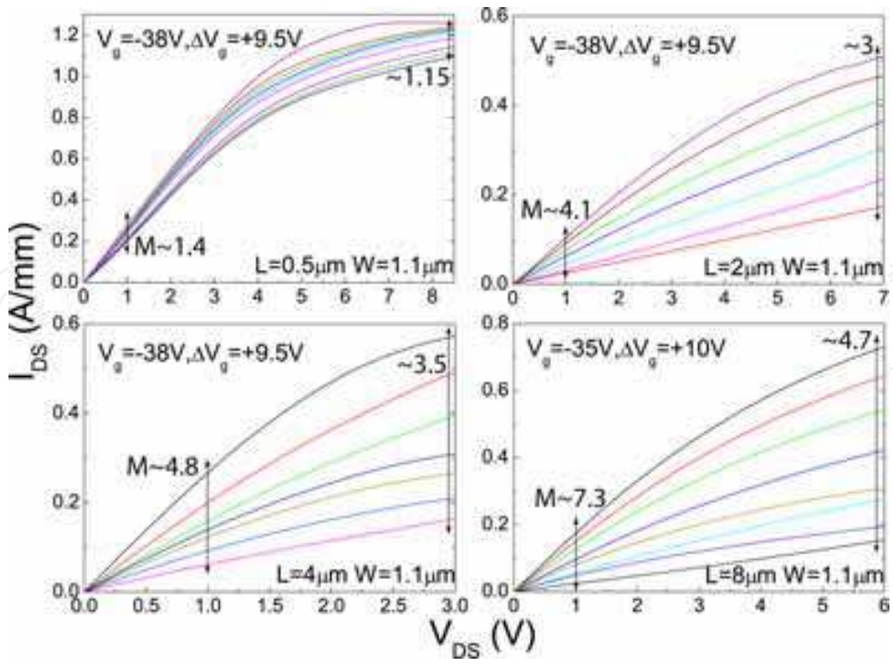


Fig. 4. Current density as a function of drain biases for FETs with different channel lengths varied from 0.5 μm to 8 μm. Clear loss of gate modulation is observed with the shrinking of the graphene channel length.

2.4. When the source/drain separation is smaller than twice the Debye length, the channel conductivity is controlled by the source/drain contacts, and the back-gate gradually loses the ability to modulate the current, as seen in the FET characteristics in Figs. 2 & 4.

2.4 Influence of metal/graphene coupling on 2D graphene transistor

Recently, many experimental studies point out that metal contacts could play a critical role on device performance of graphene transistors (Lee et al., 2008; Mueller et al., 2009). When graphene is covered by a metal electrode, the Fermi level of the underlying graphene will be shifted according to density functional theory calculations (Giovannetti et al., 2008) and have been observed in experiments (Huard et al., 2008; Nagashio et al., 2009). Here, we explore the effects of metal contacts on the operation and scalability of 2D graphene FETs using detailed numerical device simulations based on the non-equilibrium Green's function (NEGF) formalism in the ballistic limit. Our treatment of metal/graphene contacts captures (1) the doping effect due to the shift of the Fermi level at graphene contacts; (2) the Metal-Induced-States (MIS) in the graphene channel.

The modelled device is shown in the inset of Fig. 5 (left). The channel is assumed to be uniform graphene with width of 150 nm. At w = 150 nm, the current density is similar to analytical 2D results, which implies an effective 2D approximation. The contact regions are assumed to be semi-infinitely long. The top gate insulator is t_{ox} = 1.5 nm thick with a dielectric constant ε_{ox} = 20. The bottom gate dielectric SiO2 is 50 nm thick, and the Si substrate is connected to the ground. The simulated area is only the channel (dashed rectangle) with fixed boundary conditions at the source and the drain. The major challenge in experiments is the aforementioned degradation of graphene channel mobility due to the top high-κ gate dielectric; in this theoretical evaluation, a ballistic model has been assumed to describe the charge transport in the graphene channel for simplicity.

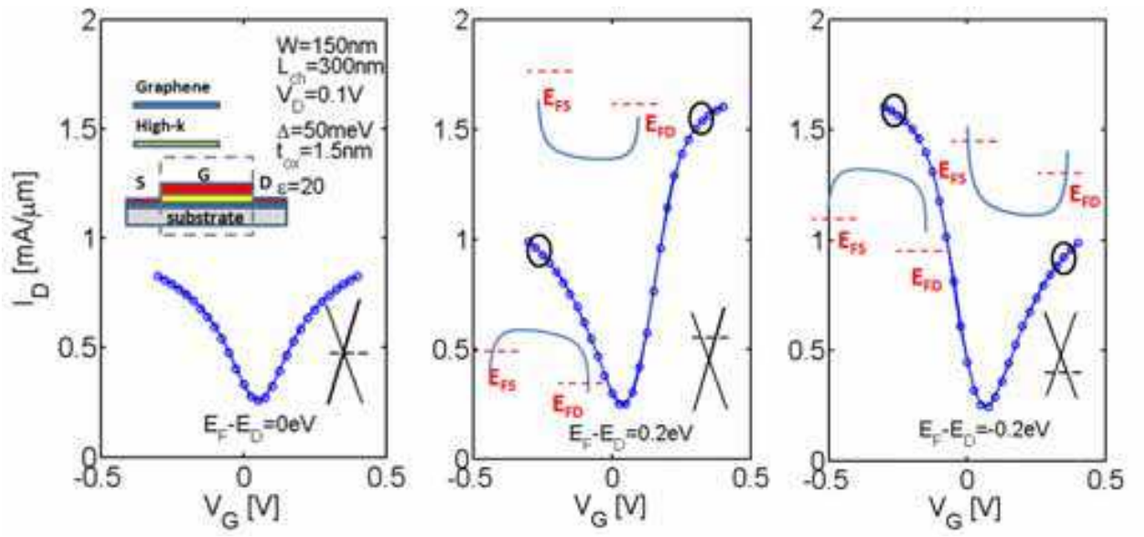


Fig. 5. (inset) Structure of the modelled device. (left) Without any shift of Fermi level in the contact region, symmetric transfer characteristics can be seen. When the Fermi level of contact regions of graphene is shifted due to the metal by E_F-E_D = 0.2 eV (center) and by E_F-E_D = -0.2 eV (right), asymmetric transfer characteristics are observed.

The channel transport is solved using a mode-space based non-equilibrium Green's function formalism. A mode space approach significantly reduces the computational cost while still maintaining the accuracy, as already demonstrated in simulations of silicon (Venugopal et al., 2002), carbon nanotube (Guo et al., 2004), and GNR (Zhao & Guo, 2009) FETs. In our calculation, we assume that the potential variation along the channel width is negligible. Based on this approximation, the electrostatics is solved in 2D, and the mode space method yields accurate results. The channel potential is computed using the 2D electrostatic solver, which also capture the shift of Fermi level at graphene contact. The details of the electrostatic solution procedure are discussed in Zhang et al., 2010. The effect of contacts on the channel is captured through the contact self-energy $\Sigma_{S,D} = \tau g_S \tau$, where τ is the coupling matrix between the contact and channel, and g_S is the surface Green's function of the contact, $g_S = [(E+i\eta+i\Delta)I-H_{contact}]^{-1}$ (Datta, 2005), where η is typically an infinitesimal quantity, and Δ describes the metal/graphene coupling (Golizadeh-Mojarad & Datta 2009; Nemec et al., 2008). By iterating between the NEGF transport solver to find the charge density and the 2D electrostatic solver to find the self-consistent potential, a self-consistent solution is obtained. The source/drain current is then computed from $I_{DS} = (2e/h)\int T(E)(f_S(E)-f_D(E))dE$, where T(E) is the source/drain transmission coefficient.

Fig. 5 shows the calculated transfer characteristics at V_{DS}=0.1 V with different Fermi level shifts of the contact regions of graphene. The metal/graphene coupling strength is Δ = 50 meV. The effects of different Δ's are discussed later. If the contact does not introduce any Fermi level shift as in Fig. 5 (left) E_F-E_D = 0 eV, the transfer curve is symmetric. The minimum conduction point locates at $V_{GS} = V_{DS}/2$. Fig. 5 (right) shows a typical case (Au contact), when the value of the Fermi level shift is E_F-E_D = -0.2 eV (Giovannetti et al., 2008). At negative V_G, carriers can directly go through the channel without experiencing any barriers (see schematic potential profile of Dirac point in Fig. 5 (right)). However at positive V_G, electron transport through the channel will be suppressed by the barrier. Thus the

positive current branch is reduced compared to the negative current branch. The complete transfer curve shows a clearly asymmetric behaviour. We point out that the minimum conduction point gate voltage is also shifted due to the barriers at contacts and I_{on} also increases with contact doping effect. When E_F-E_D = -0.2 eV as shown in Fig. 5 (center), an effective n-type doping is introduced by the metal contacts. A similar asymmetric behaviour with positive current branch larger than negative current branch is expected in that case. We point out that even though previous studies have described an asymmetric transfer characteristics in 2D FETs due to electrostatically doped graphene p-n junctions (Low et al., 2009), metal/graphene contacts themselves may also lead to asymmetric conduction as experiments have indicated (Huard et al., 2008; Nagashio et al., 2009).

Fig. 6 shows a comparison of the effect of different coupling strengths Δ at large drain bias (V_{DS}) voltages. The rigorous explanation of the values used for Δ is related to the metal/graphene hybrid system, which is beyond the focus of this study. For a comparison, we define three Δ values here, Δ = 0 eV for the intrinsic graphene case, Δ = 8 meV for weak metal-graphene coupling, and Δ = 50 meV for strong coupling. The first interesting feature that emerges is that the current drive *increases* as Δ increases. Higher Δ induced broadening

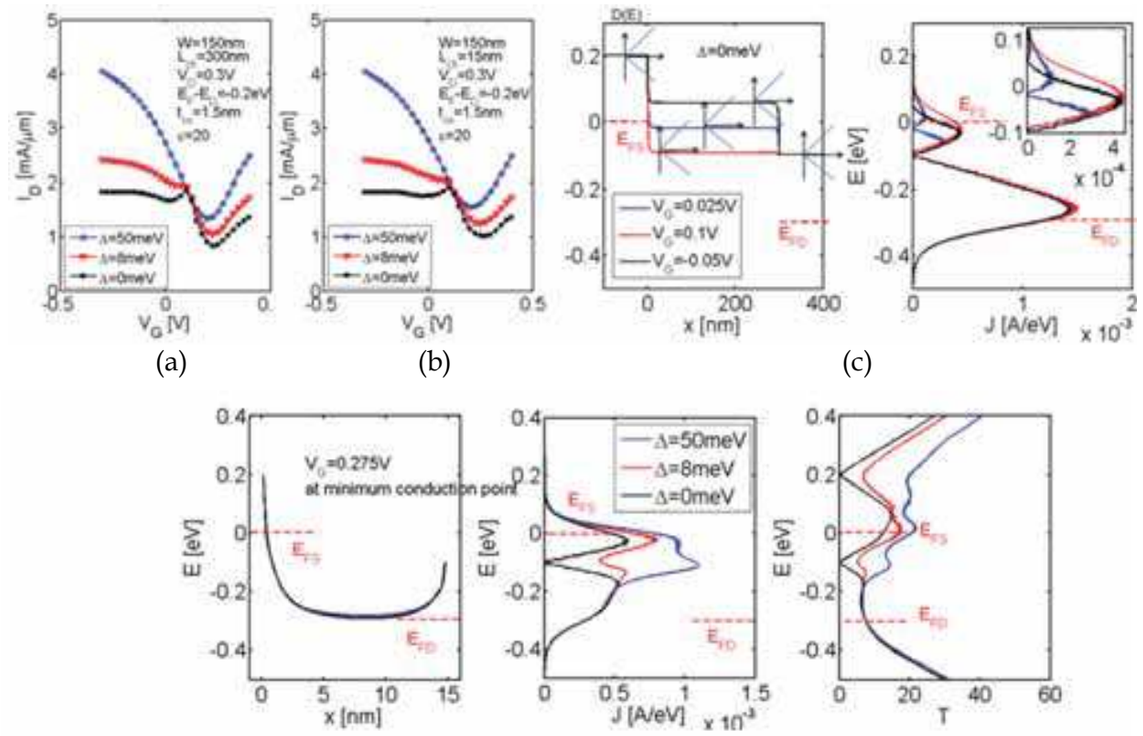


Fig. 6. (a) and (b) Effect of different coupling strength Δ at V_{DS} = 0.3 V. At about 0.2 V away from the minimum conduction point a distortion appears when metal/graphene coupling is weak (black and red lines). (c) shows S/D and channel DOS (cartoon) in series decide how total carriers transport through the channel. As Δ increases, DOS of graphene contact are broadened and distortion disappears. (d) For L_{ch} = 15 nm at V_G = 0.275 V, the drain Dirac point is between E_{FS} and E_{FD}, large Δ broaden DOS at drain contact, which increase the *T(E)*and total current.

of the DOS of graphene contacts increases the transmission coefficient *T(E)*. Larger *T(E)* leads to higher on current. When Δ = 0 eV (black curve in Fig. 6 (a)), beside the primary minimum conduction point, a distortion appears. The distortion corresponds with the minimum density-of-states (DOS) at the Dirac point of graphene. As shown in Fig. 6 (c), source, drain and channel contribute three cones in series, which decide states allowed for transport through the channel. At V_G = 0.025 V, both electron and hole cones of the channel graphene are involved, which gives a local minimum. When V_G = -0.05 V, carriers pass the channel through the channel hole half cone. In this case, the DOS minimum point of the channel is not in the transport energy windows between E_{FS} and E_{FD}, thus current increases compared with the local minimum case. When V_G = 0.1 V, carriers move through the channel electron half cone and current also increases. When the metal/graphene coupling strength increases, the DOS of the graphene contact regions are broadened. The current monotonically changes with V_G and the distortion disappears. A recent experimental work reports the presence of this type of distortion before annealing, and the disappearance of the distortion after annealing (Nouchi & Tanigaki, 2010). I_{min} also shows a dependence on Δ here. Fig. 6 (d) shows the minimum conduction point for L_{ch} = 15 nm. The drain Dirac point is between E_{FS} and E_{FD}. The broadened DOS at the drain contact increases the total current density. *T(E)* along the channel Dirac point at about -0.3 eV does not show a dependence on different coupling strengths Δ. Thus the increase of I_{min} corresponds to DOS broadening in the contacts, and not the MIS in the channel. We point out that when $V_{DS} > -(E_F-E_D)/q$ the minimum current will increase with higher metal/graphene coupling.

The performance of the FET upon scaling of the channel length is a crucial point, which is discussed in Fig. 7. As mentioned earlier, our model assumed a high-κ insulator to avoid short channel effect. I_{on} remains almost the same at different channel lengths, but I_{min} increases with short L_{ch}. As discussed in Fig. 6, at short channel lengths, I_{min} is mainly decided by direct source/drain tunnelling and the effect of MIS in the channel is weak. Here, when L_{ch} is reduced from 150 nm to 40 nm, the slight increase of I_{min} corresponds to the increase in the probability of source/drain tunnelling. When L_{ch} = 15 nm, source/drain tunnelling becomes more severe, leading to higher I_{min}.

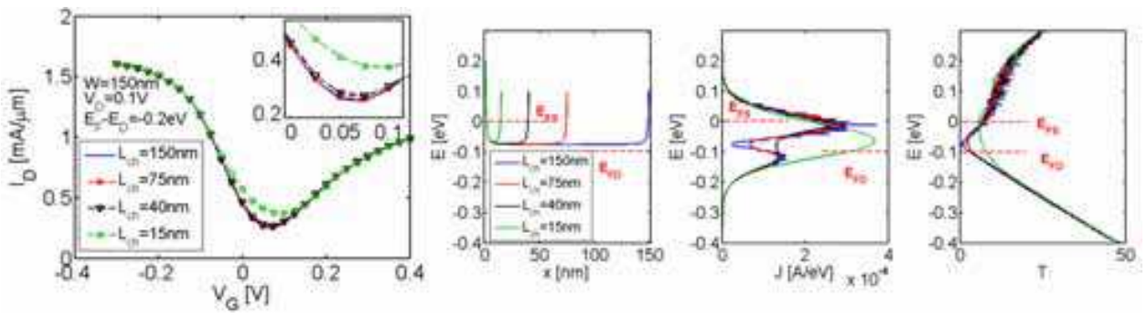


Fig. 7. Effect of channel length scaling at V_{DS} = 0.1 V. I_{on} stays the same when L_{ch} scaling down. As L_{ch} reduces I_{min} shows a slight increasing due to the direct source/drain tunnelling and at L_{ch} = 15 nm it becomes more severe thus I_{min} increase about 2 times.

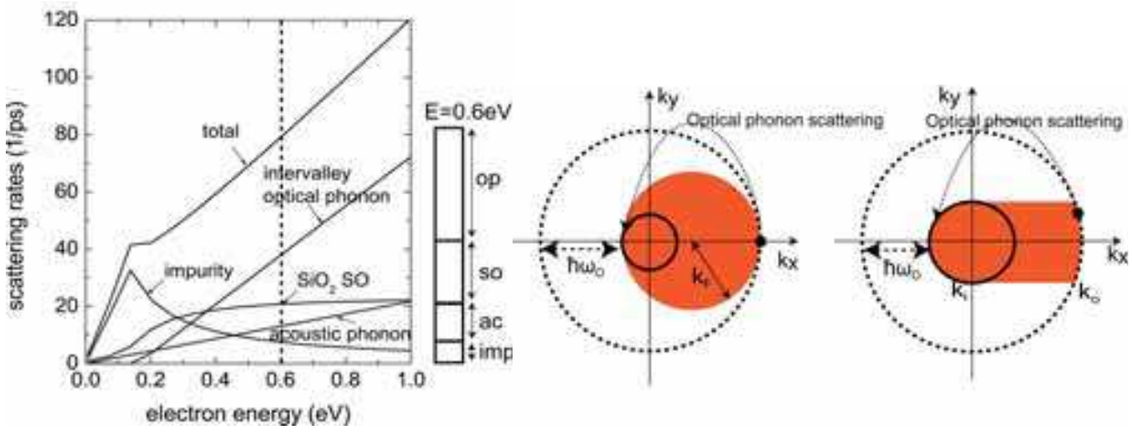
2.5 High field transport model of 2D graphene

In this section, we will answer two questions: what is the value of the saturation velocity in graphene and what are the dominant scattering mechanisms under high field. We will

discuss the role of all scattering mechanisms in high field transport. Simple models are used to estimate the saturation currents in graphene and also compared with the Ensemble Monte Carlo simulation (EMC) results.

The scattering rates of both elastic and in-elastic mechanisms at 300 K are shown in Fig. 8 (a). Two dominant modes of SiO_2 SO phonons, 60 meV and 148 meV, are considered in the plot. In order to capture high field effects, the scattering rates for 0 to 1 eV electron energies are calculated for all the scattering mechanisms. At high field, electrons are accelerated by the electric field and populate high energy states. Thus, the scattering rates at high energy states determine the current saturation. The intrinsic optical phonon scattering rate increases linearly with energy, whereas SO phonon scattering rate 'saturates' for high energy states. The impurity scattering rate decreases with the energy and is negligible at high energy. Although the acoustic phonon scattering rate increases with energy, it is smaller than the optical phonon scattering at high energies. In Fig. 8 (a), the bar plot shows the relative magnitudes of scattering rates at E = 0.6 eV. From these observations, optical phonon scattering is dominant for graphene under high field. In exfoliated graphene the substrate temperature can be heated to as high as 1000 K so that the 60 meV mode SO phonon scattering is more than one magnitude higher than at room temperature. As a result, this low energy mode plays a dominant role in energy relaxation of electrons at high temperature. Optical phonon emission is not the dominant energy relaxation mechanism in those situations. On the other hand, in epitaxial graphene grown on SiC substrate, the lowest SO phonon mode energy is 116 meV (see Section 2.2), which is higher than that in SiO_2 and close to the intrinsic optical phonon energy of graphene**.** The scattering rate is also lower than that in SiO_2 due to the weak polarization of Si-C bonds. Furthermore, the thermal conductivity of SiC is much higher than SiO_2. Thus, the high field transport property in epitaxial graphene is limited by its intrinsic optical phonon scattering. From Fig. 8 (a), the phonon scattering at high energy is more than 10 ps^{-1}. Optical phonons generated by electrons have to relax to other phonon modes before the heat can propagate into the substrate or contacts. The characteristic lifetime of optical phonon decay into acoustic phonons is around 1 to 5 ps in carbon-based sp^2 crystals. Since optical phonon lifetime is much longer than phonon generation time (<1 ps), the optical phonon population in graphene is out of equilibrium. The fast generation rate and slow decay rate of optical phonons create the non-equilibrium phonon effect in graphene.

To begin, we assume the phonon scattering is instantaneous and ignore all other elastic scatterings. Under this assumption, two possibilities of electron distribution functions are shown in Fig. 8 (b). The first model assumes that the Fermi circle keeps the shape but drifts rigidly along the electric field direction. Optical phonon emission empties the high energy states and fills the low energy states. As such, the instantaneous phonon emission stops further movement of the Fermi circle and a steady state distribution is achieved. The difference of highest energy state (dotted circle) and lowest energy state (solid circle) is exactly the optical phonon energy $\hbar\omega_0$. Fig. 8 (b) shows another possibility of the steady state distribution function. The energy difference between these dotted and solid circles is the optical phonon energy. Optical phonon emission by electrons in states between the two circles is prohibited by the Pauli exclusive principle. Optical phonon emission is allowed only for electrons approaching the dotted energy circle. The optical phonon emission continues to scatter the electrons from high energy states back to the low energy states. As a result, the Fermi circle is squeezed due to the Pauli principle. Both of the models capture



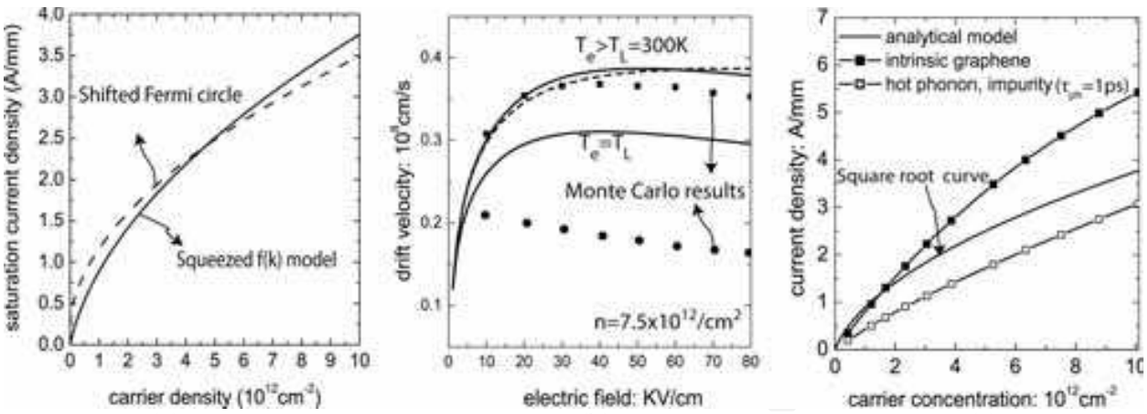
(a) (b)

Fig. 8. (a) Scattering rates vs. energy in 2D graphene: impurity density $n_{imp} = 5 \cdot 10^{11}$ cm^{-2}, T=300 K. The bar shows the relative scattering rates at an energy of 0.6 eV. (b) Current saturation model in 2D graphene: (left) The drift Fermi circle model. k_F is the Fermi wave vector. (right) Squeezed distribution function model. The outer circle radius is k_o and the inner circle radius is k_i.

the effect of carrier degeneracy, which has not been discussed in non-degenerate conventional semiconductors.

The calculated saturation currents versus carrier density for the two models are shown in Fig. 9 (a); the result of the two models are very similar. Both of the models give a roughly square root relation of saturation current versus carrier density. From $J_{sat} = en v_{sat}$, the ensemble saturation velocity v_{sat} is proportional to $n^{1/2}$. Saturation velocity in conventional semiconductors is typically a constant, e.g. $v_{sat} = 10^7$ cm/s in Si. The primary reason for the difference is the degeneracy of carriers and the Pauli principle. Non-degeneracy of carriers leads to constant saturation velocity and fully degenerate carrier leads to a square root relation for 2D systems. This theoretical model is in good agreement with the measurement for graphene on SiO_2 substrate (Dorgan et al., 2010). The agreement of the model and measurement results indicates that the carriers are degenerate in such graphene devices under high field.

The analytical models capture the carrier degeneracy effect but ignore the rise of carrier temperature due to the applied electric field. In reality, the optical phonon emission rate is not instantaneous, so that carriers have opportunities to populate high energy states giving rise to a tail of the distribution function at high energies. At the same time, other scattering mechanisms spread the carrier distribution over a wider range in k space. Moreover, electron electron (e-e) scattering is strong in graphene at high carrier densities, causing carriers to thermalize to a Fermi-Dirac distribution with a finite temperature. In order to capture all of these effects, we applied an electron temperature approximation to high field transport. Since the carriers are degenerate in graphene, a shifted Fermi-Dirac distribution function is assumed, rather than the Boltzmann distribution used for conventional semiconductors (Lundstrom, 2000).



(a) (b) (c)

Fig. 9. (a) Current vs. carrier density of the two models. (b) Velocity vs. electric field based on electron temperature approximation. Solid lines: (upper) $T_e > T_L = T_{op} = 300$ K and (lower) $T_L = T_e$, $T_{op} = 300$ K; Dashed line: $T_{op} = T_e$; $T_L = 300$ K; Squares: MC simulation, $T_{op} = T_L = 300$ K; Circles: MC simulation, with hot phonon $\tau_{ph} = 5$ ps, $T_L = 300$ K. (c) Current vs. carrier density. Solid line: analytical current saturation model; Solid square: no hot phonon, $T_L = T_{op} = 300$ K, $F = 2 \cdot 10^4$ V/cm; Open square: with hot phonon, $T_L = 300$ K, $F = 8 \cdot 10^4$ V/cm, $\tau_{ph} = 1$ ps;

The 2D electron gas, acoustic phonon and optical phonon are not fully in thermal equilibrium with each other at high field. The acoustic phonon temperature T_L is the lattice temperature. The optical phonon temperature T_{op} describes the optical phonon vibrations. In Fig. 9 (b), the upper solid curve shows the currents by assuming lattice temperature is in equilibrium with environmental temperature, $T_e > T_L = 300$ K. The current decreases if assuming the graphene lattice temperature increases with electron's temperature, $T_L = T_e$, which is shown in the lower solid curve. In these two curves, the optical phonon temperature is still assumed to be in equilibrium with room temperature, $T_{op} = 300$ K. From the comparison of the two solid curves, the current drops substantially due to lattice heating. This indicates that acoustic phonon scattering could limit the current if graphene is heated to high lattice temperature. The Monte Carlo simulation results (square and circle symbols) are also shown on Fig. 9 (b). The black square dots are in good agreement with the model prediction. This indicates that the electron temperature approximation is a reasonable model for high field transport in graphene. The optical phonon temperature T_{op} rises due to the emission of phonon by electrons. The effect of optical phonon temperature increase is considered in the dashed curve in Fig. 9 (b), in which the optical phonon temperature is in equilibrium with electron's temperature, $T_{op} = T_e$. However, the current does not show obvious degradation. This indicate that temperature rise of optical phonons has less impact on the current compared to lattice temperature. On the other hand, the squares considering non-equilibrium (hot) optical phonon show more degradation of the current. This finding indicates that the non-equilibrium phonon is dominant in high field transport in graphene.

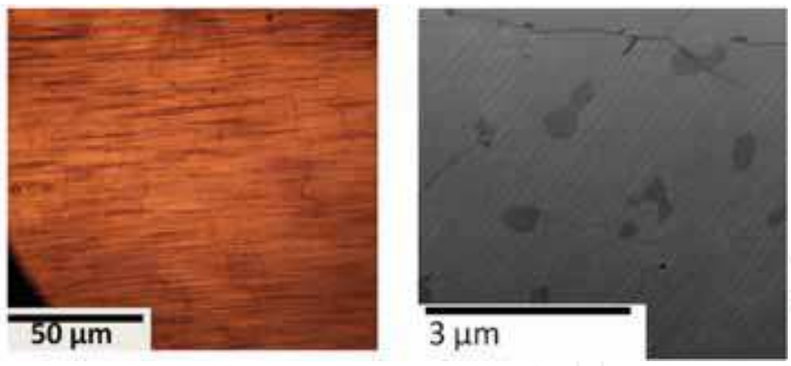
In Fig. 9 (c), the saturation current versus carrier density curves are shown. The solid black curve shows the analytical result from the squeezed distribution function model for comparison. The square-line is the intrinsic saturation currents of grapheme without hot phonon effect. In the absence of hot phonons and impurity scattering, the current-field curves show strong negative differential resistance (NDR). The currents of the squares are at a field of

F = $2 \cdot 10^4$ V/cm. The saturation current is lower than the analytical result (solid line) when hot phonon exists in grapheme (open square line). In MC simulation, we also find that the saturation currents vary with the phonon lifetime. The longer is lifetime of phonon the lower is the saturation current. At high field, the impurity scattering has an effect on saturation current, but it is minor compared to the hot phonon effect. Saturation current density around 3 A/mm has been measured in epitaxial graphene on SiC substrate (n~10^{13} cm^{-2}) (Moon et al., 2009), which is consistent with our simulation result considering hot phonon effect (open square line). At low carrier densities, J_{sat} as a function of n curves are approximately linear; the slopes correspond to the ensemble saturation velocities. The saturation velocity thus extracted for intrinsic graphene (neglecting charged impurity scattering and hot phonon effect) is $5.2 \cdot 10^7$ cm/s and $2.7 \cdot 10^7$ cm/s when hot phonons are considered. From the simulation results, the hot phonon effect determines the saturation currents in graphene on substrates without strong SO phonon coupling. The (semi-) analytical models best serve as a rough guideline, since elastic scattering processes, and especially the hot phonon effect are not captured in the model, which is done in the EMC approach.

2.6 2D graphene FETs based on CVD grown graphene on Cu

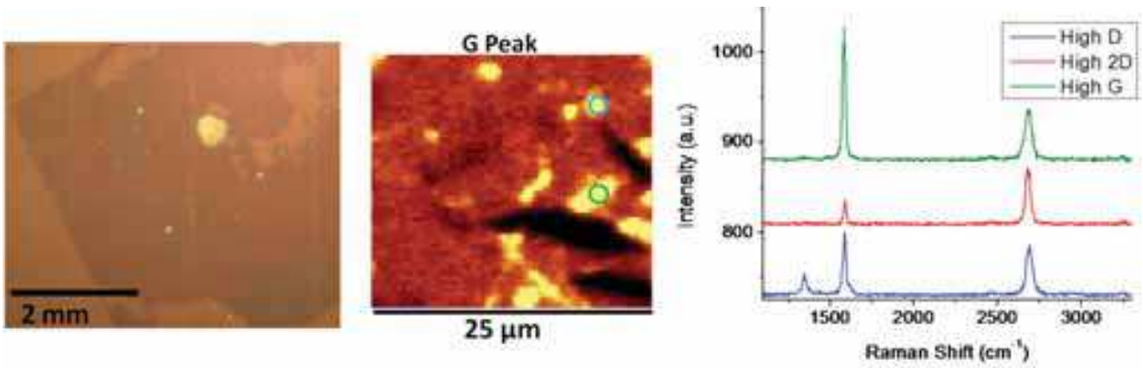
Availability of high-quality large-area graphene on suitable handling substrates will ultimately determine the success of graphene as a device platform. Recently, the formation of single layer graphene via catalyzed-chemical vapour deposition (CVD) on copper foils has generated a rapidly growing body of research (Li et al., 2009). A few groups have reported the CVD growth of graphene on copper, and transport properties including quantum Hall effect (Levendorf et al., 2009; Bae et al., 2010) in layers subsequently transferred to insulating substrates. So far, mobility in Cu-CVD based graphene transferred to SiO_2/Si wafers has been measured around 4 000 cm^2/Vs while mobility of exfoliated graphene on SiO_2/Si has been demonstrated to exceed 15 000 cm^2/Vs. The reduced mobility for Cu-CVD graphene could come from the quality of the graphene itself (eg. lower uniformity, defects, small domain size) or from contamination introduced during the wet transfer process. There have been no careful studies of FETs fabricated from CVD grown graphene. In this work, we report the characteristics of single-layer graphene FETs whose channels were grown by CVD on copper.

We grow Cu-catalyzed CVD graphene in a quartz tube furnace under flow of CH_4 and H_2 with an Ar background on copper foils and on evaporated copper films. Pre-growth chemical and thermal treatment of the copper catalyst material enables single layer graphene deposition at temperatures ranging from 800 - 1050 °C (Fig. 10). For our optimized growth step, the chamber conditions are: CH_4:H_2 gas flow of 100:20 sccm, pressure of 2 Torr, and a temperature of 1000 °C. The gas and pressure are kept at the growth conditions during cooldown until the system is below 500 °C when the growth gases are turned off and an Ar flow is introduced. Fig. 10 shows optical and SEM images of as grown graphene on a copper foil substrate. Following growth, graphene sheets are transferred to a range of host substrates (typically quartz or silicon) using wet etch methods similar to those described in other work (Li et al., 2009). Fig. 11 (a) shows an optical image of a graphene sheet following removal of the PMMA used to support the graphene during wet transfer. Large regions of clean graphene are apparent along with areas of visible contamination from processing. Improvement of the transfer process is underway to reduce contamination introduced during processing.



(a) (b)

Fig. 10. (a) Optical image and (b) SEM image of as grown graphene on Cu foil.



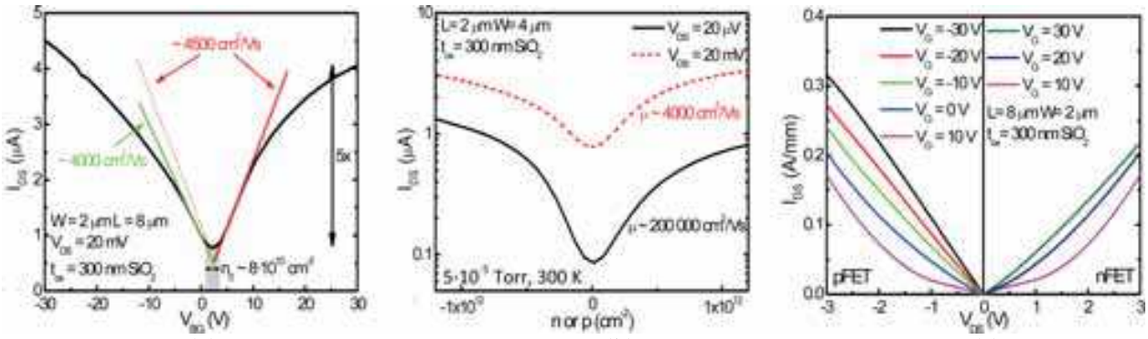
(a) (b) (c)

Fig. 11. (a) Optical image of as graphene following wet transfer to SiO_2/Si substrate. (b) Scanning Raman image of G peak of transferred graphene. (c) Raman spectra at indicated points from the G peak scan. The middle spectrum is representative of the main field of the graphene sample with characteristic 2D:G ratio of 2 of single layer graphene.

Following transfer, Raman mapping is used to determine the quality and uniformity of the CVD-graphene. Large area single-layer graphene regions are verified from the signature 2D:G peak ratio of ~2, that is uniform over large regions (Fig. 11 (a)). Complementary SEM and AFM characterization corroborate the Raman result. Fig. 11 (b) shows a map of the G peak intensity across a 25 µm x 25 µm field and the individual Raman spectra from the three circled locations are in Fig. 11 (c). The middle (red) spectrum is found in most of the graphene region consistent with the presence of high-quality single-layer graphene as indicated by the absence of a D peak at 1350 cm^{-1} and the characteristic 2D:G peak ratio > 2. The bright spots in the G peak scan have two types of associated spectra. The bottom (blue) spectrum is from a region with high defect peak intensity suggesting either contaminated or defective regions of graphene. The top (green) spectrum has a low defect peak intensity indicating high quality graphene, but has a low 2D:G peak ratio consistent with more than one layer of graphene.

Back-gated FETs were prepared by transferring the single-layer graphene to 300 nm SiO_2/conductive Si substrates, followed by conventional e-beam lithography, O_2 plasma etching of the graphene for device isolation, ohmic metal evaporation (Cr/Au), and lift-off.

The backside of the conductive Si wafer was metalized for back gating. The channel lengths of the FETs range from 1 – 8 μm and the channel widths vary between 1 – 4 μm. Based on the transfer characteristics (Fig. 12 (a)), the field-effect mobility is found to be ~4500 cm^2/Vs for electrons and slightly lower for holes. The Dirac point is at V_{BG} ~2 V, much closer to zero volt than in case of exfoliated graphene sheets, indicating close to equal amount of positive and negative charged contamination on the surfaces. The impurity concentration is estimated from the measurement to be ~$8 \cdot 10^{10}$ cm^{-2}. The devices exhibit field-effect current modulations of ~4 - 6 at 20 mV V_{DS} at gate sweeps of +/-30V (Fig. 12 (a)). Interestingly at very low applied source-drain bias (V_{DS} = 20 μV) the modulation increases significantly (Fig. 12 (b)). The current does not scale linearly; ~1000X lower bias causes less than ~10X smaller current. The apparent field-effect mobility is ~200 000 cm^2/Vs, but we stress that this is not a fundamental property of graphene, it just indicates the limitation of the traditional model to estimate the mobility of high purity graphene samples.



(a) (b) (c)

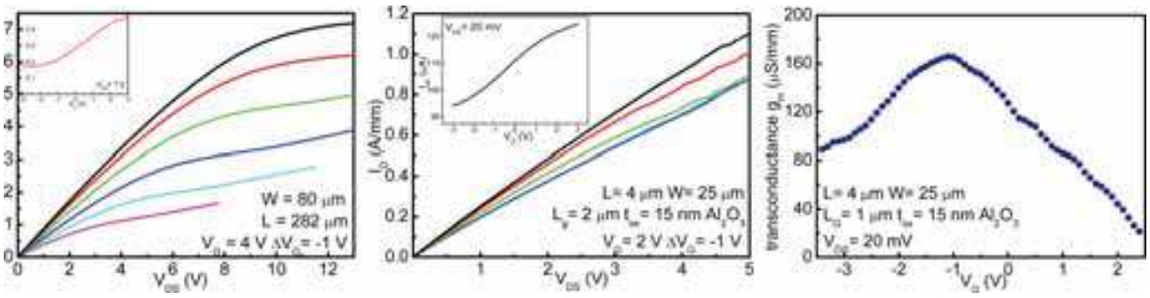
Fig. 12. (a) Transfer characteristic of a 2D graphene FET transferred to Si/SiO_2 substrate. The calculated impurity concentration is 8.10^{10} cm^{-2}. (b) Very low (V_{DS} = 20 μV) applied drain bias gives an extremely high apparent field-effect mobility. (c) High-field family I-V curves showing both sub-linear and super-linear behaviour.

At high drain bias voltages (Fig. 12 (c)), the DC output characteristics of the devices were linear up to ~1 V V_{DS}, and deviated significantly from linearity at higher drain biases. The super-linear behaviour is especially evident at gate biases close to the Dirac point, and is indicative of zero-gap single-layer graphene.

2.7 Epitaxial graphene RF FETs on SiC for analog application

While DC performance has been extensively studied just a few small signal characterizations have been done so far. The widely observed high carrier mobility naturally focuses our attention towards high frequency performance of graphene based devices. Gigahertz operation of exfoliated (Lin et al., 2009) and epitaxial (Moon et al., 2009) graphene FETs has been reported. Here we present the high frequency performance of graphene devices based on epitaxially grown graphene on SiC substrates. The measured $f_T \cdot L_G$ product of 8 GHz·μm and f_{max} of 16 GHz is in very good agreement with previously reported values (Moon et al., 2009). Surprisingly, in spite of the much lower electron mobility and transconductance, these FETs demonstrate remarkable small signal performance comparable to the small signal performance of higher mobility exfoliated graphene devices. Recently significant improvement was reported: device with $f_T \cdot L_G$ = 24 GHz·μm (Lin et al., 2010).

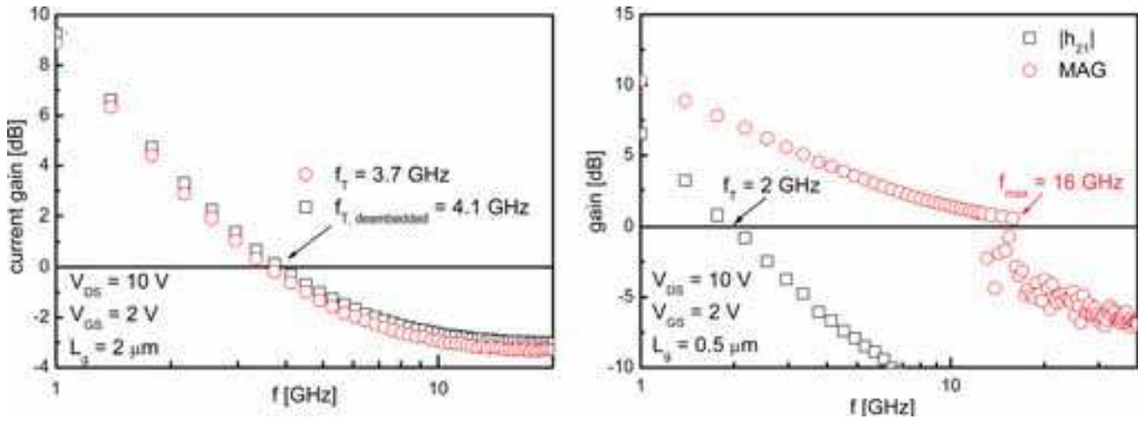
Epitaxial graphene FETs were fabricated on 2-3 layer graphene on Si-face 4H-SiC. According to AFM and LEEM characterization and Raman measurements the graphene thickness is 1.9 layers in average over the wafer (Luxmi et al., 2009). Graphene is patterned by optical lithography and etched it in O_2 plasma. Using the same resist-pattern the SiC is etched 100 nm deep in CF_4 plasma to facilitate the sticking of the metal contacts on the surface. Cr/Au source/drain contacts and e-beam evaporated Al_2O_3/Ti/Au top gate (t_{ox} = 15 nm) have been deposited to form field effect transistors (FETs). For increased RF performance short gates were fabricated using e-beam lithography. The channel lengths of the devices range from 1-4 μm and the gate length is 1 - 2 μm in optically defined and 40 - 500 nm in e-beam patterned devices. Standard ground-signal-ground probing pads are lithographically realized for the gate and drain. Open structures were used to de-embed the signals of the parasitic pad-capacitance.



(a) (b) (c)

Fig. 13. Output characteristics of a saturating large area graphene transistor (a) and the graphene transistor (b), which RF characteristic is shown on Fig. 14. Insets: transfer characteristics at V_{DS} = 1 V (a) and at V_{DS} = 20 mV (b). (c) Transconductance as a function of gate voltage at V_{DS} = 20 mV.

Hall measurements reveal μ ~ 200 – 500 cm²/Vs throughout the sample showing smooth variation and better performance in the middle of the wafer. The DC output characteristics of the devices were linear up to 5 V and slightly sublinear above 10 V. The drain current had a weak gate dependence as we swept the gate voltage between +/- 2.5 V. In the high source-drain bias range the gate modulation decreased indicating a non-reversible degradation mechanism by high electrical field. The transconductance of the devices varied between 120 – 400 μS/mm, which is significantly lower than in case of exfoliated devices having the same gate length. For very long gate lengths, reasonable current modulation and current saturation was observed as shown in Fig. 13 (a). However, with scaling of the gate length, the gate modulation and current saturation properties degraded substantially, indicating the need for improvement of material quality and gate material processing. In spite of the weak gate modulation, it is possible to envision usage of graphene FETs in low-noise amplifiers (LNAs) if RF performance improves. In addition, single layers of almost transparent graphene may be transferred to flexible insulating substrates, which can offer low-cost high frequency performance. Small signal performance of devices with gate-lengths between 2 μm and 0.5 μm on epitaxially grown graphene were measured. The used bias-conditions for the FETs are V_{DS} = 10 V and V_{GS} = 2 V.



(a) (b)

Fig. 14. (a) Current gain as function of frequency for a graphene FET with 2 μm long gate. (b) f_T and f_{max} of a graphene transistor with 0.5 μm long ebeam-defined gate.

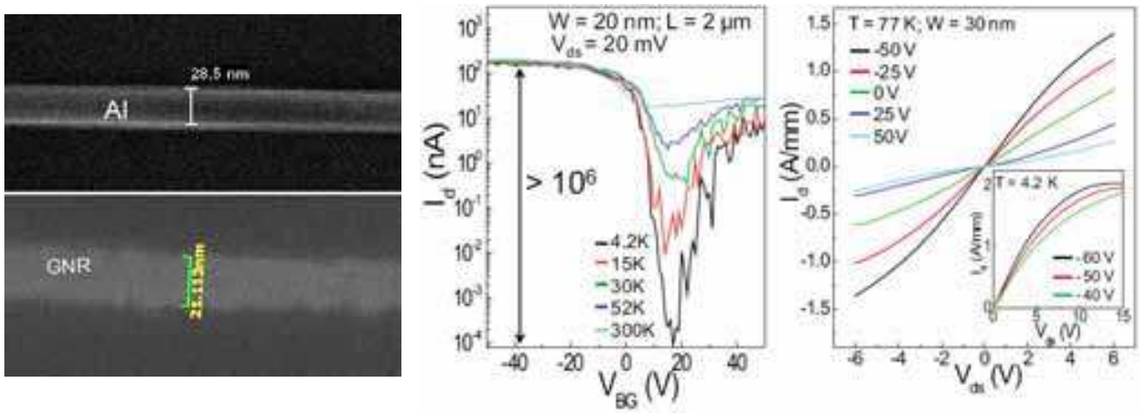
A deembedded current gain cut-off frequency f_T of 4.1 GHz for devices with 2 μm long gates was achieved (Fig. 14 (a)). For a graphene FET with a 0.5 μm long gate an exceptional high power gain cut-off frequency f_{max} of 16 GHz is demonstrated. (Fig. 14(b)). These preliminary results are very encouraging and demonstrate the potential of the epitaxially grown graphene devices for high-frequency applications. As the quality of graphene on insulating substrates improved over time indeed cut-off frequency higher than 100 GHz was demonstrated (Lin et al., 2010). Moving from zero-bandgap single-layer 2D graphene to bilayer graphene or graphene nanostructures can enable controlled bandgaps. We present our efforts to date on the latter approach in the following section.

3. Graphene nanoribbon transistors

3.1 Band gap of graphene nanoribbons

Two-dimensional (2D) graphene sheets are nearly metallic, while ultrathin graphene nanoribbons (GNRs) can show semiconducting properties with the energy bandgap scaling inversely with the ribbon width. The achievable energy bandgap, superior transport properties, and the planar manufacturability establish GNRs as promising cornerstones beyond the Si CMOS technology (Zhang et al., 2008; Murali et al., 2009). Although sub—10 nm GNRs have been demonstrated by chemical approaches (Li et al., 2008; Jiao et al., 2009), the ability to form GNRs lithographically will facilitate the fabrication compatibility with the conventional planar integrated circuit (IC) manufacturing technology. GNRs were fabricated on exfoliated graphene flakes on SiO_2/Si. The oxide thickness is 300 nm and the Si substrate is heavily doped n-type. Al metal masks were patterned by EBL and e-beam deposition. The exposed graphene was removed by O_2 plasma etching and the metal masks were removed by Al etchant. GNRs connected to two 2D graphene sheets were thus achieved. Fig. 15 (a) shows the SEM images of a 29 nm wide Al strip mask (top) and a 21 nm wide GNR (bottom). The fact that the obtained GNR is thinner than the Al mask indicates the effect of lateral etching in O_2 plasma. Cr/Au was e-beam deposited as source (drain) contacts on the 2D graphene areas to reduce the contact resistance. Al/Au was used as the back-gate contact. The length of GNRs in this work is 2 μm. Current-voltage (I-V) measurements were performed in vacuum (~10^{-6} Torr) with the temperature ranging from 4.2 K to 300 K.

The temperature dependent transfer characteristics of GNRs at V_{DS} = 20 mV are shown in Fig. 15 (b). It is clearly seen that the minimum current decreases with decreasing temperature while the maximum current (due to the hole conduction) remains almost unchanged. As a result, the back-gate modulation increases from ~ 12 at room temperature to > 10^6 at 4.2 K, indicating the formation of energy bandgap. The positive Dirac point indicates the presence of holes, which can be induced by negatively charged impurities, at zero gate bias. It is worth noting that the transfer curve does not show the symmetric V shape, with the hole conduction much stronger than the electron conduction, a phenomenon often seen in GNRs (Chen et al., 2007). This is attributed to surface impurities based on the fact that surface passivation by Al_2O_3 grown by atomic layer deposition (ALD) was found to be able to improve the electron conduction. But the exact origin remains unclear currently and is under investigation. Fig. 15 (c) shows the high field (corresponding to 30 kV/cm at V_{DS} = 6 V) family I-Vs measured at 77 K. The drain current exhibits tendency to saturate at high drain bias and the maximum current density is ~1.4 A/mm. The inset shows I-Vs measured at 4.2 K. The maximum current density reaches 2 A/mm at V_{DS} = 15 V (equivalent electric field: 75 kV/cm), indicating high current drive capability of GNRs. The source and drain electrodes were found to be exchangeable as can be seen from the symmetric I-Vs in the first and third quadrant. This is not unexpected since the back gate controls the whole GNR channel universally.



(a) (b) (c)

Fig. 15. (a) SEM image of an Al strip (top) and a GNR (bottom) formed using the Al strip as etching mask. (b) Temperature-dependent transfer characteristics at 20 mV drain bias and (c) high field family I-Vs measured at 77 K and 4.2 K (inset).

The quantum confinement in the quasi-1D GNR channel creates discrete subband energy levels, which are filled by carriers in sequence as the gate voltage increases. As a result, staircase-like features are expected in the transfer curve. Such quantum conductance was observed in the patterned GNRs. The conductance quantization was seen in different GNR devices and Fig. 16 (a) shows a typical transfer curve measured at 30 K plotted in the linear scale exhibiting conductance plateaus with roughly equal spacing. The conductance modulation by the back gate is about 200 at this temperature. GNRs with armchair edges have band structure expressed as:

$$E(k_n, k_y) = \hbar v_f \sqrt{k_n^2 + k_y^2} \tag{1}$$

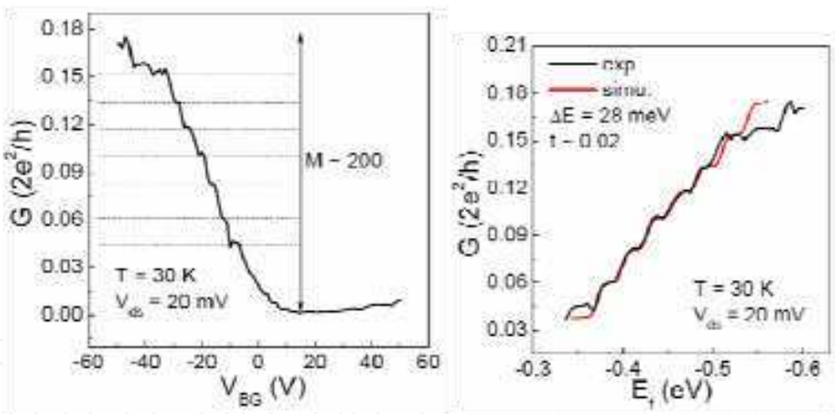
where v_f (10^8 cm/s) is the Fermi velocity, $\hbar$ is the reduced Plank's constant, and k_y is the wave vector in the GNR length direction. The transverse wave vector k_n can only take allowed discrete values defined at $n\pi/3W$ (n is non-zero integer)(Fang et al., 2008). Therefore, perfect armchair GNRs should have quantized energy levels separated by:

$$\Delta E = \hbar v_f \pi / 3W \tag{2}$$

For GNRs with W = 20 nm, ΔE is calculated to be ~ 34 meV. At zero temperature, only the energy levels below the Fermi level E_f populated with electrons in the conduction band, or those above E_f populated with holes in the valence band, contribute to the conductance. Each 1D energy level (or mode) has a finite transmission probability. The overall device conductance at a finite temperature is the summation of all the available conducting modes, and is described by the well-known Landauer formula:

$$G = \left(\frac{2e^2}{h}\right)\sum\nolimits_i t_i(E)\left(-\frac{\partial f}{\partial E}\right)dE \tag{3}$$

where t_i is the transmission probability of the i-th mode and f is the Fermi-Dirac statistics. The nearly equal spacing of the plateaus shown in Fig. 16 (a) reveals that each conduction mode should have similar transmission probability. To further analyze the measured conductance quantization using Landauer formula, the back-gate voltage needs to be correlated with the Fermi energy. The link between them is the carrier density in the channel:



(a) (b)

Fig. 16. (a) a typical transfer curve measured at 30 K showing conductance plateaus and (b) fitting of the experimental data using Landauer formula.

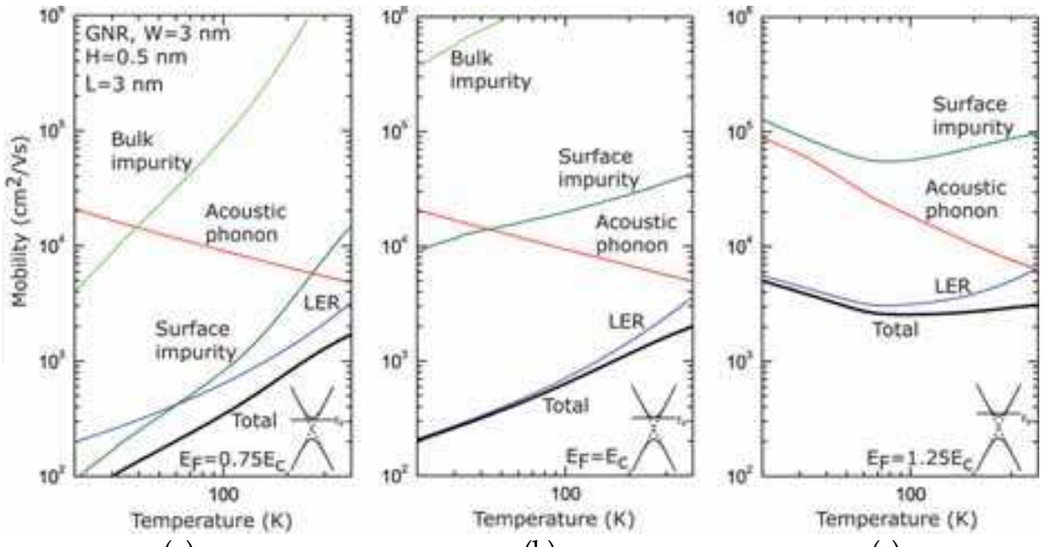
$$C_g(V_{BG} - V_{Dirac}) = E_f^2 / \pi\hbar v_f^2 \tag{4}$$

where C_g is effective gate capacitance per area (F/cm^2). Both sides of the above equation give the carrier sheet density (cm^{-2}) in the GNR channel (Fang et al., 2007). The experimental data were fitted using Eq. (3), with ΔE, t, and C_g as adjustable parameters. Excellent agreement was achieved as shown in Fig. 16 (b). The obtained subband energy separation from the fitting is 28 meV, close to the calculated value (34 meV) for W = 20 nm. The

discrepancy could be due to the likely existence of a mixture of both armchair and zigzag orientations in GNRs. The average transmission probability is $t \sim 0.02$, similar to that reported in (Lin et al., 2008). The very small t can be explained by the scattering due to GNR edge/bulk disorder which can severely suppress the conductance causing G much smaller than $2e^2/h$ (Mucciolo et al., 2009).

3.2 Low field transport in GNR

GNR with width down to 20 nm by lithography (see Section 3.1) or 2-5 nm by chemical preparation (Li et al., 2008) has been achieved. The measured carrier mobility (~200 cm^2/Vs) in the ultrathin GNRs are reported to be much lower than in corresponding 2D graphene sheets. GNR opens a bandgap by the edge confinement, but the edges induce line edge roughness (LER) scattering besides the normal scattering mechanisms present in 2D graphene. The LER scattering has W^{-4} dependence on the width of GNR, which is due to the linearity of graphene band structure (Fang et al., 2009). The effect of LER scattering depends on the width of GNR and the height of the roughness, which related to the fabrication processes. The mobility due to various scattering mechanisms was calculated in the Boltzmann transport scheme (Fang et al., 2009). Fig. 17 shows the mobility in a 3 nm wide GNR. The roughness height 0.5nm is used in the calculation. Scattering from surface impurity located at interface of GNR and substrate and line edge roughness (LER) are dominant at low carrier density shown in Fig. 17 (a). However, LER scattering becomes more important at higher carrier density (Fig. 17 (c)). This is due to the increasing of screening of the impurity charge in GNR at high carrier density. At the same time, acoustic phonon scattering also plays important role in limiting the mobility at 300K or higher temperature. The mobility from the theoretical calculation qualitatively explains the mobility measurement results in ultra-thin GNRs (Li et al., 2008).



(a) (b) (c)

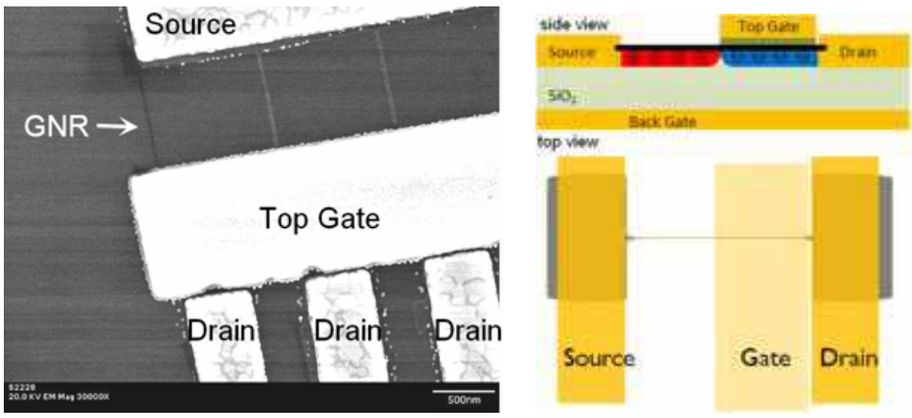
Fig. 17. Mobility in a GNR as a function of temperature for three distinct Fermi levels. The relative importance of the various scattering rates can be ascertained from the plots.

More recently, the LER scattering was investigated elaborately by measuring the carrier mobility in different width GNRs (Yand & Murali, 2010). The mobility is found to decrease

at rate W^{-4} when the width is narrower than 60 nm, which indicates the height of LER in GNR fabricated by lithography is larger than 0.5 nm. In SEM the height of LER is estimated to be 2~3 nm, so that the theoretical work and experimental measurements are in agreement. The LER also induces states in the band gap, which enhance the Zener tunnelling probability. This effect has been studied in the tunnelling field effect transistors structure by numerical simulations (Luisier & Klimeck, 2009). The LER increases the off state current, which degrades the performance of FETs by increasing the sub-threshold voltage. The experimental works to achieve thinner GNR with better edges are future tasks to realize devices based on GNRs.

3.3 Graphene nanoribbon p-n junction transistors

For the reason outlined above GNR FET devices with both top- and back-gates were fabricated. The fabrication started by back gated GNR FETs as described in Section 3.1. Then using 1 nm e-beam evaporated Al as a seed layer, 30 nm ALD Al_2O_3 was deposited. The channel length of the fabricated devices is 2 μm and the length of the top gate electrode is about 1 μm, covering half of the channel. The SEM image on Fig. 18 shows a typical FET.

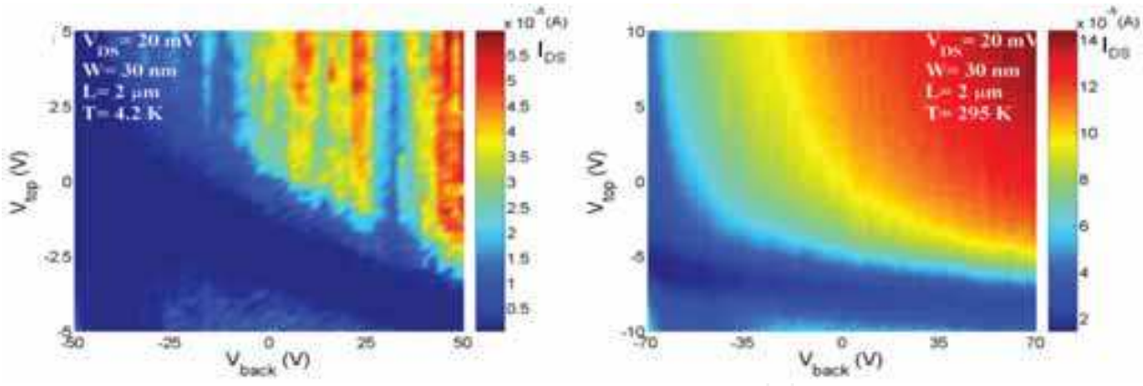


(a) (b)

Fig. 18. (a) SEM image and (b) schematics of the GNR FET. Half of the channel is top-gated, while the whole device is back-gated. Device parameters: L = 2 μm, L_G = 1 μm, W = 30 nm.

In this section the measurements of a representative device at room temperature will be presented. It is found that at high applied source drain current the temperature has very little effect on the device performance, namely at cryogenic temperature the high-field modulation is only ~10% more. Many similar devices were fabricated and similar characteristics were observed in all cases. Fig. 19 (a) and (b) shows the source-drain conductance at V_{DS} = 20 mV and at V_{DS} = 1 V respectively as a function of the top-gate and the back-gate voltage.

The back-gate capacitance is ~11 nF/cm² assuming κ = 3.9 and the top gate capacitance is 209 nF/cm² calculated based on the measurement of the minimum conductance (Dirac) point shown in Fig. 19 (b). The Dirac point is defined by the ratio of the applied voltages on both gates, the slope defining the value of C_{top}/C_{back} ~19. From either a constant back-gate or constant top-gate slice we can determine V_{TG}^0 = -6 V and V_{BG}^0 = -70 V, indicating strong n-type doping. While the devices before the top gate deposition were slightly p-type doped one can conclude that the strong n-doping is caused by trapped charges in the top gate oxide and other impurities on the graphene oxide interface.

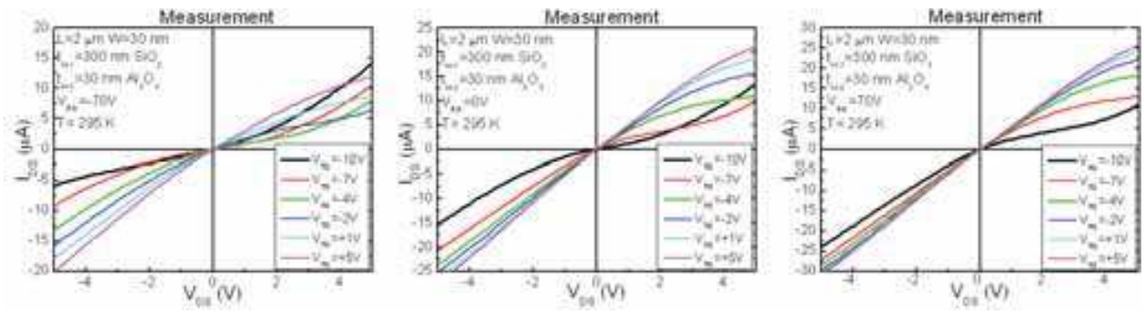


(a) (b)

Fig. 19. (a) Conductance steps at 4.2 K at low source-drain voltage (linear scale); (b) At room temperature the modulation is smaller even at low bias (V_{DS}= 20 mV).

Temperature dependent measurements have confirmed band-gap opening of >26meV depending on GNR widths, and result in 20x and 10^3x modulation at room temperature and 4 K, respectively, by varying the top gate potential between +/- 5V.

The source and drain contacts are in contact with a large 2D graphene region to ensure low contact resistance. The 2D graphene has no bandgap so the Cr/Au metal can form good ohmic contacts easily. The back-gate may vary the carrier concentration of the graphene at the contacts, but due to its large size it will always have much lower resistance than the GNR channel, always supplying the channel with enough carriers. Fig. 20 (a), (b) and (c) shows the measured I_{DS} for different top gate voltages at V_{back} = -70, 0 and +70 V respectively.



(a) (b) (c)

Fig. 20. I_{DS} versus V_{DS} of the GNR p-n junction FET at -70 V (a), 0 V (b) and +70 V (c) back gate bias. Plateauing of the IV characteristics can be observed in all three cases, but at different bias conditions.

To understand the device operation, examine the device model in detail. The channel of the devices can be separated into two distinct regions: one with a back-gate only, and the other with both top- and back-gates. A model have been developed to explain the transistor characteristics of the p-n channel GNR FET by extending the work of Meric et al., 2008. A field effect model was applied to both side of the junction, defining the only back-gated region similarly as the top-gate having V_{TG} = 0 V:

$$n(x) = \sqrt{n_0^2 + \left(\frac{C_{tg}}{q}(V_{tg} - V_{tg0} - V(x)) + \frac{C_{bg}}{q}(V_{bg} - V_{bg0} - V(x)) \right)^2}, \quad (5)$$

where is x is the distance along the channel and $V(x)$ is the potential in the channel due to the applied source-drain voltage. The current in the channel is expressed by:

$$J(x) = qn(x)\mu F(x), \tag{6}$$

where μ is the mobility and $F(x)$ is the electric field along the channel. The I-V characteristics are obtained by forcing current continuity in a self-consistent electrostatic and transport model:

$$I(V_{DS}) = q\frac{W}{L}\mu \int_0^{V_{DS}} n(x)dV(x), \tag{7}$$

where L is the channel length and W is the GNR width. Carrier drift velocity and mobility saturation is considered depending on the carrier concentration based on the work of Dorgan et al., 2010:

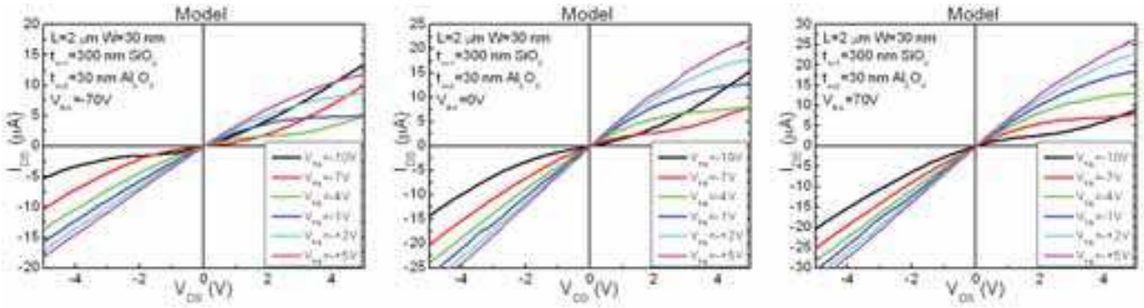
$$v_{sat} = \frac{\omega_{op}}{\sqrt{\pi n(x)}}, \tag{8}$$

where ω_{op} is the optical phonon wavelength of the dominant scattering phonons, which are surface optical phonons of the high-κ oxide. And

$$\mu = \frac{\mu_0}{\sqrt{1 + \left(\mu_0 V_{DS} / L v_{sat}\right)^2}}. \tag{9}$$

For simplicity, we assumed equal mobility and saturation velocity to describe both the electrons and holes. The solution not only provides the I-V characteristics of the device but detailed information about the carrier concentration under various bias conditions. Figs. 20 & 21 show the experimental and modelling data, displaying close agreement. As input parameters in the model we used mobility of 300 cm^2/Vs, a minimum carrier density of $5 \cdot 10^{11}$ cm^{-2} and source-drain series resistance of 0.5 Ω.mm. The saturation of current at high positive bias is caused by depletion of the carriers even in those cases when the gate biases set a high initial carrier concentration. At high negative drain bias on the other hand lack of saturation is observed. This is because the drain bias in this case further increases the carrier concentration instead of depleting. Depending on the gate bias conditions the flattening of the current occurs at different applied source-drain bias. Superlinear current increase is caused by the sharp increase of carrier concentration close to the Dirac point in conjunction with the increase of the accelerating field (V_{DS}).

In conclusion, p-n junction in GNR FETs has been experimentally demonstrated. The analysis of the device operation shows that sublinear and superlinear features observed in the I-V characteristics is caused by the device electrostatics. We point out here that the gate induced barrier at the source end of the GNR FET can be no more than the bandgap. Since the bandgap is small, interband tunnelling prevents the modulation of drain current at high drain biases. Though this is detrimental for a traditional FET, this problem can be turned around and actually used in a GNR based tunnelling FET. Such FETs have been modelled and have proposed GNR based TFETs, which is where current experimental effort is headed. (Zhang et al., 2008).



(a) (b) (c)

Fig. 21. Simulated device characteristic at the same bias conditions as the device shown in Fig. 20. I_{DS} versus V_{DS} at -70 V (a), 0 V (b) and +70 V (c) back gate bias.

3.4 Tunnelling in graphene and GNR p-n junction

Tunnelling in 2D graphene attracted a lot of attention due to the new phenomenon, Klein tunnelling of the massless Dirac particle (Stander et al., 2009). From an engineering point of view, graphene/GNR could provide higher tunnelling current if used as a channel in devices, e.g. tunnelling field-effect transistor. The current-voltage characteristics of GNR have been studied in (Low et al., 2009). The tunnelling probability in GNRs or in carbon nanotube (CNT) was found to be similar in magnitude with conventional parabolic semiconductors. However, two facts tilt the tunnelling currents decisively in favour of CNTs and GNRs. First is that the transverse kinetic energy of carriers can be large and leads to an exponential decrease in carrier tunnelling probability in bulk 3D p-n junctions, which is avoided in 1D structures. Second, if normal parabolic-bandgap semiconductors are shrunk to length scales comparable to those of CNTs and GNRs, their bandgaps and effective masses increase further due to quantum confinement. In 2D graphene, p-n junction has been realized in FETs with back and top gates. The conductance across such p-n junction has been studied both theoretically (Low et al., 2009) and experimentally (Huard et al., 2007). Here, we present the full I-V characteristics of p-n junction in 2D graphene. The tunnelling probability in 2D graphene is calculated by WKB approximation (Cheianov & Falko, 2006). At low temperature (T~ 0 K), the tunnelling current density in a biased p-n junction is calculated as

$$J_t = -\frac{e^2 V_a}{\pi^2 \hbar} \sqrt{\frac{E_{fn} + E_{fp} - q V_a}{\hbar \upsilon_F \lambda_{pn}}}, \tag{10}$$

where e is the electron charge, V_a is the applied voltage, E_{fn}/E_{fp} is the doping level at n/p region, λ_{pn} is the screening length of p-n junction (Low et al., 2009). Fig. 22 shows the full I-V characteristics of both abrupt and gradual p-n junctions. The screening length of gradual p-n junction is assumed to be λ_{pn} = 80 nm, which is achievable in real devices (Huard et al., 2007). The current includes both tunnelling and thermal emission parts. The analytical result shown in Eq. (10) gives a good estimation of the junction I-V curves. The tunnelling current is dominant at reverse bias. At high forward bias (>0.3 V) the current rises exponentially due to thermal emission. The full I-V curves show the current capability through graphene p-n junction has the magnitude around 1 A/mm, due to the zero band gap and high Fermi velocity (cm/s) in this material.

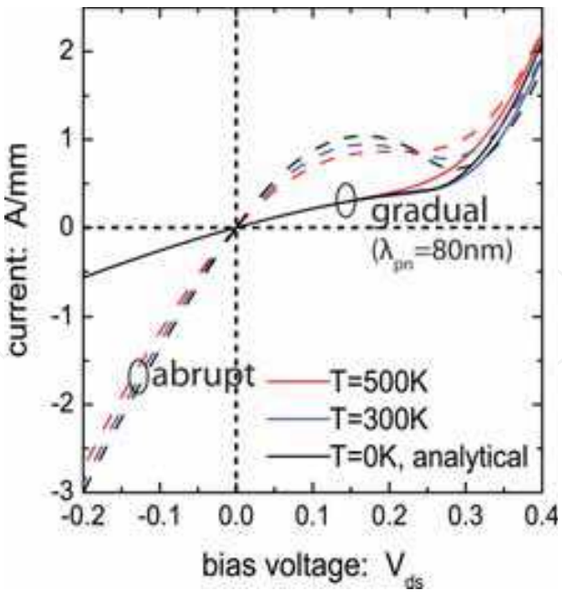


Fig. 22. I-V characteristics of graphene p-n junctions (n_1=n_2= cm^{-2}).

4. Summary

In summary, a wide variety of graphene devices and electronic device problems have been discussed. First 2D graphene transistors were made, which exhibited poor on/off ratio but promising mobility. Short channel effect has been observed, which invoked the detail exploration of the doping effect of the metal-graphene contacts. The poor saturation characteristics of the 2D graphene FETs led the attention toward the detailed study of the high field transport of graphene. The exfoliated graphene FETs were compared to CVD graphene based devices and were found to have similar performance but offering the advantage of wafer scale size. SiC based epitaxial graphene has the same size advantage along with the exceptional RF characteristics. For further improvement it became clear that band gap has to be opened by 1D confinement, which was experimentally demonstrated. The successful fabrication of p-n junction in GNR FET is a major achievement and an important step toward the realization of the GNR TFET.

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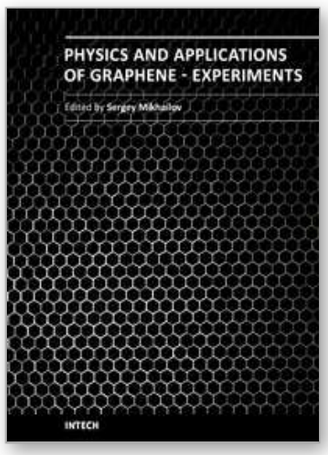

Physics and Applications of Graphene - Experiments

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The Stone Age, the Bronze Age, the Iron Age... Every global epoch in the history of the mankind is characterized by materials used in it. In 2004 a new era in material science was opened: the era of graphene or, more generally, of two-dimensional materials. Graphene is the strongest and the most stretchable known material, it has the record thermal conductivity and the very high mobility of charge carriers. It demonstrates many interesting fundamental physical effects and promises a lot of applications, among which are conductive ink, terahertz transistors, ultrafast photodetectors and bendable touch screens. In 2010 Andre Geim and Konstantin Novoselov were awarded the Nobel Prize in Physics "for groundbreaking experiments regarding the two-dimensional material graphene". The two volumes Physics and Applications of Graphene - Experiments and Physics and Applications of Graphene - Theory contain a collection of research articles reporting on different aspects of experimental and theoretical studies of this new material.

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