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Power Efficient ADCs for Biomedical Signal Acquisition

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1. Introduction

In the last years, there has been a growing interest in the design of biomedical wireless sensors (Harrison et al., 2007; Zou et al., 2009). These sensors can be used for online monitoring, detection and prevention of many diseases with a minimum disturbance to the patient and reducing the hospital expenses, so they are having a big acceptance in the medical community.

Most biomedical signals are characterized by their low voltage amplitude (in the range of mili-volts) and their low frequency ranges (few tens of kHz) (Northrop, 2001; Northrop, 2004). Also, due to the electrode used to sense them, they usually present a high DC offset that needs to be suppressed. A typical biomedical sensor interface consists on a band-pass filter, a low-noise programmable amplifier and an Analog-to-Digital Converter (ADC). The digitalization of the sensed biosignals is usually done with 8 or 12-bits of resolution (depending on the kind of signal) and with sampling frequencies between 1kS/ s and 100kS/ s (Scott et al., 2003; Verma and Chandrakasan, 2007; Zou et al., 2009).

Due to their isolation from any kind of external supply source, one of the most important design constraints of these wireless sensors is the minimization of their power consumption. Because of that, most of the works about biomedical sensor designs have been focused on low-power and low-voltage techniques and architectures.

For the design of the ADCs, many authors choose the SAR architecture with capacitive-based DACs due to their suitability for low-power and low-voltage needed requirements (Agnes et al., 2008; Hong and Lee, 2007; Saurbrey et al., 2003; Scott et al., 2003; Verma and Chandrakasan, 2007; Zou et al., 2009).

However, this architecture present some problems when the needed resolution growths. They become more area consumer, present high sensitivity to parasitic capacitances and demand more power from the supply source.

In this chapter we will present two different architectures, the most-known SAR and a new one based on a Switched Capacitor (SC) implementation of a Binary Search Algorithm, which solves many of the limitations of the SARs and present higher reconfigurability, a very important fact in these kinds of applications. The chapter will focus on the most relevant design constraints and the study of the effect of the different non-idealities, in order to get an area and power optimized design.

Two real implementations will be presented at the end of the chapter to illustrate the given theory through experimental and simulation results.

2. Low-power ADC architectures

2.1 Successive approximation architecture

The successive approximation algorithm performs the A/ D conversion over multiple clock periods by exploiting the knowledge of previously determined bits to determine the next significant bit. The method aims to reduce the circuit complexity and power consumption using a low conversion rate by allowing one clock period per bit (plus one for the input sampling).

Fig. 1a shows the typical block diagram of an *n*-bit SA ADC. It consists of a Sample-and-Hold (S&H) circuit followed by a feedback loop composed by a comparator, a Successive Approximation Register (SAR) logic block, and an *n*-bit DAC. Circuit operation is controlled by a clock signal with frequency f_{clk}. The SAR block captures the data from the comparator at each clock cycle and assembles the words driving the DAC bit by bit, from the most- to the least-significant bit, using a binary search algorithm, as Fig. 1b illustrates (Maloberti, 2007). After *n* cycles, the digital counterpart, d_{out}, of the analog sampled voltage, v_{sh}, is obtained. Besides, the S&H clock uses m clock periods for the sampling of the input signal, v_{in}. Therefore, a total of *n+m* clock intervals are required for completing an *n-bit* conversion.

At the start of the next conversion, while the S&H is sampling the next input, the SAR provides the n-bit output and resets the registers.

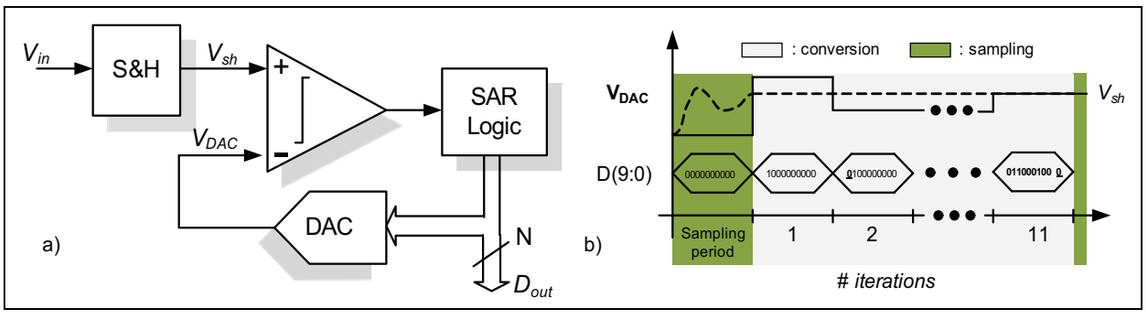

Fig. 1. a) SAR ADC architecture, b) Timing diagram

Among the very different existing architectures to perform the Analog-to-Digital Conversion, the Successive Approximation one have been chosen by many authors as the most efficient in terms of power consumption to digitalize biomedical signals. As it has been explained above, a minimum number of analog blocks and a very simple digital logic are needed to perform the complete conversion. Therefore, the overall power consumption presented by these solutions is very low.

2.2 Capacitive-based DAC

One of the most critical blocks of these solutions in terms of power consumption reduction is the Digital-to-Analog Converter. To implement it, many authors choose a capacitive-based solution (Agnes et al., 2008; Hong and Lee, 2007; Saurbrey et al., 2003; Scott et al., 2003; Verma and Chandrakasan, 2007; Zou et al., 2009) due to their low power consumption characteristics and because they can also be used as a passive S&H. As they are based on the charge

redistribution principle, they only consume power at the beginning of the conversion, when the matrix is loaded. Therefore, they are really suitable for the biomedical devices.
One of the main problems of these capacitive DACs is that their performance is in many cases strongly affected by the parasitic capacitances (Cong, 2001; Rodriguez-Perez et al., 2010). We will present an exhaustive study about the effect of the parasitic capacitances on the performance of the capacitive-based DACs.
Depending on their structure, the capacitive-based DACs can be divided in different sub-types.

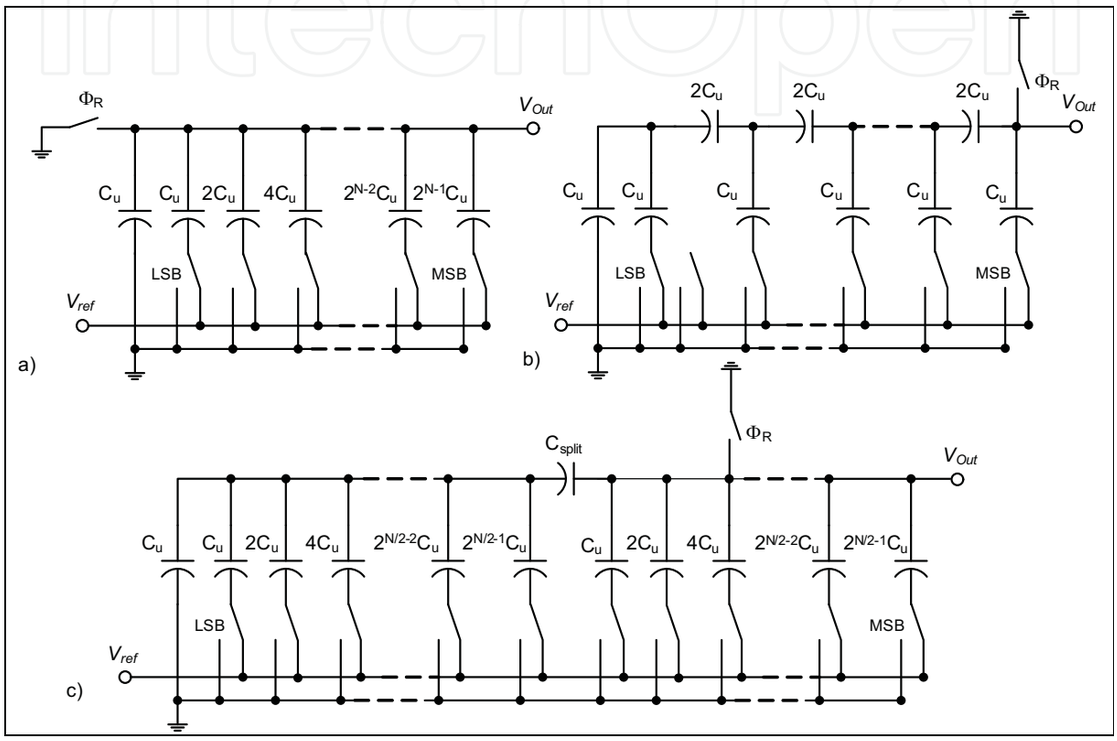

Fig. 2. Capacitive DACs architectures: a) Binary Weighted Array (BWA), b) C-2C, c) Binary Weighted Array with an attenuation Capacitor (BWAC)

Binary Weighted Arrays (BWA)

This structure is used by many authors in their works. It consists on a binary scaled array of capacitors, as Fig. 2a shows. The top of the capacitors are shorted and constitute the analog output of the DAC, while the bottoms are connected to different switches controlled by the digital input bits. The MSB is connected to the biggest capacitor while the LSB is connected to the smallest one. Then, the voltage output of the DAC will be given by:

$$V_{out} = \frac{\sum_{i=0}^{N-1} D_i \cdot 2^i}{2^N} \tag{1}$$

where N is the resolution of the DAC and D_i is the i-th input bit.
The power of these capacitive DACs is essentially due to the switching activity of the capacitive matrix, which will be given by:

$$P_{ADC} = \frac{1}{2} f_S 2^N C_u V_{DAC}^2 , \quad (2)$$

where f_s is the sampling frequency, N the resolution and C_u the unitary capacitance.
The area occupied by the DAC will be proportional to $2^N \cdot A_{cu}$, where A_{cu} is the area occupied by an unitary capacitance.
Considering that the equivalent parasitic capacitance at the top of the capacitive matrix is given by C_p (which groups parasitic capacitances at the top of the capacitors and parasitic capacitances due to the routing), the output voltage will be given by:

$$V_{out} = \frac{C_u 2^N}{C_u 2^N + C_p} \cdot \frac{\sum_{i=0}^{N-1} D_i 2^i}{2^N} \quad (3)$$

As can be extracted from the given equation, parasitic capacitances in the BWA structure produce a gain error in the final result.
The main drawback of this solution is that its power consumption and area occupation increase binarily with the resolution. Therefore, for more than 8-bits of resolution DACs, this architecture is not recommended due to the difficulty of doing a proper matched array and the huge increase in terms of area and power consumption.

Binary Weighted Arrays with an attenuation capacitor (BWAC)

As the former architectures are not suitable for medium-high resolutions because their increase in terms of power consumption, area occupation and complexity, many authors prefer to divide the BWA into two using a capacitive divider for the less significant part of the matrix (Agnes et al., 2008). The schematic of the architecture is shown in Fig. 2c), where the value of the attenuation capacitor, C_{att}, is given by:

$$C_{att} = \frac{2^{\frac{N}{2}}}{2^{\frac{N}{2}-1}} , \quad (4)$$

where N is the resolution of the converter. Then, the output voltage of the capacitive DAC is given by:

$$V_{out} = \frac{\left(2^{\frac{N}{2}} \cdot m\right) + n}{2^N} , \quad (5)$$

where m is the number of capacitors placed on the most significant part of the matrix, while n is the number in the Least Significant one. The optimum configuration in terms of area and power consumption is when m and n are the same, that is, there is the same number of capacitors in the most significant part of the matrix as in the least one.
The switching power of these architectures is given by:

$$P_{DAC} = \frac{1}{2} f_S 2^{\frac{N}{2}+1} \cdot C_u V_{DAC}^2 , \quad (6)$$

being the area occupation of these structures proportional to $2^{\frac{N}{2}+1} \cdot A_{cu}$.

It is obvious at first glance that this architecture can reduce the number of unitary elements of the BWA solutions. This reduction helps in the optimization of the power consumption and area occupation, which is one of the main objectives in the design of devices for biomedical purposes.

However, these attenuation capacitor-based architectures present higher sensitivity towards parasitic capacitances than the BWA ones. While in the second ones parasitic capacitances only induce an offset error, in this case they cause a non linearity error, which degrades the performance and the effective resolution of the DAC.

To evaluate the effect of the parasitic capacitances in these architectures, we have to distinguish between the parasitic capacitances at the top of the most significant part of the matrix, which will be named as C_{pA} and those at the least significant one, C_{pB}. Considering that the two parts of the matrix are equal and that the attenuation capacitor is almost an unitary one, the output voltage of the DAC will be given by:

$$V_{out} = \frac{V_{ref} \cdot \sum_{i=\frac{N}{2}}^{N-1} D_i \, 2^{i-\frac{N}{2}} \cdot C_u}{C_{eqMSB} + \left(C_{eqLSB} \,//\, C_{att}\right)} + \frac{V_{ref} \cdot \sum_{i=0}^{\frac{N}{2}-1} D_i \cdot 2^i \cdot C_u}{C_{eqLSB} + \left(C_{eqMSB} \,//\, C_{att}\right)} \cdot \frac{C_{att}}{C_{att} + C_{eqMSB}}, \tag{7}$$

where C_{eqMSB} is the equivalent capacitance of the MSB part the array, and C_{eqLSB} is the equivalent capacitance of the LSB part of the matrix.

$$\begin{aligned} V_{out} = & \frac{V_{ref} \cdot \sum_{i=\frac{N}{2}}^{N-1} D_i \, 2^{i-\frac{N}{2}} \cdot C_u}{\left(2^{\frac{N}{2}} - 1\right) C_u + \frac{\left(2^{\frac{N}{2}} C_u + C_{pB}\right) C_{att}}{2^{\frac{N}{2}} C_u + C_{pB} + C_{att}} + C_{pA}} + \\ & + \frac{V_{ref} \cdot \sum_{i=0}^{\frac{N}{2}-1} D_i \, 2^i \cdot C_u}{2^{\frac{N}{2}} C_u + \frac{\left(\left(2^{\frac{N}{2}} - 1\right) C_u + C_{pA}\right) C_{att}}{\left(2^{\frac{N}{2}} - 1\right) C_u + C_{pA} + C_{att}} + C_{pB}} \cdot \frac{C_{att}}{C_{att} + \left(2^{\frac{N}{2}} - 1\right) C_u + C_{pA}} \end{aligned} \tag{8}$$

Fig. 3 shows the best straight line INL for different parasitic capacitances per unit capacitances ratio for a 10-bit DAC. When the parasitic per unitary capacitance ratio rises above 3%, the non-linearity introduced by the parasitic capacitances is so high that the equivalent resolution is affected.

Then, although the architecture is better in terms of area and power consumption than the BWA one, it is more affected by the parasitic capacitances and its design must be carefully studied, as will be described later.

C-2C Structures

The schematic of the C-2C structures are shown in Fig. 2b. This kind of structures is an extension of the BWAC ones, in which the matrix is divided as many times as bits to be converted, using attenuation capacitors to divide the different unitary capacitances. The value of these attenuation capacitors is given by the expression (4), where N is two. Then,

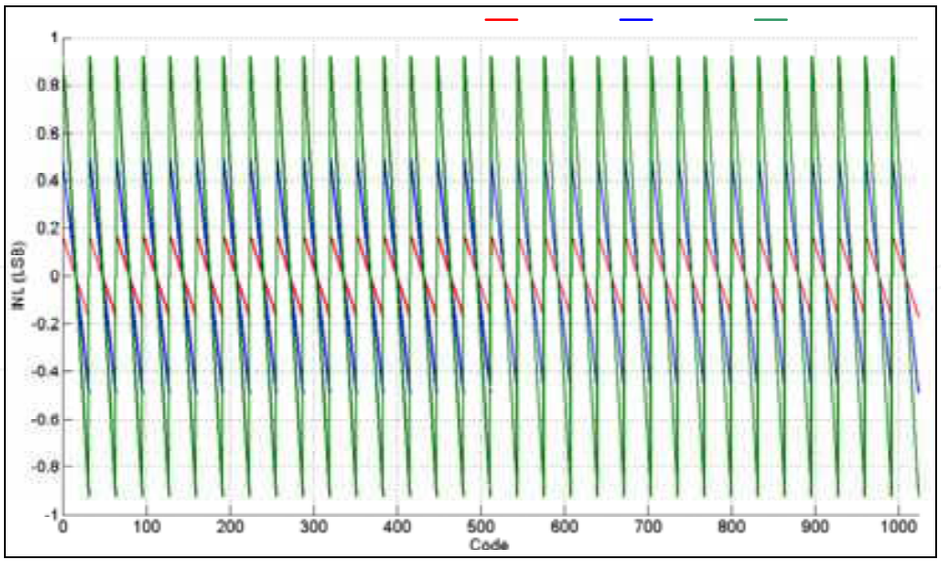

Fig. 3. INL of parasitic capacitances effect on 10-bit BWAC DAC

the value of these attenuation capacitors must be twice higher than the unitary capacitance, building the C-2C structures.

The switching power dissipated will be given by:

$$P_{DAC} = \frac{1}{2} f_S (N+1) \cdot C_u \cdot V_{DAC}^2 , \tag{9}$$

and the area occupation is proportional to $(N+1) \cdot A_{cu}$.

The area and power consumption of these architectures are drastically reduced if compared with the other solutions. However, they are rarely employed due to their extremely high sensitivity towards the parasitic capacitances, which completely degrades its performance unless they were very low, which is not feasible in standard technologies.

To study the effect of the parasitic capacitances in the C-2C structures, we have to consider the parasitic capacitances shown in Fig. 4, where $C'_{pA} = 2\left(C_{put} + C_{pub}\right)$, while $C_{pA} = 3 \cdot C_{put} + 2 \cdot C_{pub}$. As the bottom parasitic capacitances are usually bigger than those of the top, we can consider that $C'_{pA} \approx C_{pA}$ for simplicity.

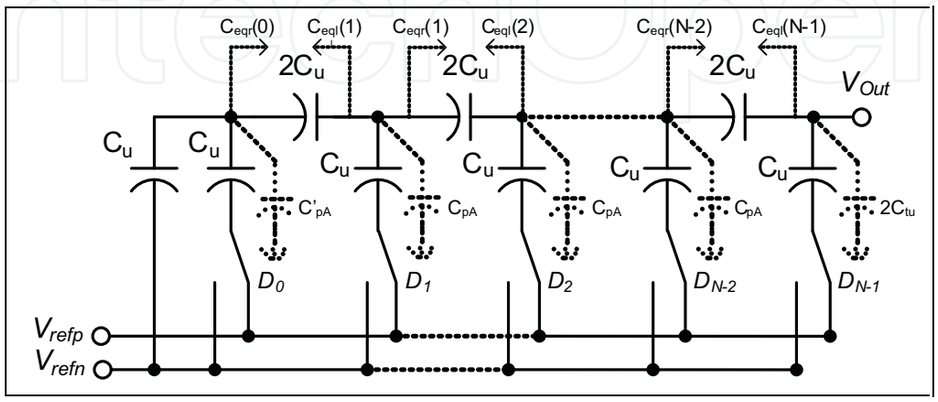

Fig. 4. Parasitic capacitances on C-2C structure

The output of the DAC can be calculated as:

$$V_{out} = \sum_{i=0}^{N-1} D_i \cdot V_{DAC}(i) \,, \tag{10}$$

where D_i will be the i-th digital input bit (with a digital value of '1' or '0'), and $V_{DAC}(i)$ is the equivalent voltage at the output of the DAC if only the bit i-th is activated. These voltages will be given by:

$$V_{DAC}(i) = \begin{cases} \dfrac{V_{ref} \cdot C_u}{\alpha + C_{eql}(i) + C_{eqr}(i)} \cdot \dfrac{2C_u}{2C_u + \beta} \prod_{n=i+1}^{N-2} \dfrac{2C_u}{2C_u + \alpha + C_{eqr}(n)} & 0 < i < N-1 \\ \dfrac{V_{ref} \cdot C_u}{\alpha + C_u + C_{eqr}(0)} \dfrac{2C_u}{2C_u + \beta} \prod_{n=1}^{N-2} \dfrac{2C_u}{2C_u + \alpha + C_{eqr}(n)} & i = 0 \\ \dfrac{V_{ref} \cdot C_u}{\beta + C_{eql}(N-1)} & i = N-1 \end{cases} \tag{11}$$

where $\alpha = C_u + 3C_{put} + 2C_{pub}$ and $\beta = C_u + 2C_{put}$. $C_{eqr}(i)$ and $C_{eql}(i)$ are the equivalent capacitance at the right and left of the i-th bit, respectively. To calculate these equivalent capacitances, the following expression can be employed:

$$C_{eqr}(i) = \begin{cases} \dfrac{2C_u \cdot \left[C_{eqr}(i+1) + \alpha \right]}{C_{eqr}(i+1) + 2C_u + \alpha} & 0 \le i < N-2 \\ \dfrac{2C_u \cdot \beta}{2C_u + \beta} & i = N-2 \end{cases} \tag{12}$$

$$C_{eql}(i) = \begin{cases} \dfrac{2C_u \cdot \left[C_{eqr}(i+1) + \alpha \right]}{C_{eqr}(i+1) + 2C_u + \alpha} & 0 \le i < N-1 \\ \dfrac{2C_u \cdot \left(\alpha + C_u \right)}{3C_u + \alpha} & i = N-2 \end{cases} \tag{13}$$

These expressions allow us to build the INL figure shown in Fig. 5, where it is clear that the parasitic capacitances induce a complete degradation in the linearity and, consequently, the performance of the DAC, even if they are small.

Although there are some solutions which try to solve the parasitic capacitance sensitivity of these ladders (Cong, 2001), they are not really implementable as they are based on non-integer scaling of the reference voltages. Also, there are some solutions which implement these structures in Silicon-Over-Insulator (SOI) technologies, where substrate parasitic capacitances are dramatically reduced due to the bulk isolation.

As a consequence, these solutions are rarely employed in real implementations.

2.3 Binary search algorithm

Although the SAR ADC architectures based on capacitive DAC matrix are widely used on biomedical sensor interfaces, they present some drawbacks which usually difficult their design:

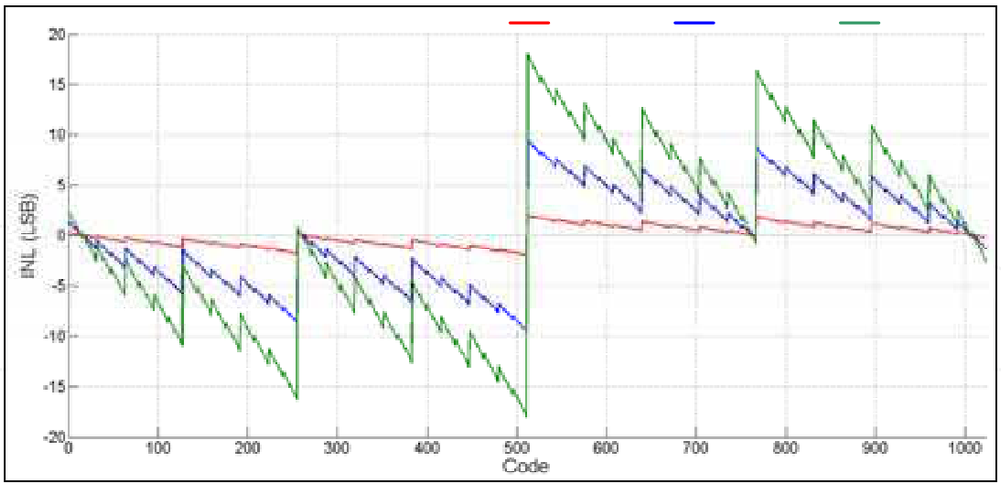

Fig. 5. INL of parasitic capacitances effect on 10-bit C-2C DAC

- **Large area occupation.** Capacitive-based DACs, and especially in the case of the BWA structures, usually require a huge area to be implemented (even more if the resolution is high), because they need many unitary capacitors. This high number of elements also complicates the routing and their proper matching.
- **Large switching power consumption.** Although one of the benefits of the capacitive DACs is that they are based on the charge redistribution principle and they don't have static power consumption is zero, the peaks of current from the supply voltage can be large, which can complicate the correct working of the circuit as they are usually supplied by unstable sources.
- **High equivalent input capacitance.** Due to the fact that the capacitive matrix is usually employed as a passive Sample & Hold in order to save power consumption, the input signal has to be load in the capacitive matrix at the beginning of the conversion. As this input signal has to be amplified and filtered by a previous active block, this latter has to load a very high capacitance, which means an increase in the power consumption.
- **High sensitivity towards parasitic capacitances.** As it has been previously studied, parasitic capacitances can affect the performance of the capacitive-based DACs, so their proper design can be complicated.

Due to the listed problems related to the design of the capacitive DACs for the SAR ADC architectures, we introduce another architecture implemented using Swithed-Capacitor Circuits (SC) and based on the Binary Search Algorithm.

The Binary Search Algorithm, which Flow Diagram is shown in Fig. 6a, is really the basis of the Successive Approximation conversion principle. It begins with the sampled of the input signal, which is compared with a certain threshold value. The result of this first comparison will set the Most Significant Bit (MSB), and we will add or subtract (depending on the result of the comparison) to the input value a certain reference voltage V_{ref}. Then we will perform again a new comparison, which will set the next bit, and after that we will add or subtract the reference voltage divided by two. This iteration is successively repeated as many times as bits to be converted, dividing by two the residual reference voltage each time. Then, after n iterations, the residual value of the reference voltage that we add or subtract will be $V_{ref} / 2^n$.

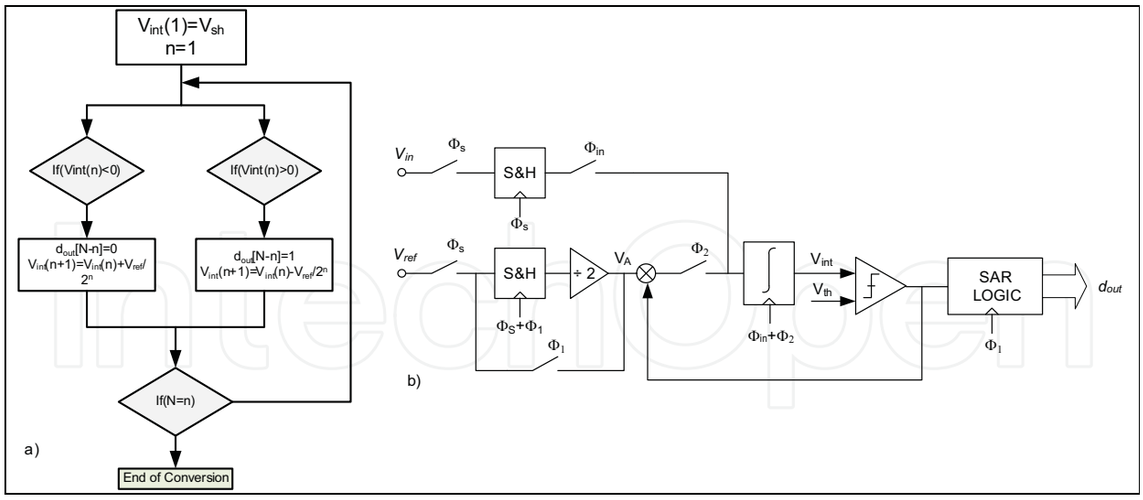

Fig. 6. Binary Search Algorith: a) Flow Diagram, b) Block Diagram schematic

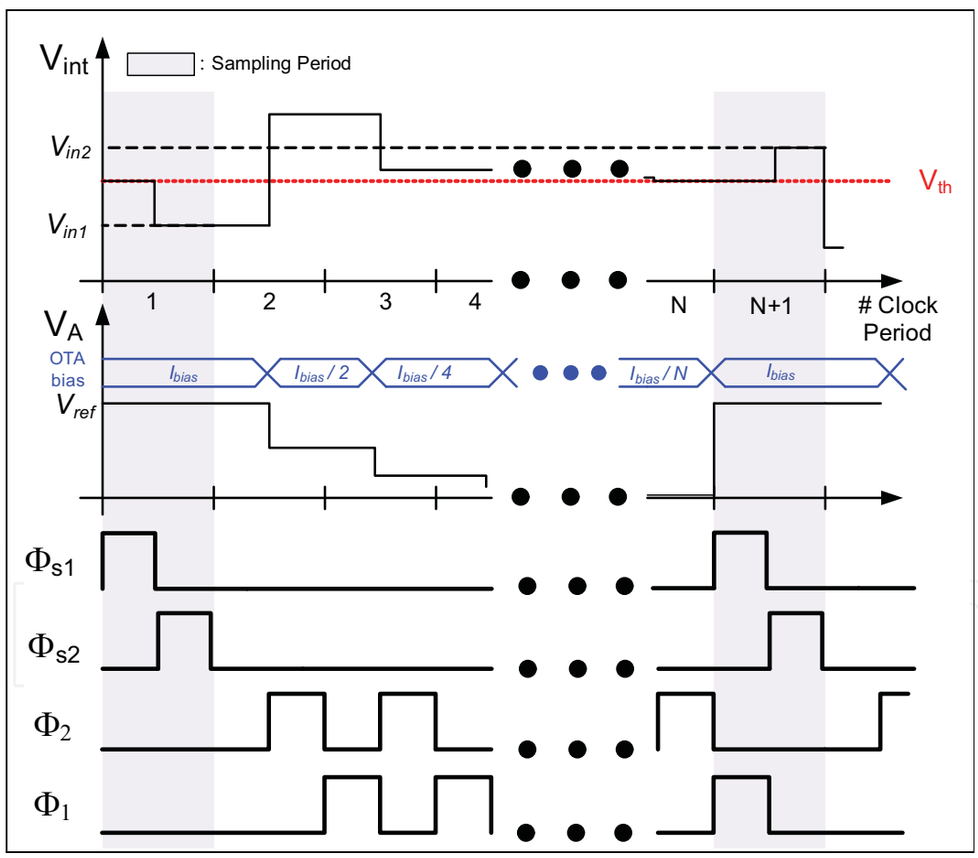

Fig. 7. Waveform of the Binary Search Algorithm implementation

Based on this algorithm, the block diagram of the proposed solution is presented in Fig. 6b. It consists on a Sample&Hold, an integrator, a divider-by-two and some logic to implement the Binary Search Algorithm. The evolution of the signals during a conversion for a certain input V_{in} is shown in Fig. 7.

2.4 Reconfigurable ADC based on SC techniques

Based on the block diagram of Fig. 6b, a Switched-Capacitor solution to implement the desired ADC in presented in Fig. 8a. The proposed solution only uses one operational amplifier in order to minimize as much as possible the power consumption (Rodriguez-Perez el al., 2009).

Fully-Differential operation reduces charge injection errors, makes easier the sum and subtraction operations and allows rail-to-rail input swing. The scheme is reconfigurable in terms of input gain (through programmable input capacitances C_{var}), resolution (controlling the number of performed iterations) and sampling frequency (through the frequency of the input clock).

The current bias of the operational amplifier is also programmed depending on the chosen configuration for the ADC in order to optimize the overall power consumed. Once a configuration has been selected, this current is also dynamically controlled during the conversion operation in order to adapt it to the residual reference voltage, which is smaller each time. Fig. 7 illustrates how the bias current is successively adapted along the conversion.

The schematic of the S&H operation is shown in Fig. 8c. This operation is performed during the first three cycles of the conversion. During the first one, the fully-differential input signal is stored on the programmable capacitor C_{var}. The next two cycles are used to transfer the stored charge on the integrator. This configuration is insensitive to parasitic capacitances (Johns and Martin, 1997).

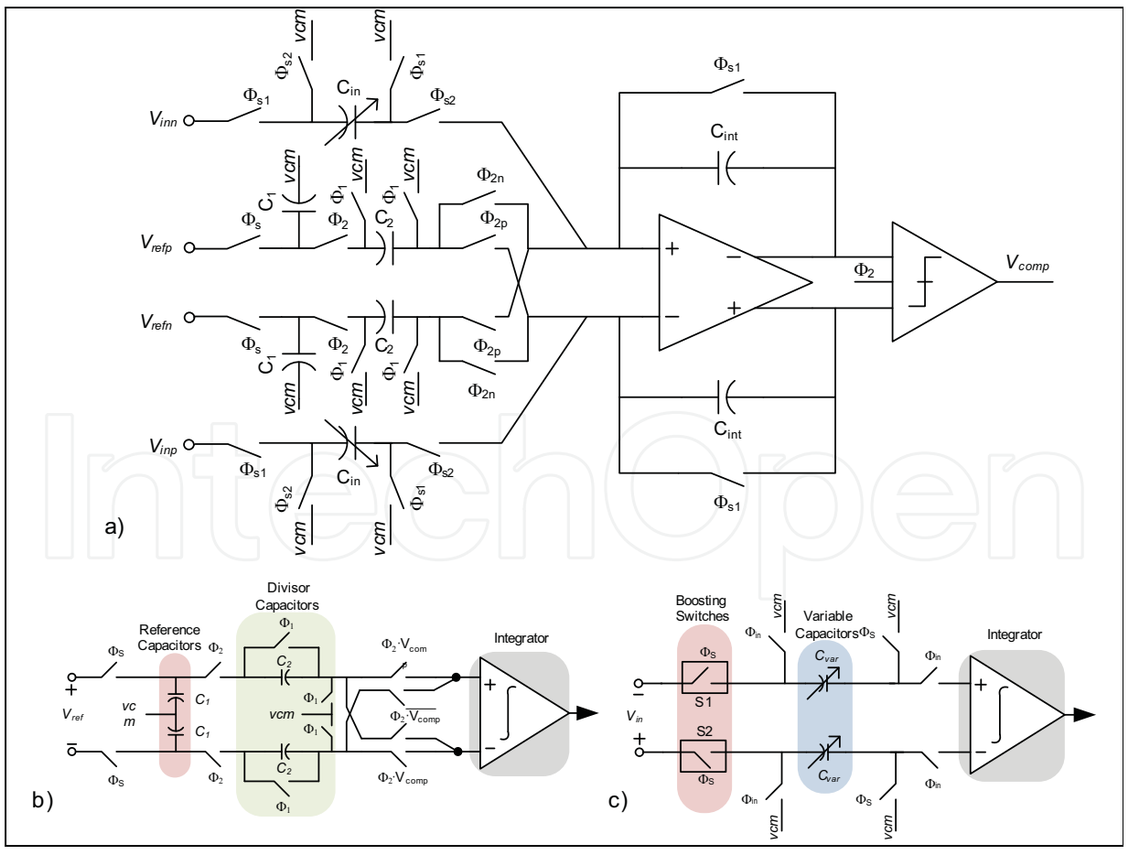

Fig. 8. Reconfigurable SC-based ADC: a) Schematic, b) Division-by-two, c) Programmable Gain Amplifier S&H

As the value of the capacitor C_{var} is reconfigurable, this architecture can be used as a Programmable Gain Amplifier, which is very useful for the biomedical interfaces as the amplitude of the input signal can vary along time.

The reference voltage division is made capacitively as Fig. 8b shows. During the first periods, the reference voltage is stored on the capacitor C_1. After that, during phase Φ_2, half of the charge is transferred to capacitor C_2 and it is either summed or subtracted to the integrated value depending on the value of the signal V_{comp}. During the phase Φ_1, capacitor C_2 is reset.

The schematic of the fully differential operational amplifier is shown in Fig. 9a. It follows a folded-cascode architecture where the transistors M2 and M3 of the input differential pair are biased in weak inversion in order to get the best g_m / I_D ratio (Enz et al., 1995). Transistors M1, M4, M5, M10 and M11, which are current mirrors, are biased in the saturation region of strong inversion in order to improve their mismatch. The width of these transistors can be programmed in order to get the dynamic bias control.

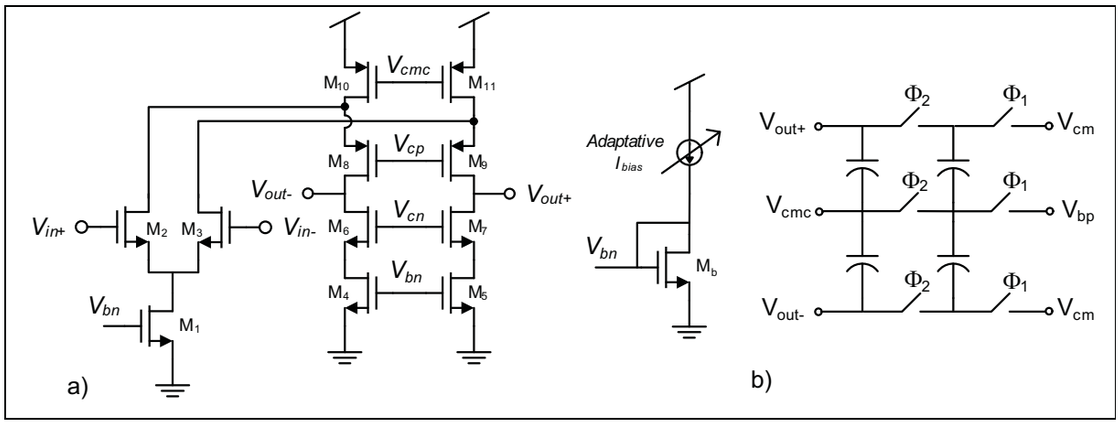

Fig. 9. a) Schematic of the folded-cascode opamp, b) SC common-mode feedback

The schematic of the capacitive common-mode control circuit in presented in Fig. 9b. This circuit controls the common-mode voltage through the control of the gate voltage of transistors M10 and M11 (Gray et al., 2001). The use of a capacitive-based configuration allows the minimization of the power consumption.

3. Basic building blocks design

3.1 Comparator

The comparator is a key block in any of the presented ADCs and one of the biggest power consumers, so its design must be carefully done in order to optimize the power consumption without a degradation in the performance of the ADC.

Many published SAR ADCs use a simple current-controlled dynamic latch as a comparator (Scott et al., 2003, Zou et al., 2009). Although these solutions are very attractive because of their low power consumption, they can present a DC offset of around 10mV due to the mismatch of their input differential pair, which imply an offset error in the performance of the ADC too. Considering that the circuit operates from rail-to-rail, this error means a loss in the input range of the converter.

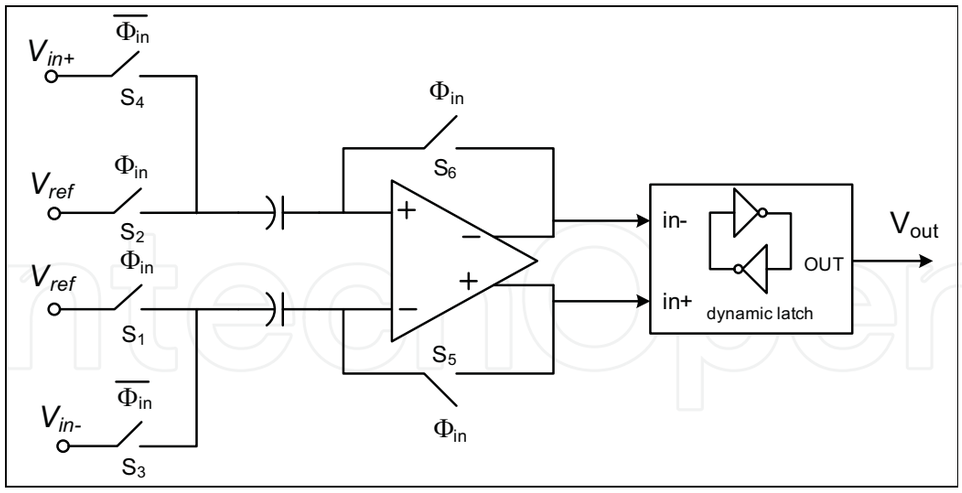

Fig. 10. Schematic of the comparator with an autozeroed pre-amplifier

Fig. 10 shows the schematic of the proposed comparator, which solves the offset problem. The comparator consists on a fully differential pre-amplifier stage with a cancellation offset scheme followed by a current-controlled dynamic-latch that boosts the pre-amplified difference to the rails. The auto-zeroing is achieved by closing a unity gain loop around it and storing the offset voltage on the input capacitors (Rodriguez-Perez et al., 2009). The gain of the pre-amplifier should be high enough in order to save the input voltage offset of the dynamic-latch.

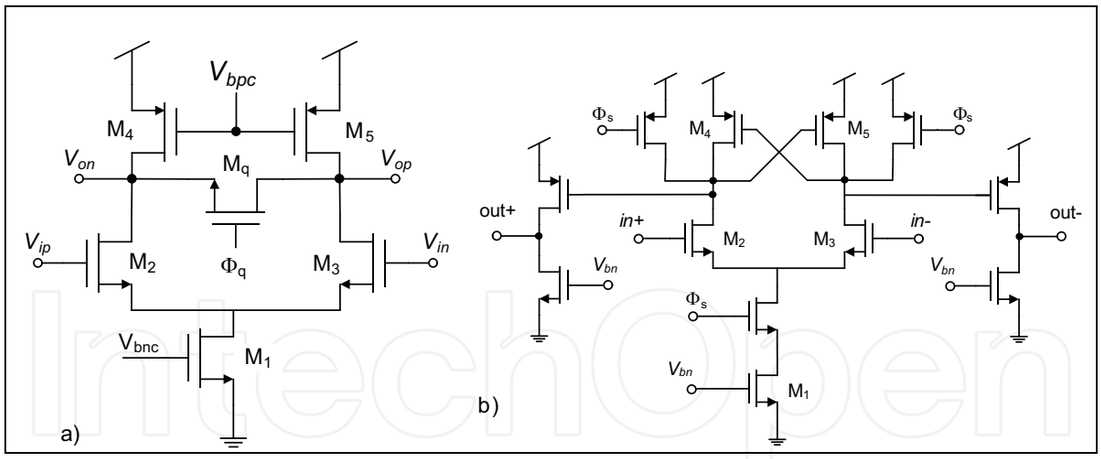

Fig. 11. a) Schematic of the pre-amplifier, b) Schematic of the dynamic-latch

The schematic of the pre-amplifier is shown in Fig. 11a. It is a single differential pair with a SC-based common-mode control circuit. In order to maximize the transconductance of the input differential pair and their matching, transistors M2 and M3 work in weak inversion. The rest of the transistors, which work as current mirrors, are in the saturation region to improve their matching.

The schematic of the dynamic-latch is presented in Fig. 11b. It is formed by an input differential pair which imbalances a pair of cross-coupled inverters, creating a positive feedback that boost the outputs to the rails. Current-controlled digital buffers are connected

at the outputs before an RS latch that gives the digital single-ended output of the comparator.

In order to optimize the power consumption of the comparator, the minimum required bias current for the pre-amplifier has to be evaluated. The design of the pre-amplifier will depend on the minimum input voltage needed at the input of the dynamic latch to counteract the offset voltage. It means that the dynamic gain of the pre-amplifier must be:

$$A_{pre} > \frac{V_{off_{latch}}}{\frac{LSB}{2}} = 2^{N+1} \cdot V_{off_{latch}}, \tag{14}$$

where $V_{off_{latch}}$ is the offset voltage of the dynamic latch and N is the required resolution. Considering that the dynamic gain of the pre-amplifier for a period T_S is approximated by:

$$A_{pre} = g_m \cdot \frac{T_S}{C_p} \tag{15}$$

where C_p represents the parasitic capacitance at the output of the pre-amplifier, and g_m the transconductance of the input transistors.

Following the *EKV* model (Enz et al., 1995), the g_m / I_D expression for MOS transistors valid for all regions is given by:

$$\frac{g_m}{I_D} = \frac{1}{n \cdot U_T} \cdot \frac{2}{1 + \sqrt{1 + 4 \cdot IC}}, \tag{16}$$

where n is the slope factor, U_T is the thermal voltage and IC is the inversion coefficient, given by:

$$IC = \frac{I_D}{2n\mu C'_{ox} \left(\frac{W}{L}\right) U_T}. \tag{17}$$

Depending on the value of this coefficient, the transistor will work in weak inversion ($IC < 0.1$), moderate inversion ($0.1 < IC < 10$), or strong inversion ($IC > 10$). To obtain the optimum g_m / I_D ratio, we will dimension the transistors to work in weak inversion.

Then, considering equations (14)-(16) we have that:

$$I_D > \frac{2^{N+1} \cdot V_{offset} \cdot nU_T \left(1 + \sqrt{1 + 4 \cdot IC}\right)}{2T_S} \tag{18}$$

For a standard technology, normal values are n=7, U_T=27mV, C_p=250fF and IC=0.1. Using this values and the needed sampling frequency in equation (18) gives us the minimum required bias current for the pre-amplifier.

3.2 Boosted switch

In order to get rail-to-rail input voltage swing, the input switch must be boosted in order to avoid a degradation of the signal due to the dependence of the switch resistance with the input voltage, especially when the input frequency is near to Nyquist.

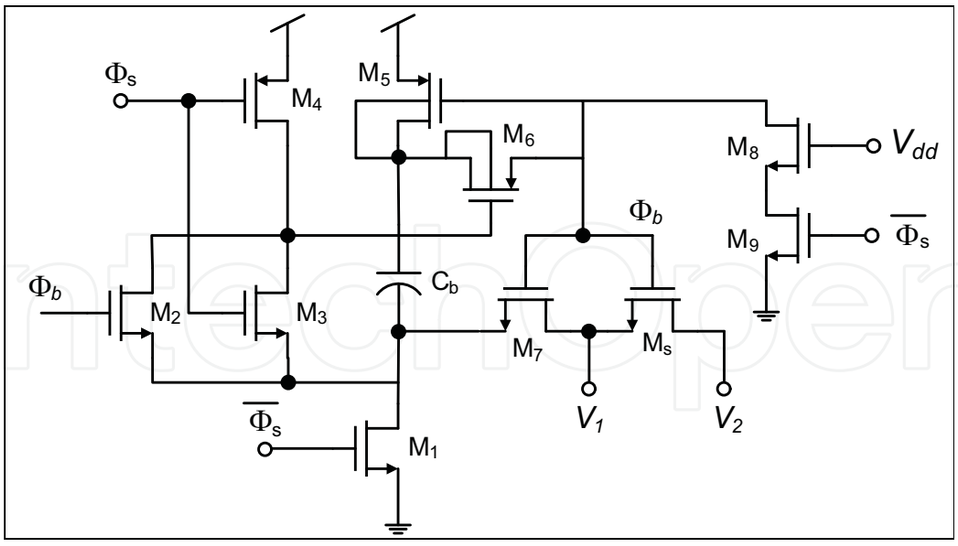

Fig. 12. Schematic of the boosting switch

The schematic of the boosted switch is shown in Fig. 12 (Dessouky and Kaiser, 1999). The circuit works as follows. When $\Phi_{sw}=0$, the supply capacitor C_b is charged to V_{DD}-V_{thp}. In the next phase, when Φ_{sw} switches on, this stored value is added to the input voltage to set the gate voltage Φ_{sw} of the input switch, M_S, which ensures a constant conductance of the input transistor during the sampling phase.

3.3 SAR logic

The Successive Approximation algorithm starts with the activation of the MSB while the others remain to zero. While the conversion is running, the rest of the bits are successively activated, while the value of the one who was activated just before will depend on the result of the comparator.

The schematic of the logic that implements the Successive Approximation operation is shown in Fig. 13a.

This architecture is based on the dependency of the state of each bit with the others bits state (Rossi and Fucili, 1996). Each bit evaluates the state of the others and in function of the result, it decides either it has to be activated, keeps its value, or take the value of the comparator.

The logic is implemented using a cascade of N+1 multiple input shift registers (Fig. 13b). Through a multiplexer and a decoder, each register (k^{th}) can choose three data inputs coming from: the output of the $(k+1)^{th}$ flip-flop, the output of the comparator or itself output. This selection will depend on itself state and the state of the following registers states.

With only 11 flips-flops to complete a 10-bits conversion, this architecture consumes nearly a forty percent less than others more popular (Anderson, 1972), which need 22 flip-flops to perform the same operation.

3.4 Current reference generator circuit

In order to generate on-chip the bias current needed for the active blocks, some current reference generator cell is needed. The non-resistance Oguey based cell shown in Fig. 14 is a good solution.

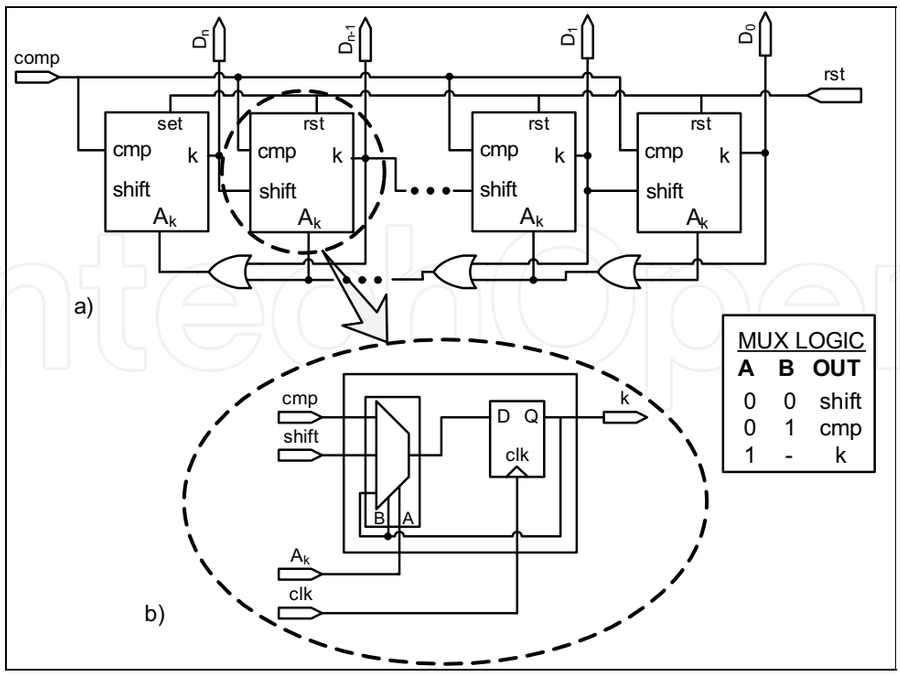

Fig. 13. Schematic of the Succesive Approximation Logic

The cell is based on the circuit presented in (Oguey and Aebischer, 1997), where the resistor has been replaced by an nMOS transistor working below saturation. The added transistors M2 and M1 provide the gate voltage for M3.
The generated current reference Iref is given by:

$$I_{ref} = n^2 \cdot \beta_{n3} \cdot V_T^2 \cdot K_{eff} \ , \quad K_{eff} = \left[K_2 - \frac{1}{2} + \sqrt{K_2 (K_2 - 1)} \right] \cdot \left(\ln (K_1) \right)^2 \tag{19}$$

where $K_1 = \frac{S_{M4} \cdot S_{M7}}{S_{M6} \cdot S_{M5}}$ and $K_2 = \frac{S_{M3} \cdot S_{M2}}{S_{M1} \cdot S_{M5}}$, being S_{Mx} the W/L ratio of the transistor M_x.

It is also important to include a start-up circuit to the current reference circuit in order to bring out the reference circuit from a zero current operation point to its normal operation point, like the presented in Fig. 14. It also provides the possibility of leaving the circuit on a standby mode (Mandal et al., 2006).

4. Simulation and experimental results

In order to validate the theoretical study done along the chapter, two different designs have been implemented and validated.

4.1 A 1-V, 10-bit, 2kS/s SAR ADC with a BWAC architecture capacitive DAC

The SAR ADC was implemented in a 0.35um CMOS standard technology with a resolution of 10-bit, 2kS/ s of sampling frequency and 1-V of voltage supply. It uses a BWAC architecture for the implementation of the capacitive-based DAC.
The layout of the ADC can be seen in Fig. 15.

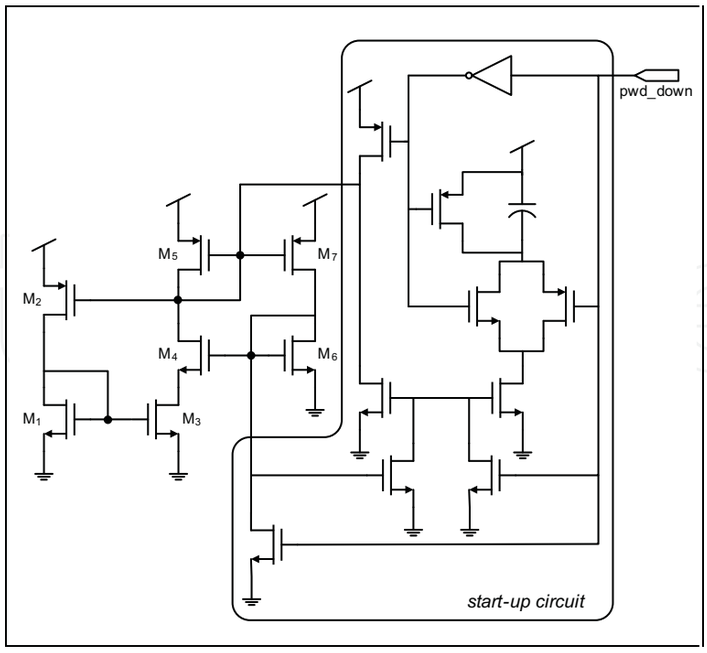

Fig. 14. Schematic of the current reference and start-up circuit

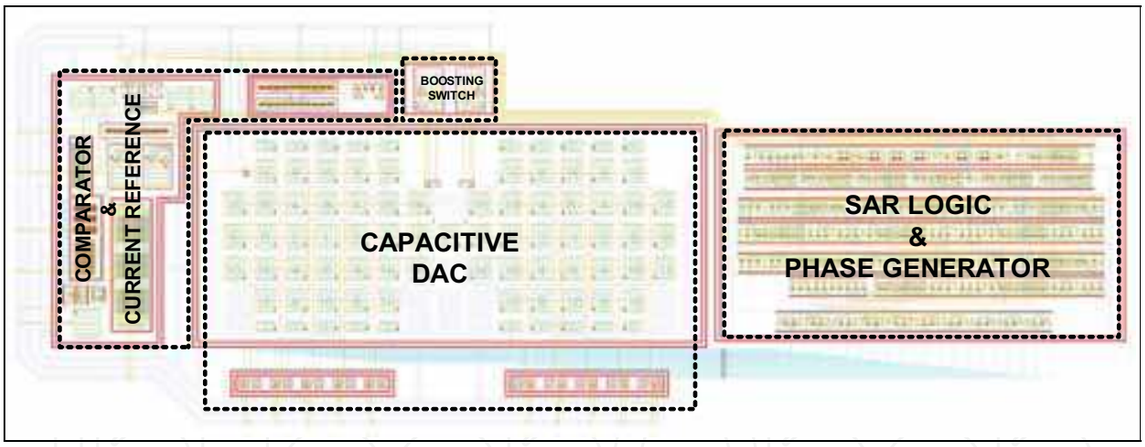

Fig. 15. Layout of the SAR ADC with capacitive DAC

Table 1 summarises the measured results of the integrated SAR ADC for the nominal conditions. The Equivalent Number of Bits (ENOB) is defined as:

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{20}$$

Fig. 16 shows the 8192-samples FFT of the ADC output response for a 140-Hz sinusoidal input signal of 1-V amplitude sampled at 2kHz at 1-V supply. The Signal to Noise Distorsion Ratio (SNDR) of 58.39dB, which gives a ENOB of 9.41-bits.

Fig. 16a compares the performance of the circuit for different input frequencies, supply voltages and sampling frequencies configurations. As can be extracted from the given graph, the ADC can work under a high range of supply voltages. This is extremely

Technology	CMOS 0.35μm
Nominal Voltage Supply	1-V
Input Voltage Range	Rail-to-Rail
Nominal Resolution	10-bits
Sampling Frequency	2kS/ s – 8kS/ s
SNDR (300Hz Input tone)	58.40dB
ENOB (300Hz Input tone)	9.4-bits
INL	< ±0.8LSB
DNL	-0.7<*DNL*<0.2 LSB
Power consumption (2kS/ s mode) Without Current Reference With Current Reference	 130nW 250nW
Area occupation	0.212mm²

Table 1. Measured Results of the SAR ADC

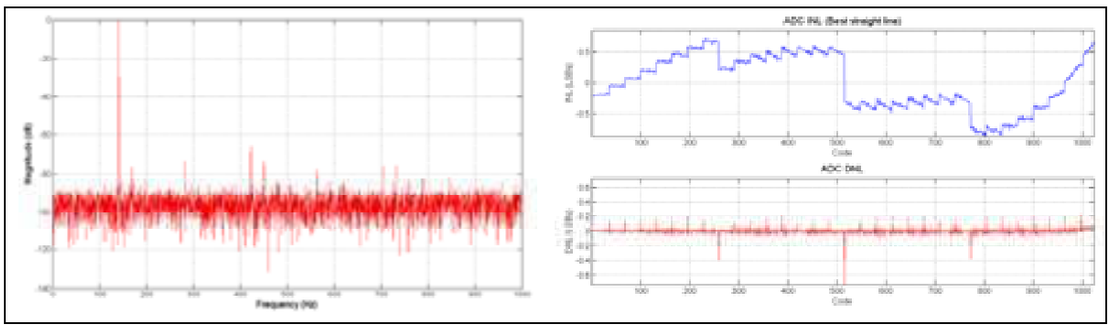

Fig. 16. a) FFT-response of the SAR ADC, b) DNL and INL response of the SAR ADC

important in biomedical wireless sensors, which voltage supply sources are weak and can present high variations. The frequency of the input signals can vary through the entire Nyquist band with a minimum loss of resolution. The ADC can be programmed to work under different sampling frequencies with a similar performance.

The integral nonlinearity (INL) and differential nonlinearity (DNL) plots are shown in Fig. 16b. The major errors in the INL and DNL curves are in the codes 256, 512 and 768, where the MSBs change. These linearity errors are due to the mismatch because of the lack of dummy capacitors. The measured INL and DNL are within $\pm 0.8LSB$ and $-0.7 < DNL < 0.2$, respectively.

The power consumption was measured using a 10fA-resolution picoamperimeter. These measures showed that the power consumption of the complete system including the current generation cell and the clock generation circuitry is 250nW for 1-V supply and 2kS/ s sampling mode, while the consumption of the ADC without the current generation cell is 130nW.

An interesting study comes from the comparison of the two different designs included in the integration, the one with dummy capacitors and the other without them. Following post-layout simulations, the parasitic capacitances introduced by the dummy capacitors

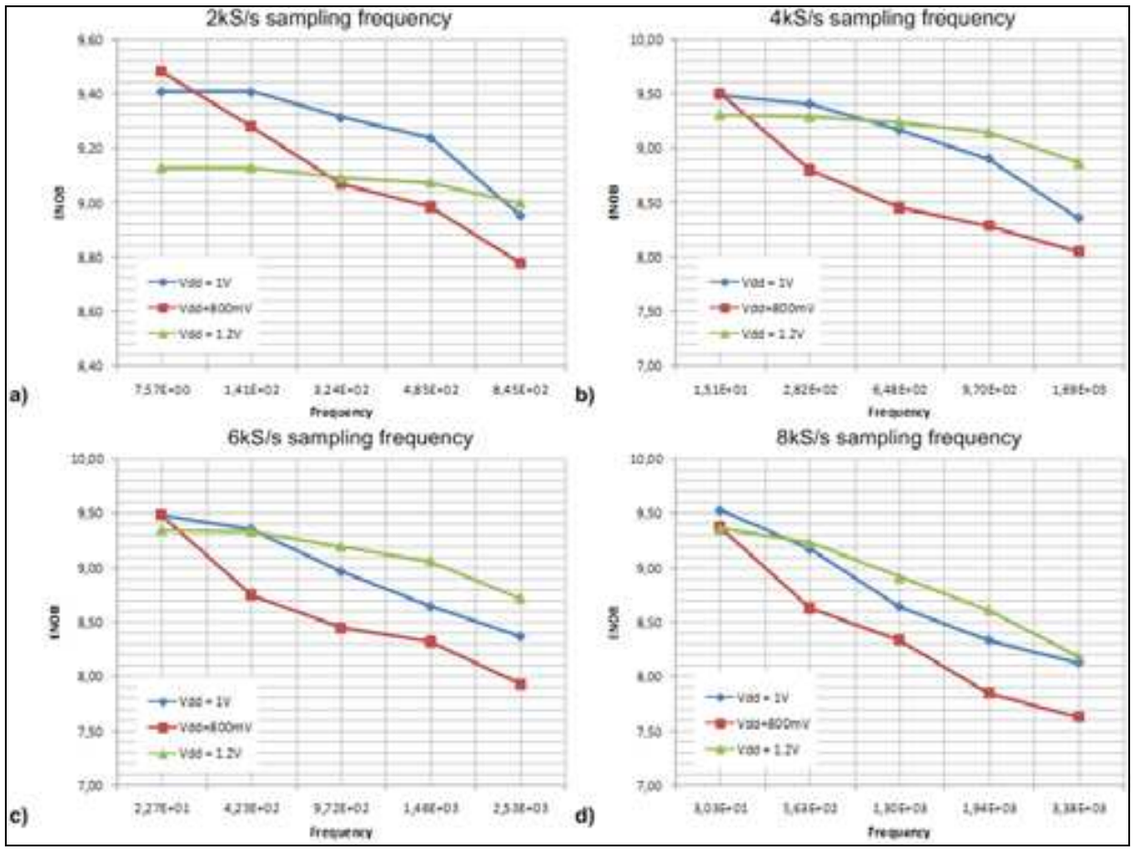

Fig. 17. Evolution of the resolution of the ADC with the input frequency for different voltage supplies under different sampling frequencies: a) 2kS/ s, b) 4kS/ s, c) 6kS/ s, d) 8kS/ s

should affect the behaviour of the ADC, degrading its resolution and linearity. This was validated in the experimental measurements, as Fig. 18 illustrate. The solution that included dummies presented higher harmonics than the other. Also, the parasitic capacitances introduced by the dummies capacitors induce higher errors in the INL and DNL than those due to the mismatch of the unitary capacitors of the capacitive array.

These linearity errors induce losses of more than 0.2-bits ENOB, as was predicted by the post-layout simulation results.

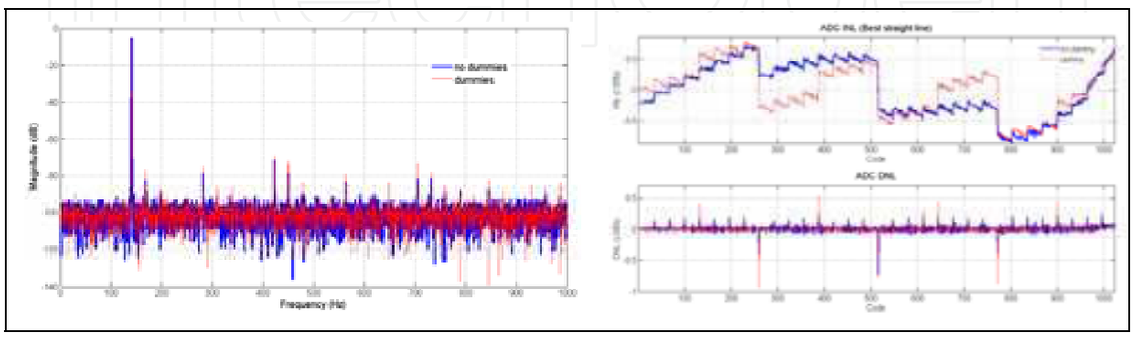

Fig. 18. Comparison of performance of the SAR ADC with and without dummies: a) FFT-response, b) INL and DNL

4.2 A 1.2-V, 10-bit reconfigurable SC-based ADC

The Reconfigurable ADC based on a Binary Search Algorithm with SC techniques was designed in a standard CMOS 130nm technology. The ADC is reconfigurable in terms of input gain (from 0.5 to 4 by means of 2-bits) and sampling frequency (from 10kS/ s to 100kS/ s). The power consumption is adapted to the chosen configuration in order to optimize it, and varies between 200nW to 2uW.

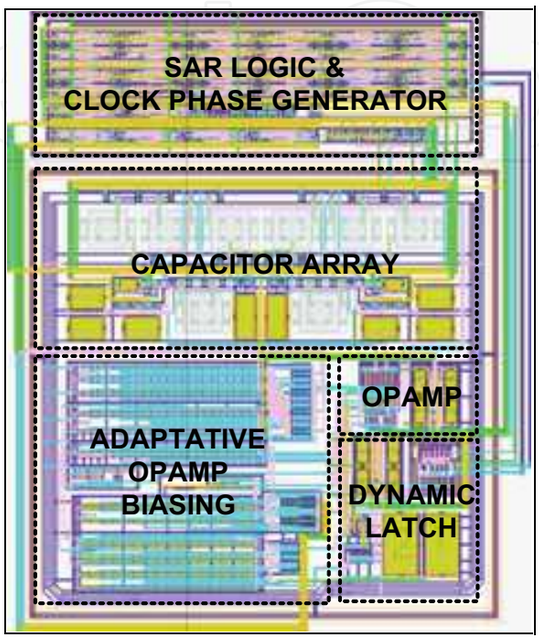

Fig. 19. Layout of the SC-based ADC

The layout of the complete ADC is presented in Fig. 19. It occupies an area of 190um x 225um.

Technology	CMOS 0.13μm
Nominal Voltage Supply	1.2-V
Input Voltage Range	Rail-to-Rail
Nominal Resolution	10-bits
Sampling Frequency	10kS/ s – 100kS/ s
SNDR	60.76dB
ENOB	9.8-bits
Power consumption 10kS/ s 100kS/ s	 200nW 2uW
Area occupation	0.043mm^2

Table 2. Performance summary of the SC-based ADC

Post-layout simulations with Process, Voltage and Temperature (PVT) variations were performed to validate the design. Table 2 summarises the main characteristics of the ADC, while Fig. 20a and Fig. 20b present the FFT-spectrum response for small and Nyquist

sinusoidal inputs frequencies sampled at 20kS/ s and 90kS/ s, respectively. Simulation results show a SNDR of 60.76dB, which gives an ENOB of 9.8-bits.

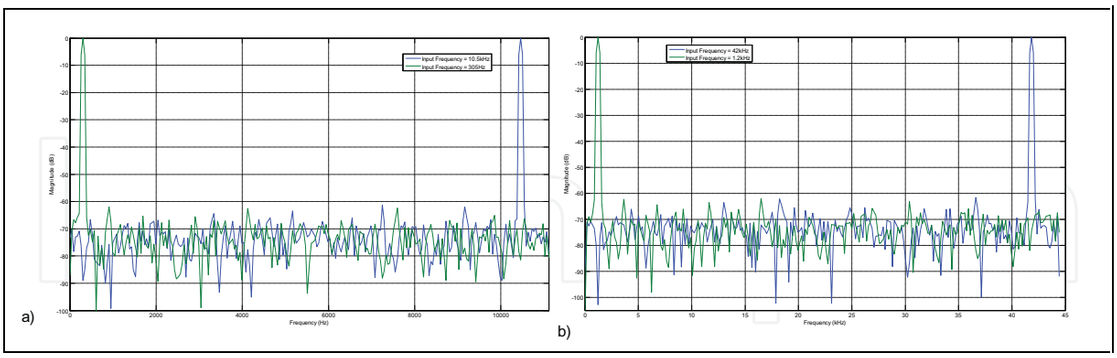

Fig. 20. FFT-response of the SC-based ADC for small and Nyquist frequency sinusoidal inputs sampled at: a) 20kS/ s, b) 90kS/ s.

5. Conclusions

This chapter have introduced the main concepts concerning to the design of ADC for biomedical interfaces, where two main architectures have been studied, concluding with the presentation and results of some real implementations.

The chapter has studied the most important design concerns of the Successive Approximation Architecture with capacitive DACs, one of the most popular ones. This architecture is very useful in a biomedical contest due to its low area and low power consumption. However, the implementation of this structures can derivate some problems related to their high sensitivity to parasitic capacitances and their high area and switching energy demand, especially when the resolution became higher than 8-bits.

The presented example includes a 10-bit SAR ADC with a capacitive-based DAC using a Binary Weighted Array with an attenuation capacitor to reduce the size of the matrix. The importance of the parasitic capacitances effect over other non-idealities was shown by means of two different implementations, one using a capacitive array with dummies an another one without them. As the first one presented more parasitic capacitances, experimental results showed that its performance was more degraded than in the case of the second one implementation without dummies, unless the mismatch of this latter was worse.

Due to some of the drawbacks of the of the SAR architecture, we have introduced in this chapter another proposal based on the Binary Search Algorithm too, but using an implementation based on SC-techniques. This architecture results highly flexible as it can be easily reconfigured in terms of resolution, sampling frequency and input gain. Also, the area occupation and switching power demand is dramatically reduced due to the elimination of the big capacitive arrays needed in the SAR capacitive DACs based architectures.

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