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# Non-Isolated High-Gain DC-DC Converter Using Charge Pump and Coupling Inductor

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## 1. Introduction

As generally acknowledged, the high-gain DC-DC converter is widely used in the sustainable energy system as the front-stage of the DC-AC converter. Therefore, it is indispensable for low voltage to be boosted to high voltage. In general, the boost converter or the buck-boost converter is widely used in such applications. However, it is not easy for such converters to achieve high voltage ratio. In theory, the voltage ratios of these two converters can reach infinity, but in actuality about three or four, limited by parasitic component effect and controller capability. Consequently, if the voltage ratio of the converter is desired to be over five, then two-stage converter based on the boost converter or the buck-boost converter is utilized, or different converter topologies [1-18] are created.

In [1-10], the Luo converter and its derivatives are presented, whose voltage lift technique is similar to that of the Cuk converter or the SEPIC converter, based on the energy transfer from one inductor via the intermediate capacitor then to the other inductor. Therefore, the transferred energy is mainly determined by the capacitance, thus causing the current stress on the capacitor to be serious. In [11][12], the voltage-boosting converter with very high voltage ratio also uses a capacitor as an energy-transferring medium, similar to the behavior of the Cuk converter or the SEPIC converter, and hence the current stress on the capacitor is also serious. In [13], the voltage-boosting converter, specified with input voltage, output voltage and rated output current being 24V, 200V and 2A, respectively, is presented. Such a converter combines the characteristics of the boost converter and the characteristics of the bootstrap scheme to achieve voltage boosting. The higher the voltage ratio is, the more the number of bootstraps and hence the more the number of diodes and capacitors. However, the surge current occurs as the energy is transferred via large capacitance, and hence the value of the capacitor can not be too large and the corresponding equivalent series resistance (ESR) is relatively large. In [14], the voltage-boosting converter has the voltage ratio of 1/(1-2D) in the continuous conduction mode (CCM), where D is the duty cycle of the main switch. And as compared with the boost converter, this converter is complicated due to four switches required. In [15], the KY converter is presented, but the maximum voltage ratio of such a converter is only two. As for [16-18], the coupled-boost converter is presented, which uses a coupling inductor as an energy-transferring medium. In [18], this converter has the voltage ratio of 1+nD/(1-D). However, in this converter, suppressing the voltage spike created due to the leakage inductance of the coupling inductor is taken into account by

adding an active voltage-clamping circuit which pumps part of the leakage inductance energy to the input. However, for the multi-phase to be considered, the more the number of phases is, the more the number of active voltage-clamping circuits.
Consequently, a new voltage-boosting converter, combining the charge pump and the coupling inductor, is presented herein, together with a passive voltage clamping circuit. There are four main merits in this converter. The first is this converter with high voltage ratio required is simpler in structure than any converter mentioned above. The second is that the primary inductor is magnetized under double the input voltage, thereby causing the input current to be reduced and hence the efficiency to be improved at light load, which is similar to the behavior of the KY converter [19]. The third is that the passive voltage-clamping circuit pumps part of the energy stored in the leakage inductance to the output. The four is that, for the multi-phase to be considered, if the number of phases is N, then only additional N-1 diodes are added. However, there is mainly one demerit in this converter. Since there is one right half-plane zero, the corresponding phase margin is reduced and hence the high-performance control of this converter is not so easy to obtain. In this paper, some mathematical derivations, and simulated and experimental results are offered to demonstrate the effectiveness of the proposed voltage-boosting converter topology.

## 2. Proposed converter configuration

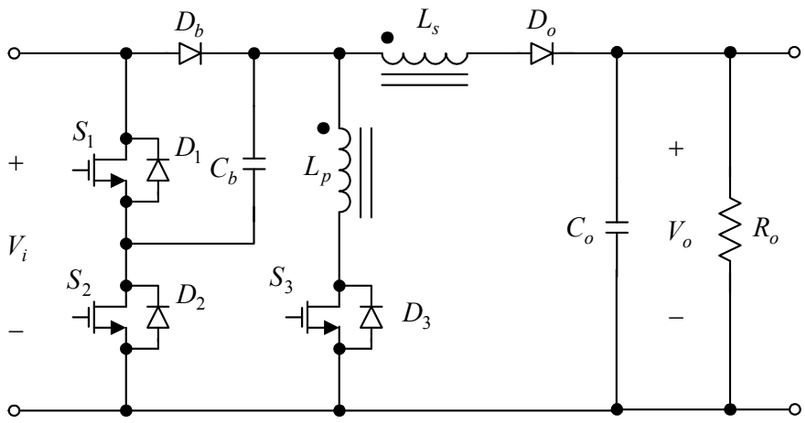


Fig. 1. Proposed voltage-boosting converter without leakage inductance considered.

Fig. 1 shows the proposed voltage-boosting converter. Such a converter contains two cells. One is the charge-pumping cell and the other is the inductance-coupling cell. The former consists of two MOSFET switches $S_1$ and $S_2$ with two body diodes $D_1$ and $D_2$ connected in parallel respectively, one diode $D_b$, and one capacitor $C_b$. The latter is comprised of one main switch $S_3$ with one body diode $D_3$ connected in parallel, and one coupling inductor made up of two inductances $L_p$ and $L_s$, which are coupled together and put at the primary and the secondary, respectively, with the turns ratio n set to $N_s/N_p$, where $N_s$ is the number of turns in the secondary winding and $N_p$ is the number of turns in the primary winding. The remainder are one output diode $D_o$, one output capacitor $C_o$, and one output resistor $R_o$. However, there is the leakage inductance existing in this coupling inductor, especially for the leakage inductance $L_{LK}$ at the primary, as shown in Fig. 2. Consequently, in Fig. 3, one passive voltage-clamping circuit, containing one inductor $L_{sn}$, one capacitor $C_{sn}$, and one diode $D_{sn}$, is added to this converter, so as to avoid the voltage spike occurring due to $L_{LK}$ and hence destroying the MOSFET switch $S_3$ eternally. Besides, if the multi-phase concept is

applied to the proposed converter, say, N-phase, then the required passive voltage-clamping circuit is the same as that for the single-phase converter except that the number of additional diodes $D_{sn}$ is N-1.

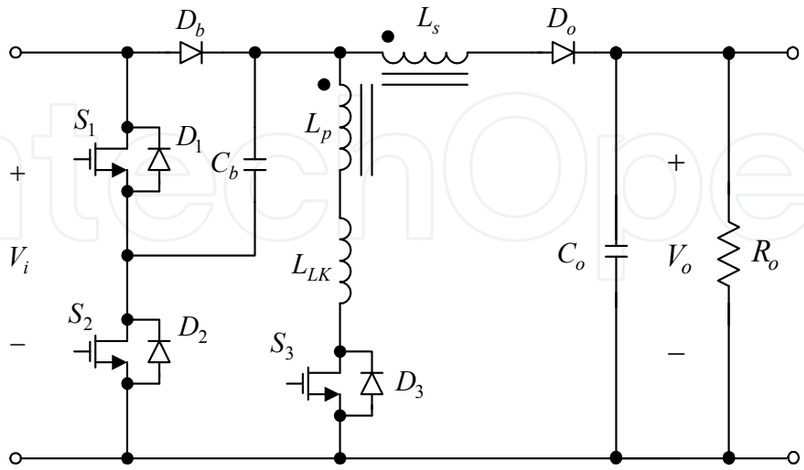


Fig. 2. Proposed voltage-boosting converter with leakage inductance considered.

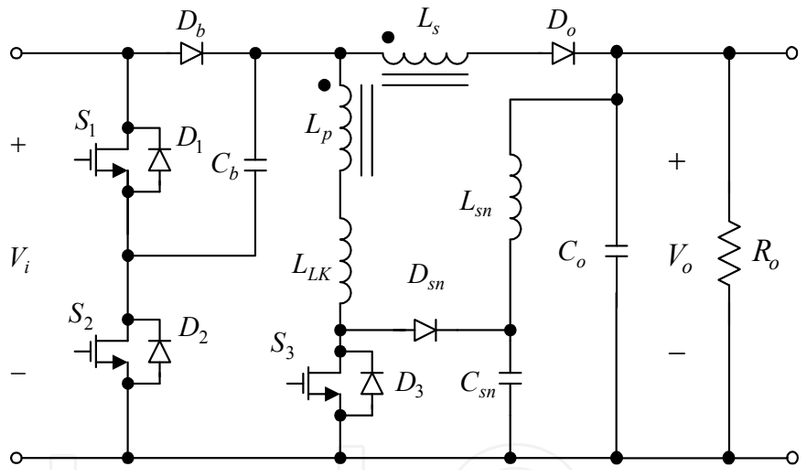


Fig. 3. Proposed voltage-boosting converter with passive voltage-clamping circuit considered.

## 3. Basic operating principles

Before this section is taken up, it is assumed that the voltage across any MOSFET or diode during the turn-on interval is negligible, there are no blanking times between $S_1$ and $S_2$, the voltage across the capacitor $C_b$ is equal to $v_i$, and the operating mode of this converter is in CCM. As shown in Fig. 4, where $T_s$ is the switching period and the gate driving signals $M_1$, $M_2$ and $M_3$ are used to drive $S_1$, $S_2$ and $S_3$ respectively, the turn-on type of three MOSFET switches is (D, 1-D, D), where D is for $S_1$ and $S_3$, 1-D is for $S_2$, and D is the duty cycle of the pulse-width-modulated (PWM) control signal for $S_1$. First of all, the basic operating principles for the proposed converter without the passive voltage-clamping circuit are described, and next the basic operating principles of the proposed passive voltage-clamping circuit are illustrated. There are two modes for the former and two modes for the latter.

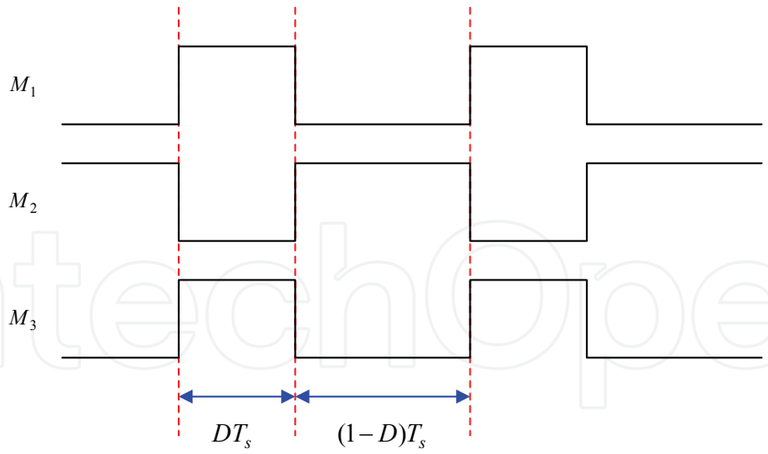


Fig. 4. Ideal timing sequence of gate driving signals $M_1$, $M_2$ and $M_3$ to drive $S_1$, $S_2$ and $S_3$ respectively, without blanking times considered.

### A. Basic operating principles of converter

1) *Mode 1:* In Fig. 5, $S_1$ and $S_3$ are turned on, but $S_2$ is turned off. There are two power flows in this mode. One is from the input through $S_1$ via $C_b$ and then to $L_p$, $S_3$ and the ground. The other is from $C_o$ to the ground. Therefore, the voltage across $L_p$ is the input voltage $v_i$ plus the voltage $v_i$ across $C_b$, thereby causing $L_p$ of the coupling inductor to be magnetized. Besides, $C_b$ is discharged. Also, $C_o$ releases energy into the output. And hence, the corresponding differential equations are:

$$\begin{cases} L_p \dfrac{\partial i_p}{\partial t} = 2v_i \\ C_o \dfrac{\partial v_o}{\partial t} = \dfrac{-v_o}{R_o} \\ i_i = i_p \end{cases} \tag{1}$$

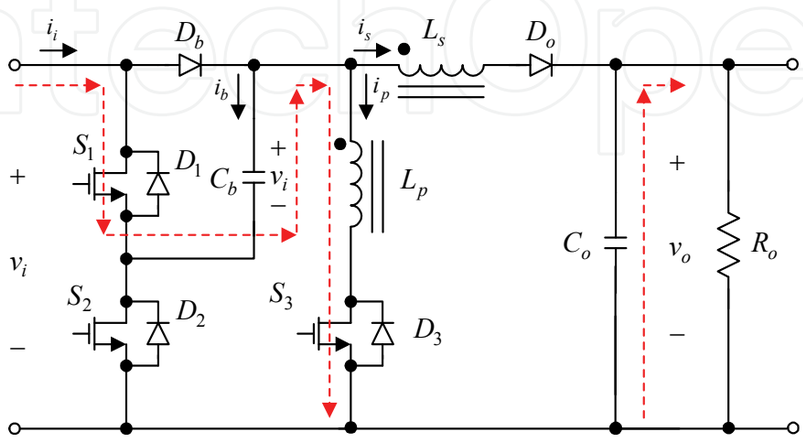


Fig. 5. Power flow of mode 1 without passive voltage-clamping circuit.

2) *Mode 2 :* In Fig. 6, $S_1$ and $S_3$ are turned off, but $S_2$ is turned on. There are two power flows in this mode. One is from the input through $C_b$ via $S_2$ and then to the ground. The other is from the input through $D_b$ via $L_s$ and then to $D_o$ and the output. Therefore, the voltage across $L_s$ is the input voltage $v_i$ minus the output voltage $v_o$, thereby causing $L_s$ of the coupling inductor to be demagnetized. Besides, $C_b$ is charged. Also, $C_o$ is energized. And hence, the corresponding differential equations are:

$$\begin{cases} L_s \dfrac{\partial i_s}{\partial t} = v_i - v_o \\ C_o \dfrac{\partial v_o}{\partial t} = i_s - \dfrac{v_o}{R_o} \\ i_i = i_s + i_b \end{cases} \tag{2}$$

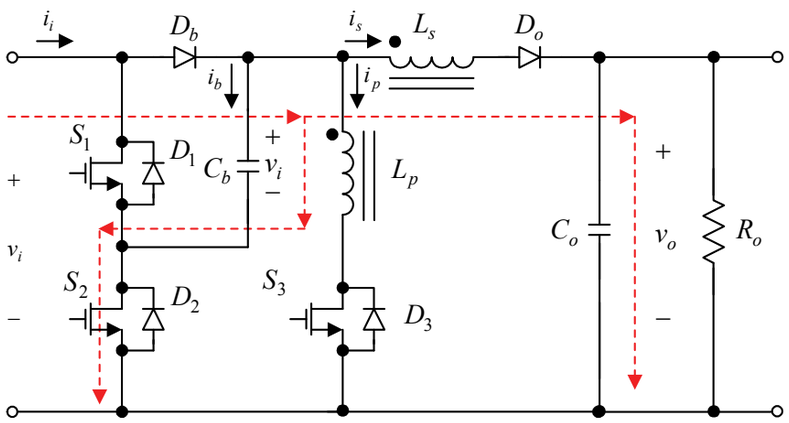


Fig. 6. Power flow of mode 2 without passive voltage-clamping circuit.

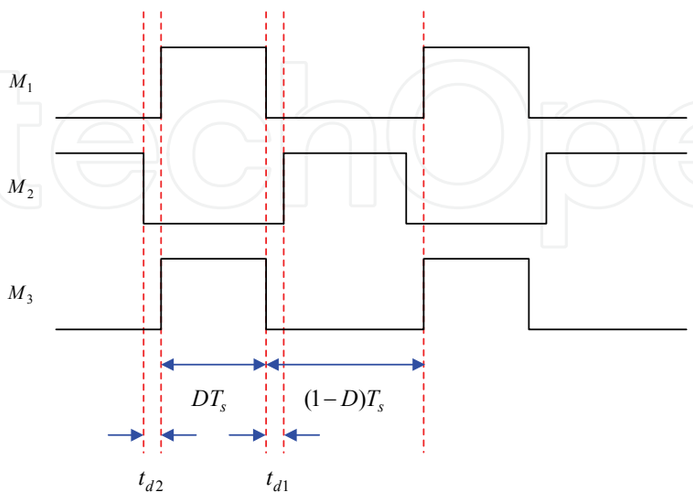


Fig. 7. Ideal timing sequence of gate driving signals $M_1$, $M_2$ and $M_3$ to drive $S_1$, $S_2$ and $S_3$ respectively, with blanking times considered.

However, in practice there are blanking times between $S_1$ and $S_2$, as shown in Fig. 7. And hence, there exist additional two modes. One mode, mode 3, locates between mode 1 and mode 2, with the blanking time of $t_{d1}$ considered. The other mode, mode 4, locates after mode 2 before mode 1, with the blanking time $t_{d2}$ considered. These two are to be described as follows.

Applying the voltage-second balance to (1) and (2), the voltage conversion ratio can be obtained to be:

$$\frac{V_o}{V_i} = \frac{(2n-1)D+1}{1-D} \tag{3}$$

3) *Mode 3:* In Fig. 8, $S_1$, $S_2$ and $S_3$ are all turned off, with the delay time of $t_{d1}$ considered. There is only one power flow that is from the ground through $C_b$ via $L_s$ and then to $D_o$ and the output. Therefore, the voltage across $L_s$ is the voltage $v_i$ across $C_b$ minus the output $v_o$, thereby causing $L_s$ of the coupling inductor to be demagnetized. Besides, $C_b$ is discharged. Also, $C_o$ is energized.

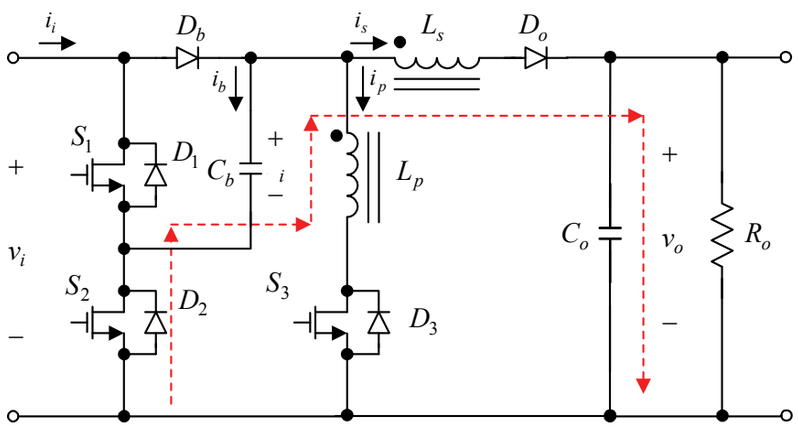


Fig. 8. Power flow of mode 3 without passive voltage-clamping circuit.

4) *Mode 4:* In Fig. 9, $S_1$, $S_2$ and $S_3$ are all turned off, with the delay time of $t_{d2}$ considered. There is only one power flow that is from the input through $D_b$ via $L_s$ and then to $D_o$ and the

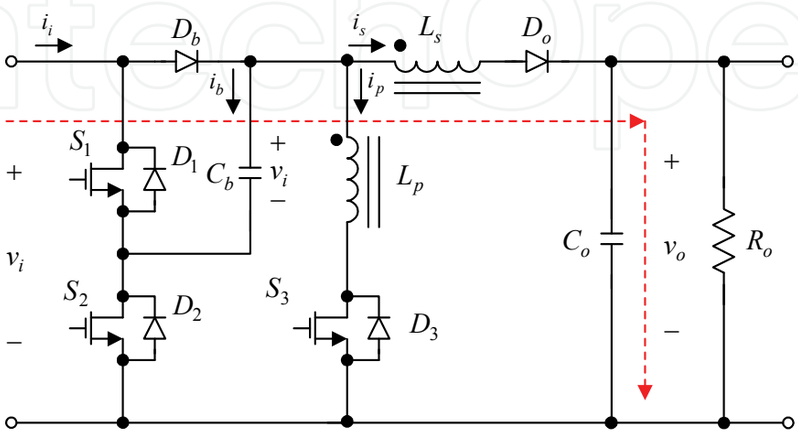


Fig. 9. Power flow of mode 4 without passive voltage-clamping circuit.

output. Therefore, the voltage across $L_s$ is the input voltage $v_i$ minus the output $v_o$, thereby causing $L_s$ of the coupling inductor to be demagnetized. Besides, $C_b$ lies idle. Also, $C_o$ is charged.

### B. Operating principles of passive voltage-clamping circuit

In this subsection, the main description focuses on the behavior of the passive voltage-clamping circuit instead of the behavior of the main power stage.

1) *Mode 1:* In Fig. 10, the moment $S_3$ is turned off, the energy stored in $L_{LK}$ is released to $C_{sn}$ via $D_{sn}$.

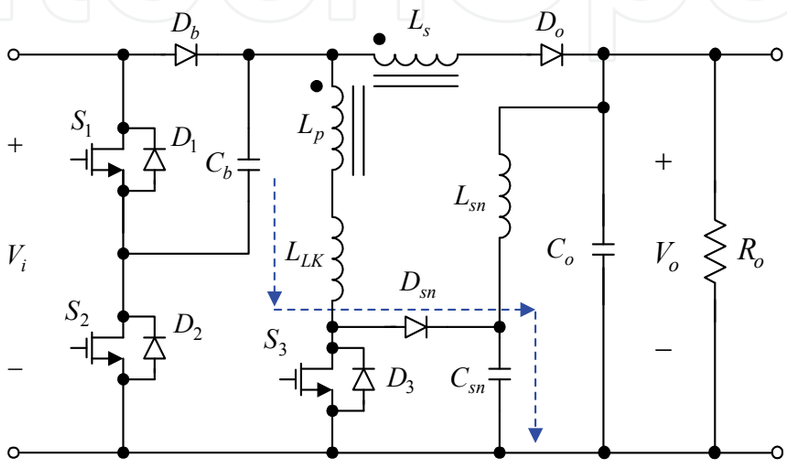


Fig. 10. Power flow of passive voltage-clamping circuit in mode 1.

2) *Mode 2:* In Fig. 11, as soon as $S_3$ is turned on, the energy stored in $C_{sn}$ is pumped into the output via $L_{sn}$.

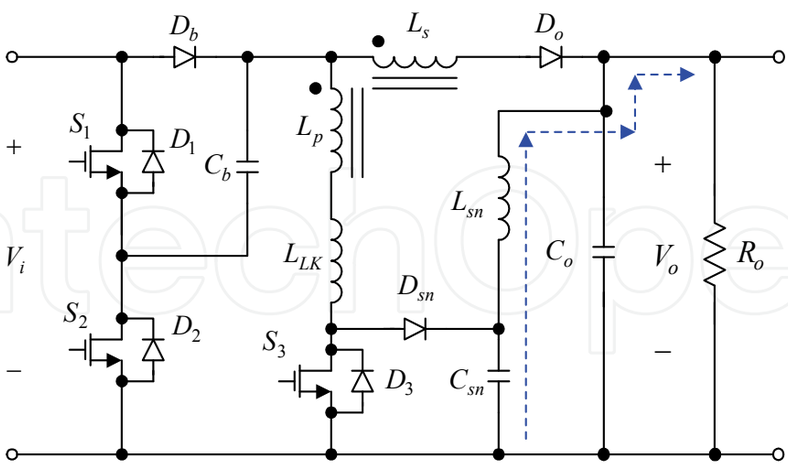


Fig. 11. Power flow of passive voltage-clamping circuit in mode 2.

## 4. Applied control method

Fig. 12 shows the proposed overall system block diagram for the proposed converter. The one-comparator counter-based PWM control without any analog-to-digital converter (ADC)

based on the field programmable gate array (FPGA) [20][21] is employed herein, and the parameters of the proportional integral (PI) controller, including the proportional gain $k_p$ and the integral gain $k_i$, are tuned at rated load. In addition, the output voltage information after the voltage divider is obtained through the comparator, and then sent to FPGA having a system clock of 100MHz to create the desired PWM control signals to drive the MOSFET switches after the gate drives.

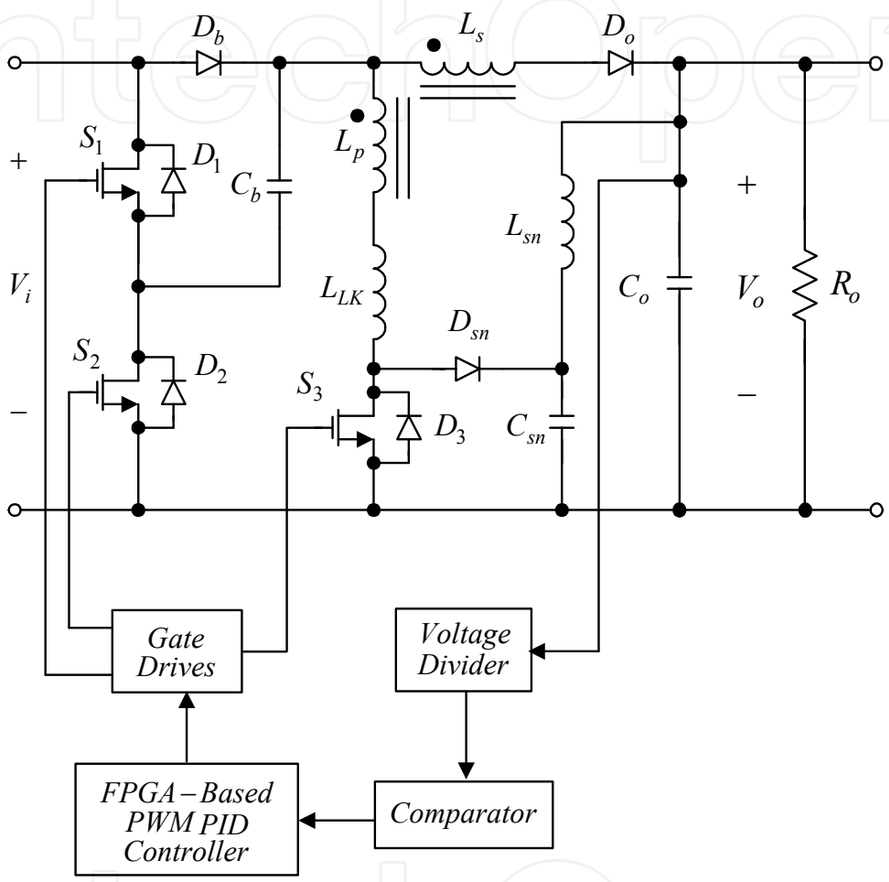


Fig. 12. Overall system block diagram for the proposed converter.

## 5. Key parameter considerations

Before this section is discussed, there are some specifications to be given as follows: (i) rated DC input voltage $V_i$ is set to 5V; (ii) rated DC output voltage $V_o$ is set to 48V; (iii) rated DC output power $P_{o\text{-}rated}$ is set to 48W; (iv) minimum DC output current $I_{o\text{-}min}$ in the boundary conduction mode (BCM) is 0.15A; (v) switching frequency $f_s$ is chosen to be 195kHz; (vi) turns ratio $N_s/N_p$ of the coupling inductor is set to 5; (vii) one 1000μF electrolytic capacitor is chosen for $C_o$; (viii) product names of $D_b$, $D_{sn}$ and $D_o$ are STPS20L25, 3CTQ100 and 3CTQ100, respectively; (ix) product names of $S_1$, $S_2$ and $S_3$ are PHD96NQ03LT, PHD96NQ03LT and IRL3705ZS, respectively; (x) product name of the control IC is EPIC3T100; (xi) PI controller parameters $k_p$ and $k_i$ are set to 0.25 and 0.0625, respectively; and (xii) blanking times $t_{d1}$ and $t_{d2}$ are both set to 100ns.

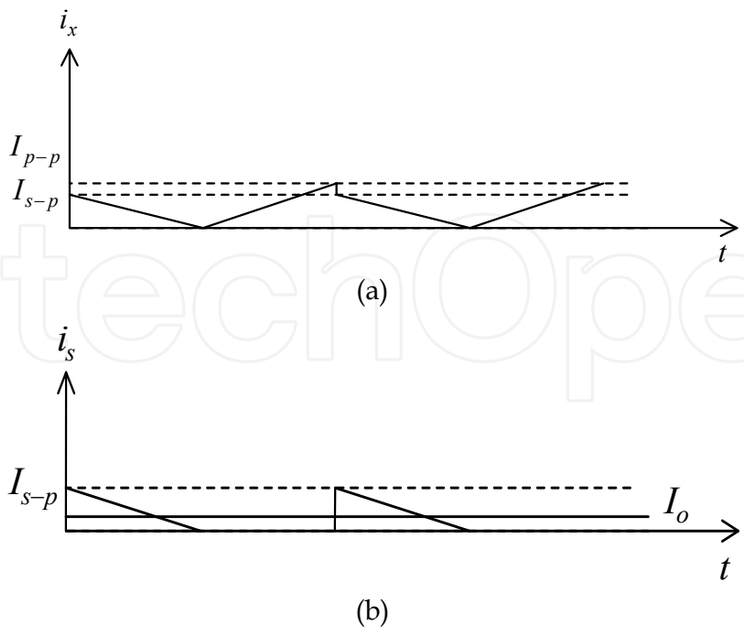


Fig. 13. Current waveforms in BCM: (a) primary-side current plus secondary-side current, $i_x$; (b) secondary-side current $i_s$.

### A. Design of main power stage

In the main power stage, there are three key parameters to be designed. One is the value of $C_b$ in the charge-pumping cell and the other two are the values of $L_p$ and $L_s$ in the inductance-coupling cell. On condition that this converter works in BCM, corresponding to the minimum load current $I_{o\text{-}min}$, the peak value $I_{p\text{-}p}$ of the current flowing through $L_p$, shown in Fig. 13, can be expressed to be:

$$I_{p-p} = nI_{s-p} = \frac{2nI_{o-min}}{1-D} \tag{4}$$

where $I_{s\text{-}p}$ is the peak value of the current flowing through $L_s$.
Consequently, the minimum energy stored in $L_p$ under BCM, $E_{L\text{-}min}$, can be represented as:

$$E_{L-min} = \frac{1}{2}L_p I_{p-p}^2 \geq \frac{1}{2}V_i D T_s I_{p-p} \tag{5}$$

Based on (4) and (5), the value of $L_p$ can be expressed to be:

$$L_p \geq \frac{V_i D(1-D)T_s}{2nI_{o-min}} \tag{6}$$

According to the given specifications and (3) and (6), the value of $L_p$ is calculated to be larger than 4.3μH, and eventually one coupling inductor is chosen with $L_p$ set to 5μH using one T106-18 core with five turns and $L_s$ set to 80μH using the same core with twenty turns.
Besides, there are some assumptions used to obtain the value of $C_b$ as follows: (i) this converter operates at rated load; (ii) $C_b$ is charged to $V_i$ in mode 2; (iii) maximum percentage

of decreased variation in voltage on $C_b$ in discharge, ε, is set to 0.5% in mode 1; (iv) input voltage is an infinite bus, i.e., the input voltage is kept constant and can be represented as infinite capacitance which is much larger than the value of $C_b$; and (v) converter efficiency $\eta$ is initially set to 80% at rated load. It is noted that the efficiency is assumed to be 80% at rated load is based on the following reason. Since this coupling inductor behavior is similar to the transformer in the flyback converter and the efficiency of the flyback converter under the traditional control technique is generally about 80%, this is why the efficiency of the proposed converter operating at rated load is roughly chosen to be 80% for the convenience of design of $C_b$.
Therefore, in mode 1, the energy $E_e$ is extracted from $V_i$ and $C_b$, and can be expressed as:

$$\begin{aligned} E_e &= \frac{1}{2}C_b\left\{(2V_i)^2 - \left[(2-\varepsilon)V_i\right]^2\right\} \\ &= \frac{1}{2}(4\varepsilon - \varepsilon^2)C_b V_i^2 \end{aligned} \tag{7}$$

Also, in mode 2, the energy $E_s$ is sent to the load, and can be represented as:

$$E_s = \frac{P_{o-rated}(1-D)T_s}{\eta} \tag{8}$$

According to conservation of energy, $E_e$ is not less than $E_s$, and hence the value of $C_b$ can be expressed to be:

$$C_b \geq \frac{2P_{o-rated}(1-D)T_s}{(4\varepsilon - \varepsilon^2)V_i^2\eta} \tag{9}$$

Based on the given specifications and assumptions and (3) and (9), the value of $C_b$ is calculated to be larger than 362μF, and finally two paralleled 330μF OSCON capacitors connected in parallel with one 22μF MLCC capacitor are selected for $C_b$ to compensate the effect of frequency on the capacitance and the reduction of the equivalent series resistance (ESR).

### B. Design of passive voltage-clamping circuit

There are two key parameters to be designed in the passive voltage-clamping circuit. One is the value of $C_{sn}$, and the other is the value of $L_{sn}$. Before doing these, we need to measure the value of $L_{LK}$ and set the maximum value of the voltage across $C_{sn}$, $V_{max}$, during the turn-off period for $S_3$ without the voltage spike considered. And hence, based on the following, the minimum value of $C_{sn}$ can be obtained to be:

$$\frac{1}{2}C_{sn}V_{max}^2 \geq \frac{1}{2}L_{LK}I_{p-max}^2 \tag{10}$$

By rearranging (10), the resulting value of $C_{sn}$ can be obtained to be:

$$C_{sn} \geq \frac{L_{LK}I_{p-max}^2}{V_{max}^2} \tag{11}$$

where $I_{p\text{-}max}$ is the maximum value of the current flowing through $L_p$ at rated load.
As for the value of $L_{sn}$, the relationship between the time required for the voltage across $C_{sn}$ to fall from the maximum value to zero without the voltage spike considered and the turn-off period for $S_3$ can be expressed as

$$(1-D)T_s \geq 0.5\pi\sqrt{L_{sn}C_{sn}} \tag{12}$$

By rearranging (12), the resulting value of $L_{sn}$ can be found to be

$$L_{sn} \leq \frac{4(1-D)^2 T_s^2}{\pi^2 C_{sn}} \tag{13}$$

Based on (13), the measured value of 1.8μH for $L_{LK}$, $V_{max}$ set to double the input voltage, and other given and calculated values, the resulting minimum value of $C_{sn}$ is worked out to be 1.98μF and finally the value of $C_{sn}$ is set to 2.2μF whereas the resulting maximum value of $L_{sn}$ is figured out to be 1.42μH and eventually the value of $L_{sn}$ is set to 1μH.

## 6. Simulated and experimental results

Before some experimental results are provided, a simulated result at startup based on MATLAB/SIMULINK/SIMPOWERSYSTEMS for the proposed converter operating under the open loop are provided to verify its feasibility, and after this, some experimental results under the closed loop are utilized to demonstrate the effectiveness of this converter. Therefore, Fig. 14 shows the simulated output voltage of the proposed converter under open-loop control during startup. It can be seen that the output voltage of this converter can stably rise to the neighborhood of the prescribed value.

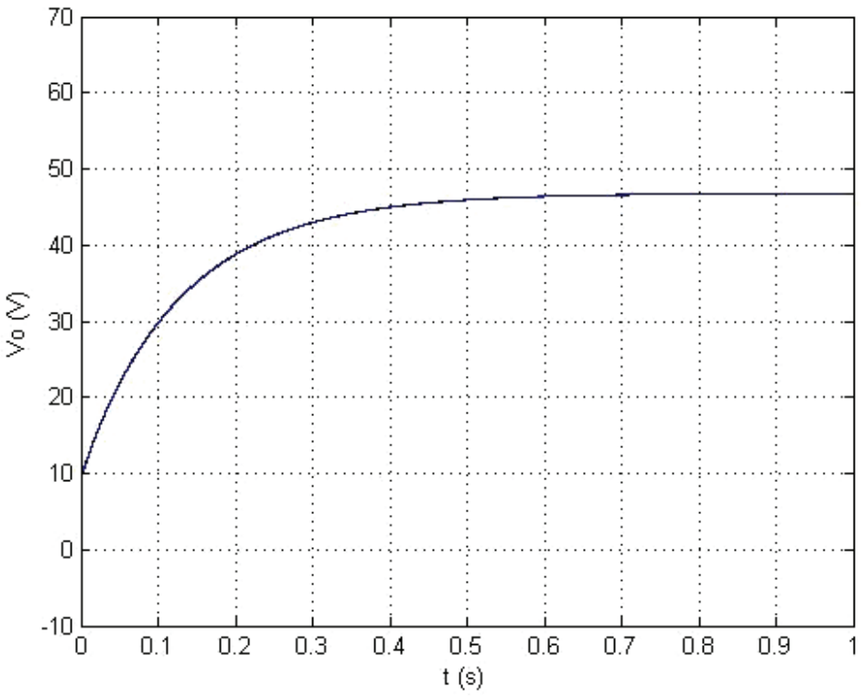


Fig. 14. Simulated output voltage during startup.

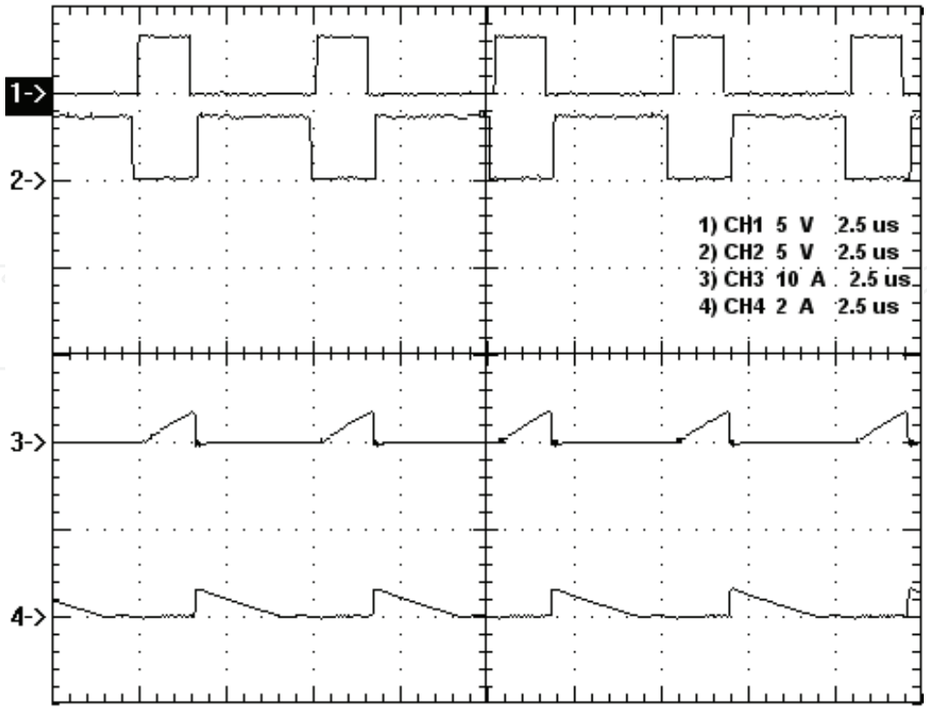


Fig. 15. Under 15% of the rated load: (1) gate driving signal for $S_3$; (2) gate driving signal for $S_2$; (3) current in $L_p$; (4) current in $L_s$.

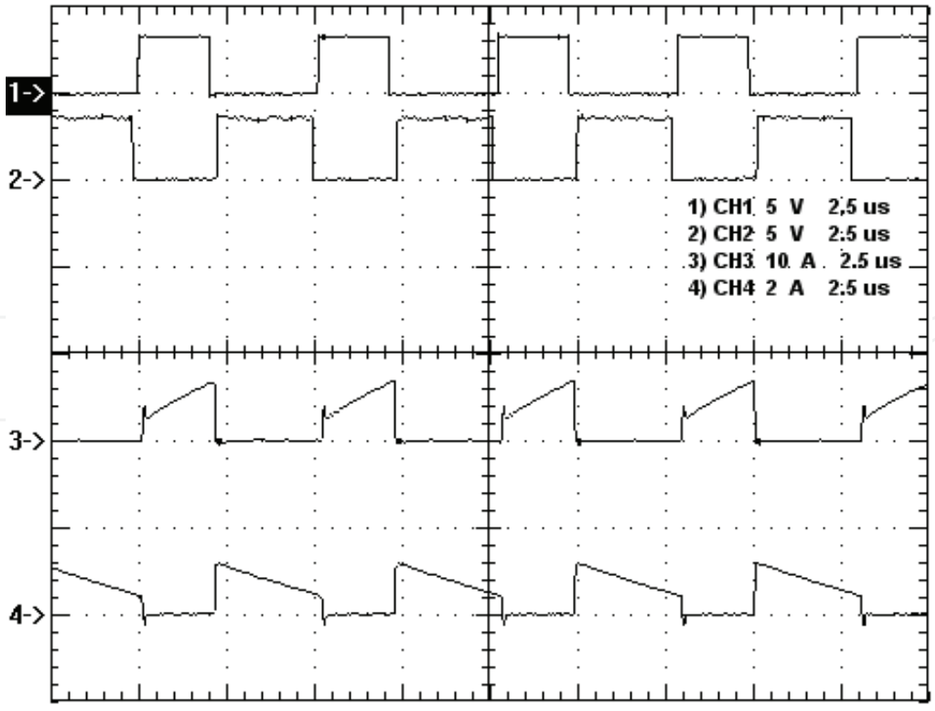


Fig. 16. Under 50% of the rated load: (1) gate driving signal for $S_3$; (2) gate driving signal for $S_2$; (3) current in $L_p$; (4) current in $L_s$.

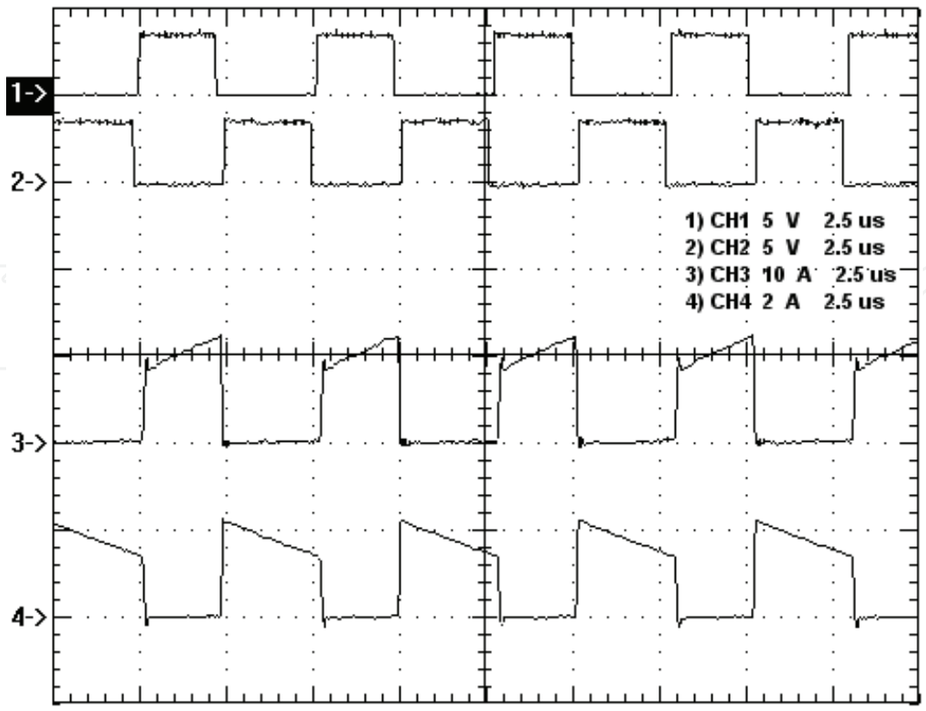


Fig. 17. Under the rated load: (1) gate driving signal for $S_3$; (2) gate driving signal for $S_2$; (3) current in $L_p$; (4) current in $L_s$.

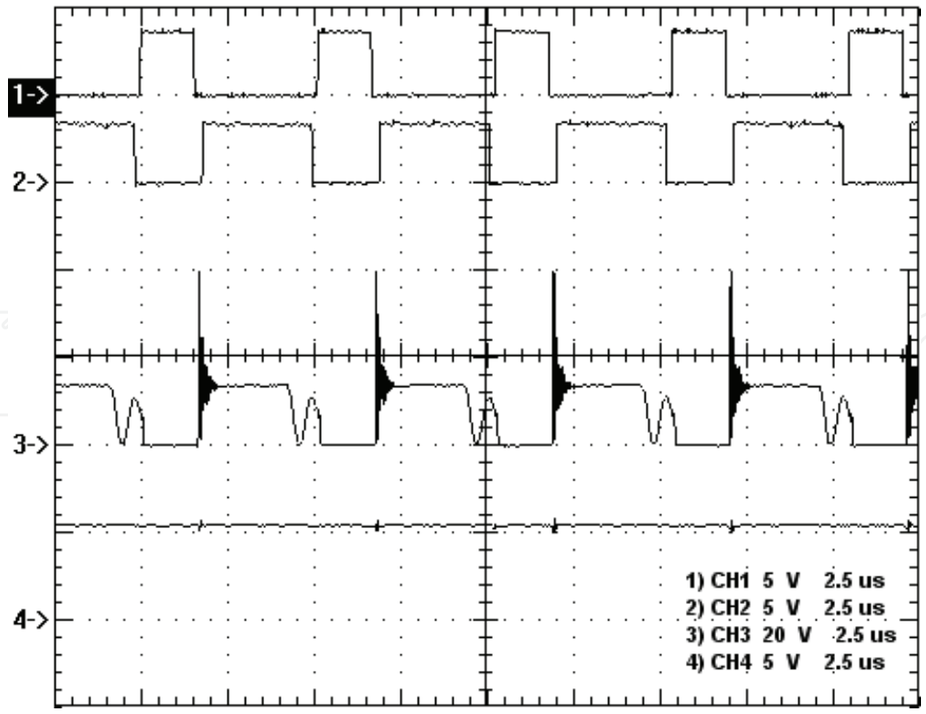


Fig. 18. Under 15% of the rated load: (1) gate driving signal for $S_3$; (2) gate driving signal for $S_2$; (3) voltage on $S_3$; (4) voltage on $C_b$.

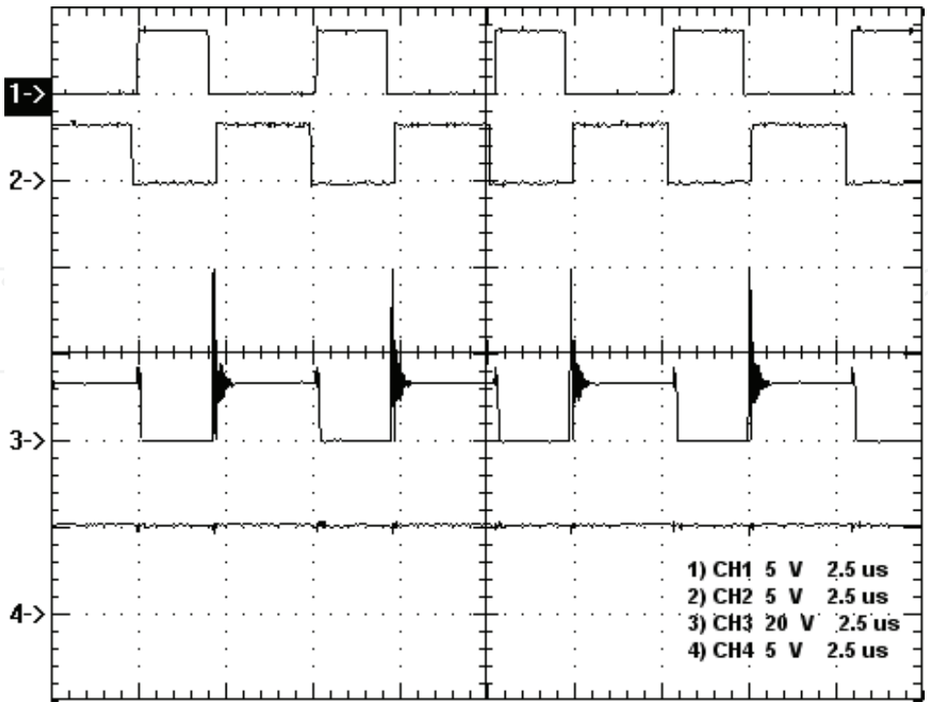


Fig. 19. Under 50% of the rated load: (1) gate driving signal for $S_3$; (2) gate driving signal for $S_2$; (3) voltage on $S_3$; (4) voltage on $C_b$.

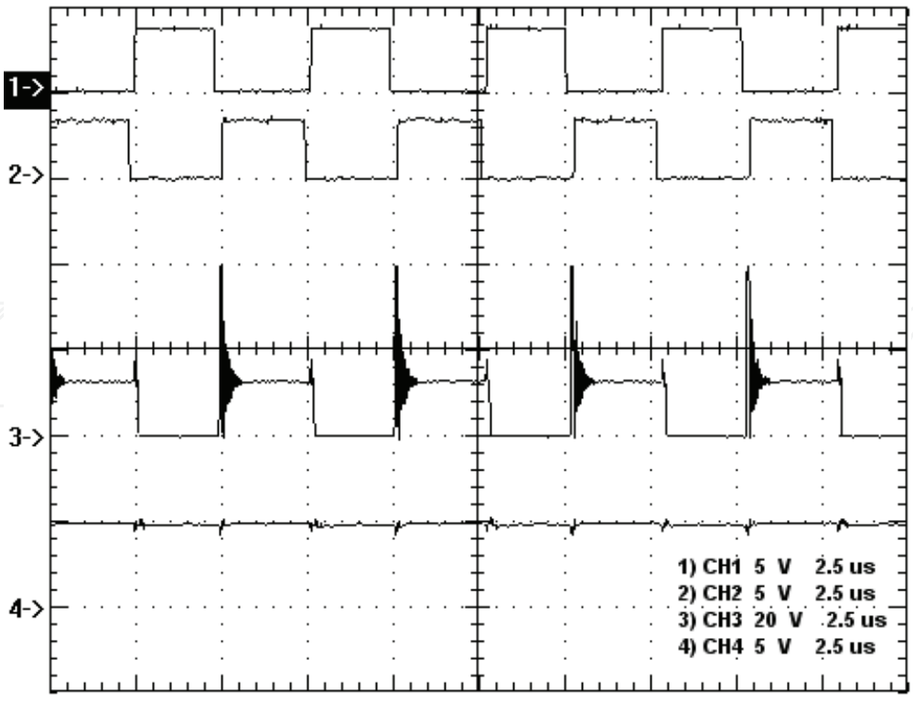


Fig. 20. Under the rated load: (1) gate driving signal for $S_3$; (2) gate driving signal for $S_2$; (3) voltage on $S_3$; (4) voltage on $C_b$.

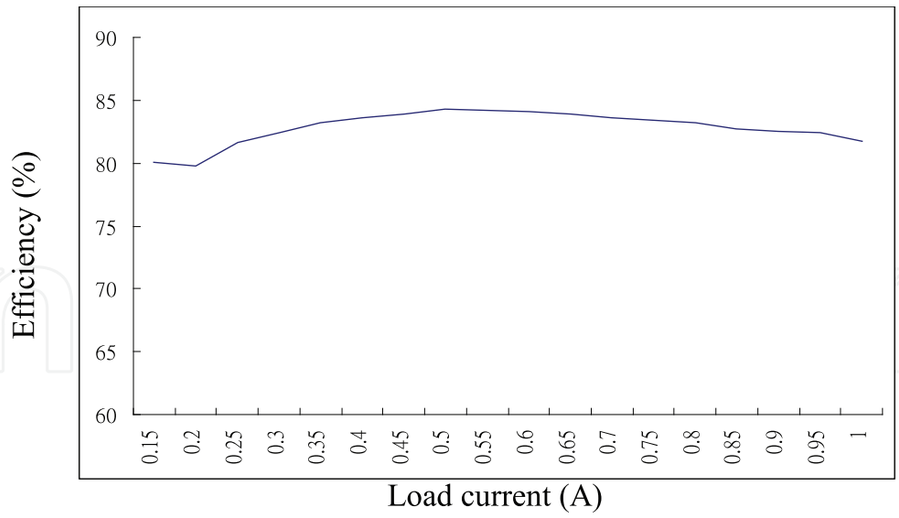


Fig. 21. Efficiency versus load current.

Afterwards, some experimental waveforms shown in Figs. 15 to 21 are provided to verify the performance of the proposed circuit topology. Figs. 15 to 17 depict the PWM gate driving signals for $S_3$ and $S_2$ and the currents in $L_p$ and $L_s$, under 15%, 50% and 100% of the rated load respectively. It is noted that the converter under 15% of rated load operates in DCM, which does not correspond to the design specifications. This is because the inductance is reduced due to the high switching frequency. Figs. 18 to 20 show the gate driving signals for $S_3$ and $S_2$, the voltage on $S_3$ and the voltage on $C_b$, under 15%, 50% and 100% of the rated load respectively. It is noted that the more the load current, the lower the voltage on $S_3$. As for the voltage spike on $S_3$, it is due to the turn-on delay created from the diode $D_{sn}$. Besides, the voltage across $S_3$ is larger than double the input voltage prescribed. This is because the value of $C_{sn}$ is reduced due to high frequency or there exists capacitance tolerance in $C_{sn}$. According to the mention above, it is evident that the proposed voltage-boosting converter can stably operate under closed-loop control.

On the other hand, Fig. 21 displays the curve of efficiency versus load current. It is noted that unlike the traditional voltage-boosting converter, the proposed voltage-boosting possesses an almost flat range of the efficiency from minimum load to rated load. This is because the charge-pumping cell is used. To explain lucidly, the primary inductance of the coupling inductor is magnetized by double the input voltage, thereby causing the input current to be reduced, and this behavior is similar to the KY converter.

## 7. Conclusion

A new voltage-boosting converter, combining the charge pump and the coupling inductor, is proposed herein, together with a passive voltage-clamping circuit. Conclusions are summarized as follows:

1. This converter with high voltage ratio required is simpler in structure than any other converter mentioned in Sec. I.
2. The primary inductor is magnetized under double the input voltage, thereby causing the input current to be reduced and hence the efficiency to be upgraded at light load, and this behavior is similar to the KY converter.
3. The passive voltage-clamping circuit pumps part of the energy stored in the leakage inductance to the output.

4. For the multi-phase to be considered, if the number of phases is N, then only additional N-1 diodes are added.

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The world's reliance on existing sources of energy and their associated detrimental impacts on the environment- whether related to poor air or water quality or scarcity, impacts on sensitive ecosystems and forests and land use - have been well documented and articulated over the last three decades. What is needed by the world is a set of credible energy solutions that would lead us to a balance between economic growth and a sustainable environment. This book provides an open platform to establish and share knowledge developed by scholars, scientists and engineers from all over the world about various viable paths to a future of sustainable energy. It has collected a number of intellectually stimulating articles that address issues ranging from public policy formulation to technological innovations for enhancing the development of sustainable energy systems. It will appeal to stakeholders seeking guidance to pursue the paths to sustainable energy.



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