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Pulse generator design

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1. Analysis of the current state of the art

The techniques normally used for generating pulses in low-cost monolithic technology (CMOS or BiCMOS) are different from those usually used in hybrid technologies. The latter mainly use edge combination methods generated from SRD diodes via quarter-wave lines or stubs (Jeongwoo Han et al., 2004). In a low-cost context, these techniques are not possible, as they cannot be integrated into the desired technologies. We shall present here only the following techniques:

- Baseband pulse transposition
- Baseband pulse filtering
- Synthesis by pulse combination.

This analysis is performed using circuits that have been built and measured and that can be found in the literature. Before commencing this analysis, it is necessary to point out that the figure of merit often used in pulse generation is the energy consumed by the pulse. This criteria is subject to a caveat, as it often fails to take into account the power consumed between two pulses, which means it is only relevant if the system is combined with power management (sometimes difficult to achieve, depending on the topology of the circuit). This is why we shall be presenting, wherever possible, an estimate of the total energy consumed by the pulse ($Ec_t=P_{DC}/D_S$) that take into account the average consumption between two pulses. The energy consumed per pulse will then be used to quantify the energy consumed during the pulse alone (τ), and if this is not given, it will be approximated as follows: $E_c=P_{DC}*\tau$. Moreover, in order to be completely suitable, the energy consumed by the total pulse must be compared to the energy of the pulse produced (E_p) by way of the energy efficiency per pulse ($n=E_p/Ec_t$). As this energy is rarely given, it will be estimated by assuming that the pulse is a sinusoid modulated by a gate of width τ and amplitude V_p ($E_p=\tau.V_p^2/2R_0$).

1.1. Baseband pulse transposition

This technique, described in Fig. 1, makes it possible to transpose a baseband pulse in a frequency band. This technique has the great advantage of being able to change the frequency band by varying the local oscillator (LO) frequency, as well as varying the bandwidth by the width of the baseband pulse. Furthermore, the doubling of the spectrum

due to the frequency transposition allows the use of baseband pulses with a width of $\tau=2/BW$. In addition, these techniques are not very sensitive to LO phase noise which only degrades the spectral purity of the lines of the discrete spectrum and does not affect the Power Spectral Density (PSD) envelope.

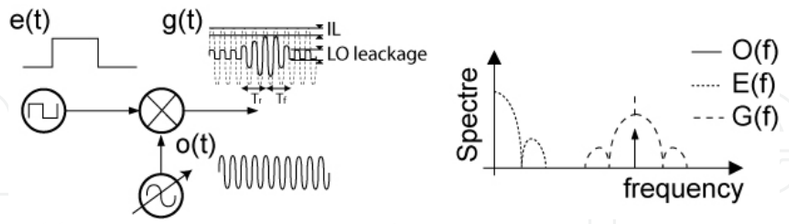


Fig. 1. Principle of frequency transposition architectures

A first transposition technique is based on the use of a switching circuit (Rui Xu et al., 2006), usually a CMOS switch or a mixer. The performance of these architectures is mainly determined by the switching circuit, since the control signal gives the envelope of the baseband pulse transmitted. The performance of these architectures mainly depends on the off-on switching time (Tr), the on-off switching time (Tf), the insertion losses (IL), and the isolation between the LO and the output, as all these parameters influence the spectrum of g(t) (G(f) in Fig. 1). The simplest architecture found in literature is based on the use of a single transistor. This topology is very limited, as its sizing makes it impossible to optimize all the performance criteria at the same time. Indeed, reducing the insertion losses involves increasing the size of the transistor, leading to increased stray capacitances, which degrades the insertion losses at high frequencies and reduces isolation from the output (Rui Xu et al., 2006).

The switching circuit can also be achieved using a double balanced mixer similar to a Gilbert cell (Wentzloff & Chandrakasan, 2006) (Datta et al., 2007). In (Wentzloff & Chandrakasan, 2006), the currents in the differential pairs are summed in order to cancel out LO leakage and improve isolation. Moreover, this topology makes it possible to generate BPSK signals by switching the baseband signal between the + or − inputs. In addition, the use of a mixer allows a better control of the signal spectrum by changing the baseband pulse shape. In (Datta et al., 2007), a passive Gaussian filter is used to shape the baseband pulse and a Gilbert cell is used to generate the bipolar signals. However, because of the LO leakages, these structures require small signals to be used for the switching (LO input). As shown in Table 1, this results in low output amplitudes and implies the use of power amplifiers (PA). In addition, the switching times of these architectures are greater than those of a single transistor. This difficulty in producing wideband mixers prevents the generation of very short (<1 ns) pulses using this topology.

Even though none of the circuits here includes the LO, the consumption is poor because of the consumption of the mixers. This implies the use of power management to turn off the LO between two pulses.

These considerations concerning LO power management have given rise to a technique that consists of switching the LO directly (On/Off LO or Switched LO) rather than its output, solving not just the problem of consumption between two pulses, but also the leakage problem. This method allows performance to be achieved (see Table 1) that represents the state of the art in 2009 in terms of consumption and amplitude, for generating 500 MHz

bandwidth signals in the 3–5 GHz band. In the case of an LC LO, (Phan et al., 2008) shows that the rise and fall times (t_r and t_f) can be equal and give rise to 3.5 ns wide pulses with component values that can be integrated into the technology used (0.18 μm CMOS). Furthermore, the use of switched capacitors makes it possible to change the oscillation frequency and to address different channels, making this technique applicable for systems to the 802.15.4 standard. The major drawback of this technique lies in the low pulse amplitude.

To improve start-up time, (Barras et al., 2006) proposes a structure that gives the LO initial conditions that are greater than those generally produced by noise. This technique also allows the modification of the start phase, thereby offering the possibility of performing BPSK modulation. As reported in Table 1, this technique makes it possible to achieve very good performance in terms of amplitude.

In order to mitigate the excessively long start-up times for LC LOs, (Sanghoon Sim et al., 2009) proposes using ring oscillators. This structure allows the pulse widths to be around 0.5 ns. Furthermore, the digital structure of these LOs makes it possible to use inverters as output buffers with better performance than voltage followers, allowing amplitudes greater than 600 mV_{pp} for a consumption of 27 pJ/Pulse in the 6–10 GHz band.

Ref.	Arch.	LO leakage PWM6	τ (ns)	V_{pp}	Ec (pJ/P)	Ec_t (pJ/P)	Ep (pJ/P)	n	Pcons	Size (mm^2)	Techn.	Mod.	Integ.
0	Gated-LO (SW)	10	0.4	1.2	0.7*	120	1.44	0.012	1.8 mW @ 15 MHz	0.6	0.18 CMOS	OOK	Ext. LO
0	Gated-LO (Mix)	~10	1.7 – 3.3	0.25	100*	313	0.52	0.0016	31.3 mW @ 100 MHz	nc	0.18 SiGe	BPSK	Ext. LO
0	Gated-LO (Mix)	5	1	0.014	15*	120	0.0005	4.10^{-6}	15 mW @ 125 MHz	nc	0.25 SiGe	BPSK	Full
0	On/Off-LO (LC)	0	3.5	0.18	18	18	0.284	0.016	6.52 mW @ 125 MHz	0.39	0.18 CMOS	OOK	Full
0	On/Off-LO (LC)	0	2.5	0.9	180	180	5.06	0.028	1.8 mW @ 10 Mp/s	0.57	0.18 CMOS	BPSK	Full
0	On/Off-LO (rings)	0	0.5	0.673	27	nc	0.56	0.021**	nc	0.11	0.18 CMOS	OOK	Full

* Estimate (Ec=Pdc*τ), ** (Ec/Ep)

Table 1. Main characteristics of LO switching generators.

Table 1 lists the key characteristics of the works presented. With this technique, efficiencies of the order of 1 % and levels below 1 V are reached. Let us note here that only the works presented in 0 and 0 consume no power between two pulses ($Ec=Ec_t$).

1.2. Baseband pulse filtering

The principle of this technique, represented in Fig. 2, is based on the excitation of a filter by one or more baseband pulses produced by the combination of logic edges.

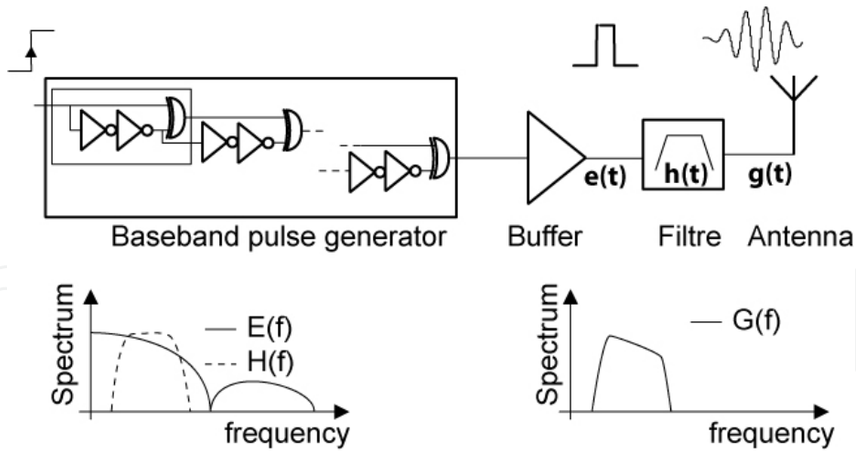


Fig. 2. Principle of baseband pulse filtering.

The expression of the generated pulse (g(t)) and its Fourier transform (G(f)) are dependent on the baseband pulses (e(t)) and the filter's transfer function in the manner described by 0 and 0. In particular, the filter makes it possible to adapt the signal's spectrum to a particular frequency band.

$$g(t) = e(t) * h(t) \tag{1}$$

$$G(f) = E(f).H(f) \tag{2}$$

This technique is particularly interesting for a low cost on package integration (System on Package – SoP) of the generator (Lee et al., 2008), as the generation of baseband pulse can be easily achieved in CMOS (here, 0.35 µm CMOS) and the filter can easily be produced "Off Chip" with coplanar or micro-strip technology at the same time as the interconnection with the antenna. In this work, excitation is achieved by a 2 ns wide pulse with an amplitude of 2.8 V, produced by a logic edge combiner which is described in Fig. 2. The signal is then filtered by a stub filter integrated onto a low-cost substrate (FR4). This technique makes it possible to generate pulses of substantial amplitude (0.65 V_{pp}) thanks to the filter's modest insertion loss (2.3 dB) and the strong excitation. Moreover, the total SoP size does not exceed 40 mm * 40 mm.

In order to be independent of the production of the chip carrier inherent to SoP technologies, it is possible to implement this technique in a System on Chip (SoC) with 0.13 µm CMOS technology (Bourdel et al., 2009). Indeed, in the case of UWB signals occupying the whole FCC band, the constraints on the filter are fairly minimal, and a 3rd-order is enough to meet the FCC mask, which leads to reasonable losses despite the poor quality of passive circuits of these technologies. Here, the filter is current driven by a C class biased transistor, which reduces the consumption (Ec) to 2.2 pJ/Pulse for a 1 V_{pp} pulse. Moreover, the authors show that the use of SoP technology would improve generator performance and that the use of conventional (non-ECL) logic would reduce the static consumption to 0 W. This performance represents the state of the art in terms of pulses generation covering the whole FCC band, and will be presented in detail in this chapter.

However, these techniques are limited when the filter order increases in order to generate pulses with lower spectral occupation (Bourdel et al., 2007). Filtering a 75 ps elementary

pulse requires a 5th order to meet the ECC mask. It is then necessary to use an active filter in order to compensate the integrated filter's losses, which heavily penalizes the consumption, as shown by the circuit characteristics presented in Table 2. Furthermore, such a filter requires a significant number of inductors, which greatly increases the circuit's size.
In order to relax the constraints on the filtering, it is possible to use a sequence of elementary pulses instead of a single pulse (Smaini et al., 2006). In this way, it is possible to concentrate the pulse energy around the pseudo frequency of the sequence, thereby making filtering around this frequency easier. This technique can be used to generate pulses with a bandwidth of 500 MHz for applications in the 802.15.4 standard (Wentzloff & Chandrakasan, 2007). Eleven 120 ps elementary pulses at 120 ps spacing make it possible to generate a pulse in Channel 2 (4.05 GHz) after a simple filtering of the DC component. Varying the width, spacing, and number of pulses makes it possible to address different bands. Here, the consumption increases compared with the previous works presented, but it remains acceptable when compared with the energy of the pulse produced. However, it is not possible to achieve the consumption performance of the LO swintching designed for this same type of application using this technique, whereas small size (0.08 mm²) can be achieved due to the absence of inductors.
Table 2 summarizes the main characteristics of generators using pulse filtering. Here too, efficiencies are of the order of 1 % and levels do not exceed 1 V. However, this technique makes it possible to achieve higher bandwidths than those obtained with LO switching.

Ref.	t (ns)	BW (GHz)	Vpp (V)	Ep (pJ/P)	Ep (pJ/P)	Ep (pJ)	n	Pdc	Size (mm^2)	Techn.	Mod.	Integ.
0	2	nc	0.65	nc	nc	2.11	nc	nc	0.5	0.35 CMOS	OOK	SoP
0	0.6	4.3	1	2.25	13.5	2.16	0.16	2.7mW@200MHz	0.54	0.13 CMOS	OOK	SoC
0	1.8	2.5	0.35	23.6*	52.4	0.55	0.01	13.1mW@250MHz	1.02	0.13 CMOS	BPSK	SoC
0	0.6-0.8	2-4	0.35–0.45	8*	62.5	0.41	0.006	10mW@160MHz	1.56	0.13 CMOS	BPSK	SoP
0	3	0.5	0.65	47	nc	3.17	0.07**	nc	0.08	0.09 CMOS	BPSK	SoC

* Estimate (Ec=Pdc*τ), ** Ep/Ec
Table 2. Performance of baseband pulse filtering generators.

1.3. Synthesis by pulse combination

This technique is based on the principle (described in Fig. 3) that multi-cycle pulses s(t) are a combination of elementary single-cycle pulses $e_n(t)$.

$$s(t) = \sum_{n=0}^{N-1} g_n . e_n \left(t - \sum_{n=0}^{N-1} \tau_{n-1} \right) \quad (3)$$
$$with \quad \tau_{-1} = 0$$

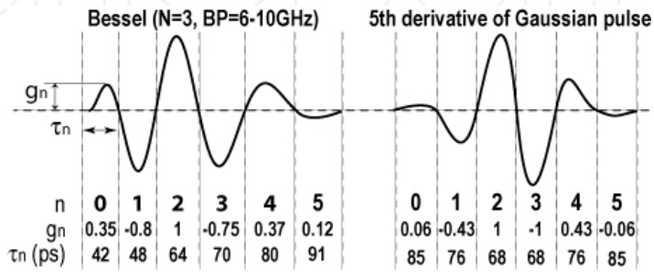


Fig. 3. Principle of synthesis by pulse combination.

It appears that varying the shape of the elementary pulse has little influence on the final spectrum, and that only its amplitude and width have any real influence (Vauché et al., 2009). Hence it is possible to synthesize a complex pulse using a same pulse e(t) delayed and amplified. The major advantage of this technique lies in the fact that it is no longer necessary to use filters or oscillators and that it can be achieved without inductors. This gives to this technique a great deal of potential, particularly with the developments of submicronic technologies. The other major interest of this technique lies in its programmability. Indeed, it then becomes possible to adapt the pulse to a channel, to change its frequency band, to produce predistortion, or to compensate for process variation associated with manufacturing. However, this technique is not mature and few circuits have so far been produced.
The main studies carried out to date use the same technique for generating elementary pulses, namely an edge combiner based on a voltage controlled delay line (VCDL). However, these studies are characterized by the use of different combination methods. The elementary pulses can be current-combined by transistors of different sizes (Kim et al., 2004). The nature of the transistor (P or N) makes it possible to achieve the positive or negative alternation of the pulses. The consumption is very good (15 mW @ 500 MHz) as the output stage is unbiased and operates in switching mode. It is also possible with this technique to address different frequency bands by varying the combiner delays (Kim et al., 2006) (Kim et al., 2005). However, this topology remains limited in terms of programmability, as it is not possible to change the number of amplitude of the elementary pulses.

It is also possible to use current combination with differential pairs, which makes it possible to control the amplitude of the pulses by varying the biasing of the pairs (Bourdel et al., 2007). The positive and negative alternation of the pulses is achieved by cross-connecting the path of the differential pairs. Here, the number and amplitude of the pulses are not limited, which gives a great deal of latitude in programming. However, an output stage configured as a voltage follower is necessary to drive the power into a 50 Ω load. This output stage limits the performance in terms of amplitude ($0.6V_{pp}$ simulated using a 0.13 µm CMOS Design Kit) and static consumption. The energy consumed per pulse remains acceptable (26.4 pJ/P) if high-performance power management is used, otherwise the circuit consumes 202 pJ/P @ 100 Mbs^{-1}.
The principle of current summing using differential pairs can be used to produce bipolar pulses, or to relieve the constraints on the filtering in order to be able to achieve complete integration (SoC), using only an integrated output transformer (Demirkan et al., 2008). The circuit's consumption is substantial (71 pJ/P) because of the high data rate. However, the principle of this approach is validated with a measured pulse amplitude of 220 mV_{pp}.
Triangular pulses and a charge pump can also be used to vary the amplitudes of the elementary pulses (Norimatsu et al., 2007). The value of the current in the charge pump sets the amplitude of the triangle. This circuit produces a pulse using just digital cells, and the size of the circuit reaches 0.4 mm^2 in 0.18 µm CMOS technology. Moreover, the circuit achieves good performance in terms of amplitude and pulse width ($1.24V_{pp}$ measured for a width of 1.75 ns). The main limitations lie in the consumption (29.7 mW @ 36 MHz) and the use of a discrete transformer for the positive and negative alternations of the elementary pulses.

Ref.	t (ns)	BW (GHz)	Vpp	Ec (pJ/P)	Ect (pJ/P)	Ep (pJ)	n	Pdc	Size (mm^2)	Techn.	Mod.	Integ.
0	0.38	7.2	0.7	5.7*	30	0.47	0.015	15 mW @ 500 MHz	nc	0.18 CMOS	OOK	No
0	0.38	7.2	0.92	0.74*	23.41	0.84	0.034	1.88 mW @ 77 MHz	0.78	0.18 CMOS	BPSK	No
0	0.36	6	0.6	26.4	202	0.32	0.002	20.24 mW @ 100 MHz	nc	0.13 CMOS	BPSK	No
0	0.53	4	0.22	68.4*	71.7	0.06	0.008	129 mW @ 1.8 GHz	2.83	0.09 CMOS	BPSK	SoC
0	1.75	1.4	1.24	52*	825	6.73	0.008	29.7mW @ 36 MHz	0.4	0.18 CMOS	BPSK	SoP

* Estimate ($Ec=Pdc.\tau$)

Table 3. Main characteristics of pulse synthesis generators.

1.4. Conclusions on the state of the art

This analysis of the state of the art highlights the major efforts that have been made to reduce pulse generator consumption, since the energy efficiency per pulse produced has gone from around 0.10 % to nearer 10 % in just a few years. In this context, baseband pulse filtering seems to have the greatest potential in terms of efficiency. It proves capable of generating pulses of large amplitude and of widths making it possible to address different bands, and particularly the broadest bands. However, "narrowband" (500 MHz) generation, particularly at higher frequencies, requires the use of a significant number of delays and logic functions in the combiner. This worsens consumption, as well as integration because of the balance needed for each path when designing the masks. For applications in the 500 MHz bands, the LC LO switching techniques yield the best results. However, the times response and the output buffers limit the pulse amplitude as well as efficiency, preventing these architectures from being able to address the highest bands. The use of a ring VCO (Sim et al., 2009) is an interesting example of convergence between these two techniques (pulse filtering and LO switching). Indeed, on the one hand the long delay lines needed for generating in the 500 MHz bands of the high band (> 6.5 GHz) seem destined to be replaced by switched ring VCOs, while on the other, using this type of function requires a shaping filter because of the high energy levels it generates in the lower bands. As far as pulse synthesis is concerned, this is currently slightly behind in terms of efficiency. The future of these techniques depends on the development of the technologies or on the needs of applications which may justify this increase in consumption that is inherent in pulse programming.

2. Analysis of the FCC and ECC standards

This section gives an analysis of the FCC and ECC standards using theoretical models, in order to evaluate the potential of UWB-IR systems in terms of range and data rate. In the case of switched signals, it appears that PSD increases as a function of the level of the pulse and as a function of the data rate. It is then possible to reduce the data rate in order to increase pulse amplitude (and hence detection) while maintaining a PSD that meets the standard. However, there is also a restriction on the peak value of the transmitted signal with the peak PSD limit, in order to restrain this practice. By analysing the average PSD (PSD_{av}) and peak PSD (PSD_{pk}) together we can evaluate the maximum amplitude value (g_{0max}) allowed for a given modulation and the associated data rate. This analysis is

performed in the case of linear modulations (OOK, BPSK, PAM) for which the transmit signal (s(t)) and its PSD ($S_{ss}(f)$) are expressed as:

$$s(t) = \sum_{k=0}^{K-1} q_k g\left(t - kT_k\right) \tag{4}$$

$$S_{ss}(f) = \frac{\sigma_q^2}{T_s}\left|G(f)\right|^2 + \frac{\mu_q^2}{T_s^2}\left|G(f)\right|^2 .W_{Fs}(f) \tag{5}$$

where q_k is a random sequence with mean value μ_q and variance σ_q, $g(t)$ is the pulse waveform, and $G(f)$ its Fourier transform. This analysis especially gives the potential of OOK and BPSK modulations in terms of detection and data rate in order to see which types of applications they are compatible with. Lastly, we assume here an ideal pulse with a spectrum defined by the FCC or ECC masks, in order to evaluate the maximum theoretical amplitude value and the associated data rate value.

2.1. Mean PSD

The mean PSD of a UWB signal is limited by the masks shown in Fig. 4

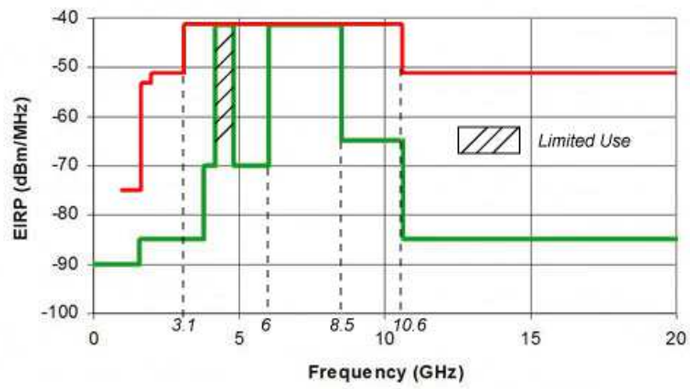


Fig. 4. FCC and ECC masks

If we ignore the power in the unallocated bands, the spectrum of the signal with the best spectral occupation is given by equation (3). It is a square function with a width (BW_{TOT}) defined by the allocated band, and which is centred on the middle of this band (f_0). Its inverse Fourier transform gives the ideal base pulse (equation 0).

$$G(f) = G_0\left[\Pi_{BW_{TOT}}\left(f - f_0\right) + \Pi_{BW_{TOT}}\left(f + f_0\right)\right] \tag{6}$$

$$g(t) = 2.G_0.BW_{TOT}.\mathrm{sinc}\left(\pi BW_{TOT}t\right).\cos(2\pi f_0 t) \tag{7}$$

with (for the FCC standard): BW_{TOT} = 7.5 GHz and f_0 = 6.85 GHz and (for the ECC standard): BW_{TOT} = 2.5 GHz and f_0 = 7.25 GHz. The peak amplitude of the ideal pulse is then given by:

$$g_0 = 2G_0 BW_{TOT} \tag{8}$$

The ECC and FCC standards require the use of a spectrum analyser whose resolution filter bandwidth (RBW_{av}) is set to 1 MHz. The measured PSD (single-sided) can then be expressed as follows, from 0:

$$DSP_{av}^{+}(f) = 2\frac{|G(f)|^2}{Z_0} D_s \left\{ RBW_{av}.\sigma_q^2 + D_s \mu_q^2 W_{FS} \right\} \tag{9}$$

For both standard, the maximum value of the average PSD is set to −41.3 dBm/MHz and can be expressed as follows:

$$DSP_{\max} = \max\left\{ \frac{2\sigma_q^2}{Z_0} D_s RBW_{av} G_0^2 ; \frac{2\mu_q^2}{Z_0} D_S^2 G_0^2 \right\} = 10^{-7.13} \tag{10}$$

Using 0 and 0, it is then possible to establish a relationship between the maximum amplitude allowed by the standard and the symbol rate as follow:

$$g_{0\max} = \min\left\{ \left(\frac{2BW_{TOT}^2 Z_0 .DSP_{\max}}{D_s RBW_{av} \sigma_q^2} \right)^{1/2}, \left(\frac{2BW_{TOT}^2 Z_0 .DSP_{\max}}{D_s^2 \mu_q^2} \right)^{1/2} \right\} \tag{11}$$

In Fig. 6, g_{0max} is represented as a function of D_s for OOK and BPSK modulation. However, it appears that if we consider only the limit imposed by the mean PSD, the maximum magnitude allowed value for data rates of the order of 10 kbs^{-1} exceeds 100 V. It is then necessary to evaluate the peak PSD.

2.2. Peak PSD

The ECC and FCC standards limit the peak power as follows. The peak PSD of the transmitted signal must be measured using a spectrum analyser in "peak detection" mode and in a 50 MHz resolution bandwidth (RWB_{pk}). At the frequency where the mean PSD is maximum, the peak PSD must not exceed 0 dBm. This measurement can be interpreted in the following way: the peak power of an elementary pulse filtered by an ideal 50 MHz bandpass filter centred on f_0 must not exceed 0 dBm. This interpretation is only valid where the symbol data rate is less than the spectrum analyser's RBW. Above this limit, the filter does not have the time to respond and the peak detector measures the power of the filter response to several pulses. However, it is at lower data rates (< 50 MHz) that this measurement is most meaningful, and this area of validity is sufficient for estimating the maximum allowed pulse magnitude.

Since the spectrum of the ideal pulse defined above is flat, the spectrum of the pulse filtered by the resolution filter (assumed to be ideal) together with its inverse Fourier transform can be expressed as follows:

$$G_{pk}(f) = G_0\left[\Pi_{RBW_{pk}}\left(f - f_0\right) + \Pi_{RBW_{pk}}\left(f + f_0\right)\right] \tag{12}$$

$$g_{pk}(t) = 2G_0.RBW_{pk}.\mathrm{sinc}\left(\pi RBW_{pk}t\right).\cos(2\pi f_0 t) \tag{13}$$

From 0, the peak power of the resolution filter output signal (which is the image of the peak PSD defined by the standard) can be expressed with G_0 as follow:

$$P_{pk} = \frac{4.G_0^2.RBW_{pk}^2}{Z_0} = DSP_{pk} \text{ for Ds < 50 MHz} \tag{14}$$

This interpretation of the evaluation of the peak PSD is validated by the measurements given in Fig. 5. Here, the peak PSD obtained from (11) is compared to the measurement, performed under the conditions imposed by the FCC standard, of an OOK sequence using RZ (Return to Zero) pulses of width τ = 1 ns and amplitude A = 1 V. Let us note that the standard allows this measurement to be performed using an RBW lower than 50 MHz (but necessarily greater than 1 MHz). In this case, the measurement must be corrected by a factor equal to 20 log (RBW/50 MHz).

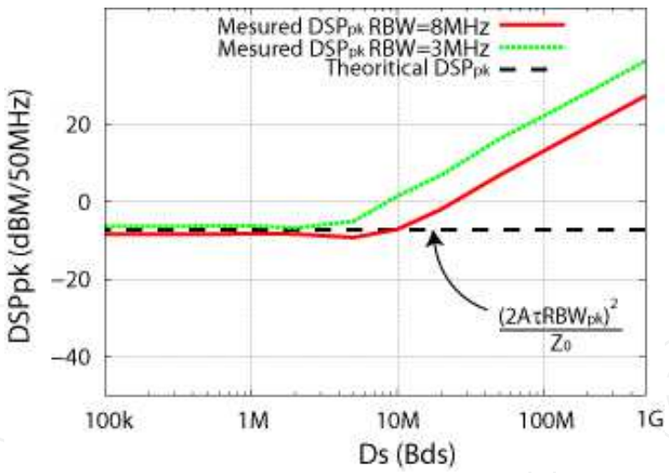


Fig. 5. Comparison of the model of the peak PSD and its measurement for OOK modulation using RZ pulses with an amplitude of A=1 V and a width of τ=1 ns.

From 0 and (11), the peak PSD can be expressed as a function of D_s in the case where the pulse amplitudhe is adjusted to achieve the maximum allowed PSD ($g_0 = g_{0max}$).

$$P_{pk} = \min\left\{\frac{2.DSP_{\max}.RBW_{pk}^2}{D_s\sigma_q^2.RBW_{av}}; \frac{2.DSP_{\max}.RBW_{pk}^2}{D_s^2\mu_q^2}\right\} \tag{15}$$

2.3. Interpretation

Fig. 6 and Fig. 7 (for the FCC and ECC standards respectively) show the maximum value of the ideal emitted pulse (g_{0max}) given by 0 and the peak PSD (P_{pk}) given by 0 in the case where the value of the mean PSD is the maximum allowed by the standards ($DSP_{max} = 10^{-7.13}$). OOK and BPSK modulations are being considered here to compare their potential for low-cost applications.

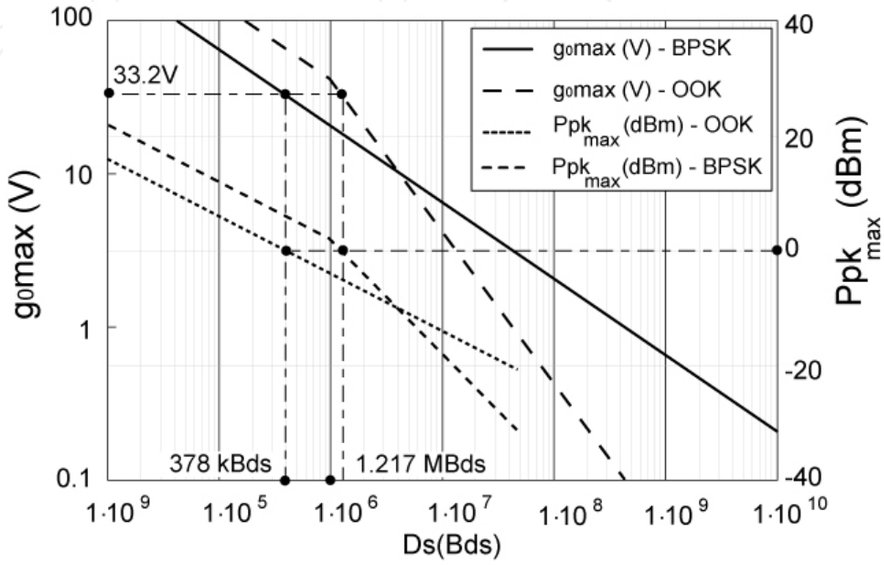


Fig. 6. Maximum value of the transmitted pulse (g_{0max}) and peak PSD (P_{pk}) as a function of the data rate (Ds) for $PSDav_{max} = 10^{-7.13}$ in the case of the FCC standard.

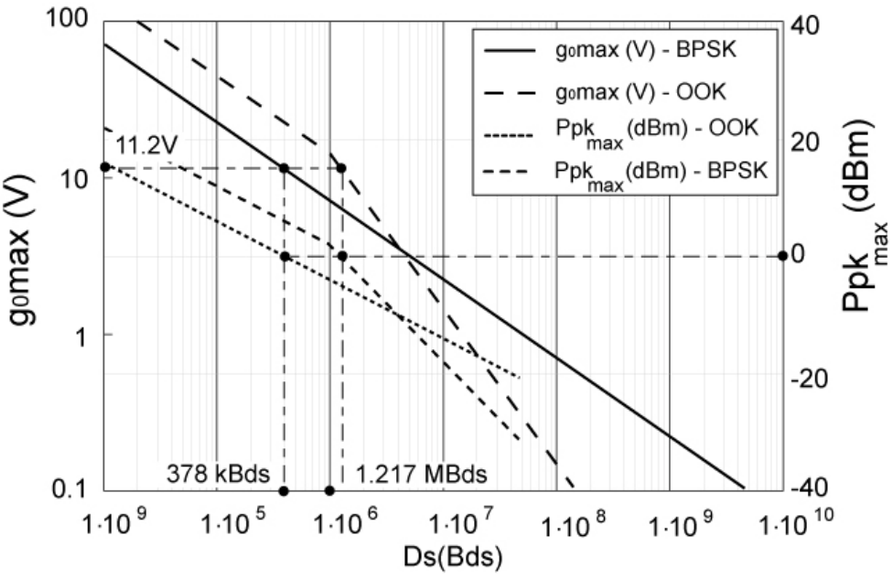


Fig. 7. Maximum value of the transmitted pulse (g_{0max}) and peak PSD (P_{pk}) as a function of the data rate (Ds) for $PSDav_{max} = 10^{-7.13}$ in the case of the ECC standard.

Looking at $g_{0max}(D_s)$, the discontinuous spectrum limit in the case of OOK modulation appears clearly for data rates greater than RBW_{av}. In fact, for data rates above 4 Mbs^{-1}, BPSK modulation has greater potential. However, it is possible to generate pulses greater than 1 V in OOK u to 40 Mbs^{-1} for the FCC standard and 14 Mbs^{-1} for ECC For data rates below 4 Mbs^{-1}, OOK modulation has greater potential than BPSK, because of the different variance. Let us note, moreover, that the values permitted by the FCC standard are higher than those of the ECC standard, since as the band is wider, the pulse energy is lower.
Observing the peak PSD shows that it is possible to reduce the data rate in order to increase the amplitude of the pulse up to 1.217 Mbs^{-1} in OOK and 378 kbs^{-1} in BPSK. Beyond these values, it is no longer possible to increase the amplitude by reducing Ds due to the peak power limitation. For these limit values, the pulse amplitude is 33.2 V in FCC and 11.2 V in ECC. In the case of 500MHz bandwidth signals, this value drop to 2V. Here again, OOK modulation has the greater potential.
In conclusion, it is preferable to choose OOK modulation when the intended data rates are lower than 4Mbs^{-1} and BPSK when data rates are above 40 Mbs^{-1} in FCC and 14 Mbs^{-1} in ECC. The choice between the two may be influenced by the application needs and technical constraints. In an integrated circuit context where it is difficult to generate pulse amplitudes exceeding 1 V, OOK modulation is sufficient to achieve such a level up to 40 Mbs^{-1} (or 14 Mbs^{-1} in ECC). If application requirements in terms of detection (range) or data rate is more stringent so demand, BPSK modulation may be considered, at the expense of increased complexity.

3. Designing an FCC generator using elementary pulse filtering

The technique described here has been used in various works (Bourdel et al., 2009) (Bourdel et al. 2010) (Bachelet et al., 2006) and performs the best results in terms of amplitude and energy per pulse for frequency bandwidth above a few GHz. The principle of this technique is that given in Fig. 2. It is applied for the whole FCC band for an application requiring a data rate of 36 Mbs^{-1} and an amplitude $g_0 > 1$ V.

3.1. Sizing

The first step in the design of the device shown in Fig. 2 consists in sizing the transmit filter. Several combinations of filters (h(t)) and baseband pulses (e(t)) can meet the FCC mask. In the case where e(t) is modelled by a square function ($\pi_\tau(t)$) of width τ and amplitude A, g(t) and its Fourier transform are:

$$g(t) = \frac{A}{\sqrt{l}}.\pi_\tau(t) * h_e(t) \tag{16}$$

$$G(f) = \frac{A\tau \mathrm{sinc}(\pi\tau f).H_e(f)}{\sqrt{l}} \tag{17}$$

where h(t) is the ideal pulse response of the filter, and *l* the power losses.
Fig. 8 shows the spectrum, evaluated from 0, of four pulses defined for different *h(t)* and different τ. Because of its very broad nature, the FCC mask can be satisfied using low-order

filters, which is a major advantage for monolithic design in CMOS technology, where inductances have substantial losses.
Of all these different pulses, *pulse 2* (Fig. 8b) exhibits the best compromise. First of all, it has good voltage efficiency (α), which represents the ratio between the amplitude (A) of the drive pulse (e(t)) and the amplitude (g_0) of the filter output pulse (g(t)). Furthermore, the value of τ is higher, which relaxes the constraints on the baseband generator. Lastly, the component values needed to produce it (Table 4) are compatible with the intended technology.

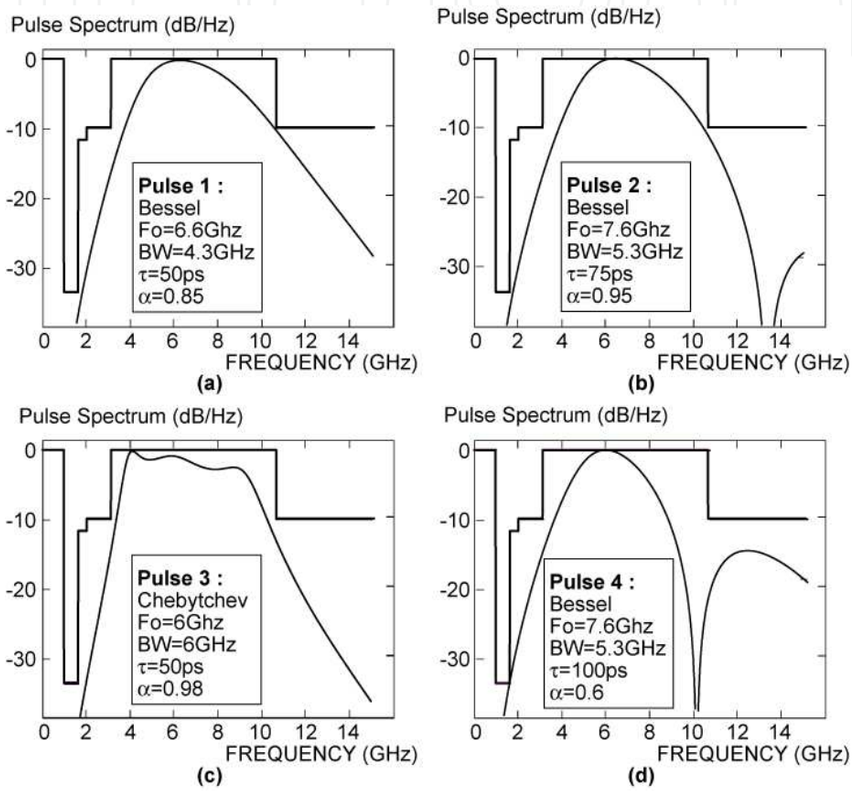


Fig. 8. Normalized spectral density ($|G(f)|^2/G_0$) for different 3rd-order filters and different pulse widths.

The Fig. 6 shows that it is theoretically allowed to generate pulses exceeding 1 V magnitude with a data rate of 36Mbs^{-1} when using OOK modulation. For the case study presented here, the same analysis as presented in section 2 can be performed with a pulse g(t) given by 0 instead of 0 (Bourdel et al., 2010). From this analysis, a more accurate specification for the generator characteristics can then be deduced. In the case of *pulse 2*, we then have g_0 = 1.73 V. 0 enables us then to evaluate the amplitude of e(t): A = 2.56 V.

3.2. Design

The architecture of the circuit presented is given in Fig. 9. The generator consists of a digital edge combiner (also referred to as a triangular pulse generator) producing the baseband

pulse, a driver, and an integrated filter. The filter is driven in current mode in order to provide an amplitude (A) at its input greater than the supply voltage (V_{DD} = 1.2V).

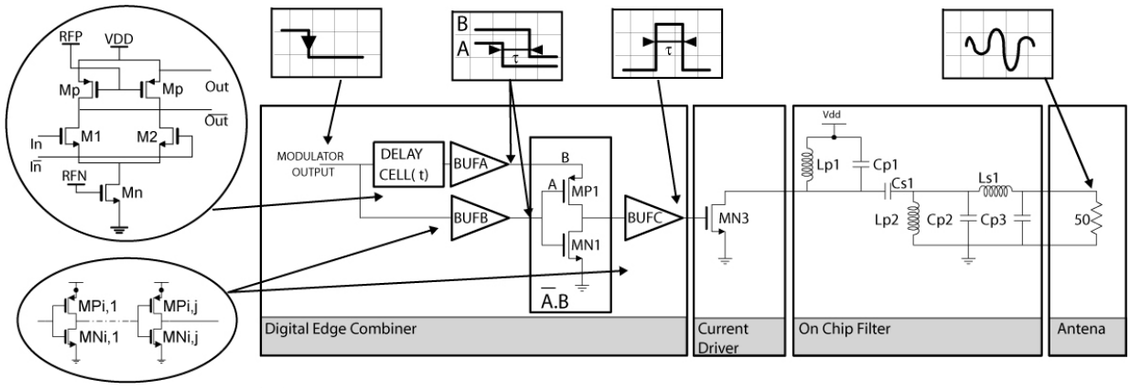


Fig. 9. Architecture of the FCC generator.

The design of the integrated filter is highly determined by the performances of the passive circuits available in the technology, especially the inductors. A preliminary study must be achieved to evaluate these performances. Inductor losses and self-resonance frequencies (srf) are actually heavily dependent on the inductor value (L). In the technology used in this design (0.13 μm CMOS), best performance is achieved by inductors with 0.4nH<L<1.5 nH. For these values, the Q remains greater than 10 over the whole FCC band and the srf remains above 15 GHz. The capacitors exhibit better RF performance, as the range of values that ensure proper operation (Q > 50 and srf > 24 GHz) is from 100 fF to 2 pF. However, for higher values, a significant discrepancy between the nominal value and the value at 7 GHz is noted (10 % for 2 pF) and will need to be taken into account during the design.
The narrow range of possible inductor values imposes the major restriction on the choice of filter. Very fortunately, the relative bandwidth of the FCC band is close to unity, which limits the spread of component values. For any one filter, several topologies are possible, and the choice is determined by the value of the components they require. The topology chosen here (which is not a classic ladder filter topology) gives the component values given in Table 4.

Lp1 (nH)	Cp1 (pF) (ideal)	Cp1 (pF) (Real)	Cs1 (fF)	Ls1 (nH)	Lp2 (nH)	Cp2 (fF)	C3 (fF)
460	1.43	0.5	677	1.15	1.08	420	260

Table 4. Component values for the integrated filter.

From the filter values it is then possible to size the current driver (MN3). The size of the transistor depends on A and the filter's input impedance R_{in}, for which this filter topology is the same as R_{out} = 50 Ω (antenna impedance). As the baseband pulse (0–V_{DD}) is applied to the gate of MN3, the current supplied to the filter by the transistor during the conduction time (τ) can be approximated according to the small signal theory. The size of the transistor can then be expressed as follows:

$$W = \frac{L.A_{\max}}{R_{IN}.\mu_0.C_{ox}\left(V_{DD} - V_t\right)^2} \tag{18}$$

The current needed to drive 2.56 V into 50 Ω is I_0 = 51 mA, leading to a very large transistor. For such a transistor, the output impedance (R_{ds} and C_{ds} shown in Fig. 10) must be matched to the filter.

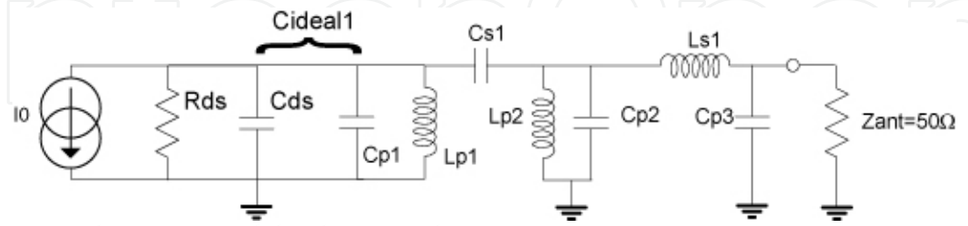


Fig. 10. Equivalent circuit of the driver and transistor.

Due to the high capacitance value in the first resonator, the effect of C_{ds} can easily be compensated for with C_{p1}. However, using such a simple topology, power matching (R_{ds}=R_{in}) cannot be achieved independently of the value of I_0. The size of the transistor then becomes a compromise between the value of I_0, the matching (R_{ds}), and the driver consumption (size of MN3), which is the highest in the circuit. The size finally adopted (W = 100 μm) provides a current of 58 mA (close to A_{max}/R_{out}) leading to an output of g_0 = 1.73 V. The value of R_{ds} is 122 Ω. Better matching would have been obtained with a larger transistor, at the expense of an increased consumption.

The edge combiner's delay cells are made using mode current differential logic (MCDL) as shown in Fig. 9. The main interest of this logic is its speed, together with its low dynamic consumption. The delays can be varied by applying a control voltage to the gates of the P transistor, thereby modifying their dynamic resistance. Each cell produces a delay that can vary from 17 ps to 300 ps, thereby making it possible to compensate for variations in the manufacturing process and achieve the desired value of τ. The edge combination is performed in a logic cell ($A.\overline{B}$) using only two transistor, in this way making it possible to generate pulses of up to 50 ps. Lastly, buffers are needed to match the sizes of the transistors between the logic circuits, which use smaller transistors, and the driver. In order not to place all the constraint on buffer C, an initial series of buffers (buffers A and B) are placed between the delays and the logic function.

3.3. Results

The main measurement results are given in Fig. 11. The circuit (shown in Fig. 11a) occupies 0.54 mm². Pulse amplitude is 1.4 V_{pp} with a 1.2 V supply as presented in Fig. 11b and the spectrum of the generated pulses is FCC compliant as shown in Fig. 11c. Moreover, the FCC mask is satisfied for a 36 Mbs^{-1} data rate (Fig. 11d). The mean consumption is 3.8 mA @ 100 MHz. The energy consumed per pulse is estimated at 9 pJ, especially due to the driver (MN3), which operates in C class. However, this performance can only be achieved if power management is used, as this estimation does not take DC consumption

between two pulses into account. Indeed, like most of previous published works present in the literature, this generator dissipates DC power, making the total energy consumed per pulse (Ec_t) dependent on the data rate.

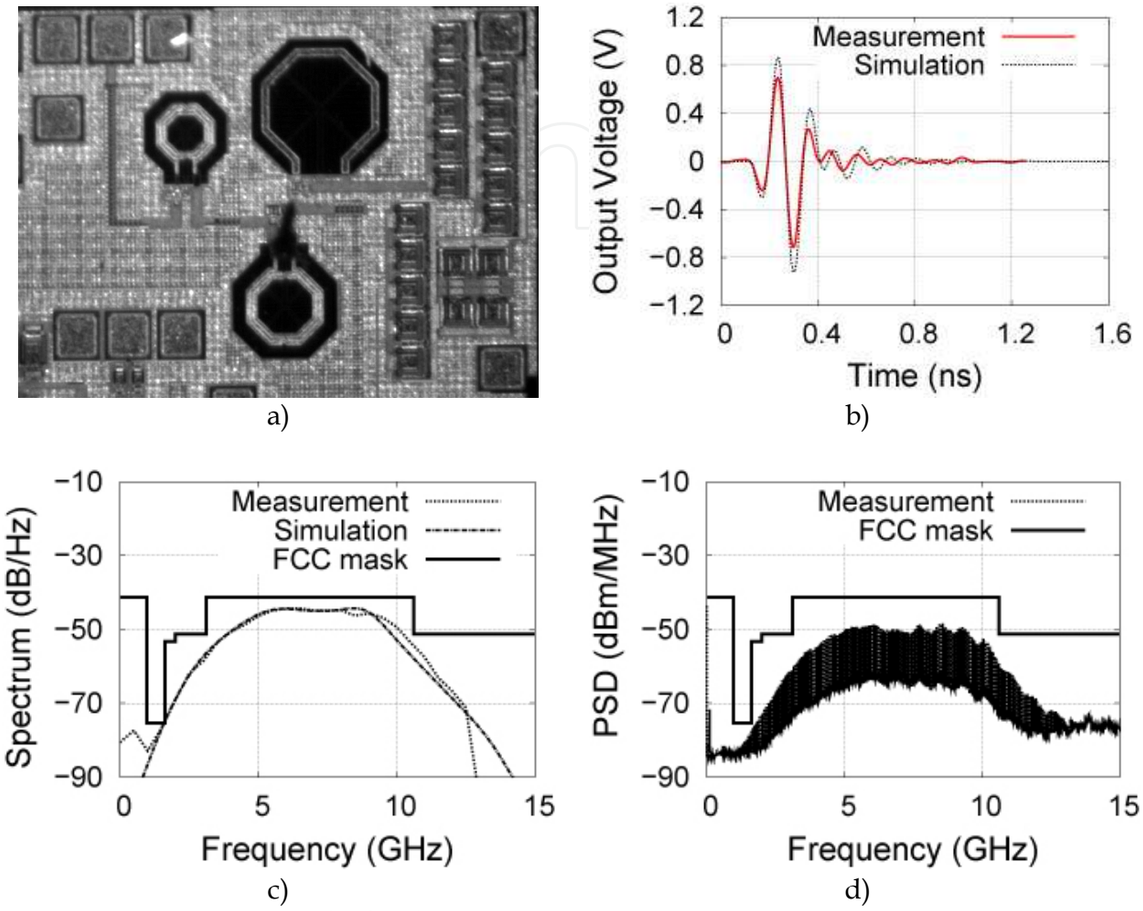


Fig. 11. Measurement results for the FCC generator.

4. Designing a pulse synthesizer for the FCC band

4.1. Principle

The principle of the pulse synthesizer is shown in Fig. 12. It uses the elementary pulse combination method presented in section 1.3. With this technique different pulse shapes can be synthesized using a single generator, in particular to compensate for PVT variations. The study presented here demonstrates the effectiveness of this technique in terms of programming and integration. The synthesizer is dimensioned to enable generation of the 5th derivative of a Gaussian pulse, together with the impulse responses of a Bessel filter presented in Fig. 3. In order to achieve this, the generator must include six stages in order to generate the six elementary pulses shown in Fig. 3**Error! Reference source not found.**.

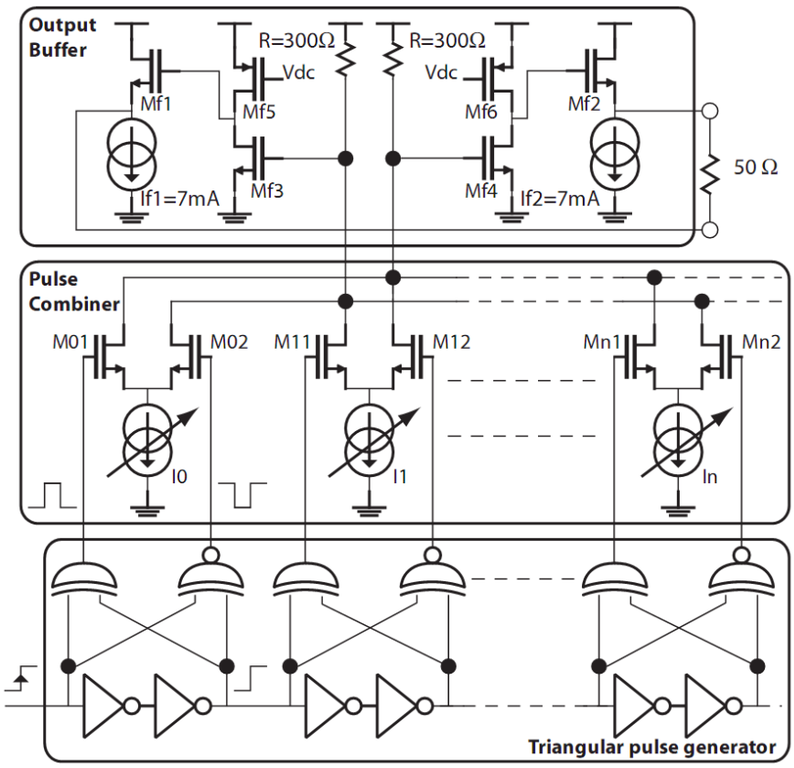
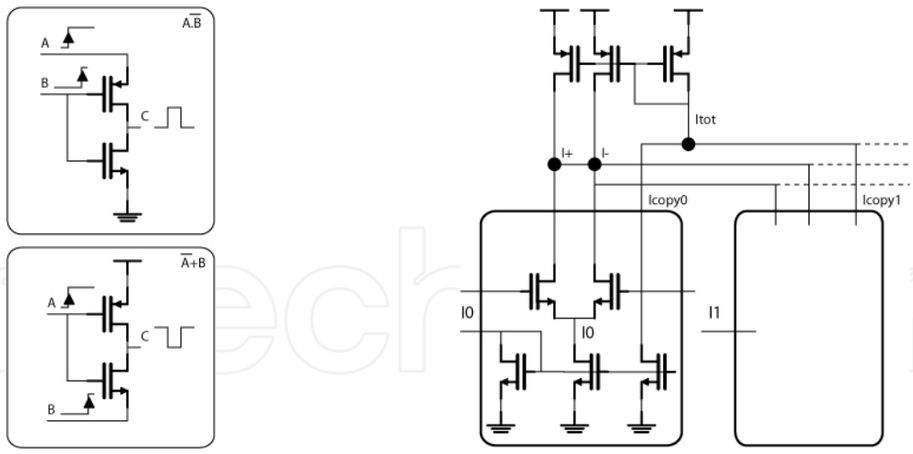


Fig. 12. Principle of combination using cross-connected differential pairs.

One of the main difficulties in pulse combination lies in the need to alternate the polarity of successive elementary pulses. The use of cross-connected differential pairs resolves this issue. Current summing is achieved into a load and each output is alternately cross-connected with the next in order to achieve the polarity alternation. The bias current (I_n) in each pair then sets the absolute value of g_n.

4.2. Design

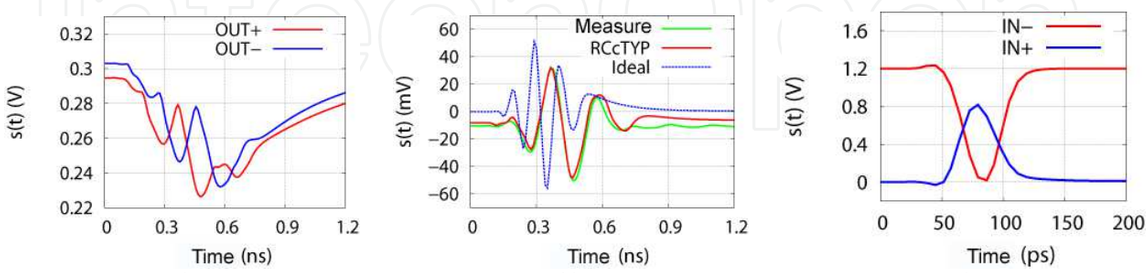
The use of differential pairs implies the use of a differential elementary pulse. In principle, this necessity does not prevent the use of a logic combiner. However, this introduces an asymmetry into the combiner, which has to use complementary logic functions to produce the positive pulse and its complement. Given that the width needed for a Gaussian pulse (τ_n = 75 ps) is close to the minimum achievable in the considered technology (0.13 µm CMOS), this asymmetry (represented in Fig. 14c) will lead to an imperfection in the driving of the differential pairs and the generation of a common mode. The delay cells used in the combiner are the ones given in Fig. 9 of the section 3. The complementary logic functions (shown in Fig. 13a) are ($A.\overline{B}$) and ($\overline{A}+B$) because these can be achieved using only two transistors, involving high speed performances.



a) b)

Fig. 13. Generating the elementary pulse and its complement (a), current mirroring (b).

Moreover, driving a high-amplitude signal into the 50 Ω load imposed by the antenna constitutes one of the main constraints of this design. Indeed, insofar the use of inductors must be avoided to optimize integration, the gain-bandwidth product of the active cells that can be achieved in 0.13 µm CMOS technology considerably limits the amplitude of the transmitted pulse. In fact, the size of the transistors needed to drive such a load imposes cut-off frequencies well below 10 GHz. Several solutions have been implemented to mitigate this problem. First of all, the differential structure imposed by the combination structure is maintained right up to the antenna, thereby making it possible to double the output voltage. Common-mode rejection can be problem in a differential structure, however here, the distortion introduced by this common mode can be compensated for by the value of the g_n co-efficients. In our case, the time constant for establishing this common mode, represented Fig.14a, is much slower than the elementary pulse, which leads to stretching of the final pulse s(t). This stretching can be cancelled out by adding an extra stage with a gain inverse to the common-mode value observed at the end of the pulse. The comparison of the current values I_n with the normalized value of g_n (given in Table 5) highlights this common-mode compensation. This specific feature demonstrates this structure's ability to compensate for distortions.



a) b) c)

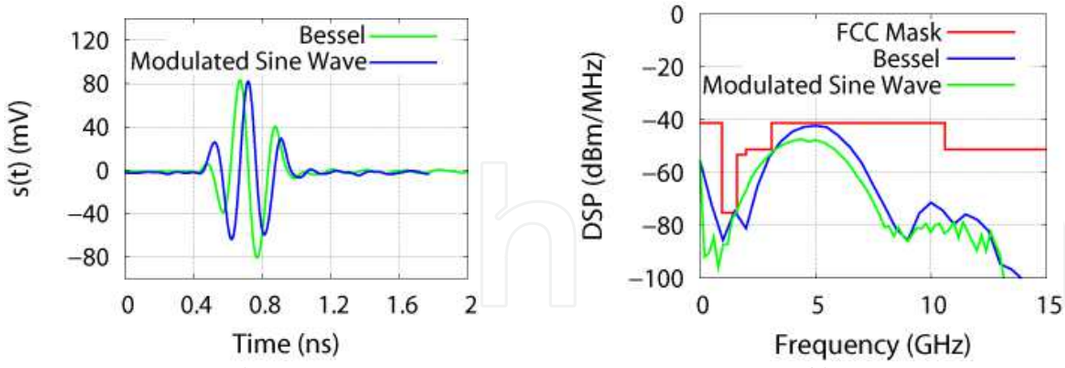
Fig. 14. ("post-layout") simulation of the single (a) and differential (b) output pulses and the drive (c).

N	0	1	2	3	4	5	6
g_n	0.06	−0.43	1	−1	0.43	−0.06	0
I_n (mA)	0.005	0.82	2.2	3.4	2.28	0.63	0.1

Table 5. Comparison of g_n and I_n values for the 5th derivative of a Gaussian pulse.

The differential pairs are combined into an active load biased by the mirroring of the I_n currents (shown in Fig.13b) making it possible to ensure a constant output stage gate voltage (Mf3 and Mf4), regardless of the values of g_n required to produce the pulse. The differential pair transistors are dimensioned to ensure the maximum gain into a high-impedance load, leading to a small size (3 µm).
The output stage allows matching to the antenna. Several circuit arrangements have been envisaged. The voltage follower (SF) used in (Bourdel et al., 2007) was ultimately replaced by a common source (CS) circuit with a resistive load. Indeed, even though the SF circuit offers an output impedance of $r_0 = 1/g_m$ over a very wide bandwidth (allowing it to perform "active" matching, coupling it to the CS buffering circuit (Mf3/Mf5 and Mf4/Mf6) leads to a total gain (CS plus SF) of significantly less than unity (Razavi, 2001). Furthermore, the DC current required by the output stage (7 mA) to achieve $1/g_m$ close to 50 Ω degrades the consumption performance.

Lastly, the measurements of this structure, given in Fig. 15, show an amplitude of 160 mV_{pp} (200 mV_{pp} allowing for the 2 dB loss in the measuring cable) for pulses meeting the FCC mask. These voltage levels are obtained using a modest technology (0.13 µm CMOS), without the use of inductors, and for signals with a 10 dB bandwidth of 3.5 GHz, which constitutes a good performance. However, these levels are still low and do not make it possible to achieve the ranges necessary for the intended applications. Hence other structures need to be studied in order to get over this limit.



a) b)

Fig. 15. Measurement of the various elementary pulses a) and their spectrum b).

The circuit's total consumption is 38.4 mW @ 100 MHz, while the consumption per pulse during the pulse time (achievable assuming the use of power management) is 72 pJ. This performance is lower than that of the non-programmable structure. However the area occupied is very small (0.06 mm^2) as no inductors are used and the programming ability offers the possibility of compensating for PVT variations or transmission distortion. This shows the great potential of this approach if the consumption bottleneck is overcame.

5. Conclusion

In this chapter, several aspects relating to the generation of UWB pulse signals have been addressed. The bibliographic study presented at the beginning of this chapter shows the advantages and limitations of the various techniques that are mainly being used. It also shows the significant effort put in to reducing the consumption of the generators and their great potential in terms of power saving, but also the limitations imposed by the technologies on the pulse amplitude and programming.

The standards appear to have a considerable effect on transmitter design. They have a high incidence not only on the spectrum of the transmitted pulse, but also on the modulation, the data rate, and the amplitude of the transmitted signal. Especially, understanding the relationship between the data rate and pulse amplitude enables the designer to best select the modulation required for an application, as well as to best size the generator.

Substantial research effort has recently been devoted to optimizing consumption and pulse amplitude in order to meet the requirements of low-cost and low-power applications. In this context, the generation technique based on exciting an integrated filter shows a great deal of potential. This technique makes it possible to produce pulse generators with the lowest dynamic consumption quoted in the literature to date for output amplitudes over 1 V, also giving them the best dynamic efficiency (Bourdel et al., 2009) (Bourdel et al., 2010).

In the field of programmable generators, research efforts have recently been begun with the aim of producing generators able to generate different pulse shapes, at high amplitudes, and occupying a limited area of silicon. Pulse programming needs to make it possible to address several frequency bands, as well as to compensate for PVT variations. An initial study based on pulse synthesis shows the feasibility making fully-programmable generator that consumes very small silicon area.

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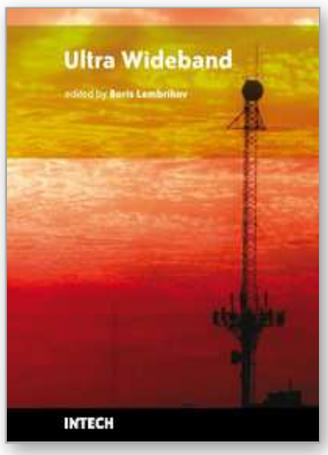

Ultra Wideband

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Ultra wideband technology is one of the most promising directions in the rapidly developing modern communications. Ultra wideband communication system applications include radars, wireless personal area networks, sensor networks, imaging systems and high precision positioning systems. Ultra wideband transmission is characterized by high data rate, availability of low-cost transceivers, low transmit power and low interference. The proposed book consisting of 19 chapters presents both the state-of-the-art and the latest achievements in ultra wideband communication system performance, design and components. The book is addressed to engineers and researchers who are interested in the wide range of topics related to ultra wideband communications.

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