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# Carrier storage in Ge nanocrystals grown on silicon oxide by a two step dewetting / nucleation process

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## 1. Introduction

In microelectronics, dimensionality miniaturization theoretically leads to reliability increase. However, an important concern in silicon technology is the effective reliability of MOS (metal-oxide semiconductor) devices such as MOSFETs (MOS field-effect transistors) and memory cells as they are scaled to smaller dimensions. Indeed, as the silicon dioxide ( $\text{SiO}_2$ ) in CMOS technology is thinned below 2 nm for higher density and performance, limitations associated with the poly-silicon gate become increasingly important. These limitations include increasing poly-depletion effects, high gate resistance, doping impurity penetration,...As a consequence, some problems affecting the CMOS devices reliability appear. Among the main problems, the exponentially increased gate leakage current, the reduced threshold for dielectric breakdown and oxide charging which results in voltage shifts. To avoid these difficulties, group IV nanocrystals embedded in a  $\text{SiO}_2$  matrix have been studied extensively because of their potential for integrated optoelectronic devices on silicon substrates. The use of silicon (Si) nanocrystals (NCs) instead of standard polycrystalline silicon floating gate was proposed and many studies have been made describing the NC capabilities in different devices (Tiwari et al., 1995; Park et al., 2003; Conibeer et al., 2006). However, due to their large bandgap variations and their potential for bringing a strong quantum confinement, germanium NCs have attracted more interest than Si-NCs as reported in many studies (Choi et al., 1999; Skorupa et al., 2003; Chatterjee et al., 2008).

For non-volatile memory device application, a long charge retention time at room temperature is the most important. This is the reason why the study of the NC specific properties is of principal importance. Indeed, device reliabilities are strongly affected by the variation of the NC structural parameters; namely, their density, their size, and consequently the NC spacing. The NC spacing controls the energetic potential recovery of the NCs and promotes the carrier hopping between them. Some of these effects cannot be evaluated by the standard techniques, because the evolution of the curves contains a global

response; all the NCs are involved in the transport and storage, so one obtains just average information which is affected by the NC size fluctuation and density.

It is interesting to obtain information on an isolated NC (or a limited number of NCs) in a given structure to optimize the device functionalities. Indeed, electric transport through NCs and carrier storage in NCs depend on the NC structural properties. It appears that the use of the atomic force microscopy (AFM) is very appropriate if the properties of individual NCs or quantum dots (QDs) are to be exploited with nm-scale resolution (Okada et al., 2002; Stomp et al., 2005; Smaali et al., 2006, Smaali et al., 2010, Gacem et al., 2010). So, in this work, we present two kinds of results; results obtained with standard methods in which one brings average information, and results obtained by use of the C-AFM technique. The standard techniques consist of the use of high frequency (1 MHz) capacitance - voltage (*HFC-V*) and current - voltage (*I-V*) methods usually applied in microelectronic industry. Note that the kind of carriers involved in the electric transport and the charge storage depends on the nature of the electrode/sample contacts. With the standard methods, for which a metallic contact is used, electrons are concerned. However, conduction by holes dominates when working with a conductive AFM using a *p*-doped diamond probe, which leads to formation of an artificial nano-heterojunction at the contact with a large conduction band discontinuity. Obviously, if the C-AFM probe was a metallic probe (*Pt-Ir, Cr-Co,...*), electric conduction could be governed by electrons. Indeed, in a recent study, we studied the carrier transport through quantum dots by the C-AFM technique using two kinds of conductive AFM probes (*p*-doped diamond and metallic probes), and showed that the type of the carriers flowing through the nanostructure depended on the used AFM probe (Smaali et al. 2010).

*HFC-V* and *I-V* were used to study the carrier storage capabilities of the Ge-NCs in a large temperature range [77 - 300K]. For these techniques, the studied sample is similar to a MOS (metal - oxide - silicon) capacitor. This work allowed us to study not only the carrier transport and storage but also to evidence at room temperature a Coulomb blockade effect for nanocrystals of 3.5 nm average diameter. The latter appears for increasingly low voltages when the temperature decreases.

The C-AFM method was used to study carrier storage in a single NC in vacuum and at room temperature. With this technique, electric images of NCs of any arbitrary positions on the sample surface can be studied using the same conductive AFM probe. However, this technique requires that the NCs are not capped with an additional thick layer. In our case, the studied samples were elaborated in the same conditions than those used for standard techniques but without layer covering the NCs. The C-AFM brought interesting information on the NCs, especially on conduction characteristics and carrier storage. This study was performed with a home made AFM working inside a scanning electron microscope (SEM) (Troyon et al., 1997).

## 2. Sample elaboration

The crystalline silicon substrate used to elaborate samples is (100) oriented, boron doped and thermally oxidized to ~ 5 nm thick. The amorphous germanium layer was deposited by Molecular Beam Epitaxy (MBE) in ultra-high vacuum ( $10^{-11}$  Torr) at room temperature. The Ge-NCs were formed after 30 min in situ annealing at 700°C by the combination of unwetting and crystallization processes (Karmous et al., 2006; Szkutnik et al., 2008). The

mean diameter ( $D$ ) of Ge-NCs is uniquely controlled by the nominal thickness ( $t$ ) of the amorphous layer following a relation  $D \propto t$ . The thickness was varied between 0.5 and 5 nm leading to NC mean diameters between 3.5 and  $\sim 34$  nm. For all samples, Ge-NCs present a unique aspect ratio (height over diameter) of about 0.8 which strongly differs from the aspect ratio (about 0.15) of Ge quantum dots in epitaxy on Si substrate (Berbezier et al., 2002).

In the present work, our samples are labelled *A* and *B*. For the *A* samples, the silicon substrate was boron doped to  $\sim 10^{15}$  cm<sup>-3</sup>, and a 18 nm thick amorphous silicon (a-Si) was deposited as a capping layer. The use of a-Si layer leads to an electrical conduction between one electrode and Ge-NCs for very weak biases. This situation could not be obtained if we had an insulating layer, as in memory devices, where the carrier exchange through the oxide makes damages and finally leads to an oxide breakdown. From an energetically point of view, the a-Si bandgap is higher than that of the Ge-NC, which reinforces the spatial confinement of the carriers in Ge-NCs, and at the same time remains small to have an electronic transport under biases as weak as those applied in this study. Weak biases avoid oxide damages in order to have reproducible measurements. In other words, it is not necessary to apply a high bias to the sample for characterization measurements. The samples of this series are labelled  $A_{3.5}$ ,  $A_{17}$ ,  $A_{21}$  and  $A_{35}$  and characterized by their average size and density (i.e., 3.5 nm and  $2.4 \times 10^{12}$  cm<sup>-2</sup> for  $A_{3.5}$ , 17 nm and  $1.5 \times 10^{11}$  cm<sup>-2</sup> for  $A_{17}$ , 21 nm and  $6.7 \times 10^{10}$  cm<sup>-2</sup> for  $A_{21}$ , 35 nm and  $2.4 \times 10^{10}$  cm<sup>-2</sup> for  $A_{35}$ ). Transmission electron microscopy (TEM) cross-section image shown in Fig. 1(a), gives a typical example of the stack layers for Ge-NCs with an average diameter of 3.5 nm. It can be clearly seen that Ge-NCs are monocrystalline ( $\{111\}$  plans are identified) and free of extended defects as shown in Fig. 1(b).

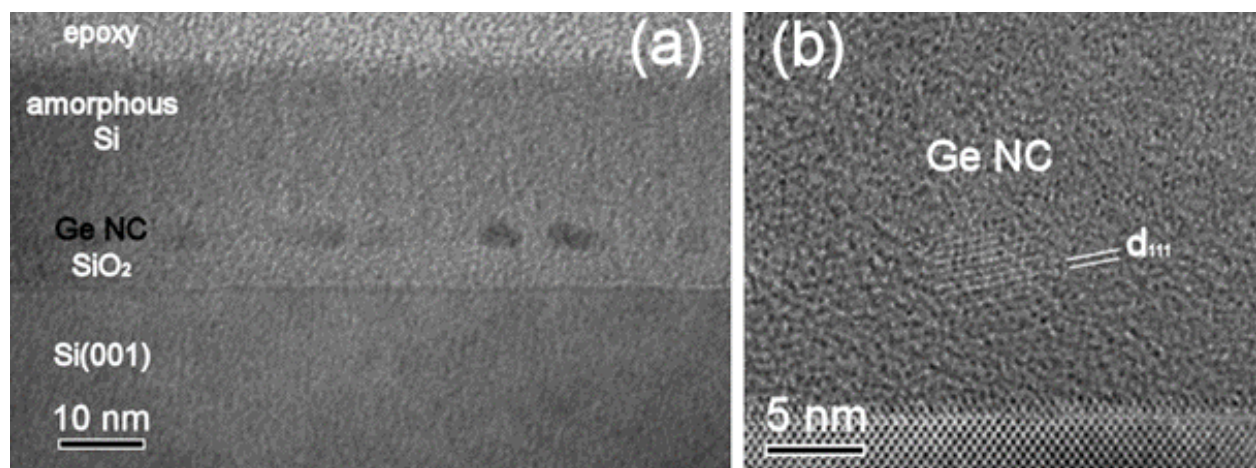


Fig. 1. (a) TEM image (cross sectional view) of Ge-NCs formed by annealing of an amorphous Ge layer (0.5 nm thickness) deposited on an ultrathin SiO<sub>2</sub> (5 nm thickness) for 30 min at 700 °C and capped by a 18 nm of amorphous silicon. (b) High resolution TEM image (cross sectional view) of a Ge-NC where the distance between  $\{111\}$  plans are evidenced (Szkutnik et al., 2008).

For the *B* sample, the silicon substrate was *n* doped to  $\sim 5 \times 10^{18}$  cm<sup>-3</sup> and the Ge-NCs were not capped in order to allow electrical AFM measurements. This sample contains  $6 \times 10^9$  Ge-NCs per cm<sup>2</sup> the average diameter of which is equal to 70 nm.

### 3. Experiments

#### 3.1 C-V and I-V techniques

For the study of the *A* samples, electrical contacts were made using silver bond on the two faces of each sample. The structure is similar to a MOS capacitor (see Fig. 2). The area of the silver bond electrode is approximately circular and its diameter is about 2 mm. *HFC-V* and *I-V* measurements are obtained by limiting the gate bias to relatively low values ( $\leq 3$  V) in order to prevent the silicon dioxide damaging and are carried out at various temperatures from 300 K down to 77 K. *I-V* measurements were made with a HP4140B picoammeter and *HFC-V* characteristics were performed with a HP4284A RLC-meter. We only focus here, on the *HFC-V* in order to have a direct response of the carrier exchange (trapping/detrapping) effect. The *HFC-V* measurements were made from inversion (positive gate bias) to accumulation (negative gate bias) regimes and immediately back to the inversion regime with the same voltage sweep rate. The carrier trapping/detrapping process was shown by the occurrence of the hysteresis cycle in the *C-V* curves.

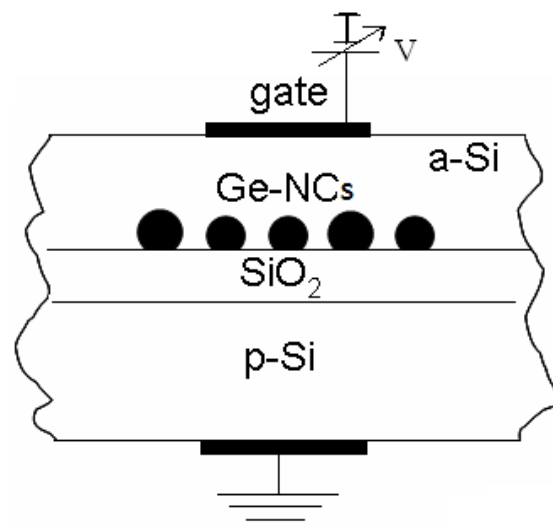


Fig. 2. A schematic cross section of the studied samples of the *A* series.  $V$  is the bias polarization: the structure is at inversion regime if  $V > 0$  and at accumulation regime if  $V < 0$ .

#### 3.2 Conductive-AFM/SEM technique

The sample *B* was studied by using a home-made AFM combined to a scanning electron microscope (SEM) (Troyon et al., 1997) equipped with a field emission gun (LEO Gemini). Our measurements were made with this AFM/SEM combined instrument because working inside the SEM allows one to get rid of the influence of the water layer covering the surface in ambient atmosphere which hinders the electric measurements. Indeed, working in wet atmosphere may create local oxidation of the surface at the tip/surface contact (Okada et al., 2001). Furthermore, this hybrid instrument allows obtaining three simultaneous images; electric, topographic and secondary electron images. For example, the secondary image shown in Fig. 3 allows the verification of the probe geometry and check the state of the probe and of the sample surface. Ge-NCs are well seen and are randomly distributed at the surface of the sample. Note that precise analysis of the Ge-NC structural (average size and

density) properties, the size distribution and the density have been previously studied and it was shown that the distribution of the NC size is very narrow (Szkutnik et al., 2008).

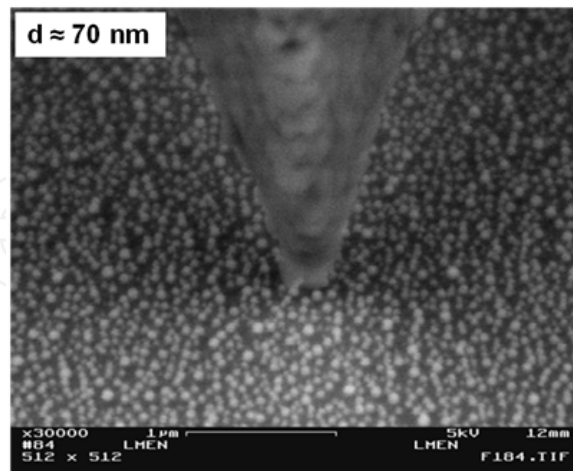
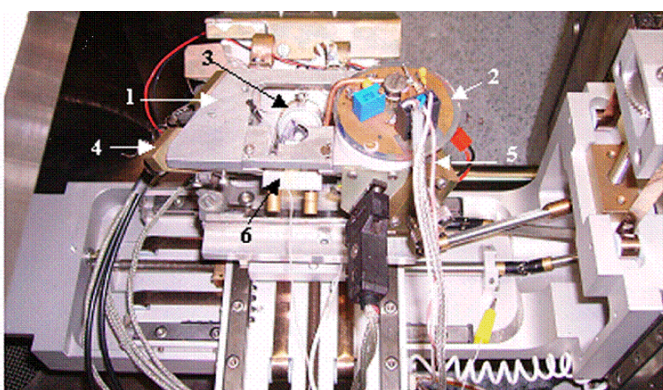


Fig. 3. Secondary electron image showing a *p*-doped diamond AFM tip in contact with Ge-NCs of 70 nm in diameter.

Another important reason to perform measurements inside the SEM is that this particular sample requires a preliminary electron beam irradiation in the condition for obtaining an electron beam induced current (EBIC) image to obtain afterwards (electron beam off) a measurable conduction current. Indeed, due to the thickness of the SiO<sub>2</sub> layer it was impossible to get a C-AFM image for polarization voltages smaller than  $\pm 8$  V. The reason why a preliminary electron beam irradiation is needed is explained in section 4.3.



- (1) AFM Head.
- (2) Preamplifier.
- (3) Piezo-tube supporting the sample.
- (4) Position of the laser diode.
- (5) Photodiode adjustment system.
- (6) AFM cantilever support.

Fig. 4. View of the AFM mounted inside the specimen chamber of the SEM.

Fig. 4 gives an image showing the various components of the AFM and Fig 5 gives a schematic representation of the hybrid system used in the present work. The detected current remains very low. So, we installed a low noise ( $\sim 5$  pA RMS, 1 MHz bandwidth) current/voltage amplifier ( $10^7$  gain) close to the AFM tip, inside the SEM, to limit the electric noise. An ohmic contact was made on the back side of the samples by depositing an aluminium layer. The sample surface (the top side) was probed in the contact mode while a sample bias  $V$  was applied to the substrate with respect to the tip, which is itself referenced to the ground through the preamplifier. In our system, the sample is scanned with respect to

the AFM probe. The electron-beam irradiation of the samples was performed in the conditions used for obtaining a nano-EBIC image with the e-beam focused in a fixed position just in front of the AFM probe and as close as possible to it (Smaali et al., 2008); the electron primary energy was 5 keV, the primary current was 1 nA, the sample bias was  $V = 0$  volt and the images (256×256 pixels) were acquired at a line scanning frequency of about 0.5 Hz.

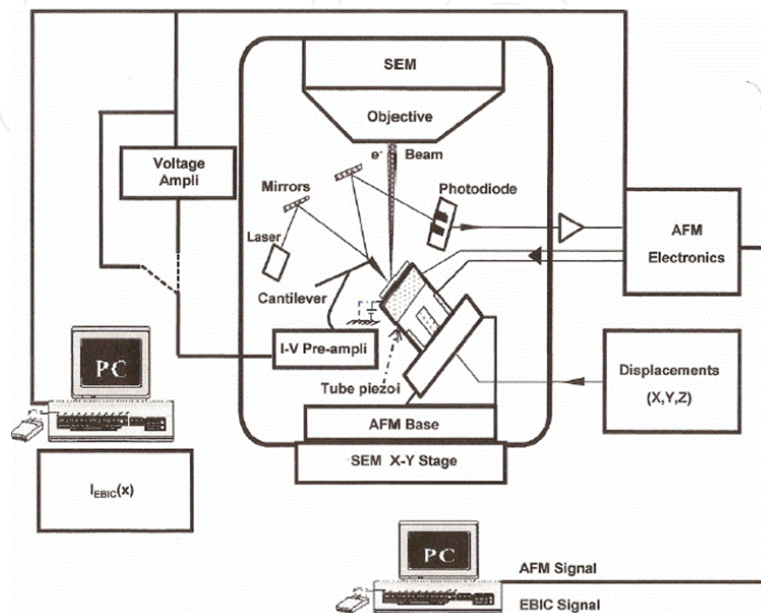


Fig. 5. Schematic representation of the experimental combined AFM/SEM set-up.

## 4. Results and discussion

### 4.1 Capacitance – voltage characteristics

*HFC-V* and *I-V* measurements cycling on *A* samples show the hysteresis loops representative of the carrier storage. The question is: where does the carrier storage occur? Does it appear in NCs and/or in the oxide bulk? To give an appropriate response, Fig. 6(a) shows typical *HFC-V* curves with arrows indicating the sense of the measurement. The same cycle is obtained whatever the beginning of the measurement direction from positive or negative gate bias. Note that the silicon substrate is *p*-doped. The *HFC-V* curves measured from positive to negative gate bias are shifted towards negative biases compared to the *HFC-V* curves measured in the opposite direction. This highlights the electron trapping/detrapping in Ge-NCs and clearly indicates that this process is either non-existent or negligible in oxide.

Let us describe the electron trapping process. In inversion regime (when the silicon substrate is negatively polarized), electrons in the substrate accumulate close to the Si/SiO<sub>2</sub> interface and holes (the majority carriers) move away from this interface towards silicon bulk. On the other side of the sample, the trapped electrons can be emitted from Ge-NCs to the gate via a-Si. Hence, the *HFC-V* curve is shifted to negative bias (this curve is taken as reference to calculate trapped charge due to *HFC-V* shift). If the bias is reversed, electrons can be injected in Ge-NCs and the *HFC-V* curve is moved to positive bias as shown by the arrows in Fig. 6(a). These electrons do not come from the substrate because of the electric

field orientation, but from the other side via the a-Si. The contribution of the current coming from electron trapping in a-Si layer, which is expected due to the presence of defects (such as dangling bond and vacancies), is not considered here since carrier emission and capture in these defects are very fast in comparison to the time measurement. Indeed, since the energy levels of the defects are close to the conduction and valence bands they produce very fast conduction paths for electrons and holes. Note that the electron trapping is enhanced at low temperature.

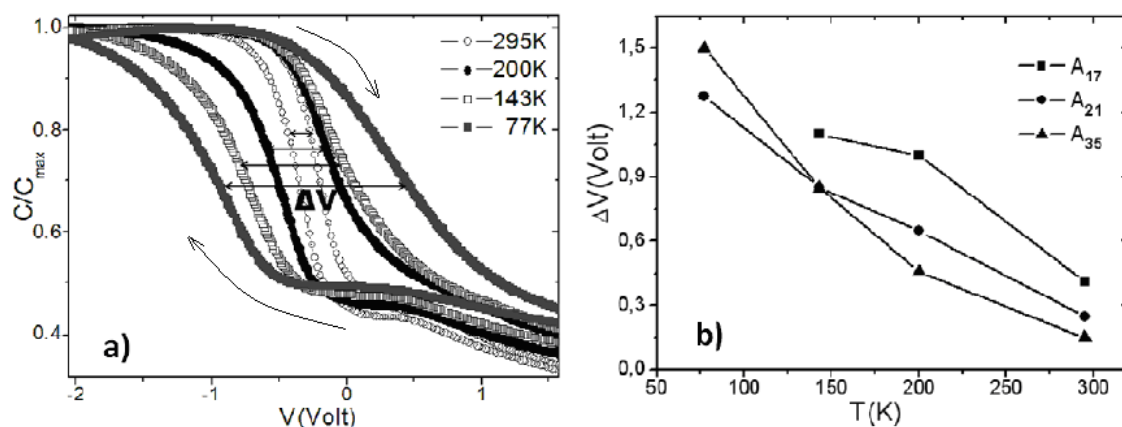


Fig. 6. (a) Electron storage in nanocrystals and its effects on the capacitance - voltage cycles, the temperature effect is also shown, (b) electron storage amplitude for three samples ( $A_{17}$ ,  $A_{21}$  and  $A_{35}$ ).

In Fig. 6(b), we present the hysteresis width ( $\Delta V$ ) deduced from the HFC-V cycles for three samples of the A series as a function of the temperature.  $\Delta V$  is reduced when the temperature increases and is also reduced for samples containing NCs with high average diameter as shown in Fig. 6(b). Note that  $\Delta V$  represents the global stored charge. The analytic expression of  $\Delta V$  is given by Tiwari et al. (Tiwari et al., 1995), which shows that  $\Delta V$  is directly related to the Ge-NC density, to the number of electrons stored by NC and to the NC mean diameter. Two main parameters control the  $\Delta V$  amount: the Ge-NC size and density, but their effects can be different. If the NC size controls the trapped charge density (represented by  $\Delta V$ ) the trapping process will be stronger in NCs with high average diameter. This seems true at low temperature ( $< 150$  K) as shown in Fig. 6(b); the total charge trapping is much more efficient in large Ge-NCs than in smaller ones. But at high temperature ( $> 150$  K), the Ge-NC density controls the stored charge amount. The temperature plays thus a particular role in Ge-NC size and density effects on the global stored charge.

As it has been quoted above, eventual carrier storage can occur in the oxide after flowing through the oxide interfaces barrier height. Nevertheless, this is screened by the effective charge stored in NCs. Finally, the carrier exchange is made between the Ge-NCs and the gate as quoted in Fig. 7 giving a schematic and qualitative situation for electron storage in NCs when the gate is negatively polarized by reference to the Si substrate (on the left of Fig 7) and NCs discharging when the bias polarization is inverted (on the right of Fig. 7).



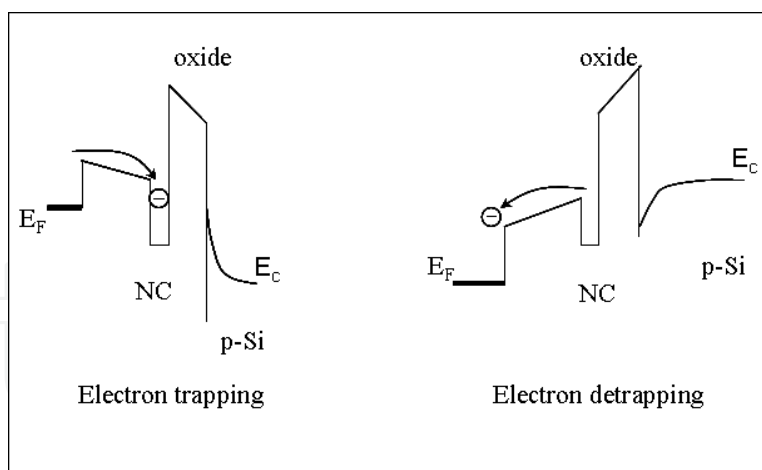


Fig. 7. Energetic band diagram showing carrier trapping in NCs and detrapping according to the bias polarization.

#### 4.2 Current – voltage characteristics

The carrier trapping phenomena are also observed in  $I$ - $V$  curves as shown in Fig. 8 where the measurements are performed from negative (-3 V) to positive (+3 V) and back to negative gate voltage. Note that the charge storage in standard MOS capacitors and its effects on the  $I$ - $V$  curves is well known (Balland & Barbottin, 1989; El Hdiy et al., 1993). The shift of the  $I$ - $V$  curve along the voltage axis is controlled by the type of the effective oxide charge; a positive oxide charge causes a negative voltage shift of the  $I$ - $V$  curve, while a negative one leads to a positive voltage shift. Moreover, if the stored charge is located near the interfaces (gate/oxide or  $p$ -Si/oxide), the  $I$ - $V$  curves show a distortion without shift (or with a very weak shift) along the voltage axis (El Hdiy et al., 1993).

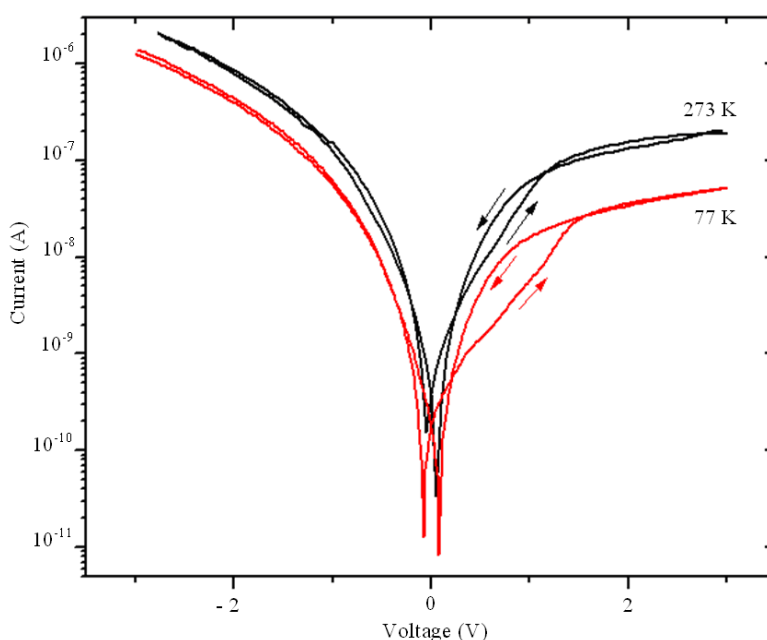


Fig. 8. Typical result showing occurrence of the hysteresis in the  $I$ - $V$  curves obtained in the sample containing NCs of 21 nm diameter ( $A_{21}$ ). The enlargement of the cycle is due to the thermo-electronic effect reduction.

Let us remark that only the  $I$ - $V$  characteristics in inversion regime present a hysteresis cycle. And this hysteresis increases when the temperature is reduced indicating the increase of the carrier storage as previously reported (Kuo & Nominanda, 2006). We also notice that the  $I$ - $V$  curves are not shifted indicating that the trapping/detrapping phenomena do not occur in the oxide bulk but more in the Ge-NCs as explained in the following.

The measurement first begins at negative bias (-3 V). At negative bias, holes move from the  $p$ -Si valence band to the gate by tunnelling effect, namely Fowler Nordheim tunnelling (FNT) effect, while electrons move from the gate to Ge-NCs, but their energy and their density are affected in the a-Si. Hole (majority carriers) density is higher than that of electrons (minority carriers). It is expected that trapping process (electrons and/or holes trapping) appears in both oxide bulk and in Ge-NCs; holes in the oxide and electrons in NCs. Indeed, when the bias voltage increases from -3 V to zero, becomes positive and reaches +3V, hole density is reduced but the density of electrons coming from Si substrate becomes more and more important showing a current increase at positive bias voltage (from 0 to +3 V). When the applied voltage turns back from +3 V to 0 V, the current presents higher values than the first scan. In this case, one has two possibilities leading to increase of current; the first process is the hole detrapping from the oxide, and the second process is the electron detrapping from the Ge-NCs. Both processes can appear during the scan of the bias from zero to +3 V. However, if the hysteresis was related to the hole trapping/detrapping in the oxide, the sense of the hysteresis cycle, indicated by the arrows in the figure would be inverted. Because hole trapping reduces the electron barrier height and the tunnelling distance, leading to a higher current when the bias voltage varies from 0 to +3 V than when it varies from +3 to 0 V.  $I$ - $V$  measurements were also performed at low temperatures. The results show that the hysteresis size depends on the temperature; the hysteresis width expands when the temperature decreases suggesting that the carrier trapping is enhanced as also shown by the HFC-V technique. Finally the same carrier trapping process is revealed by both  $I$ - $V$  and HFC-V characteristics.

Let us note that the use of the Fowler-Nordheim tunnelling standard expression can qualitatively lead to determine the density of the carriers trapped in Ge-NCs, or at least it can inform on the trapping efficiency versus the temperature. This approach was previously made in the case of the standard MOS capacitor (DiMaria et al., 1993; El Hdiy & Ziane, 2001) to extract the trapped charge density from  $I$ - $V$  measurements. We carefully use it according to the following assumptions: (a) there is no trapped carriers in the oxide, or the eventual stored carriers do not affect the initial oxide field  $E_0$ , (b) the charge contained in the NCs is supposed to be distributed in a thin layer at the NC/oxide interface and (c) the supplementary field caused by the carrier storage process remains lower than  $E_0$ .

The standard FNT expression (Fowler & Nordheim, 1928) is:

$$I = AE^2 \exp(-B/E) \quad (1)$$

Where,  $I$  is the tunnelling current,  $A$  and  $B$  are the FNT parameters considered to be constant.  $E$  is the electric field near the injecting electrode (the interface which is negatively polarized). Note that the expression given in Eq. (1) is valid only for high voltages; at low voltages, we must take into account the total expression of the tunnelling current (FNT and direct tunnelling) (Schuegraf & Hu, 1994). The oxide electric field can be expressed as:

$$E \approx E_0 - \frac{q\Delta N}{\epsilon_{Ge}} \quad (2)$$

Considering that the contribution of the stored electrons in NCs to the electric field  $E$  variations remains relatively negligible, the density of the trapped electrons is given by:

$$\Delta N(T) = -\frac{E_0^2 \epsilon_{Ge}}{qB} \text{Ln}\left(\frac{I}{I_0}\right) \quad (3)$$

Where,  $E_0$  is the field when the NCs are totally empty,  $q$  is the elementary charge,  $\epsilon_{Ge}$  is the Ge permittivity ( $\epsilon_{Ge}$  is used instead of  $\epsilon_{oxide}$  because the charge is stored in Ge-NCs) and  $\Delta N$  is the density of the stored electrons.  $I_0$  and  $I$  are the current before charge storage ( $\Delta N = 0$ ) and after carrier storage ( $\Delta N \neq 0$ ), respectively.

During the measurement under negative gate bias, electrons are trapped by NCs because of their weak energy at the injecting electrode. When the gate bias is inverted, the negative charge stored in NCs affects the tunnelling current leading to a current  $I$  lower than  $I_0$ . The use of Eq. (3) to data of Fig. 8, allows us to show that the stored charge density at 77 K is twice higher than that trapped at 300 K;  $\Delta N(77 \text{ K}) / \Delta N(300 \text{ K}) \approx 2$ . On the other hand,  $\Delta N$  can be measured by taking the current ( $I$  and  $I_0$ ) values at bias voltage corresponding to the large width of each cycle hysteresis.

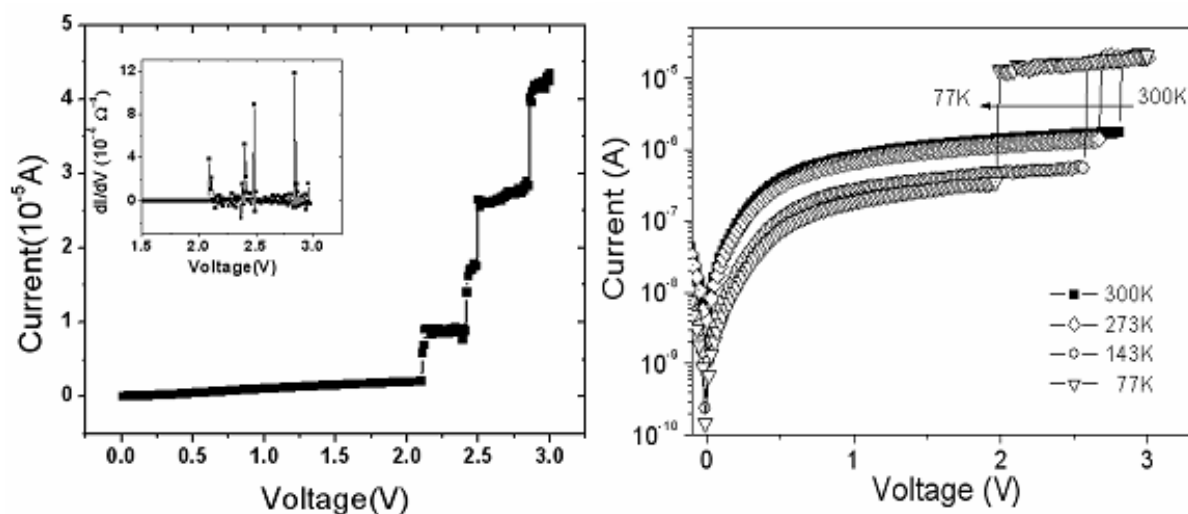


Fig. 9. (a) Current-voltage characteristic at a positive gate bias (inversion regime). The steps observed in the reverse  $I$ - $V$  curve are related to electron resonant tunnelling via Ge NC discrete levels. The inset contains the corresponding conductance as a function of gate voltage. (b) Evolution of current-voltage characteristics with temperature. Current jumps appear for increasingly weak voltages when the temperature decreases.

In addition to the carrier trapping evidence, we notice the remarkable behaviour exhibited by NCs which have a mean diameter of 3.5 nm and an average density of  $2.5 \times 10^{12} \text{ cm}^{-2}$ . Their  $I$ - $V$  curves present steps in the reverse part as shown in Fig. 9(a). The observed jumps

are not linked to the oxide breakdown for the following reasons. The maximum value of the oxide field is lower than 6 MV/cm (value from which damage in the oxide can occur), and to prevent defect creation in the oxide, the bias was scanned rapidly for higher values (from 2 to 3 V). Moreover, to be sure that the observed steps do not correspond to the oxide breakdown, the  $I$ - $V$  characteristics were repeated many times indicating approximate reproducible results. This little difference in terms of the plateau voltage position and height can be linked to both the temperature and size dispersion effects. Moreover, other measurements made at low temperatures have shown that the plateaus became larger. These jumps are representative of a resonant tunnelling of electrons into the discrete energy levels of Ge-NCs. Such tunnelling resonance behaviour has been attributed to the Coulomb blockade effect in Si quantum dots embedded in Si-rich SiO<sub>2</sub> deposited in plasma phase (Kim, 1998). Other recent studies have also shown the Coulomb blockade at room temperature in roughly spherical nanocrystalline silicon dots the main diameter of which was 5 nm (Wu et al., 2004).

Let us now explain this resonant tunnelling current. It is well known that in tunnelling resonance, electrons accumulate between double barriers (Goldman et al., 1987; Kim, 1998, Kareva et al., 2002; Vexler et al., 2006). In the case of our sample, electrons can temporarily accumulate at the Si/SiO<sub>2</sub> interface quantum well and between the double barrier formed by Ge-NCs, *a*-Si, and oxide. Under a positive bias, electrons are injected from the Si/SiO<sub>2</sub> quantum well through the oxide to the subband levels of the Ge-NCs where they fill the same energy levels as in the Si/SiO<sub>2</sub> quantum well. A simple description of the tunnelling resonance process can then be given: if we consider that electrons have the energy level of the silicon conduction band edge at the Si/SiO<sub>2</sub> interface ( $E_{c0}$ ), when the gate is positively biased, current flows only if  $E_{c0}$  is swept through the first quantum energy level ( $E_1$ ) of Ge-NCs resulting in a current peak in the  $I$ - $V$  curve. Since current continues to flow after  $E_{c0}$  is swept past  $E_1$ , one observes current steps rather than peaks in the  $I$ - $V$  curves. Two main conditions for observing the Coulomb blockade effect are (a) the tunnelling resistance between Ge NC and the electric contacts must be higher than the quantum resistance ( $Rt \gg h/e^2 \approx 26 \text{ k}\Omega$ ) and (b) single electron charging energy ( $E=e^2/2C$ ) $\gg k_B T$ , where  $C \approx 4\pi\epsilon_0\epsilon_{a-Si}r = 2.277 \text{ aF}$  is the self-capacitance of an approximately spherical Ge NC and  $\epsilon_{a-Si} = 11.7$  (Ref. Orwa et al.'2005) (this expression of  $C$  gives an overestimation of the capacitance value, since the spherical form of the Ge-NC is truncated at the contact with the oxide). This capacitance gives a single electron charging energy  $E$  of about 35 meV, supporting the existence of the Coulomb blockade effect. The first criterion can be met by weakly coupling the NC to two electrodes which is the case in our sample. The NCs are confined between SiO<sub>2</sub> and non doped amorphous silicon. The second criterion depends on temperature. At room temperature, the Coulomb blockade condition occurs when the capacitance is smaller than the thermal one,  $C_{th} = 3.1 \text{ aF}$  ( $3.1 \times 10^{-18} \text{ F}$ ), for a single quantum dot (or a diameter  $\leq 5 \text{ nm}$ ). In the situation investigated here, the capacitance values are smaller than  $C_{th}$ . Consequently, the charge energy ( $e^2/C$ ) is higher than the thermal energy ( $k_B T$ ). On the other hand, Fig. 9(b) shows that current jumps appear for increasingly weak voltages when the temperature decreases (Gacem et al., 2007). Note that this Coulomb blockade effect appears only for the NCs with the smallest main diameter (3.5 nm), and not in the other studied samples which probably would require temperatures lower than 77 K. This is related to the strong quantum confinement in 3.5 nm Ge-NC than in the others. Indeed, figure 10(a) gives a schematic energetic band diagram of the studied samples

showing the bandgap of each element and corresponding to a thermal equilibrium situation characterized by the alignment of the Fermi level. The conduction and valence band bending are not shown for convenience. The minimum difference between the a-Si and Ge-NC conduction bands is about 0.15 eV (here a-Si gap is equal to 1.7 eV), because it is well known that the bandgap of thin amorphous silicon may be substantially increased as compared to bulk a-Si owing to the confinement effect. This means that the bandgap value of the a-Si could be higher than 1.7 eV. Fig. 10(b) shows the NC gap as a function of the mean diameter obtained from calculation developed by Niquet et al. (Niquet et al., 2000) for spherical Ge nanocrystals. The Ge-NC band gap weakly increases from the sample  $A_{35}$  to  $A_{21}$  and then  $A_{17}$ , but takes a high value ( $\sim 1.55$  eV) for the sample  $A_{3.5}$ . This behaviour is remarkable and its consequence on electric characteristics is to lead a stronger quantum confinement than for the other samples, which is even revealed at room temperature.

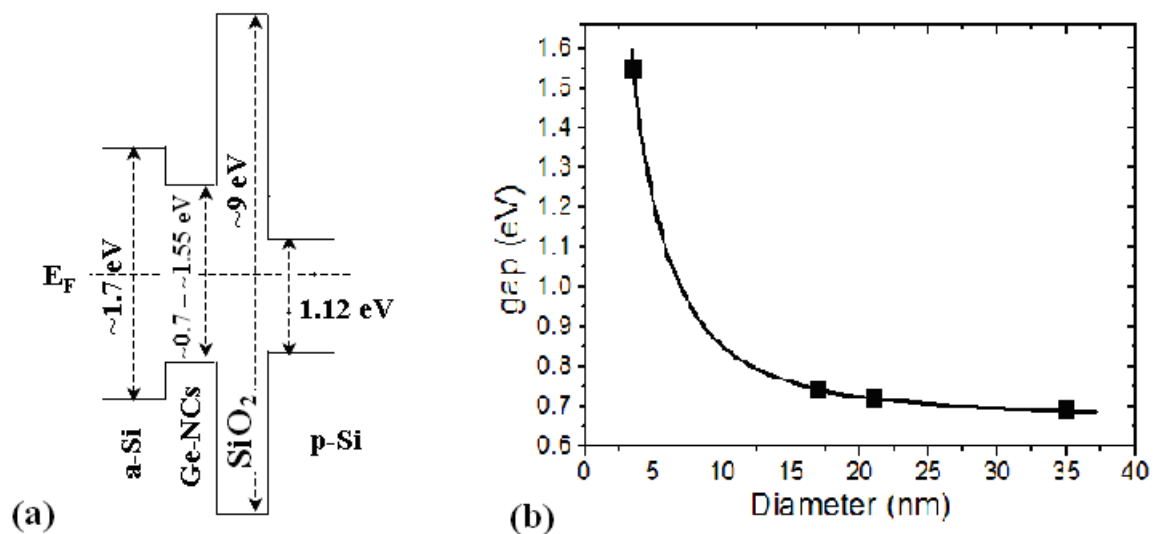


Fig. 10. (a) Schematic band diagram of the sample structure. The conduction and valence band bending are not shown here. (b) Energy bandgap of spherical Ge nanocrystals versus NC size; the line corresponds to theoretical calculation extracted from (Niquet et al., 2000).

#### 4.3 Conductive-AFM measurements

*I-V* and *HFC-V* measurements show that the electron trapping process occurs in Ge-NCs. But these techniques cannot allow the study of what happened in a single NC. They give average information which must be completed by supplementary data on single NC. This is the reason why we used the AFM technique to study the transport and the trapping/detrapping process in a NC.

The study was done by conductive atomic force microscopy (C-AFM). The measurements were performed on sample *B* at room temperature. The tip that we used was *n*-doped silicon tip covered with *p*-doped diamond-like carbon (resistivity  $\approx 0.003\text{--}0.005 \Omega \text{ cm}$ ) and the nominal cantilever stiffness was 2 N/m. In preliminary experiments, we first collected C-AFM images in which the measured current was a few pA which is not enough to obtain good resolution images. For detecting measurable current at a reasonable bias voltage (lower than  $\pm 8$  V) we were obliged to preliminary irradiate the sample with the electron

beam in the condition for obtaining a nano-EBIC image. Note that this phenomenon has also been observed for InAs/GaAs quantum dots (Troyon & Smaali, 2008).

First of all, let us explain what is the nano-EBIC technique. Its principle is schematically represented in Fig. 11.

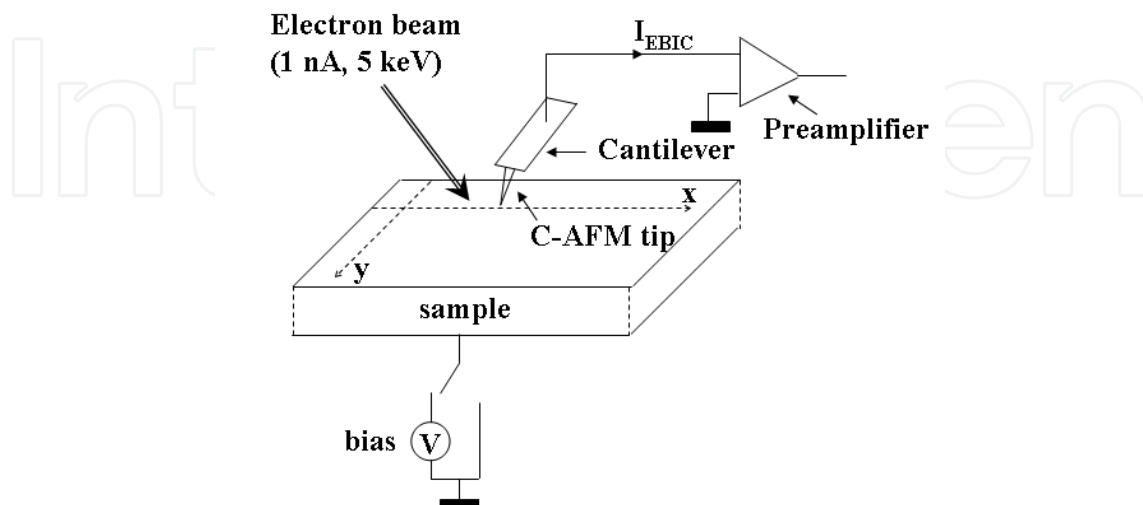


Fig. 11. Schematic representation of the set up used for the nano-EBIC technique. The AFM tip and the electron beam focused near this one are both immobile, whereas the sample is scanned in the  $(x, y)$  plane.

The AFM and EBIC images are simultaneously obtained by scanning the sample with respect to the fixed AFM probe by using the piezoelectric tube of the AFM. During image acquisition the electron beam is focused in a fixed position just in front of the AFM probe and as close as possible to this one. The back side of the sample is connected to the ground and the current is punctually collected by the conductive AFM tip near the electron probe during scanning the sample. The tip-sample contact constitutes a nano-heterojunction with formation of a very small depletion zone which is able to collect the electron beam induced current. The size of the depletion zone determines the resolution. We have demonstrated that a resolution of the order of 20 nm can be obtained (Smaali et al., 2008; Troyon & Smaali, 2008).

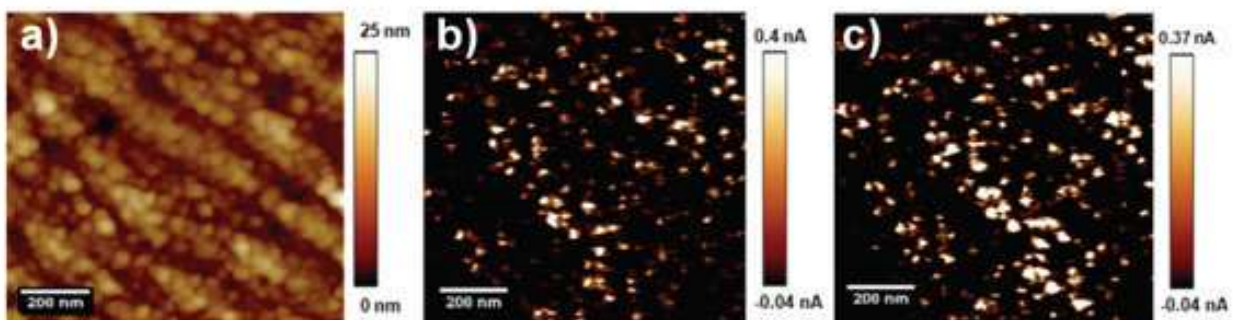


Fig. 12. Topographic image a), b) electric image obtained at 0 V just after acquisition of an e-beam induced current image (e-beam off) and c) second electric image obtained two hours after in the same irradiated zone.

After electron beam irradiation in the condition for obtaining electron beam induced current, C-AFM measurements without electric biasing (0 V) were performed at different times with the electron beam off. Typical results are shown in Fig. 12. This figure gives a comparison between three kinds of images acquired on the same area of a sample containing NCs of 70 nm diameter: (a) is an AFM topographic image, (b) is a C-AFM image obtained without sample bias (e-beam off) just after acquisition of a nano-EBIC image and (c) is obtained in the same condition as image (b) but 120 minutes later. Although the tip radius is large ( $\sim 150$  nm), the NCs are well resolved; this can be probably explained by the presence of small diamond nanocrystals or grains formed at the extremity of the tip during the fabrication process. Note that even at 0 V, 0.4 nA of current is obtained. The fact that a current could be collected without bias is explained by the charge transfer resulting from the alignment of the Fermi levels of the sample and probe during scanning.

The C-AFM images afterwards obtained on the previously irradiated zone show that the current flowing through the NCs remains of the same order of magnitude as the image taken two hours before, although the sample is not polarized. This process shows that charges have been trapped in the NCs during the electron beam irradiation and produce a current, which is a hole current. Indeed, the contact between the *p*-doped diamond AFM tip and the sample surface forms a nano-heterojunction. This kind of nano-contact leads to the transport and trapping of holes, but prevents electrons to flow due to the high conduction bands discontinuity. This mechanism is explained by the energetic band diagrams of Fig. 13. Fig. 13(a) shows the band diagram of the contact between the AFM diamond tip and the oxide and Fig. 13(b) shows the band diagram when the AFM tip is in contact with the NC. In both cases, electrons cannot flow because of the large conduction band discontinuity.

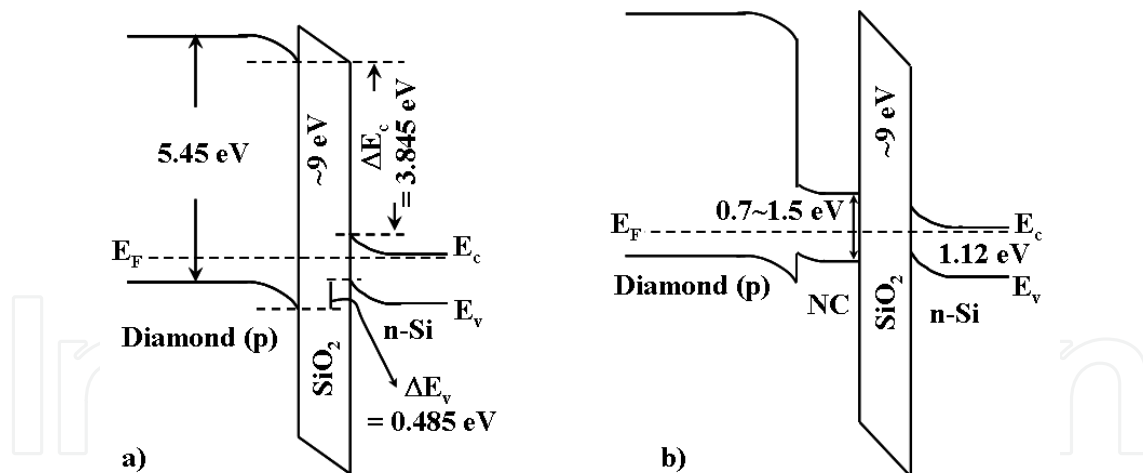


Fig. 13. Energy band diagrams of the probe-sample nano-contact when (a) the probe is positioned in contact with the oxide and (b) when it is positioned above the NC the bandgap of which (0.7~1.5 eV) is size-dependent.

During scanning, holes can move from the tip to the NC because of the weakness of the band bending at the tip/NC interface. Coming from the substrate by tunnelling through the oxide, some of holes are trapped in the quantum well (in the NC) and could accentuate the NC energy band bending. With no contact between the AFM tip and the sample, holes remain stored in the NCs because of the presence of a native oxide covering the NCs and also of the vacuum which creates a barrier confining holes in the NCs. The hole detrapping

begins when the AFM tip is in contact with the NC in two situations; unbiased and negatively polarized tip. In the unbiased tip case, a part of stored holes can tunnel through the little barrier from NCs to the AFM tip. While a negative polarization to the tip (which does not affect the barrier height at the NC/tip interface) accentuates the band bending at each interface enhancing the hole current through the structure. Whatever the sign of the electric polarization, electrons cannot move through the system (tip/NC/oxide/silicon) because of the strong conduction band pseudo-discontinuity added to the barrier height due to the presence of the oxide.

As quoted above, electric conduction results from hole detrapping from NCs. This discharging effect of Ge-NCs has been clarified by the analysis of a series of C-AFM images recorded on one single NC just after the acquisition of a NF-EBIC image, without polarizing the sample. Five images have been recorded every 30 min. Between two images the C-AFM probe is retracted to avoid contact with the sample. The successive electric images show a progressive reduction of the intensity with a total extinction of the NC at the fifth image when the NC is completely discharged. Fig. 14 shows the evolution of the maximum current measured in the NC versus time and on the right part the corresponding current images and the simultaneously acquired topographic images which were extracted from larger images. These images reveal a detrapping phenomenon. The C-AFM images obtained without sample bias, demonstrate the capacity of the NCs to trap charges and also to release charges after each passage of the C-AFM tip on the NCs in the condition of no sample bias. Losing charge during acquisition of an electric image reduces the current in the next image. Indeed, during contact between the AFM tip and an isolated NC under 0 volt bias, the Fermi levels alignment leads to hole emission from previously charged NC because of the low effective barrier height at this contact which facilitates the current flow. Obviously, silicon hole tunnelling effect through the oxide is unlikely because of its thickness (~5 nm). So, after the acquisition of the following electric images the hole current is more and more reduced.

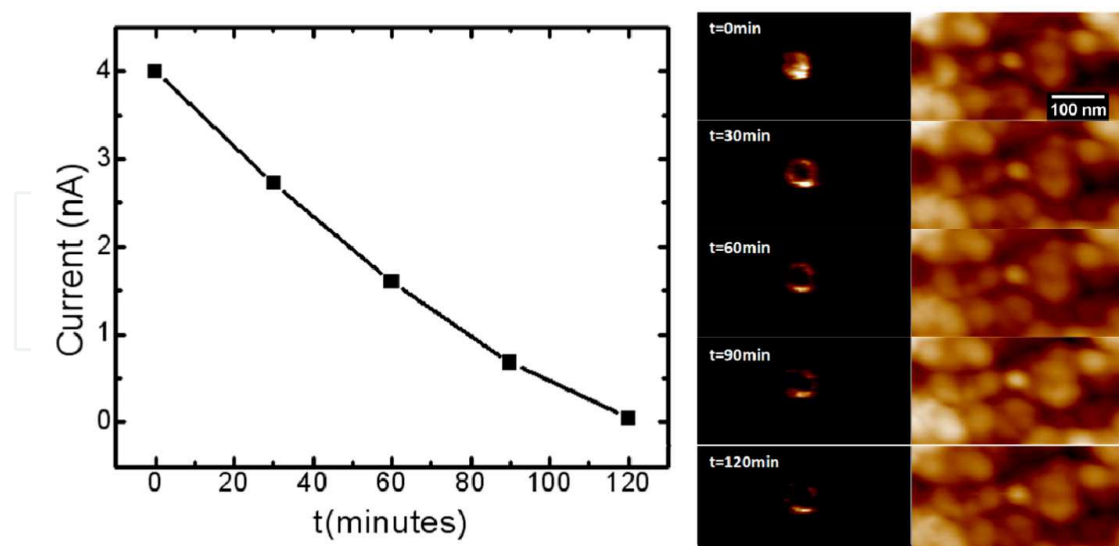


Fig. 14. Variation of the maximum current flowing through an NC versus time in a series of five images ( $V = 0$ ) illustrating a hole detrapping process. The electric images recorded every 30 min after irradiation, are presented on the right as well as the simultaneously acquired topographic images.



The charge retention is an important and crucial parameter which requires attention in both elaboration procedure and reliability characterization. The use of NCs to replace the standard floating gate in memory devices is necessary since many problems can be avoided. It is interesting to make comparison between both characterization techniques used in this work even if two kinds of nanostructures (containing capped or no capped NCs) have been differently studied. Both methods give information on carrier transport and storage. They also underline dominant role of the Ge-NCs in the carrier capture and storage. However, it is clearly seen that the C-AFM technique is required if information on an isolated NC (or a limited number of NCs) in a given structure is needed. It would be interesting to study the stored charge amount as a function of the NC size. This could be performed by Electrostatic Force Microscopy technique which is our future ambition.

## 5. Conclusion

Ge nanocrystals grown by a two step dewetting / nucleation process on an oxide/*p*-(or *n*-) doped silicon substrate have been electrically studied by standard methods (capacitance - voltage and current - voltage) and by conductive atomic force microscopy technique. The kind of the carriers involved in the electric transport and the charge storage depends on the nature of the electrode/sample contacts. With the standard methods, for which a metallic contact was used, electrons were concerned. The study was performed over a wide range of temperature varying from 300 down to 77 K and results evidenced an electron storage phenomenon in nanocrystals. The temperature effect in the enhancement of the electron retention was revealed by the enlargement of the hysteresis cycles obtained on *HFC-V* and *I-V* measurements. Indeed, the reduction of the measurement temperature reduces the thermo-electronic emission from NCs and facilitates carrier storage. Resonant tunnelling effect through germanium nanocrystals with large voltage gaps was observed at room temperature in ultradense Ge nanocrystals of  $\sim 3.5$  nm mean size. It appeared for increasingly low voltages when the temperature decreases. All these results are consistent with a Coulomb blockade effect in ultras-small Ge nanocrystals. Conditions for the occurrence of the Coulomb blockade have been reminded.

On the other hand, the C-AFM technique using a *p*-doped diamond probe was used to study uncapped Ge-NCs. The current flowing through the conductive probe was measured for imaging local conductance, while the deflection of cantilever was optically detected for revealing geometrical structure. The heterojunction resulting from the AFM tip/sample contact allowed hole transport through the structure and hole storage in Ge-NCs. Preliminary electron beam irradiation in the conditions for obtaining a nano-EBIC image was needed for performing the C-AFM study. Without this e-beam irradiation, no noticeable current could be detected.

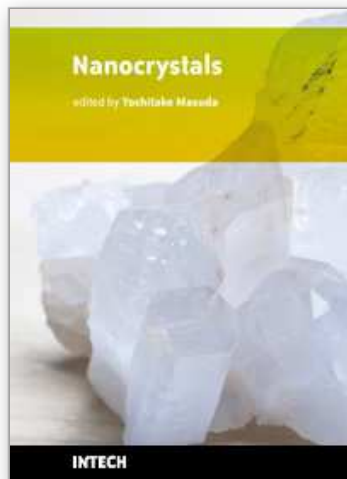
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