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# a-Si:H TFT and Pixel Structure for AMOLED on a Flexible Metal Substrate

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## 1. Introduction

Flexible displays have attracted enormous interest from research institutes. The images of the flexible displays include bendable display, and electronic paper. The technology of flexible displays includes many domains: the display modes, flexible substrates, and backplanes.

Organic light emitting diodes (OLEDs) are considered the natural choice for flexible displays because of wide viewing angle, no cell gap problem, and the potential for using solution process. In addition, OLEDs can also be fabricated at relatively low temperature, which enable the use of plastic substrate. However, a key challenge for flexible OLEDs display is oxygen and moisture sensitivity. A device lifetime of 10,000 hrs requires maximum moisture permeability of  $5 \times 10^{-6}$  g/m<sup>2</sup>/day. Plastic has 10~1000 g/m<sup>2</sup>/day of moisture permeability. Other challenge for OLEDs is high power consumption, which is also one of key issues for portable flexible displays along with weight and thickness. In the long run, OLEDs are excellent candidate for flexible application.

Thin metal foils have an alternative flexible substrate for the fabrication of OLED displays. They have potential advantages over plastic such as lower moisture permeability and higher process temperature. They have much better dimensional stability, and present a perfect diffusion barrier to water and oxygen. Because the metal foils have higher elastic modulus (~200 GPa), and lower coefficient of thermal expansion (18 ppm/°C), they have excellent dimensional stability, which allows multi-photo process comparable to those of glass. Conductive substrate can provide for common power signal and shielding as well as heat dissipation. However, the metal surfaces are usually rougher than most plastics, and the foils can wrinkle if flexed to very small bending radius.

In this paper, hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) fabricated on a metal foil substrate is reported for active matrix OLEDs (AMOLEDs) displays. The electrical properties of a-Si:H TFTs fabricated on a metal foil substrate are introduced. To increase the stability of a-Si:H TFTs fabricated at low temperature on a metal foil substrate, negative bias applied to metal foil substrate can also recover the shifted threshold voltage during idle time. A new cathode-contact structure employing a normal top-emitting OLED, which is suited to n-type a-Si:H TFT backplane is proposed.

## 2. Electrical performances of a-Si:H TFT fabricated on a metal foil

### 2.1 Fabrication of a-Si:H TFT on a metal foil

Metal foils have potential advantage over plastic. They tolerate high temperature processes in contrast to glass and even more to plastics. They also have much better dimensional stability because the metal foils have higher elastic modulus ( $\sim 200$  GPa), and lower coefficient of thermal expansion ( $\sim 10$  ppm/ $^{\circ}$ C).

However, flexible metal foil substrates do not easily process with traditional TFT equipments such as stepper, PECVD, and etchers that are compatible with rigid glass substrates. To utilize traditional TFT equipments, a flexible metal foil substrate can bond to a rigid glass plate. In this case, the adhesive used for bonding the metal foil to a rigid glass plate reduces the maximum process temperature from the value that the substrate itself would withstand.

The adhesive covered on the rigid glass plate and 76- $\mu$ m-thick metal foil was stuck on them. A spin-on polymer (SOP) or spin-on glass (SOG) as an initial surface planarization spread on a metal foil substrate in order to reduce the surface roughness of the metal substrate. 200-nm-thick silicon nitride (SiN<sub>x</sub>) formed by plasma-enhanced chemical vapor deposition (PECVD). This layer insulates electrically TFT layers from metal substrate. The electrical insulation layer also served as the mechanical bond between the TFT layers and the substrate. The root-mean-square (RMS) roughness of the metal foil substrate after planarization was 5 nm. The structure of the a-Si:H TFT was an inverted staggered-type structure, which was fabricated by a conventional five-mask process. The flexible metal substrate carrying TFT array separated from the rigid glass plate. To protect mechanical stress from being able to degrade the electrical performance of a-Si:H TFT, the adhesive between the metal foil and the glass plate was softened by chemical before separation. The performance of TFT did not change before and after separation the flexible metal substrate carrying TFT array from the rigid glass plate. Fig. 1 shows a cross section of a-Si:H TFT, which was fabricated on flexible metal foil.

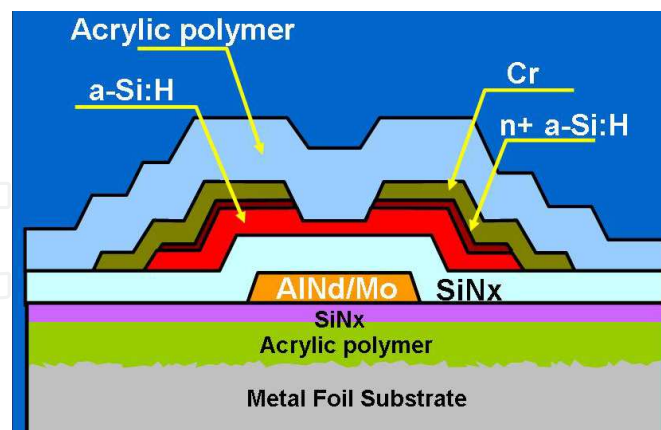


Fig. 1. Structure of TFT fabricated on metal foil substrate

### 2.2 Electrical performances of a-Si:H TFT dependent on planarization layer

In flexible displays employing metal foil substrate, planarization is required to reduce the surface roughness of metal foil and electrically insulate TFT array from conductive metal foil. Spin-on glass (SOG) and spin-on polymer (SOP) were selected as planarization dielectric. 2

$\mu\text{m}$ -thick siloxane as SOG or 2  $\mu\text{m}$ -thick acryl as SOP were coated and 0.2  $\mu\text{m}$ -thick SiNx insulation was deposited by PECVD.

Table 1 shows the result for capacitance and leakage current for SOG/SiNx, SOP/SiNx, and single SiNx layers. Both SOG/SiNx and SOP/SiNx are acceptable as planarization and insulation layer in the viewpoint of the insulation and capacitive coupling characteristics. For large display, the unit capacitance of less than 2 nF/cm<sup>2</sup> was suggested.

Hence, the capacitance of 1.2 and 2.1 nF/cm<sup>2</sup> for SOG/SiNx and SOP/SiNx, respectively is allowable. Surface root-mean-square (RMS) roughness of bare metal foil was 110 nm. It improved to 12 and 10 nm after the planarization layer such as SOG/SiNx and SOP/SiNx was coated on the metal foil substrate, respectively.

Planarization	Curing Condition(°C)	Insulation Layer	Capacitance (nF/cm <sup>2</sup> )	Leakage Current (nA/cm <sup>2</sup> )
SOG 2 $\mu\text{m}$ (Siloxane)	230	SiNx 200 nm	1.2	24
SOP 2 $\mu\text{m}$ (Acryl)	150	SiNx 200 nm	2.1	23
-	-	SiNx 200 nm	27.1	720

Table 1. Capacitance and leakage current for a package of planarization and insulation layers

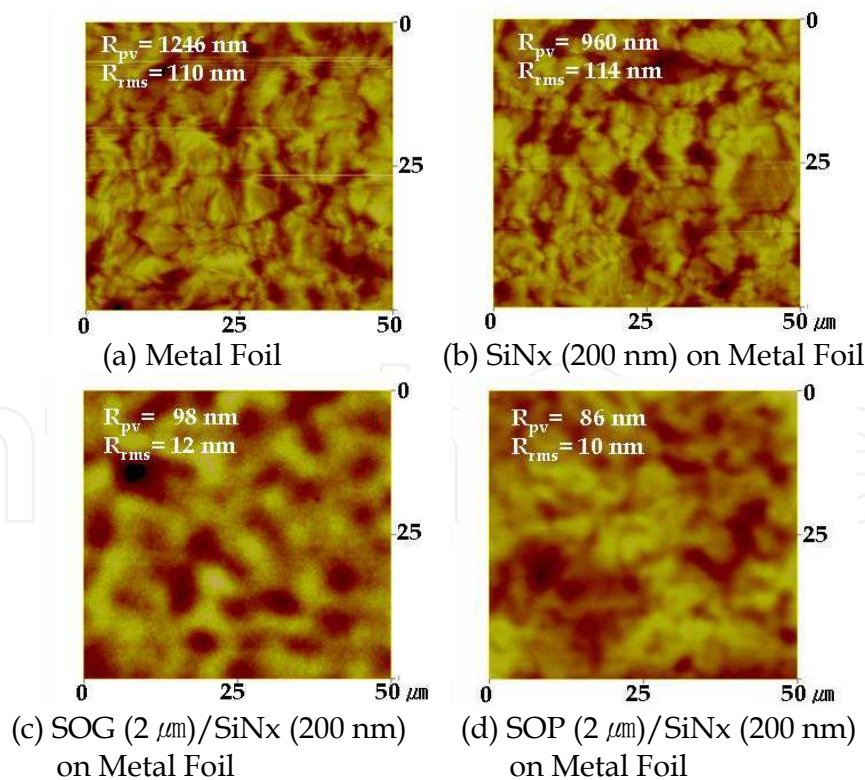


Fig. 2. AFM images and surface roughness of (a) metal foil and planarized with (b) SiNx 200 nm, (c) SOG 2  $\mu\text{m}$  / SiNx 200 nm, and (d) SOP 2  $\mu\text{m}$  / SiNx 200 nm

The surface images measured by atomic force microscope (AFM) are shown in Fig. 2.

Inverted staggered a-Si:H TFTs were fabricated by the process flow as mentioned in the previous section. Fig. 3 shows the transfer characteristics of a-Si:H TFTs as planarization layers. Electrical properties measured by semiconductor characterization system (Keithley 4200). The electrical performances of a-Si:H TFTs as planarization layers is compared as shown in Table 2.

There were not remarkable differences of the electrical performances of a-Si:H TFTs as planarization layers of SOG/SiNx and SOP/SiNx. For both TFTs, the off current is about  $10^{-13}$  A and the on current at gate voltage of 20 V is about  $10^{-6}$  A at a drain voltage of 10 V, resulting in an on-off current ratio of  $10^7$ . We obtain a subthreshold slope  $0.62 \sim 0.64$  V/decade, demonstrating a sharp device turn-on. We also obtain a threshold voltage and mobility of  $0.3 \sim 0.6$  V and  $0.27 \sim 0.45$   $\text{cm}^2/\text{Vs}$ , respectively, in the saturated regime.

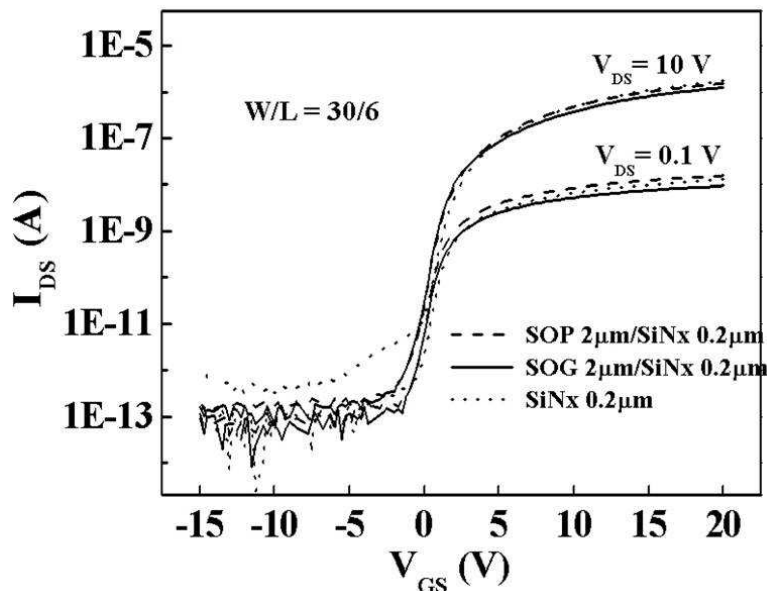
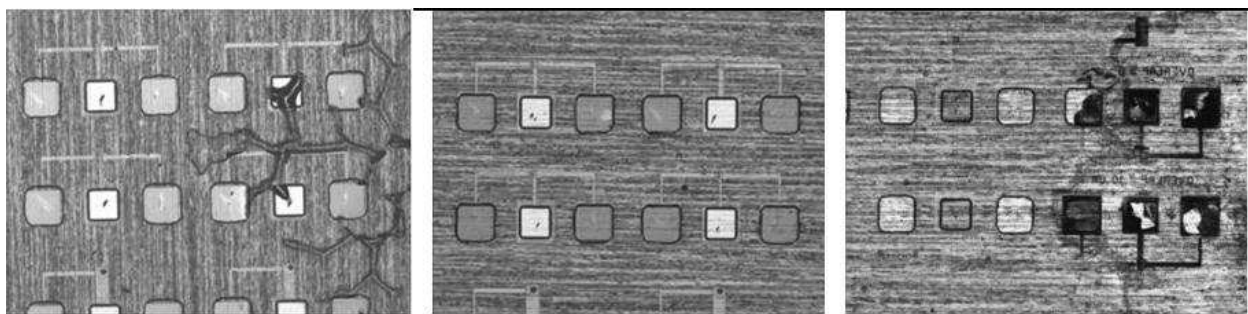


Fig. 3. Transfer characteristics of a-Si:H TFTs as planarization layers: SiNx 200 nm, SOG 2  $\mu\text{m}$  / SiNx 200 nm, and SOP 2  $\mu\text{m}$  / SiNx 200 nm. The size of TFT is  $W = 30 \mu\text{m}$  and  $L = 6 \mu\text{m}$ .

No	Planarization	Insulation Layer	TFT Characteristics				Remark
			Mobility ( $\text{cm}^2/\text{Vs}$ )	Threshold Voltage(V)	Subthreshold Slope(V/dec.)	Off Current(A)	
1	SOG 2 $\mu\text{m}$ (Siloxane)	SiNx 200 nm	0.30~0.44	0.33	0.639	$2.1 \times 10^{-13}$	From 5 TFTs
2	SOP 2 $\mu\text{m}$ (Acryl)	SiNx 200 nm	0.27~0.45	0.61	0.618	$2.0 \times 10^{-13}$	From 5 TFTs
3	-	SiNx 200 nm	0.40	1.08	0.647	$8.0 \times 10^{-13}$	From 1 TFT

Table 2. Electrical performances of a-Si:H TFTs as planarization layers

However, SOG/SiNx wrinkled after TFT fabrication as shown in Fig. 4 (a). Many TFTs on the wrinkled SOG failed to measure. All TFTs employing SOP/SiNx secured electrical performances. The SOG/SiNx wrinkled after passivation process. We used acrylic polymer for passivation, which is the same material as a planarization. Dimension mismatch may occur between SOG and acrylic polymer during thermal treatment of passivation material. The length of SOG is the same as that of acrylic polymer. As the sample cools to room temperature, the SOG and acrylic polymer want to contract by different amounts due to the difference of the coefficient of thermal expansion (CTE). The CTE of the SOG is usually smaller than that of the acrylic polymer ( $\alpha \approx 1 \times 10^{-6}/^{\circ}\text{C}$  for the SOG,  $\alpha \approx 50\sim 70 \times 10^{-6}/^{\circ}\text{C}$  for the acrylic polymer). The strain of the SOG is negative as compared with that of acrylic polymer, this means that the SOG is under compressive stress. This compressive stress can make the SOG film wrinkle. When a single SiNx was used as a planarization, the off current is high as  $8 \times 10^{-13}$  A, and the threshold voltage is also high as 1.08 V because of the large surface roughness of single SiNx on the rough metal foil. The rms roughness of 200 nm-thick SiNx on rough metal foil is 114 nm. After fabrication of TFT on metal foil planarized by SiNx, most of TFTs were delaminated from substrate as shown Fig. 4 (c).



(a) SOG/SiNx Planarization (b) SOP/SiNx Planarization (c) SiNx Planarization  
Fig. 4. Optical images of a-Si:H TFT as planarization materials

### 3. Effect of passivation materials on electrical performances of a-Si:H TFTs fabricated on a metal foil

#### 3.1 Electrical performances of a-Si:H TFTs passivated with SiNx or acrylic polymer

a-Si:H TFTs were fabricated on flexible metal foil as mentioned in previous section. 200 nm-thick SiNx and acrylic polymer were chosen as passivation layer on TFT channel. Fig. 5 shows the transfer characteristics of a-Si:H TFTs dependent on passivation materials.

In the case of SiNx-passivation, the off current is about  $10^{-13}$  A and the on current at gate voltage of 20 V is about  $10^{-6}$  A at a drain voltage of 10 V, resulting in an on-off current ratio of  $10^7$ . We obtain a subthreshold slope  $\sim 0.69$  V/decade, demonstrating a sharp device turn-on. We also obtain a threshold voltage and mobility of 2.1 V and  $0.61 \text{ cm}^2/\text{Vs}$ , respectively, in the saturated regime. In the case of acrylic polymer employed as a passivation layer, most electrical characteristics of the acrylic-passivated TFT except threshold voltage were comparable to those of the SiNx-passivated TFT. The off current is about  $10^{-13}$  A and the on current at gate voltage of 20 V is about  $10^{-6}$  A at a drain voltage of 10 V, resulting in an on-off current ratio of  $10^7$ . We obtain a subthreshold slope  $\sim 0.61$  V/decade, demonstrating a sharp device turn-on. We also obtain a threshold voltage and mobility of 1.0 V and  $0.54 \text{ cm}^2/\text{Vs}$ , respectively, in the saturated regime.

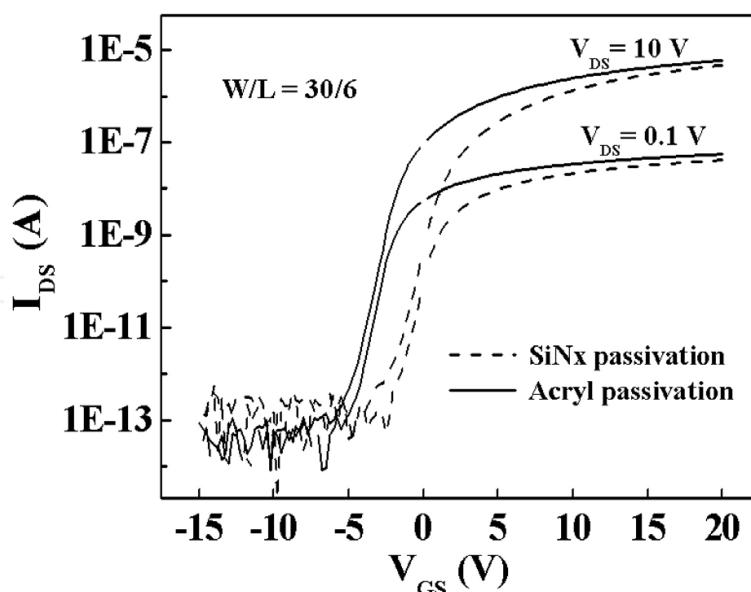


Fig. 5. Transfer characteristics of a-Si:H TFTs as passivation materials: SiNx and acrylic polymer. The size of TFT is  $W = 30 \mu\text{m}$  and  $L = 6 \mu\text{m}$ .

The lower threshold voltage of the acryl-passivated TFT was explained by more positive fixed charge at the back interface. Less hydrogen and nitrogen in the acryl-passivation could not eliminate the fixed charges. Then some free electrons which were accumulated in the back interface were controlled by the gate bias.

### 3.2 Effect of passivation materials on electrical performances of a-Si:H TFTs under mechanical stress

To investigate the effect of passivation layer on the performances of a-Si:H TFTs under mechanical stress, we stressed both TFTs by outward cylindrical bending at the radius of curvature  $R = 5 \text{ mm}$  as shown in Fig. 6. Less than  $R = 4 \text{ mm}$ , most of TFTs employing acrylic polymer or SiNx as passivation layer were failed. When the radius of curvature was  $5 \text{ mm}$ , the strain on the surface of acryl and SiNx was  $0.0082$  ( $0.82 \%$ ) and  $0.0077$  ( $0.72 \%$ ), respectively. Eq. 1 considering single acryl ( $3 \mu\text{m}$ ) or SiNx (substrate-insulation, gate-insulation and backchannel passivation  $0.9 \mu\text{m}$ ) layer calculated the strain.

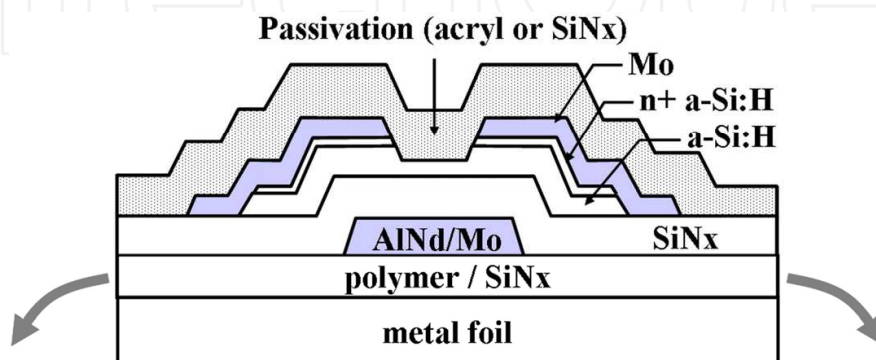


Fig. 6. Cross section of an inverted staggered type TFT fabricated on a flexible metal substrate. The arrows indicate the bending direction.

$$\varepsilon_{top} = \left[ \frac{(d_f = d_s)}{2R} \right] \frac{(1 + 2\eta + \chi\eta^2)}{(1 + \eta)(1 + \chi\eta)} \quad (1)$$

where  $\eta = d_f/d_s$ ,  $\chi = E_f/E_s$ , here  $d_f$  (acryl) = 3,  $d_f$  (SiNx) = 0.9  $\mu\text{m}$  and  $d_s = 76 \mu\text{m}$  are film and substrate thickness, respectively.  $E_f$  (acryl) = 3.2,  $E_f$  (SiNx) = 183 and  $E_s = 200 \text{ GPa}$  are Young's modulus of film and substrate, respectively.

Before bending the TFTs, electrical performances were measured. The TFTs were stressed for 24 hours. The transfer characteristics of TFTs in the bended condition ( $R = 5 \text{ mm}$ ) were measured at arbitrary intervals as shown in Fig. 7. A zero hour duration time meant that TFTs measured as flattened before bending them.

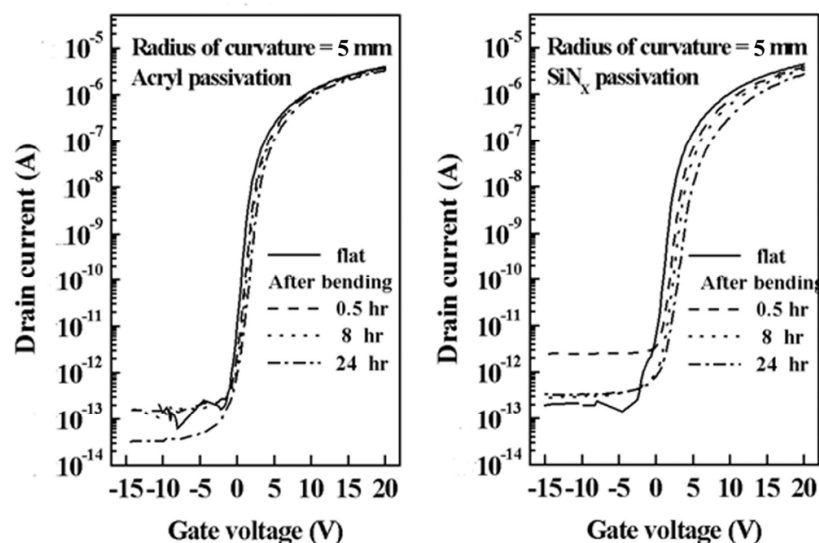


Fig. 7. Transfer characteristics for the acryl and SiNx-passivated TFT as bending duration time. The radius of curvature  $R$  is 5 mm.

As the bending duration time increased, the transfer curves shifted to the right direction and the electrical performances deteriorated as shown in Fig. 8. The field effect mobility decreased and the sub-threshold slope increased. The field effect mobility and the subthreshold slope are much dependent on the width of the tail state. The field effect mobility is smaller and the subthreshold slope is larger as the a-Si:H tail state increases. This increase of the width of the tail states might be due to the relative increase of the deep states in tail states. When the flexible TFTs are bended outward, Si-Si bonds in a-Si:H, close to the gate dielectric interface, are shrunk. The increase in the number of the strained Si-Si bonds implies a wider conduction-band-tail distribution. This may be the reason why the field effect mobility decreases and the subthreshold slope increases as the TFTs are bended. The threshold voltage also increased as the bended-duration time increased. Stutzmann proposed that the mechanical stress could influence the metastable defect creation in an a-Si:H film and that defect formation was enhanced in strained regions. The increased threshold voltage decreased again as time passed after the bended-TFTs flattened and almost recovered after thermal annealing. This meant that the degraded electric characteristics were curable. Hence, we may also conclude that the increased threshold



voltage by an increase in strained regions is attributed to increasing the number of the meta-stable dangling bonds.

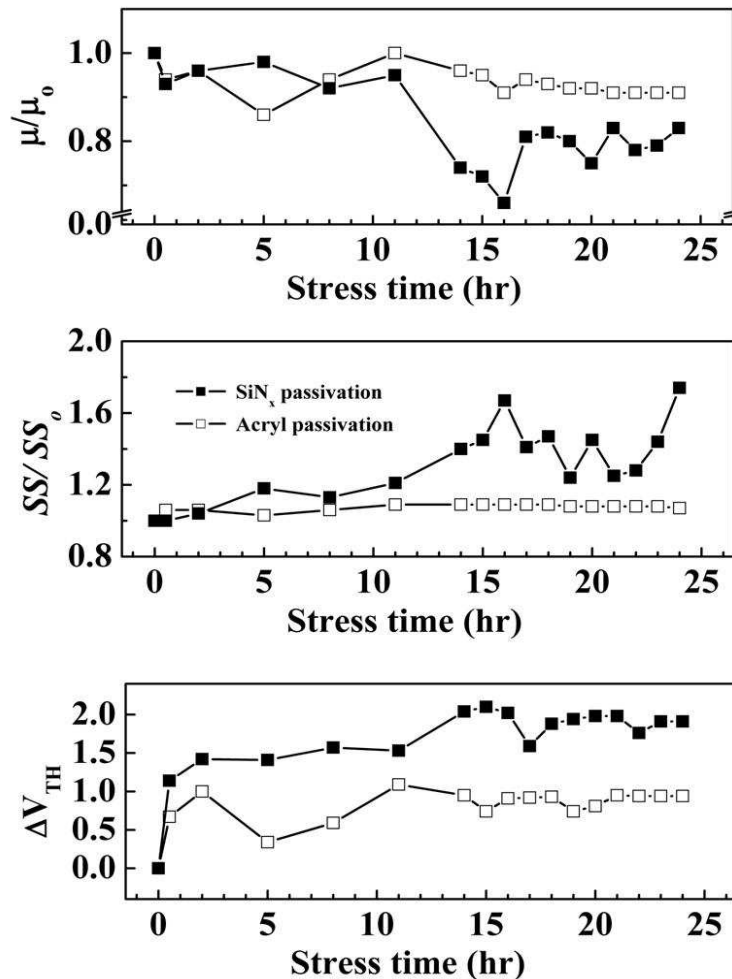


Fig. 8. Relative field-effect mobility, subthreshold slope and threshold voltage plotted as functions of stress time. TFTs were measured as bended except 0-hour stress time. The data at 0-hour stress time were measured from the flattened-TFTs before bending.

The deterioration of the electrical performances in the SiN<sub>x</sub>-passivated TFT under mechanical stress was more severe than that in the acryl-passivated TFT. Under an outward bending, the bending momentum elongates the TFT-films in the upper part of TFT on a metal substrate and compresses the flexible metal substrate in the lower part. Neutral plane is free from any stress between the elongated and the compressed part. The Young's modulus of acrylic polymer (3.2 GPa) is lower than that of SiN<sub>x</sub> film (183 GPa). As the 3  $\mu\text{m}$ -thick acrylic polymer was employed as the passivation layer in place of 0.3  $\mu\text{m}$ -thick SiN<sub>x</sub> film, a total thickness of TFT-films was increased. Therefore, the position of the neutral plane may shift from mid-surface toward the TFT-films. It accompanies with decrease of stress applied on the TFT-films. Hence, the acryl-passivated TFT could endure mechanical stress better than the SiN<sub>x</sub>-passivated TFT.

### 3.3 Effect of passivation materials on electrical performances of a-Si:H TFTs by humidity permeation

To investigate moisture permeation phenomenon dependent on the passivation materials, a humidity-temperature test was carried out at 65 °C and 90 % relative humidity (RH). We compared the electrical performances of the SiN<sub>x</sub>-passivated and the acryl-passivated TFTs after 3-hour humidity-temperature test. Fig. 9 shows transfer curves before and after the humidity-temperature test. We could not find any significant shift of the threshold voltage in the SiN<sub>x</sub>-passivated TFT. The SiN<sub>x</sub> passivation did not allow moisture to penetrate into TFT. On the other hand, threshold voltage shifted as large as 2.8 V for the acryl-passivated TFT. The acrylic polymer could not keep the moisture from permeating. Other researchers have reported the effect of moisture on a-Si:H TFT.

Moisture increases the conductance of a-Si:H films. When an a-Si:H TFT without passivation was exposed to the air, the off current increased due to the absorbed air humidity. However, we could not find any increase of off current after the humidity-temperature test. The effect of the moisture on the acryl-passivated TFT might be different from the unpassivated-TFT. The moisture can not affect a front interface at the bottom of a-Si:H layer because it cannot penetrate a-Si:H layer. The negative fixed charges may increase at the back interface after the moisture permeates the acryl passivation. Then the negative charges may perhaps make the threshold voltage shift to the positive direction. More investigations are required to analyze what affects the threshold voltage increment after the humidity-temperature test.

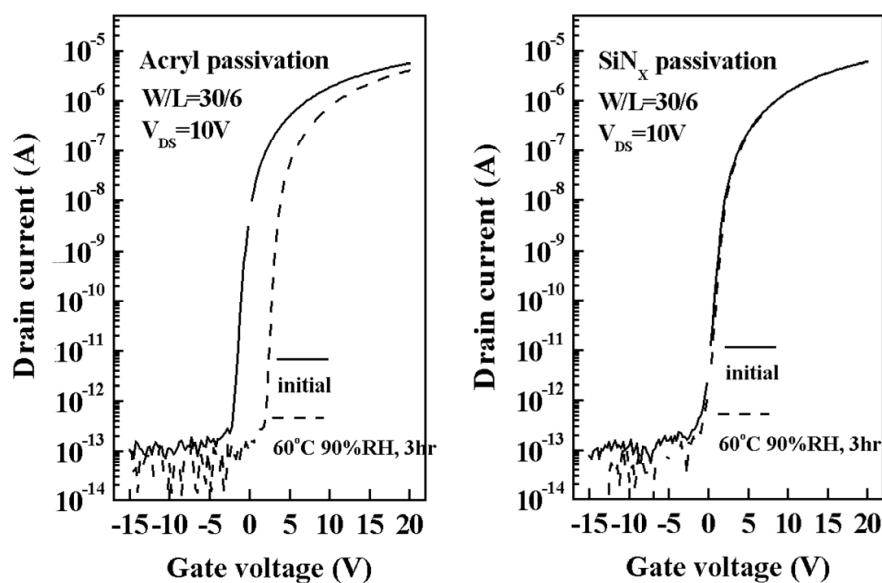


Fig. 9. Transfer characteristics for the acryl and SiN<sub>x</sub>-passivated TFT were measured before and after they were stored at 60°C and 90 % RH for 3 hours.

### 3.4 Effect of hybrid passivation layer on a-Si:H TFTs electrical characteristics

A hybrid structure which was composed of 50 nm-thick SiN<sub>x</sub> and 3 μm-thick acrylic polymer was chosen as passivation layer as shown in the Fig. 10. TFTs were stressed by outward cylindrical bending at the radius of curvature R = 5 mm. Before bending the TFTs, electrical performances measured. The TFTs were stressed for 24 hours. The transfer characteristics of

TFTs in the bended condition ( $R = 5$  mm) were measured at arbitrary intervals as shown in Fig. 11 (left) and 12. A zero hour duration time meant that TFTs were measured as flattened before bending them. The mobility change ( $\mu_{fe}/\mu_{feo}$ ) of 0.92, the subthreshold slope change ( $SS/SS_0$ ) of 1.04, and the threshold voltage shift ( $\Delta V_{TH}$ ) of 1.03 are almost same as those of TFT employing the single acrylic passivation. As the 50 nm-thick SiNx and 3  $\mu\text{m}$ -thick acrylic polymer were employed as the passivation, the position of the neutral plane may shift from mid-surface toward the TFT-films. These results are similar to that of a single acrylic polymer passivation.

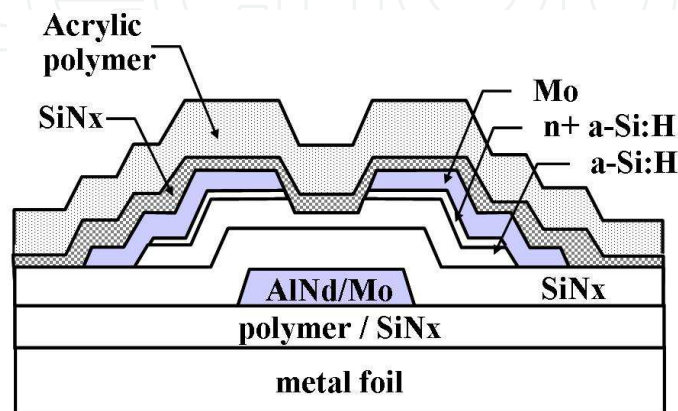


Fig. 10. Cross section of an inverted staggered type TFT employing 50 nm-thick SiNx and 2  $\mu\text{m}$ -thick acrylic polymer passivation

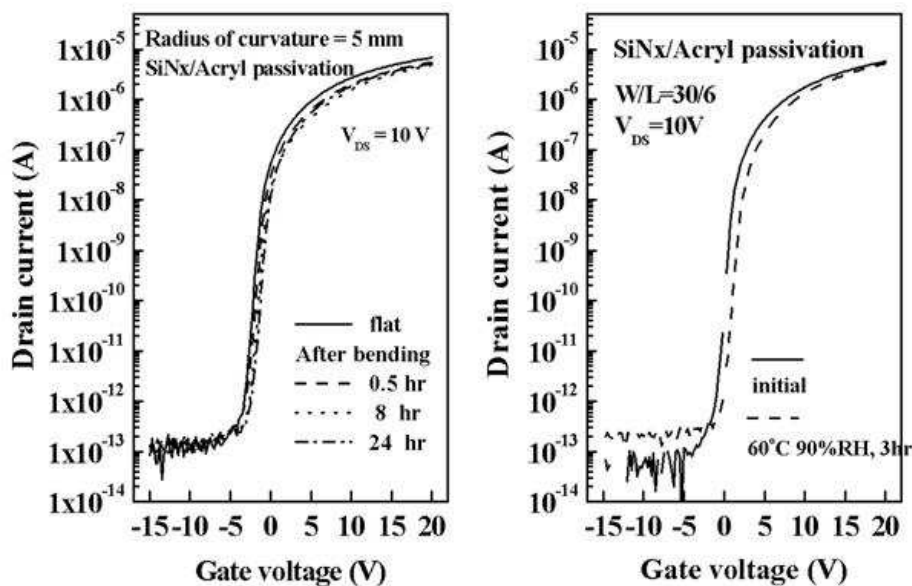


Fig. 11. Transfer characteristics for the hybrid passivation TFT as bending duration time. The radius of curvature  $R$  is 5 mm (left). Transfer characteristics for the hybrid passivation TFT stored at 60°C and 90 % RH for 3 hour (right)

To investigate moisture a permeation phenomenon dependent on the passivation materials, TFTs were kept at 65 °C and 90 % relative humidity (RH). The electrical performances of the

SiN<sub>x</sub>/acryl-passivated TFTs were measured after 3-hour humidity-temperature test. Fig. 11 (right) shows transfer curves before and after the humidity-temperature test. The threshold voltage shift was 1 V after 3-hour humidity-temperature test. It was reduced compared to the threshold voltage shift of the single acryl passivated TFT (2.8 V). 50 nm-thick SiN<sub>x</sub> could somewhat prevent moisture penetrating into TFT.

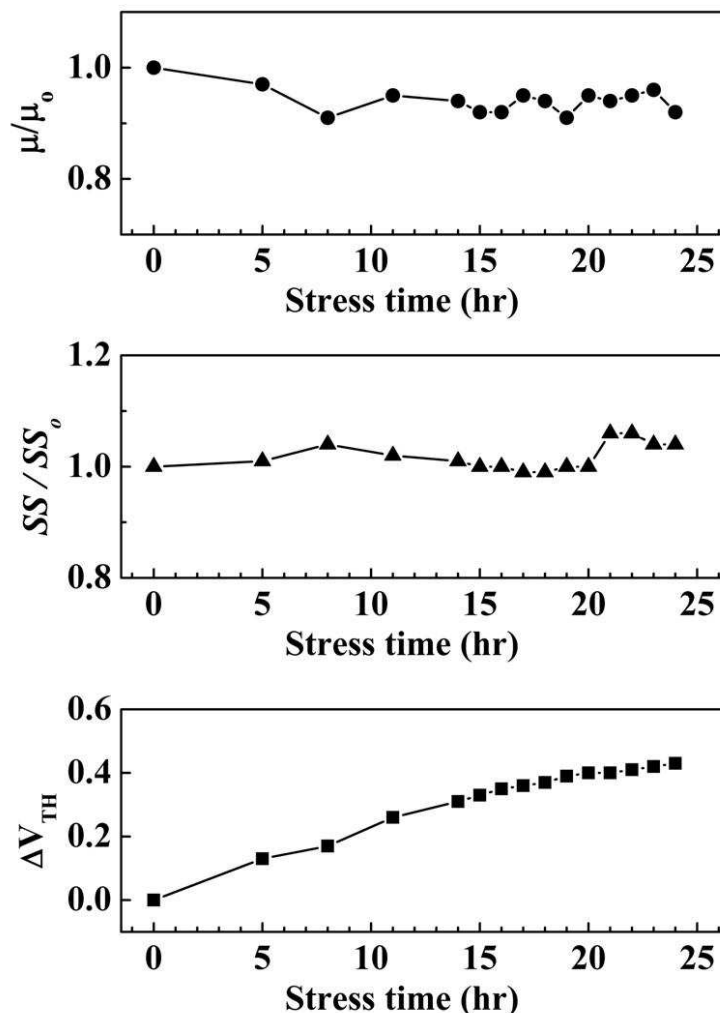


Fig. 12. Electrical performances for the hybrid passivation TFT are shown as bending duration time. TFTs were measured as bended except 0-hour stress time. The data at 0-hour stress time were measured from the flattened-TFTs before bending.

#### 4. Substrate bias effect on the recovery of shifted threshold voltage in a-Si:H TFTs

##### 4.1 Negative gate bias effects

TFT stability is a key issue for AMOLED displays. The threshold voltage of the a-Si:H TFTs changes with the application of the gate bias voltage. In a conventional 2-TFT pixel circuit, the output current is sensitive to the  $\Delta V_{TH}$  of the driving TFT. This leads to a degradation of the luminance of the OLED pixel over time. The  $\Delta V_{TH}$  is because of carrier trapping and the

creation of dangling bonds at the interface of the a-Si:H and SiN<sub>x</sub> layers. Electrical performances measured under a prolonged gate bias of +15 V and a drain bias of +15 V at 65 °C applied for 3,500 s. Fig. 13 shows a drain current drop, a mobility change, and a  $\Delta V_{TH}$  under BTS measurements. The BTS decreased the drain current by 32 % in comparison with the initial drain current. The threshold voltage shift was about 2.3 V whereas the mobility almost maintained under BTS measurements. The drain-current reduction was due to the threshold voltage shift not to the mobility change.

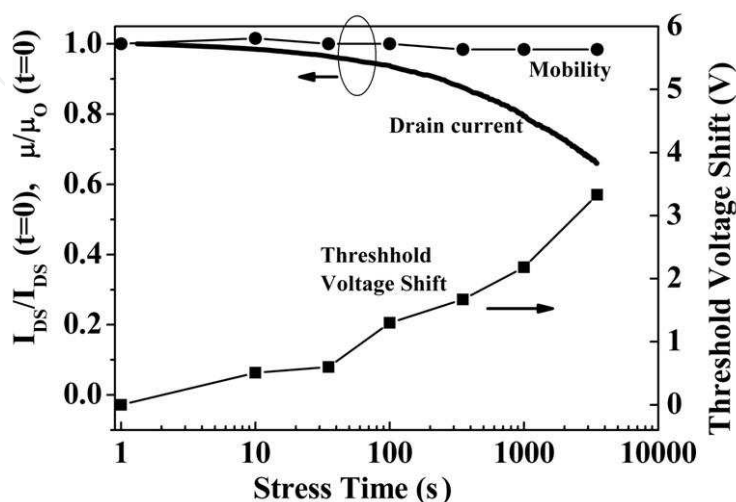


Fig. 13. Drain current, mobility, and threshold voltage transition of a-Si:H TFT under a bias-temperature-stress measurement ( $V_{GS}=V_{DS}=15$  V, 65 °C). The current drop is attributed to the threshold voltage shift in a-Si:H TFT.

Researchers have introduced several methods to reduce the sensitivity of the current to  $\Delta V_{TH}$ . They are the current-programmed circuit, voltage-programmed circuit, and reverse bias annealing methods. In particular, the reverse bias annealing method used the effect of negative gate bias applied to a-Si:H TFT on the negatively  $\Delta V_{TH}$ . The electrons which were trapped at the interface of a-Si:H and SiN<sub>x</sub> by the positive gate bias were injected from the interface so that the gate potential for a desired electron current is reduced by de-trapped electrons. In reverse bias annealing method,  $\Delta V_{TH}$  reduced by a fraction time annealing. During the fraction time, we applied a reverse bias to the gate electrode of a driving transistor. Then  $\Delta V_{TH}$  was suppressed and the reduced drain-current can recover as the negative gate voltage. However, all of these methods need more than three TFTs and many bus lines for each pixel. These methods are too complicated in a driving scheme to achieve a highly reliable display.

When we used metal foil as a substrate, the surface of the metal foil should be planarized and insulated by dielectric materials, which is called as the planarization layer. We have to consider the captive coupling between the display circuits and the conductive metal foil substrate for the design of displays. The captive coupling from the metal foil substrate caused more data and scan line delay than in the glass substrate case. Therefore, the planarization layers preferred a larger thickness and a low dielectric constant to reduce the captive coupling. On the other hand, we can use the metal foil substrate as a common power. If a negative bias is applied to the metal foil substrate the captive coupled gate electrode is

induced as a negative bias, which recovers the  $\Delta V_{TH}$  of the a-Si:H TFT without additional complicated circuits.

#### 4.2 Substrate bias effect on the recovery of shifted threshold voltage in a TFT array

We planarized the metal foil substrate by dielectric materials in order to reduce the surface roughness of the substrate. This planarization layer acted as a capacitor between the gate electrode and the metal foil substrate. When we grounded  $V_{DD}$  and biased the substrate as a negative voltage during idle time, the floating gate electrode of the driving transistor was charged with a negative voltage by the dielectric capacitor. If we use the substrate bias effect in AMOLED displays, we should consider the pixel circuits with two transistors and one capacitor (2T1C) as shown in Fig. 14. Just before idle time, a constant  $V_{DATA}$ , for example 0 V, is required to set the initial voltage of the floating gate electrode of the driver TFT. Next, a negative select voltage is required to maintain the off state of the switch TFT during the idle time. During the idle time, we grounded  $V_{DD}$  and  $V_{SUB}$  supplied a negative voltage to enable recovery of the degraded driver TFT. In the 2T1C circuit, the voltage of the floating gate ( $V_{FG}$ ) is also influenced by the storage capacitance ( $C_{ST}$ ). After the driving transistors were degraded, which meant a drain-current drop and a threshold voltage increase, the negative voltage at the substrate and grounded- $V_{DD}$  lines during idle time enabled recovery of the degraded transistors.

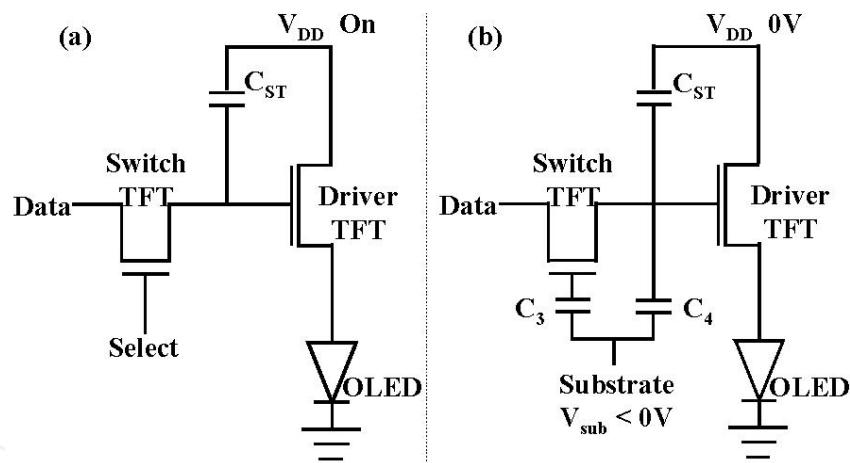


Fig. 14. Two-transistor and one-capacitor pixel circuits for AMOLED: (a) the operating circuit and (b) the recovery circuit during idle time ( $V_{SUB} < 0$  V,  $V_{DD} = 0$  V)

4-inch diagonal TFT array was designed for AMOLED display of which pixel circuit was 2T1C configuration. Fig. 15 shows pixel circuit considering parasitic and substrate capacitances. Node A indicates the floating gate electrode of the driving TFT, which will be induced negative bias by the negative substrate bias. The capacitance per unit area of planarization, SiNx/a-Si:H, and SiNx passivation is  $2.4 \times 10^{-17}$ ,  $1.27 \times 10^{-16}$ , and  $1.51 \times 10^{-16}$ , respectively. The voltage at node A, which was charged by substrate bias, was verified by SPICE simulation. One pixel design and the simulation parameters are shown in Fig. 16.

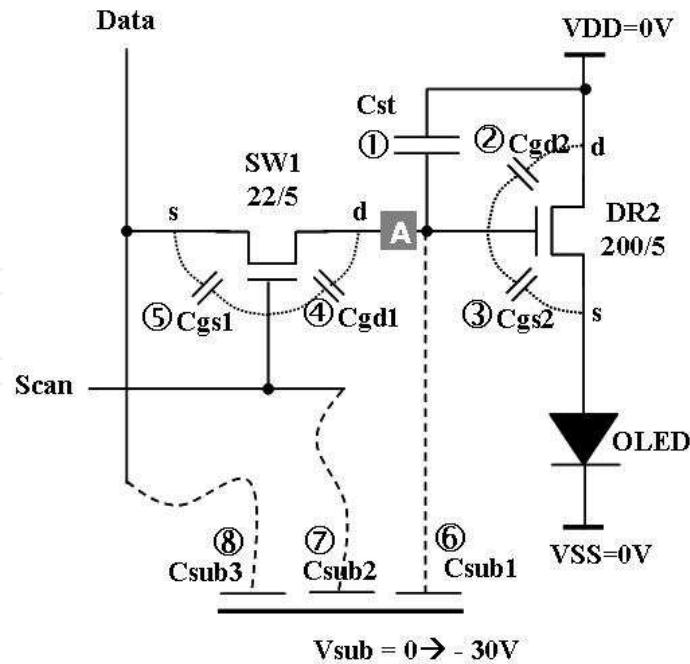


Fig. 15. Pixel circuit considering parasitic capacitances and substrate capacitances. The size of switching and driving TFT is  $22/5 \mu\text{m}$  and  $200/5 \mu\text{m}$ , respectively. Node A means the floating gate electrode of the driving TFT.

Before supplying a negative bias at the metal foil substrate,  $V_{DD}$  was set as 0 V. Data and scan line were applied 0 and -5 V, respectively, then both lines were cut off from electrical sources. The gate electrode of the driving TFT floated.  $V_{SUB}$  swung from 0 to -30 V then the floating gate electrode of the driving TFT was negatively biased. The level of voltage is defined as capacitance sharing among capacitances connected to the node A. The voltage of the node A can be calculated by a following relationship.

$$V_A = \frac{C_{sub1}}{C_{st} + C_{gd2} + C_{gs2} + C_{gd1} + C_{sub1}} \cdot V_{sub} \quad (2)$$

Fig. 17 shows the simulation results of the voltage applied to node A as  $V_{SUB}$  swung from 0 to -30 V. The voltage of Node A ( $V_A$ ) was compared from data simulated by SPICE and data calculated from Eq. (2).

4-inch diagonal TFT array which had  $320 \times 3 \times 240$  pixels was fabricated for AMOLED display of which pixel circuit was 2T1C configuration. Fig. 18 shows a-Si:H TFT backplane fabricated on a metal foil substrate. The a-Si:H TFT array and magnification of one pixel including 2-transistor and 1-capacitor is shown in Fig. 19. The recovery of the drain current and the negative shift of threshold voltage, as a function of the substrate bias, are shown in Fig. 20. The size of driving TFT is  $W = 200$  and  $L = 5 \mu\text{m}$ . The  $V_{TH}$  of the TFT increased as 0.95 V and the drain-current decreased as 83 % of the initial value under a gate bias of +15 V and a drain bias of +15 V at  $65^\circ\text{C}$  applied for 3,500 s.  $V_{TH}$  decreased as -1.19 and 1.74 V and the drain-current recovered 111 and 154 % of its initial value when the substrate voltage was -25 and -30 V at  $65^\circ\text{C}$  applied for 3,500 s, respectively.

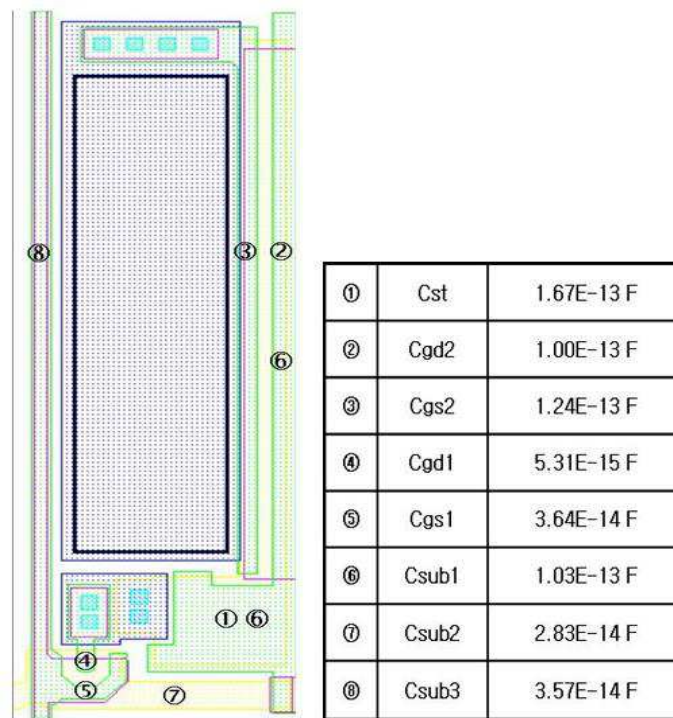


Fig. 16. Lay-out of one pixel and simulation parameters to get the voltage at the floating gate electrode by the substrate bias

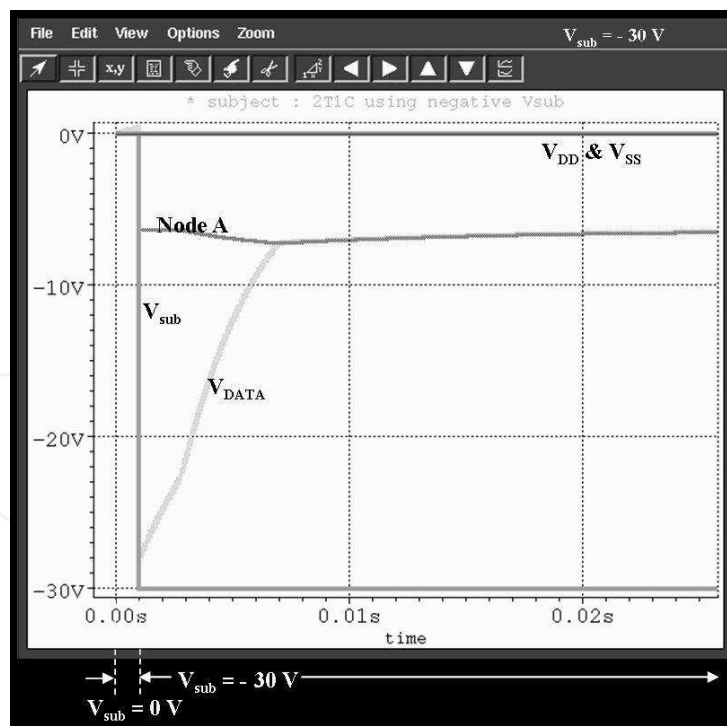


Fig. 17. Simulation results of the voltage applied to node A as  $V_{SUB}$  swung from 0 to -30 V. About -7.2 V is induced at the Node A.



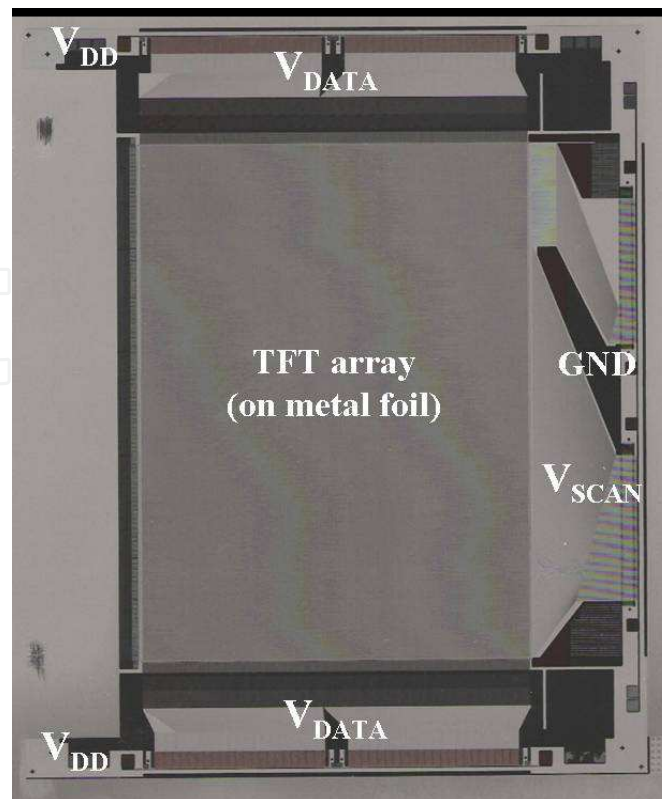


Fig. 18. 4 inch diagonal a-Si:H TFT backplane fabricated on a metal foil substrate. This is designed for AMOLED display.

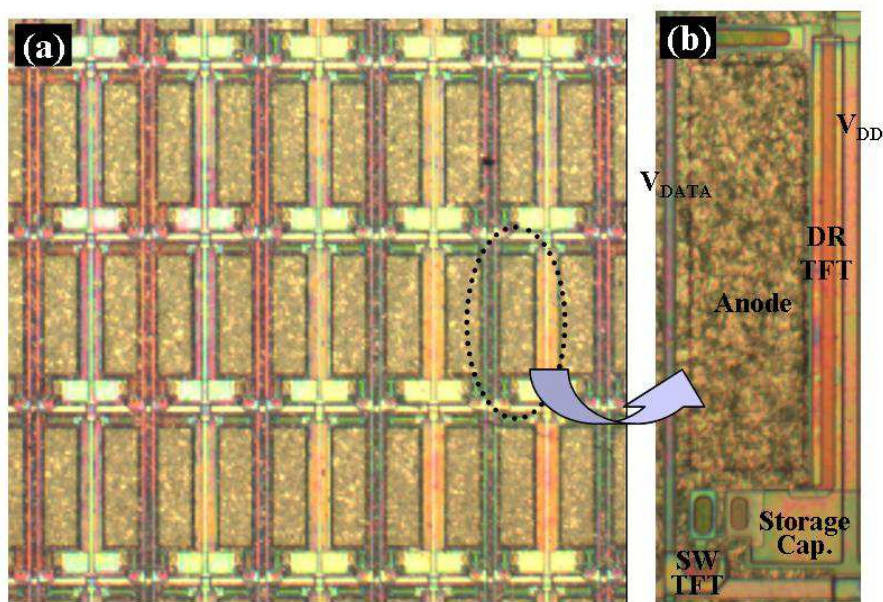


Fig. 19. (a) a-Si:H TFT array fabricated on a metal foil substrate (b) magnification of one pixel including 2-transistor and 1-capacitor.

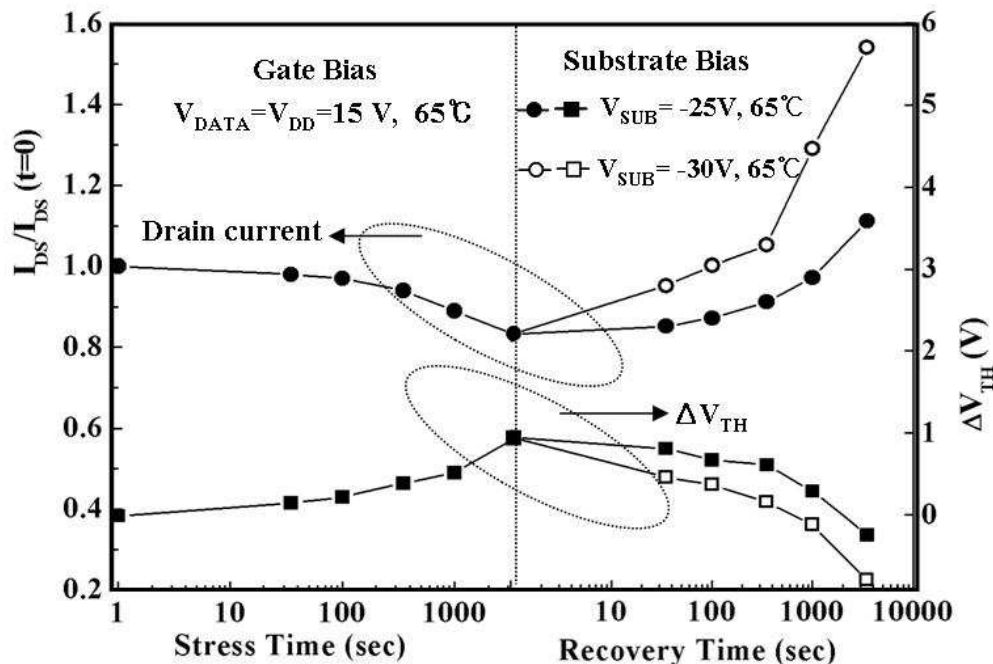


Fig. 20. Drain current and threshold voltage transition of a driving TFT as a function of stress and recovery time.  $V_{\text{DATA}} = V_{\text{DD}} = 15\text{V}$  is applied to the driving TFT at  $65^\circ\text{C}$  for stress time and  $V_{\text{SUB}} = -25$  and  $-30\text{V}$  is applied to metal foil substrate at  $65^\circ\text{C}$  for recovery time.

## 5. Cathode contact top emitting OLED

### 5.1 Comparison between anode-contact and anode-contact configuration

To control the current of the OLED through the a-Si:H TFT, optimum pixel circuit designs should be considered. Since the conventional top emitting OLED (TOLED) has an anode at bottom and a cathode on top, it is electrically connected to the driving TFT through the anode. We call this structure an anode-contact structure with the TOLED (ACTOLED) as shown in Fig. 21 (a). In this structure, the current of the driving TFT is dependent of the operating voltage of the OLED ( $V_{\text{OLED}}$ ). The situation can get even worse during the degradation of the display since the  $V_{\text{OLED}}$  increases affecting the gate-source voltage of the driving TFT. Some groups have proposed a cathode-contact structure to solve the problems generated from the ACTOLED. They employed an inverted-TOLED, i.e. making TOLED that has a cathode at bottom and an anode on top. However, one major challenge in the inverted-TOLED has been to prepare a reflective cathode providing an effective electron injection. Based on such considerations, low work-function metals, such as Mg and Li were introduced to reduce the turn-on voltage. However, there remained issues in employing highly reactive metals particularly their handling and operational stability. Another group has demonstrated a more complicated structure using an ultra thin  $\text{Alq}_3\text{-LiF-Al}$  trilayer as the electron-injection layer.

In this section, we propose a new cathode-contact structure employing the normal TOLED (CCTOLED) that has an anode at bottom and a cathode on top (Fig. 21 (b)). We also compare the electrical characteristics between the CCTOLED and ACTOLED pixel structure.

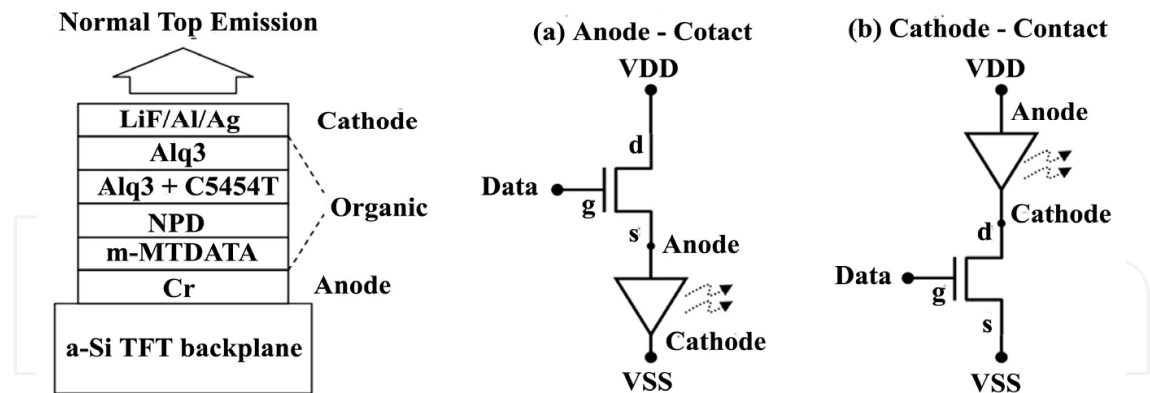


Fig. 21. Structure and circuit implementation of normal top-emission AMOLED (TOLED) pixel: (a) anode-contact with a-Si:H TFT (ACTOLED) and (b) cathode-contact with a-Si:H TFT (CCTOLED)

## 5.2 Process flow to make cathode-contact pixel structure

The schematic of the fabrication process is illustrated in Fig. 22. The a-Si:H TFT was fabricated on the glass substrate (Fig. 22 (a)). The structure of a-Si:H TFT was an inverted staggered type, which was made by a conventional 5-photomask process. We deposited a reflective anode by a sputter process and patterned by photolithography. It covered all the pixel-area as a common electrode keeping away from the contact area on the drain electrode of the TFT (Fig. 22 (b)). A step-covering layer was located over the step area of the anode to minimize the probability of the breakdown of the emission layer at the step area of the anode. It was made by 1  $\mu\text{m}$ -thick polyimide which was spin-coated and photo-patterned opening the drain electrode of TFT. A separator layer which separates cathode layer as sub-pixels was made by 2  $\mu\text{m}$ -thick negative photo-resist from spin coating and photolithography (Fig. 22 (c)). All organic layers including common layers for each color, such as hole-injection, hole-transport, and electron-transport layer were thermally evaporated through the shadow mask on the anode, not evaporated on the drain electrode of TFT (Fig. 22 (d)). Finally, electron-injection layer, cathode aluminum (Al) and silver (Ag) were thermally evaporated and then were made to contact the drain electrode of the TFT (Fig. 22 (e)). Each of the cathode layers of sub-pixel is automatically patterned during evaporation by separator. Then, the cathode-contact structure, employing a normal TOLED, was completed. The organic layers of the TOLED were prepared with the following structures: Cr (100 nm) / m-MTDATA (30 nm) /  $\alpha$ -NPD (30 nm) / Alq<sub>3</sub>+C545T (25 nm) / Alq<sub>3</sub> (35 nm) / LiF (0.5 nm) / Al (1 nm) / Ag (15 nm). The organic multilayer structure sequentially consisted of 4,4',4''-tris(3-methylphenylphenylamino) triphenylamine (m-MTDATA, 30 nm) as the hole-injection layer,  $\alpha$ -naphthylphenylbiphenyl ( $\alpha$ -NPD 30 nm) as the hole-transport layer, tris-(8-hydroxyquinoline) aluminum doped with 1 wt% 10-(2-Benzothiazolyl)-2,3,6,7-tetrahydro-1,1,7,7-tetramethyl-1H,5H,11H-(1)-benzopyrano (6,7-8-i,j)quinolizin-11-one (Alq<sub>3</sub>+C545T, 25 nm) as the emitting layer, and tris-(8-hydroxyquinoline) aluminum (Alq<sub>3</sub>, 35 nm) as the electron-transport layer.

Fig. 23 shows a SEM image of the fabricated pixels. The cathode layer of sub-pixel is successfully isolated by separator (Fig. 23 (a)). And it is connected with the drain of a-Si:H TFT through the via hole which is formed by step-covering layer (Fig. 23 (b)).

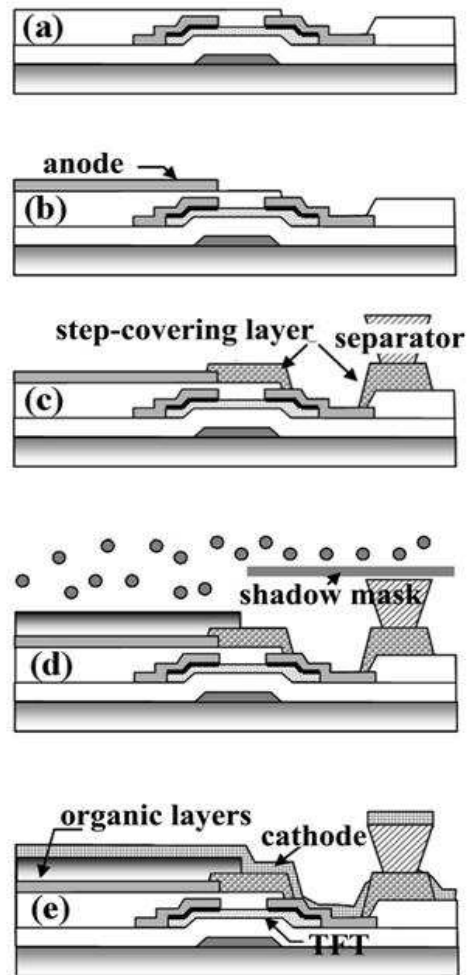
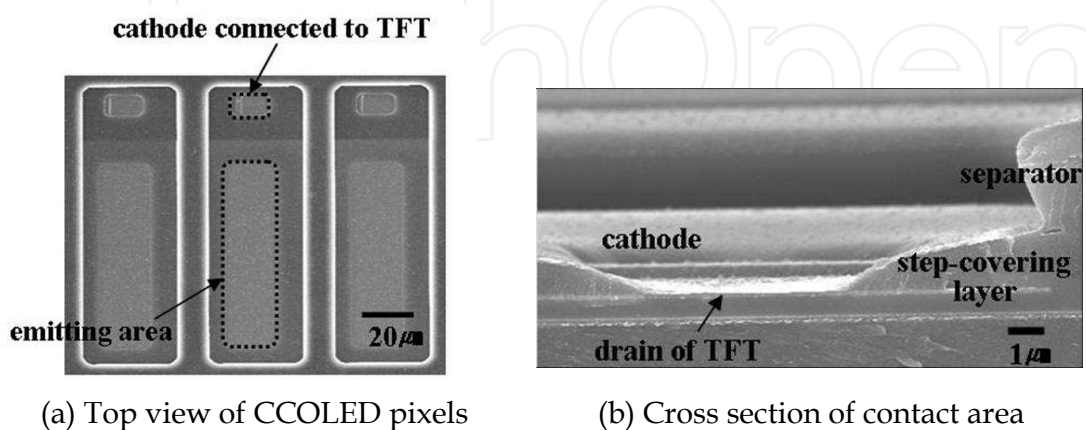


Fig. 22. Fabrication process flow of a newly proposed normal top-emission OLED pixel employing cathode-contact structure (a) a-Si:H TFT, (b) reflective anode, (c) step-covering layer and separator, (d) organic layer evaporation through the shadow mask on the anode, (e) cathode evaporation.



(a) Top view of CCOLED pixels (b) Cross section of contact area  
 Fig. 23. SEM image of fabricated cathode-contact type OLED pixel

### 5.3 Electro-optic characteristics

To investigate the pixel performances of the CCTOLED and ACTOLED cells employing the same TFT and TOLED, we designed and fabricated a unit cell having an emitting area of  $1 \times 1 \text{ mm}^2$ . The off current of TFT was about  $10^{-9} \text{ A}$ . The on current, at a gate voltage of  $20 \text{ V}$ , was about  $10^{-3} \text{ A}$  at a drain voltage of  $10 \text{ V}$  resulting in an on-off current ratio of  $10^6$ . We obtained a subthreshold slope of approximately  $0.74 \text{ V/decade}$  demonstrating a sharp device turn-on. The threshold voltage and the saturation mobility were  $1.8 \text{ V}$  and  $0.34 \text{ cm}^2/\text{Vs}$ , respectively. Fig. 24 shows the current of the OLED ( $I_{\text{OLED}}$ ) as a function of the  $V_{\text{DATA}}$ . When the  $V_{\text{SS}}$  was grounded, the ACTOLED showed lower  $I_{\text{OLED}}$  as compared with the CCTOLED. The  $I_{\text{OLED}}$  of the ACTOLED and the CCTOLED at  $V_{\text{DATA}} = 14 \text{ V}$  and  $V_{\text{DD}} = 27 \text{ V}$  were  $1.2 \times 10^{-4} \text{ A}$  and  $9.5 \times 10^{-4} \text{ A}$ , respectively.

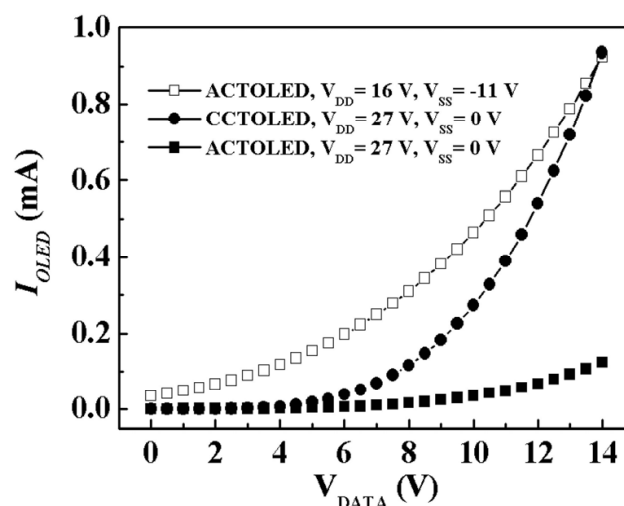


Fig. 24. Current of the OLED as a function of  $V_{\text{DATA}}$  compared between the ACTOLED and the CCTOLED

In the case of the ACTOLED, the effective gate voltage ( $V_{\text{GE}}$ ) of the driving TFT decreased, which was defined as the difference of the  $V_{\text{DATA}}$  and the source voltage of the driving TFT ( $V_{\text{S}}$ ) as shown in Fig. 21. The lower current of the ACTOLED was attributed to this lowered- $V_{\text{GE}}$ . As a result, the ACTOLED was inappropriate for a high luminance display when the  $V_{\text{SS}}$  was grounded. When a negative voltage was supplied at the  $V_{\text{SS}}$  in order to increase the current value in the ACTOLED as shown in Fig. 21, the  $I_{\text{OLED}}$  of the ACTOLED could reach the same amount as that of the CCTOLED at  $V_{\text{DATA}} = 14 \text{ V}$ . However the  $I_{\text{OLED}}$  of the ACTOLED at  $V_{\text{DATA}} = 0 \text{ V}$ ,  $V_{\text{DD}} = 16 \text{ V}$ , and  $V_{\text{SS}} = -11 \text{ V}$  and the CCTOLED at  $V_{\text{DATA}} = 0 \text{ V}$ ,  $V_{\text{DD}} = 27 \text{ V}$ , and  $V_{\text{SS}} = 0 \text{ V}$  were  $3.4 \times 10^{-5} \text{ A}$  and  $3.6 \times 10^{-8} \text{ A}$ , respectively. In the case of the ACTOLED even though the  $V_{\text{DATA}}$  was set as  $0 \text{ V}$ , the  $V_{\text{GE}}$  was not zero because the  $V_{\text{S}}$  of the driving transistor was induced as a negative voltage when the  $V_{\text{SS}}$  was set as a negative value. The contrast ratio, which means the ratio of the white and black level, is low because of a leakage light at the black level. On the other hand, the  $I_{\text{OLED}}$  of the CCTOLED independent of the  $V_{\text{OLED}}$ , this meant that the  $V_{\text{GE}}$  was always equal to the  $V_{\text{DATA}}$ . Therefore, the CCTOLED was suitable for better image performances having high luminance and contrast ratio at the same driving conditions. Fig. 25 shows the current density characteristics of the CCTOLED as a function of the  $V_{\text{DATA}}$  and the  $V_{\text{DD}}$ . Well-saturated

characteristics were shown over  $V_{DD} = 15$  V and less than  $V_{DATA} = 10$  V which were the driving condition for real displays.

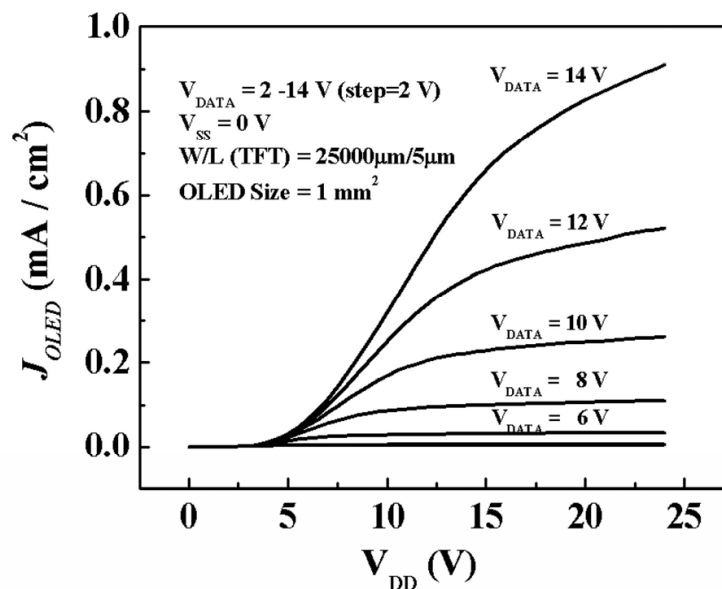


Fig. 25. Current density of the OLED as a function of  $V_{DD}$  and  $V_{DATA}$

## 6. Conclusion

In this paper, electrical performances and new approaches to increase the stability of a-Si:H TFT fabricated on a metal foil substrate were reported. A new cathode-contact structure employing a normal top emitting OLED also was proposed and compared with an anode-contact structure by experimental data.

76- $\mu$ m-thick metal foil laminated on the rigid glass plate. On top of this foil, the rough surface was planarized and the inverted staggered a-Si:H TFT was fabricated at 150°C. The acrylic polymer as a planarization layer was well matched to a-Si:H TFT fabricated at 150°C. The a-Si:H TFT of which size was  $W=30$   $\mu$ m and  $L=6$   $\mu$ m showed the good electrical performances. The off current was about  $10^{-13}$  A and the on current at gate voltage of 20 V is about  $10^{-6}$  A at a drain voltage of 10 V, resulting in an on-off current ratio of  $10^7$ . We obtained a threshold voltage and mobility of 1.0 V and  $0.54$  cm<sup>2</sup>/Vs, respectively, in the saturated regime.

The effect of passivation layer on the performances of a-Si:H TFT under mechanical stress was investigated. The acryl-passivated TFT could endure mechanical stress better than the SiNx-passivated TFT. However, a larger threshold voltage shift was observed for the acryl-passivated TFT when a humidity-temperature test was carried out. The hybrid passivation, which was composed of SiNx and acrylic polymer was proposed. It secured the degradation of electrical performances under the mechanical stress and somewhat prevented moisture penetrating into TFT.

We have studied a negative bias effect using the substrate bias without additional circuits to enable recovery of the degraded drain-current of a driving TFT in 2T1C pixel circuit, which was fabricated on a metal foil substrate. When  $V_{DD}$  was grounded and the substrate was biased as a negative voltage during idle time, the floating gate electrode of the driving

transistor was induced as a negative voltage by the dielectric capacitor. The degraded drain current of the driving transistor can be recovered during the idle time by simply applying a negative substrate bias. The power consumption can be neglected during the idle time because no current flows.

Cathode-contact structure pixel structure employing normal TOLED was proposed for a-Si:H TFT backplane. The new top-emission AMOLED pixel structure employing the TOLED as well as the cathode-drain contact structure was proposed and fabricated. The structure of TOLED had a cathode at bottom and an anode on top. The negative photo-resist separator wall successfully patterned the pixel cathode layers. As the electrical performances of CCTOLED and ACTOLED were compared, the CCTOLED was verified more suitable for better display performance having a high luminance and a high contrast ratio.

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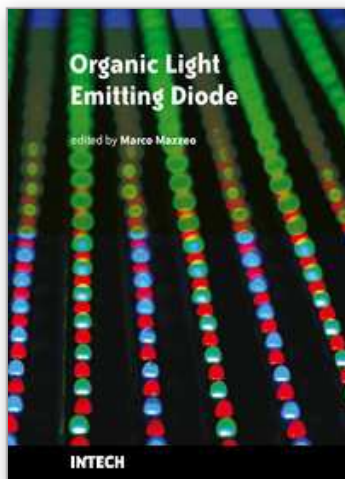
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## **Organic Light Emitting Diode**

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Organic light emitting diodes (OLEDs) have attracted enormous attention in the recent years because of their potential for flat panel displays and solid state lighting. This potential lies in the amazing flexibility offered by the synthesis of new organic compounds and by low-cost fabrication techniques, making these devices very promising for the market. The idea that flexible devices will replace standard objects such as television screens and lighting sources opens, indeed, a new scenario, where the research is very exciting and multidisciplinary. The aim of the present book is to give a comprehensive and up-to-date collection of contributions from leading experts in OLEDs. The subjects cover fields ranging from molecular and nanomaterials, used to increase the efficiency of the devices, to new technological perspectives in the realization of structures for high contrast organic displays and low-cost organic white light sources. The volume therefore presents a wide survey on the status and relevant trends in OLEDs research, thus being of interest to anyone active in this field. In addition, the present volume could also be used as a state-of-the-art introduction for young scientists.

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