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TFT-LCD Driver IC Design

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1. Introduction

With the rapid evolution of liquid crystal display (LCD) television (TV), there is a large demand for developing high resolution, high color depth driver integrated circuits (ICs) [1-3]. The panel of an LCD-TV is larger, and has higher definition, than that of a computer monitor. As a result, its color quality requires more accuracy. For example, computer monitors have $2^{6\times3}$ (262,144) or $2^{8\times3}$ (16,777,216) colors. However, a typical LCD-TV has $2^{10\times3}$ (1,073,741,824) colors [2-3]. To develop a high-quality display module, LCD-TV driver systems require higher color depth and resolution. An LCD driver system generally includes column drivers, row drivers, a timing controller, and a reference source. The column drivers are especially critical for achieving a high-quality display [1, 4-5]. For LCDTV applications, drivers must process 10-bit digital input codes and then convert the input codes to analog levels [6-7].

A column driver generally includes shift registers, input registers, data latches, level shifters, DACs, and output buffers [1, 8-9]. Among these components, the DACs occupy the largest area. Due to the hundreds of channels built into a single chip, it is desirable to reduce the area of the DAC, especially for high color depth displays.

To improve the lifetime of the liquid crystal material, the liquid crystals of active matrix liquid crystal displays (AMLCDs) should be driven by the so-called inversion method, which alternates the positive and negative polarities between the liquid-crystal cells with respect to a common backside electrode. Designers use four inversion methods for AMLCD driving: frame, line, column, and dot inversions. High-quality displays prefer the dot inversion method [1, 8]. Figure 1 schematically shows the operation of the dot inversion method. In this method, the backside electrode is at a fixed voltage and a negative-to-positive or positive-to-negative voltage with respect to the fixed voltage of the backside electrode must be driven from the LCD column drivers with alternating polarities between data lines and line times [1, 10]. Hence, the LCD driver IC should supply both positive and negative polarity voltages for a digital sub-pixel code. This increases the resolution of the DAC by one bit, and hence increases the die area.

Figure 2(a) shows the characteristic transmittance-voltage curve of a liquid crystal (LC), which exhibits a nonlinear response to the applied voltage. To obtain a linear luminance output with the digital input code for an LCD, the DAC response is usually set as the inverse of the LC characteristic, as Figure 2(b) indicates [10]. The DAC output should cover both positive and negative polarity voltages. The LCD driver IC usually utilizes R-DACs. To compensate for the nonlinear LC characteristic, gamma correction voltages are applied to

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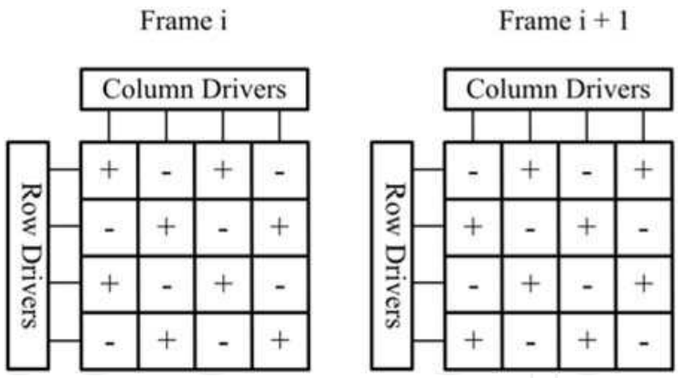

Fig. 1. The operation for the dot inversion method.

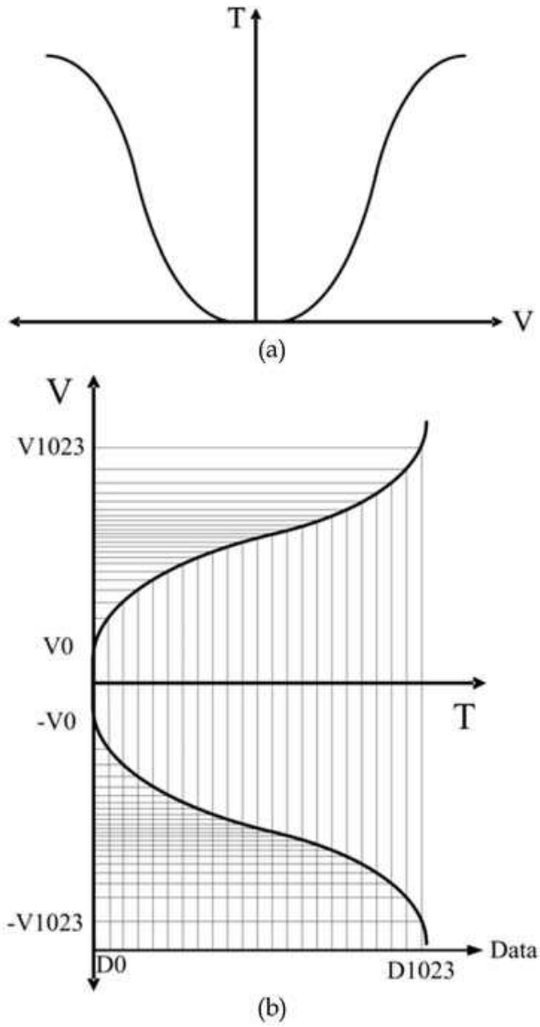

Fig. 2. (a) The characteristic of the liquid crystal. (b) The response of DAC.

the R-DAC resistor string, which makes the resistor values unequal [2-3]. However, the area of the R-DAC and its metal routing will be prohibitively large for a high resolution data converter. This makes the R-DAC impractical for use in column driver ICs for high color

depth displays. As an alternative, previous research has proposed an LCD column driver using a linear switched capacitor DAC [2-3]. In this case, the timing controller compensates for the nonlinear LC characteristic, which greatly reduces the die area. To reduce the die area, the current study proposes a 10-bit LCD column driver, the use of an R-DAC, and a charge sharing DAC (C-DAC) for each channel. This approach applies gamma voltages to the R-DAC to fit the inverse of the liquid crystal characteristic. The gamma correction can also be digitally fine-tuned in the timing controller or column drivers.

2. Conventional column drivers

Figure 3 shows the conventional column driver architecture [1, 8]. The column driver supplies high analog voltages to the LCD panel. To reduce power consumption, the digital circuit uses a low voltage power supply. Digital display data is fed to the RGB inputs and sampled into the input registers. A wide data latch presents one row of serial input pixel data to the level shifters inputs. The level shifters then boost the digital signals to higher levels. The DAC of each channel outputs a voltage level corresponding to a digital sub-pixel code. The output buffers drive the highly capacitive data lines of the LCD panel [11-12]. For a dot inversion operation, the DACs offer voltages with positive and negative polarities for the same digital input code. Hence, 11-bit DACs are needed for a 10-bit column driver.

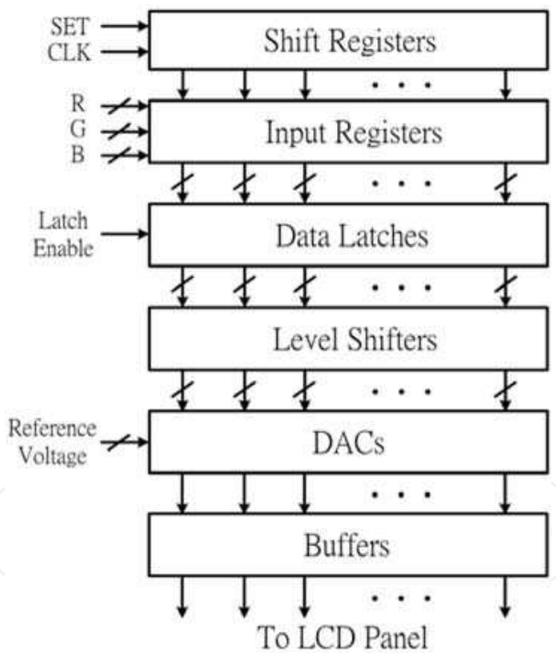

Fig. 3. The conventional column driver architecture.

Since the transmittance response of the liquid crystal to the applied voltage is nonlinear, a nonlinear DAC is needed to obtain a linear transmittance with the digital code. Applying certain gamma voltages to the resistor string of the nonlinear DAC, and the resistor string is made up of unequal resistors to fit the nonlinear curve.

Figure 4 depicts the layout of a conventional column driver. One resistor string is put in the middle of the chip to supply the reference voltages to all channels. Each channel needs a decoder to route the reference voltage, corresponding to the digital input code, to the

corresponding output buffer. Since several hundreds of channels are built into a single chip, the die area of the routing lines connecting the resistor string and the decoders is very large. For example, a 10-bit column driver IC requires 2048 metal lines. Hence, these metal lines and the decoders occupy a very large percentage of the column driver IC's area, especially for high color depth displays.

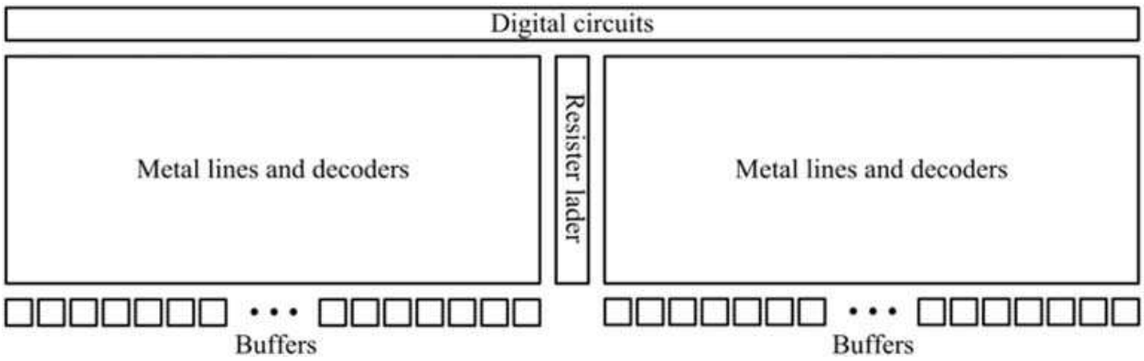

Fig. 4. The layout of the conventional column driver.

To reduce the die area of a column driver for a higher color depth display, Bell employed a linear switched capacitor DAC in his column driver [2-3]. In this arrangement, the timing controller digitally compensates for the nonlinear liquid crystal (LC) characteristic. Since the DAC is linear, additional bits are needed to compensate for the nonlinear LC characteristic. This approach reduces effective resolution.

3. Proposed column driver

This section proposes a 10-bit LCD column driver consisting of piecewise linear DACs.

3.1 Data converter scheme

This study utilizes a piecewise linear compensation mechanism in the proposed column driver to reduce the die area and increase the resolution for a higher color depth display. This design applies gamma voltages to the resistor string of the R-DAC, and uses unequal resistor values to compensate for the nonlinear LC characteristic. Figure 5 shows the characteristic of the piecewise linear DAC and the reverse response of the LC, where V_{G1}, V_{G2}, …, V_{G16} are the external gamma reference voltages. The voltage curve of the piecewise linear DAC is very close to that of the reverse LC response, so these two curves look like identical. Since the characteristic curve of the piecewise linear DAC is much closer to the inverse response of an LC than a fully linear DAC, fewer additional bits are needed to compensate for the nonlinear LC response. Therefore, the effective color depth is much greater than that of a fully linear data conversion. External reference voltages make coarse gamma correction, and a simple digital circuit makes fine compensation adjustments. This digital circuit can be built in the timing controller or the column driver.

Since the proposed column driver IC drives the LCD with positive and negative polarities, the DACs and output buffers are classified into positive and negative components. Figure 6 shows the data conversion scheme. Each channel contains one R-DAC decoder, one C-DAC, and one buffer. Two neighboring channels are grouped together, and take turns driving a pair of adjacent data lines of the LCD panel. One channel is responsible for driving positive

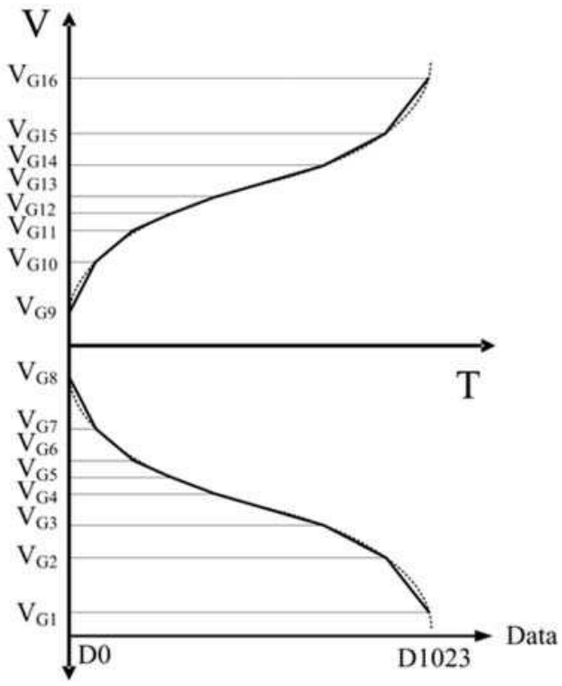

Fig. 5. The characteristic of the piecewise linear DAC and the reverse response of LC.

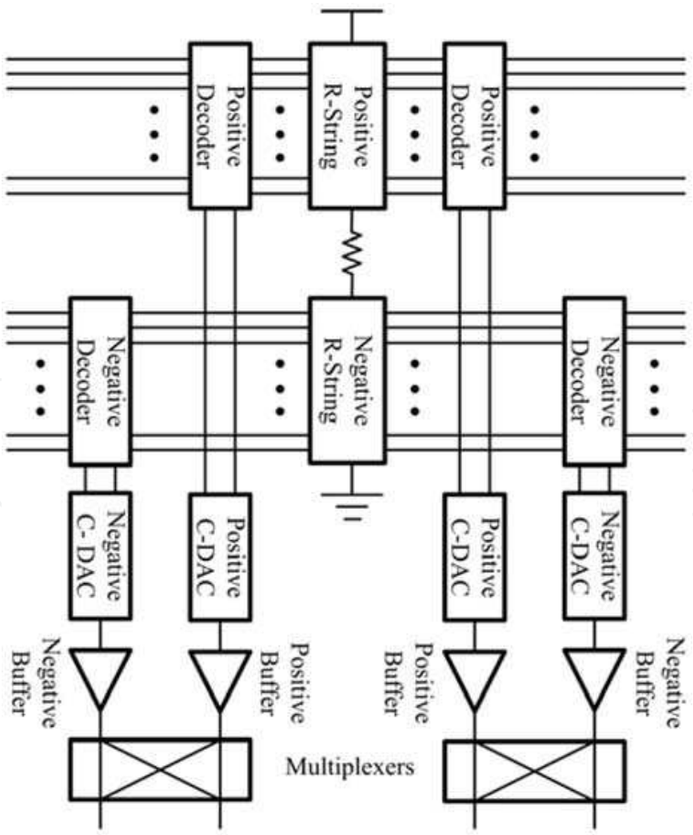

Fig. 6. The data conversion scheme.

polarity and the other for driving negative polarity. The odd DACs and buffers are designed for the negative polarity operation, while the even DACs and buffers drive the positive polarity operation. When the odd column lines are under negative polarity and the even column lines are under positive polarity, the input codes and the output buffers are in a normal order. However, when the polarities of the column lines are exchanged, i.e., the odd and even column lines are alternated to positive and negative polarities, respectively, the orders of the input codes, DACs, and output buffers are exchanged. The negative buffers and the odd DACs still take responsibility for negative polarity operation, and vice versa for the positive buffers and the even DACs. This arrangement reduces the number of decoder bits by one. In other words, only 10-bit decoders are needed for a 10-bit column driver.

3.2 Data converter

The DAC includes a coarse section and a fine section to reduce both the die area and the data conversion time. The 10-bit DAC in this study contains a 7-bit coarse section and a 3-bit fine section implemented by R-DACs and C-DACs, respectively. One resistor string generates the voltage references for all R-DACs in a column driver. Since the DACs cover the positive and negative polarities, the column driver requires an 8-bit resistor string. Each channel contains one 7-bit nonlinear R-DAC and one 3-bit linear C-DAC. Reducing the bit number from 11 to 7 greatly reduces the area of the R-DACs.

Data conversion is serially implemented by the R-DAC and C-DAC. The R-DAC decoder selects two neighboring voltages according to the 7 MSBs and sends them to the CDAC. The C-DAC then uses the two neighboring voltages to perform voltage division and passes the final voltage to the buffer. Figure 7 shows a schematic of the R-DAC, in which the resistor string divides the voltage and generates 256 voltage segments. The upper half of the voltage segments and decoder are used for the positive polarities; the lower ones for negative polarities. The decoders are controlled by the 7 MSBs (b9 ~ b3) in Figure 7. An offset switch array obtains two neighboring voltages (v_i and v_{i+1}) for the C-DAC.

The voltage division in the C-DAC is based on precharging and charge redistribution. Figure 8 shows the schematic of the C-DAC, which consists of 3 binary weighted capacitors, an additional unit capacitor, and a set of switches that can connect the capacitors to the input voltages. Two phases are needed to accomplish the voltage division in this circuit. In the pre-charge phase ($\phi = 0$), the weighted capacitors are connected to v_{i+1} or v_i depending on the 3-bit code (b2 ~ b0). In the evaluation phase ($\phi = 1$), all capacitors are disconnected from the inputs and connected to the output. A charge-redistribution then occurs, and the reconstructed analog value finally appears at the output. The output voltage can be expressed as

$$\begin{aligned} v_{out} &= \frac{2^2 \cdot \left(v_{i+1}b_2 + v_i\bar{b}_2\right) + 2 \cdot \left(v_{i+1}b_1 + v_i\bar{b}_1\right) + \left(v_{i+1}b_0 + v_i\bar{b}_0\right) + v_i}{2^3} \\ &= \frac{\left(4b_2 + 2b_1 + b_0\right)}{8}\left(v_{i+1} - v_i\right) + v_i \end{aligned} \tag{1}$$

Equation (1) shows that the C-DAC divides the voltage for each segment voltage of the R-string and exhibits a 3-bit DAC behavior.

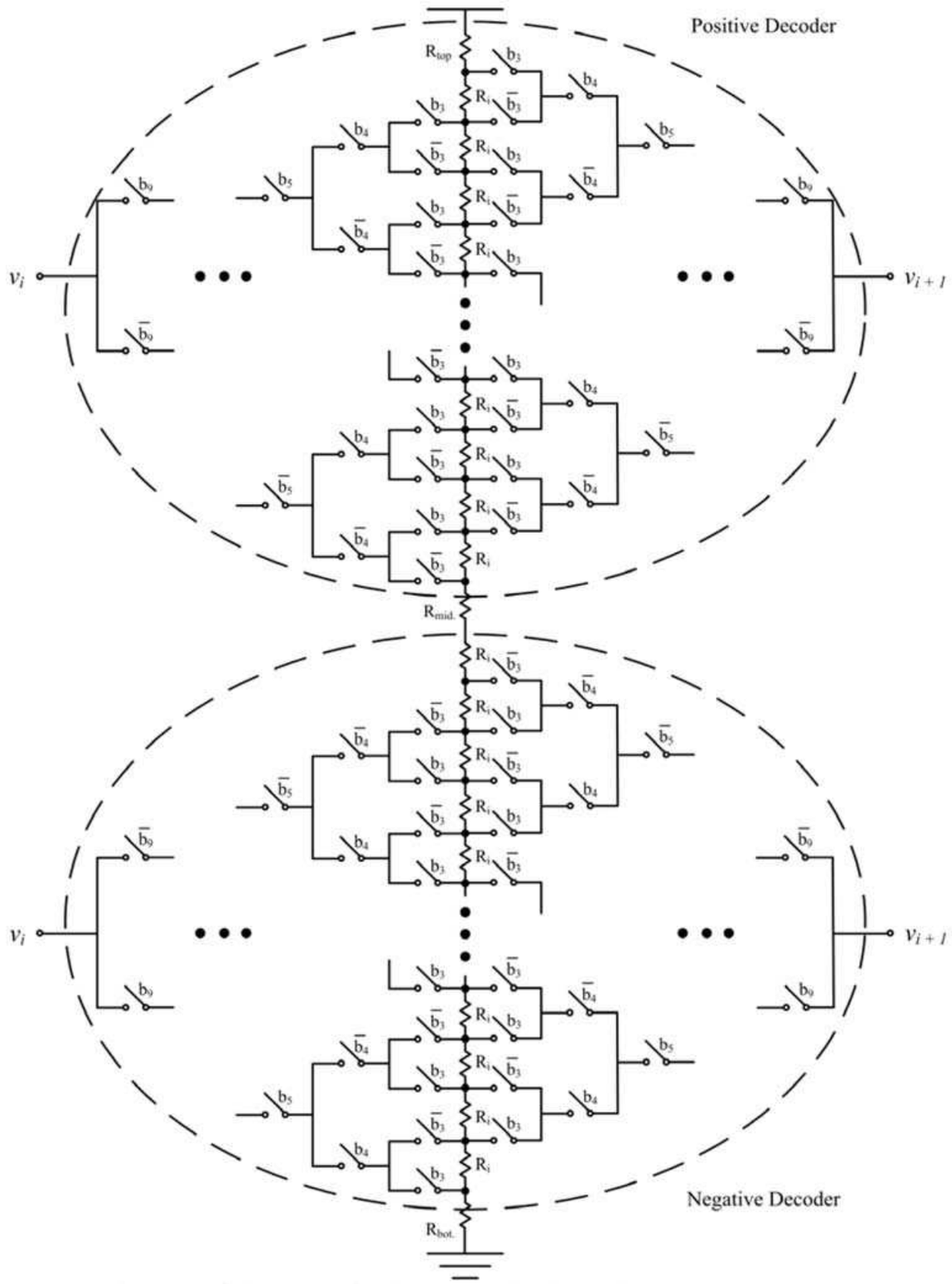

Fig. 7. Schematic of the R-DAC for the proposed column driver.

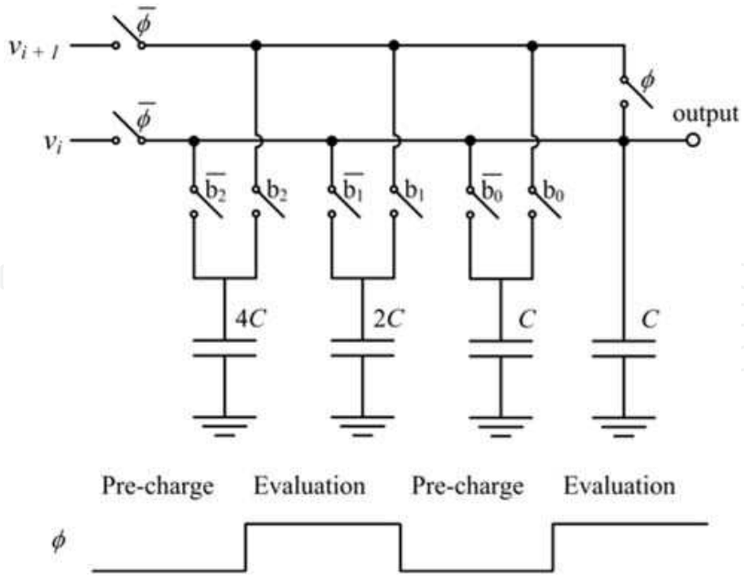

Fig. 8. Schematic of the C-DAC for the proposed column driver.

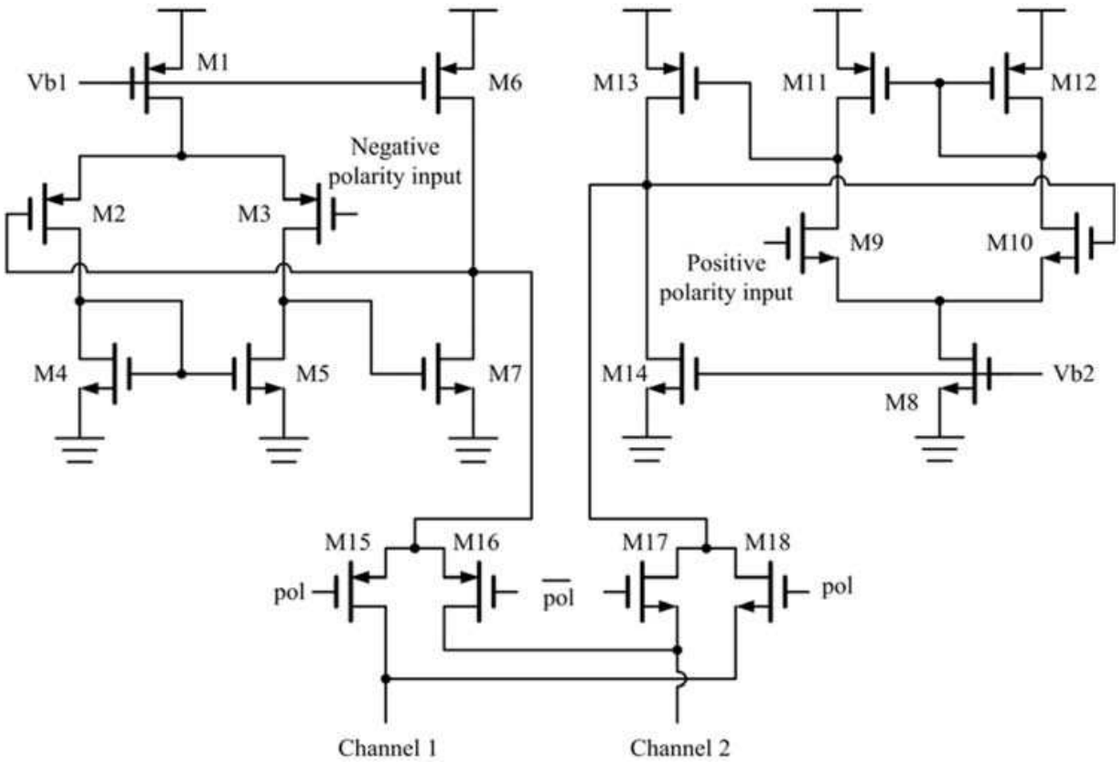

Fig. 9. Schematic of a pair of complementary differential buffers with the switches.

3.3 Output buffer

To drive the data lines of the LCD panel, each channel needs an output buffer. The output buffers, which are usually made of operational amplifiers, drive highly capacitive data lines.

Since the approach in this study classifies the buffers into positive and negative components, rail-to-rail amplifiers are not needed. The PMOS input buffer has a large discharge capability and its common mode input voltage can reach a very low level. Hence, it is used to drive positive-to-negative polarity operation. Similarly, an NMOS input buffer is suitable for the negative-to-positive polarity transition. Figure 9 shows a schematic of a pair of complementary differential buffers with switches [1]. The switches M15-M18, which are controlled by the polarity control signal "pol," are used for the inversion operation. The transistors M1-M7 and M8-M14 are constructed as a PMOS input differential amplifier and an NMOS input differential amplifier, respectively. The compensation scheme has been described previously [1, 4].

3.4 Column driver architecture

Figure 10 shows a block diagram of the LCD column driver based on the data conversion scheme above. In this arrangement, data exchange circuits are attached between the latches and the level shifters to implement the proposed data conversion scheme. The digital input codes are serially read into the input register, which is controlled by the shift registers. After all the data of one row is read and latched on the data latches, it is sent to DACs through the data exchange circuits in parallel. The"pol" signal controls the polarity inversion. The data conversion is implemented by R-DACs and C-DACs in series. The buffers described in the prior section drive the capacitive column lines.

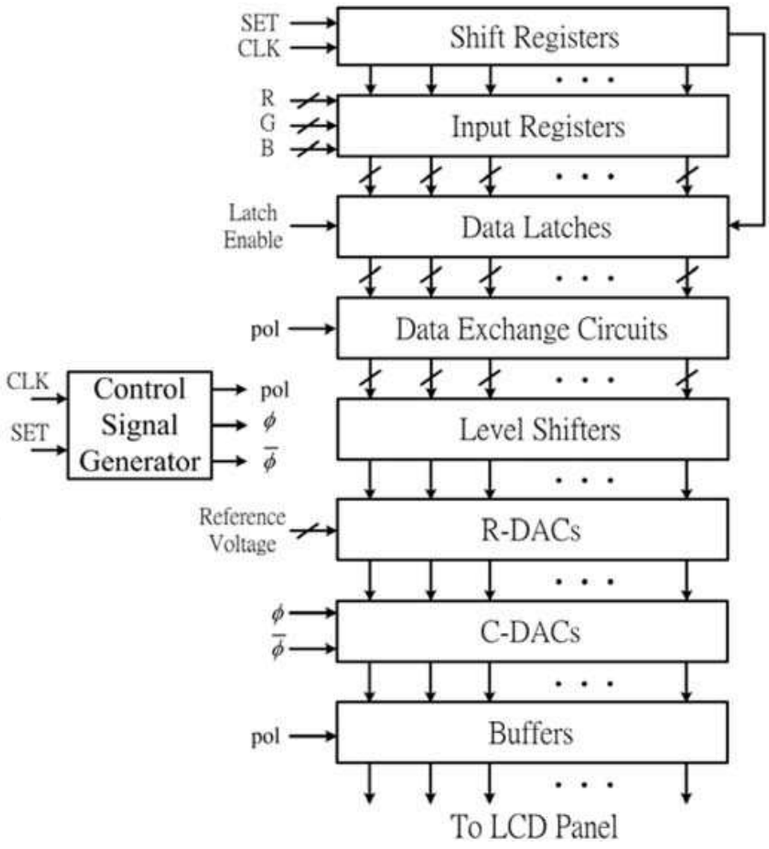

Fig. 10. The implemented block diagram of the LCD column driver architecture.

4. Experimental results

Since the reference voltages are connected to all channels, many DACs may use the same reference voltage. The more DACs there are connected to a single reference voltage, the larger the required C-DAC settling time. This study simulates the settling time for different numbers of connected DACs using a 0.35-μm 5-V CMOS model. Figure 11 shows the simulated results where the settling time is measured at 99.9% of its final voltage for a full swing (0.266 V ~ 4.75 V). The settling time is 5.2 μs when 200 DACs are connected to a single reference voltage. Although a column driver IC contains several hundreds or even up to a thousand DACs, these DACs are distributed to 256 (2^8) reference voltages. This means that not all the DACs are connected to a single reference voltage. A typical UXGA (1600×1200) display has a pixel clock frequency of 162 MHz and a horizontal scanning time of 9.877 μs [4]. Hence, the proposed column driver is suitable for UXGA displays.

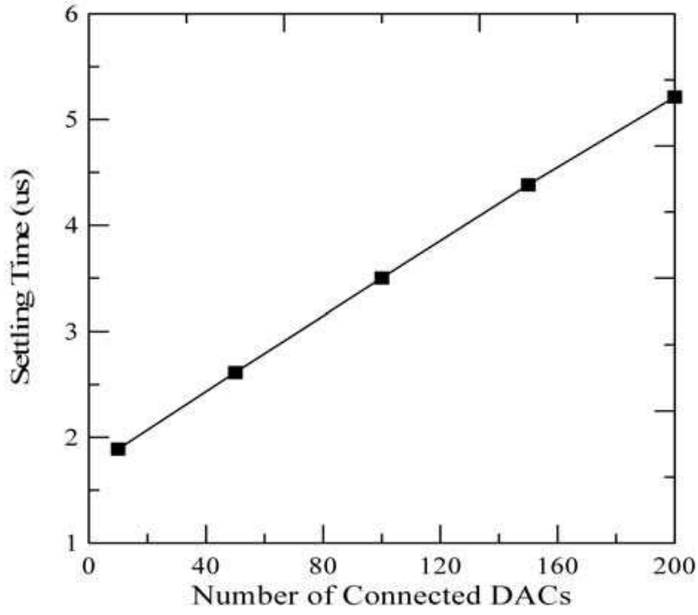

Fig. 11. The simulated maximum settling time of the DAC for different numbers of connected DACs.

Due to the limited silicon area, the proposed LCD column driver has only four channels. The 10-bit LCD column driver with R-DAC and C-DAC was fabricated using a 0.35-μm 5-V CMOS technology. Table I shows the device sizes used in the proposed column driver, where R_{top}, R_{mid}, R_{bot}, and R_i are designated in Figure 7. Figure 12 is a photograph of the die. Except for the resistor string of the R-DAC, the die area is 0.2×1.26 mm^2 for four channels. Each RGB digital input code is 10-bits wide.

The Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) are typically measured for a DAC. However, it is difficult to determine these two specifications for a nonlinear DAC. To demonstrate the performance of the proposed circuit, the nonlinear gamma voltages are not applied to the R-string and the resistor values of the resistor string are made equal. Since an LCD panel needs several column drivers, the uniformity of different drivers is very important. Figure 13 shows the measured transfer curves of a DAC for eight off-chip column drivers. To show the deviation between different chips, Figure 14 provides an

Buffer	M1 $\frac{3\mu\times4}{3\mu}$	M6 $\frac{7\mu\times3}{0.5\mu}$	M11 $\frac{4.3\mu\times3}{2.8\mu}$
	M2 $\frac{8\mu\times5}{3\mu}$	M7 $\frac{11\mu\times2}{0.5\mu}$	M12 $\frac{4.3\mu\times3}{2.8\mu}$
	M3 $\frac{8\mu\times5}{3\mu}$	M8 $\frac{4\mu\times4}{3\mu}$	M13 $\frac{10\mu\times3}{0.5\mu}$
	M4 $\frac{4\mu\times3}{2.5\mu}$	M9 $\frac{6\mu\times5}{3\mu}$	M14 $\frac{8\mu\times2}{0.5\mu}$
	M5 $\frac{4\mu\times3}{2.5\mu}$	M10 $\frac{6\mu\times5}{3\mu}$	
Resistance of R-DAC	R_{top}		800Ω
	$R_{mid.}$		550 Ω
	$R_{bot.}$		800 Ω
	R_i		50 Ω
Switch size	PMOS		$\frac{3\mu}{0.5\mu}$
	NMOS		$\frac{1\mu}{0.5\mu}$
Capacitance of C-DAC	C		1pF

Table I The device sizes used in the proposed column driver.

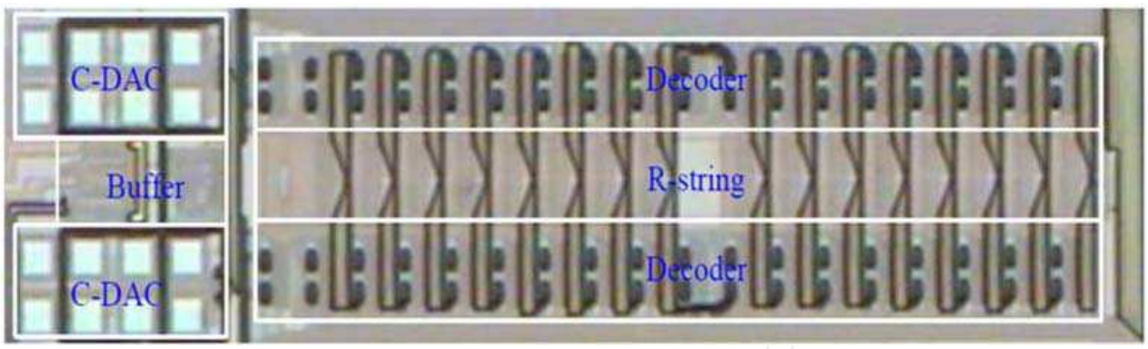

Fig. 12. Photograph of the proposed column driver.

enlarged view of the transfer curves, where the maximum deviation is 3.5 mV from the mean. This deviation is mainly due to process variations. The approach in this study uses no error correction. Hence, the deviation can be reduced by applying an offset canceling technique to the buffer amplifier. Figures 15(a) and (b) show the DNL values for positive and negative polarities, respectively. Figures 16(a) and (b) show the INL values for positive and negative polarities, respectively. The combination of R-DACs and C-DACs creates two groups of DNL values. The maximum DNL and INL values are 3.83 and 3.84 LSB, respectively. This study uses a 1-LSB voltage of 2.44mV to calculate the INL and DNL

values. The linearity, however, is less important than the deviations between off-chip drivers for LCD drivers [2].

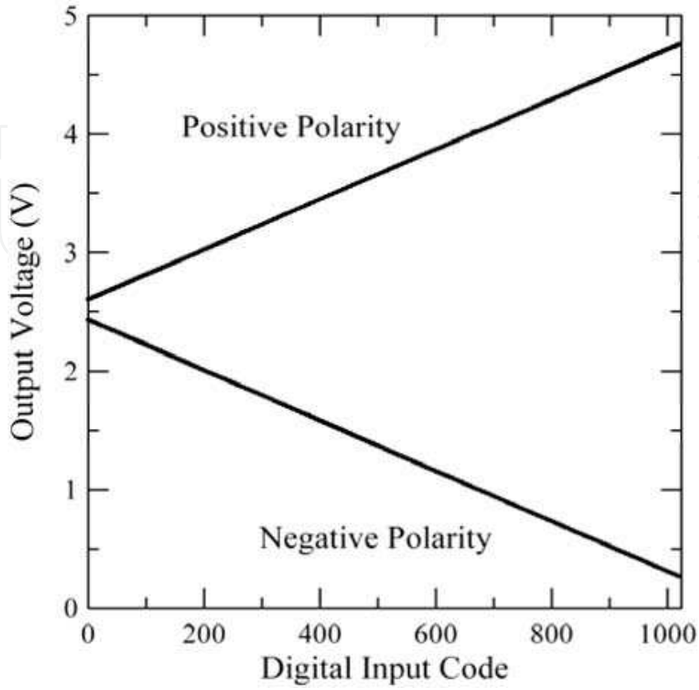

Fig. 13. The measured output responses of column drivers for 8 chips.

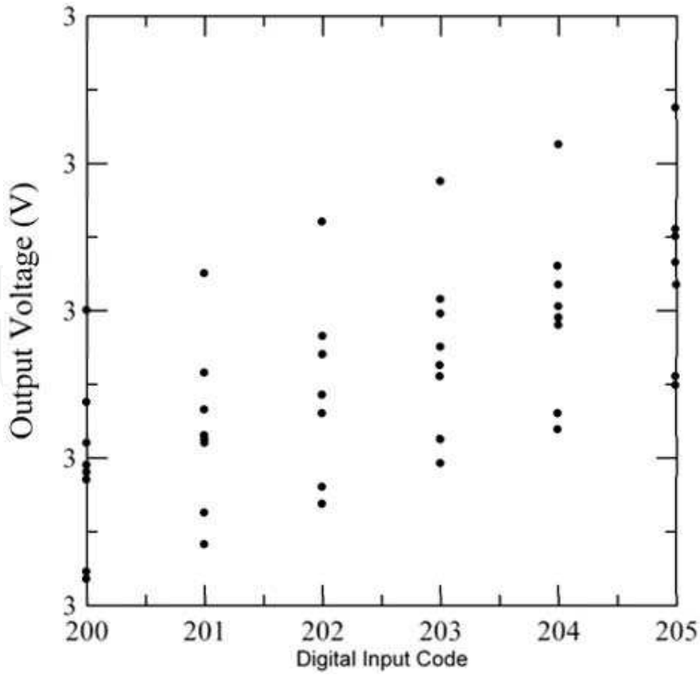

Fig. 14. The enlargement of the output response of the column driver for the digital input code of 200 ~ 205.

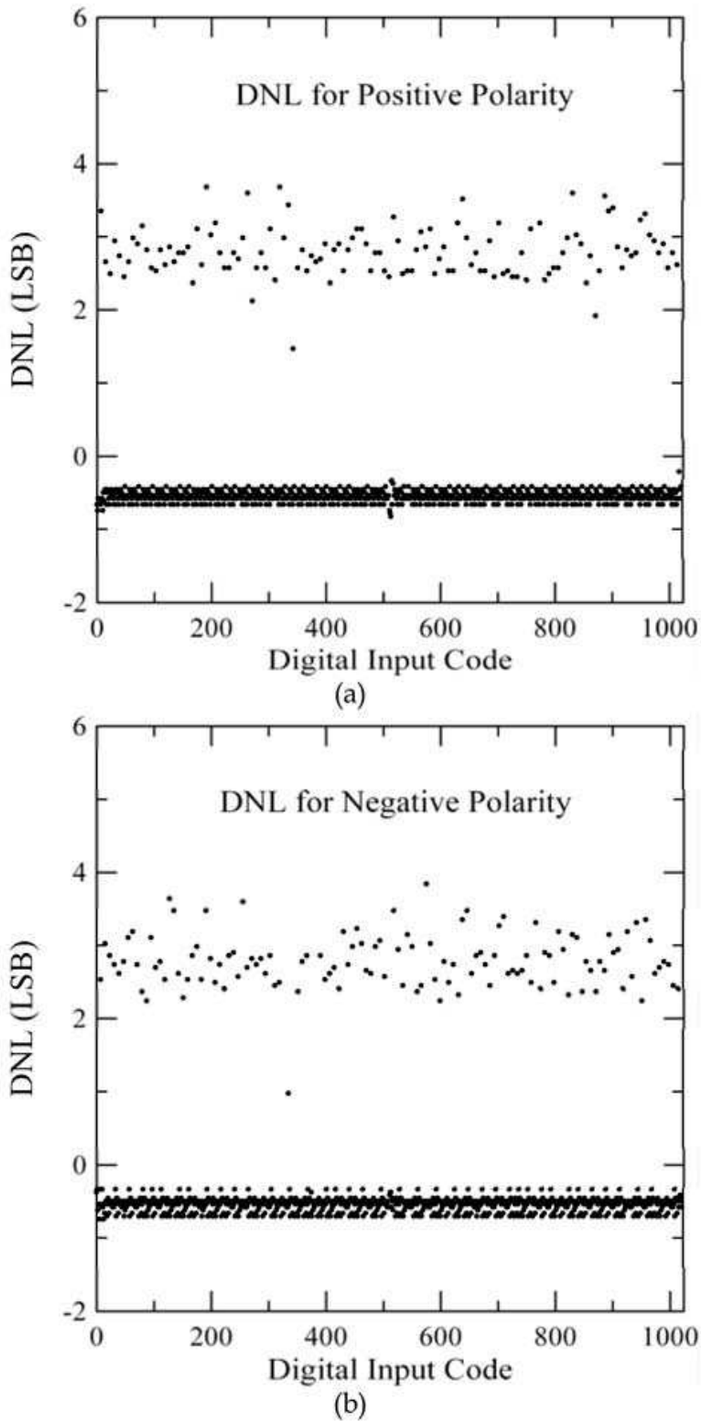

Fig. 15. The measured DNL for (a) positive polarity (b) negative polarity of the proposed column driver.

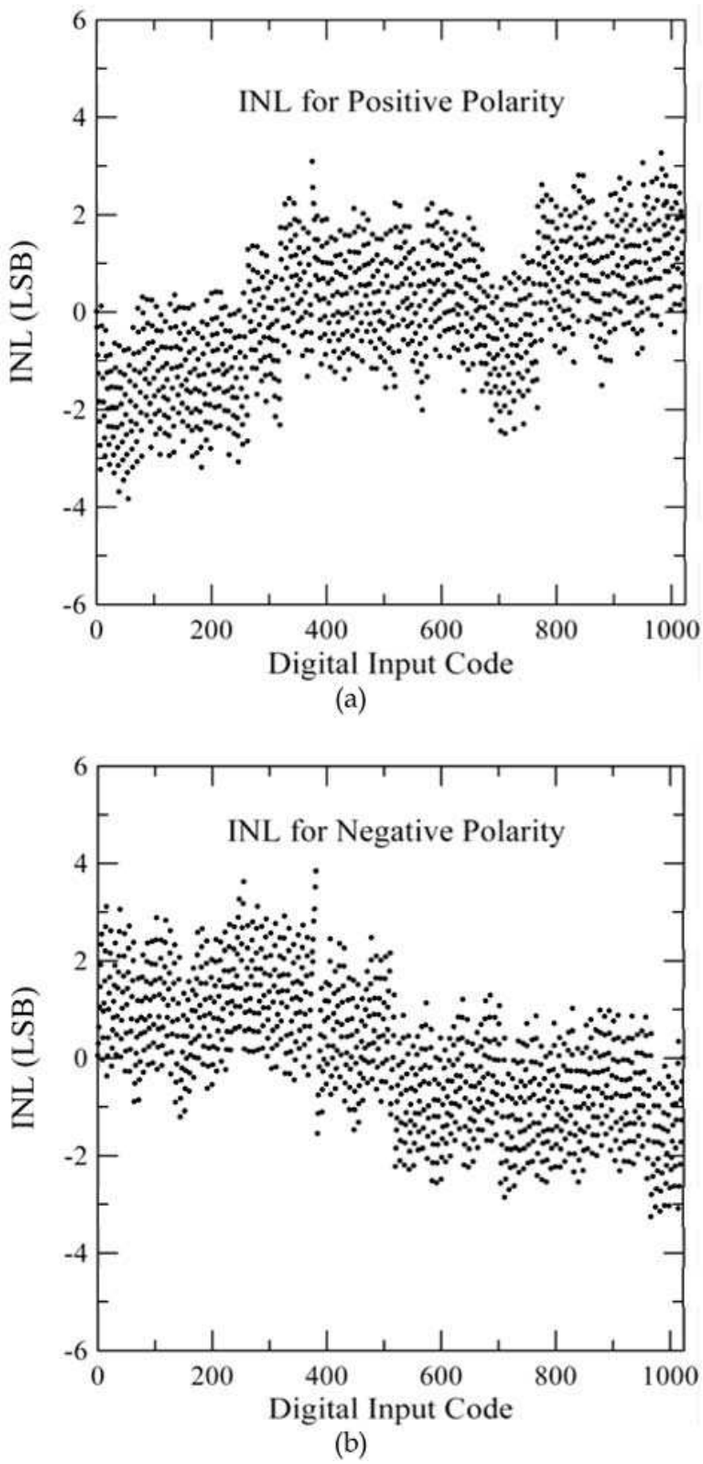

Fig. 16. The measured INL for (a) positive polarity (b) negative polarity of the proposed column driver.

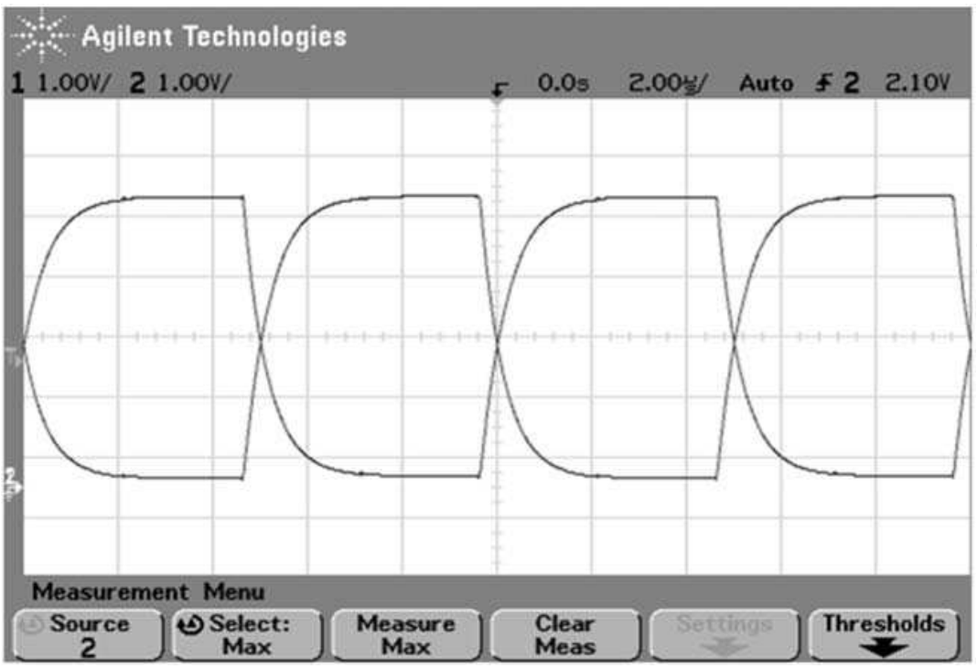

Fig. 17. The measured output waveform of two neighboring channels under dot inversion for the RGB digital inputs of '1111111111', where the voltage levels for negative and positive polarities are 0.266 V and 4.75 V, respectively.

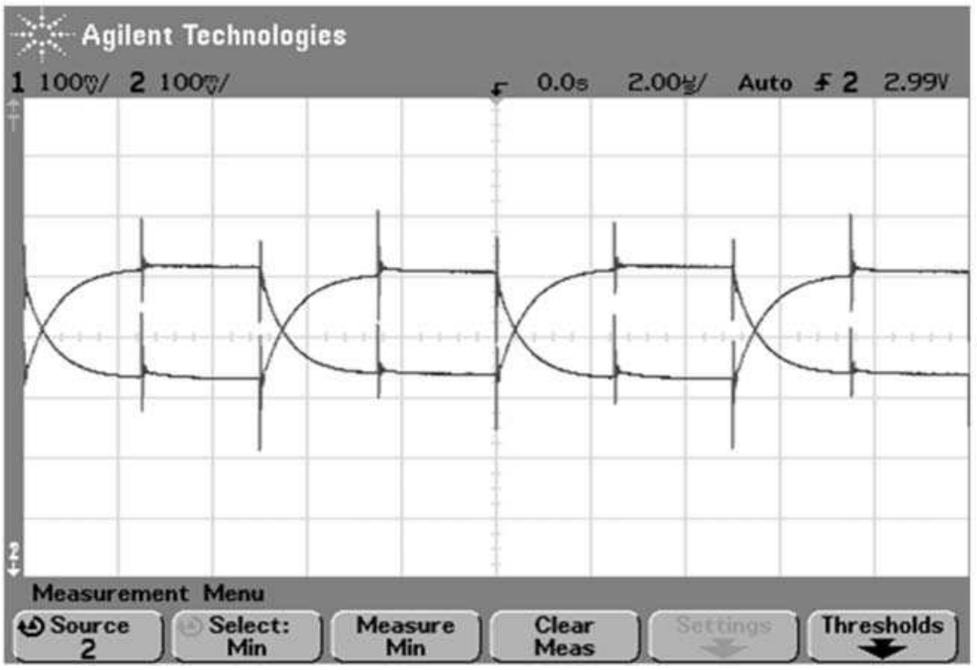

Fig. 18. The measured output waveform of two neighboring channels under dot inversion for the RGB digital inputs of '0000000000', where the voltage levels for negative and positive polarities are 2.425 V and 2.598 V, respectively.

Figure 17 shows the measured output waveforms of two neighboring channels under dot inversion for the RGB digital inputs of '1111111111.' Here, the voltage levels for negative and positive polarities are 0.266 V and 4.75 V, respectively. A load resistor of 5 kΩ and a capacitor of 90 pF were used. Figure 18 shows a similar waveform for '0000000000' inputs, where the corresponding voltage levels for negative and positive polarities are 2.425 V and 2.598 V, respectively. These two figures show that the settling time is within 3 μs, which is smaller than that of previously published work [2] and standard UXGA displays [5]. Table II summarizes the performance of the proposed column driver IC. The average area per channel is 0.063 mm^2, which is smaller than the reported areas of fully R-DAC-based column drivers [5, 8]. These experimental results show that the proposed column driver is suitable for UXGA LCD-TV applications.

	This work	[2]	[5]	[8]
Process technology	0.35 μm CMOS	N/A	0.6 μm CMOS	0.8 μm CMOS
Power supply	5 V	N/A	5 V	10 V
Number of bits	10	8 ~ 12	6	6
Maximum Deviation	1.43 LSB	±1 LSB@12 bits	N/A	N/A
Maximum DNL of DAC	3.83 LSB	N/A	N/A	N/A
Maximum INL of DAC	3.84 LSB	N/A	N/A	N/A
Settling time	3 μs for R_L = 5 kΩ and C_L = 90 pF	16 μs	8.3 μs for C_L = 30 pF 28.3 μs for C_L = 30×402 pF	2 μs for C_L = 100 pF
Buffer Power	3 μA/buffer	N/A	8.2 μA/buffer	N/A
Silicon area	0. 2×1.26 mm^2 for 4 channels*	16.5×0.9 mm^2 for 420 channels	18.1×2.35 mm^2 for 402 channels	100×2 mm^2 for 18 channels

*except for resistor string

Table II Performance summary of the proposed column driver.

5. Conclusion

This study presents a 10-bit LCD column driver consisting of piecewise linear DACs. This design uses external reference voltages and unequal resistor values in the resistor string to make coarse gamma correction. A simple digital circuit built into the timing controller or the column driver makes fine compensation adjustments. These features decrease the die area

and increase effective resolution. The experimental results show that the settling time is within 3 μs. The average die area per channel is 0.063 mm^2, which is smaller than those of full R-DAC-based column drivers. The maximum deviation from the channel mean is 3.5 mV for 8 off-chip drivers. This deviation can be further reduced by employing an offset canceling technique in the buffer amplifier. The measured maximum DNL and INL values are 3.83 and 3.84 LSB, respectively. Therefore, the proposed column driver is suitable for UXGA LCD-TV applications.

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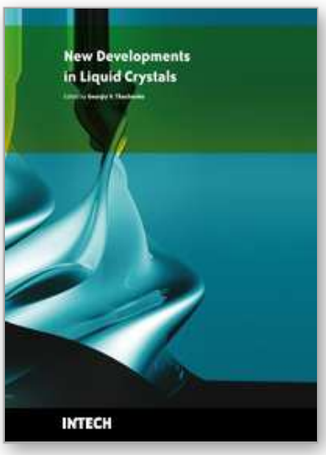

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Liquid crystal technology is a subject of many advanced areas of science and engineering. It is commonly associated with liquid crystal displays applied in calculators, watches, mobile phones, digital cameras, monitors etc. But nowadays liquid crystals find more and more use in photonics, telecommunications, medicine and other fields. The goal of this book is to show the increasing importance of liquid crystals in industrial and scientific applications and inspire future research and engineering ideas in students, young researchers and practitioners.

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