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Vertical Transmission Lines in Multilayer Substrates and Highly-Integrated Filtering Components Based on These Transmission Lines

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1. Introduction

Multilayer substrates such as interposers and printed circuit boards (PCBs) are basic interconnect technologies in modern and next-generation systems in which chip, package and board have been used as constructing elements. Consequently, multilayer substrates have been intensively studied in worldly dispersed electronics packaging research centers in which questions related to how to improve electrical, mechanical, thermal and reliable performances are on the agenda. Moreover, interconnection items affect directly on miniaturization, integration, cost-effectiveness and electrical characteristics of electronics components and, as a result, on promotion of electronics products to the market.

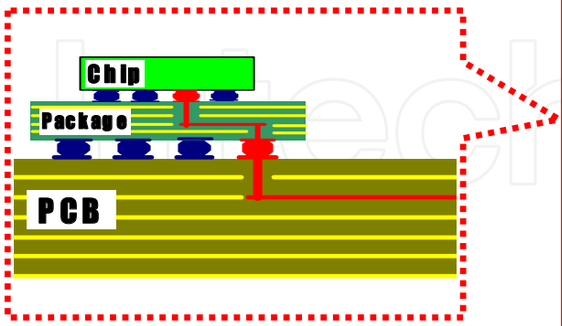


Fig. 1a. A chip-package-board part of a system

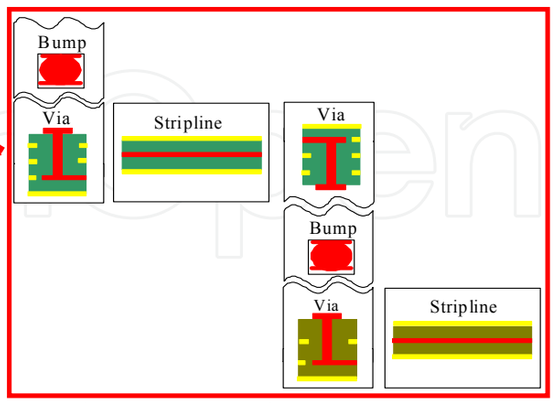


Fig. 1b. A division of an interconnection on bulding blocks

Microwave and millimeter wave areas extremely enhance difficulties in electrical design of interconnected circuits based on multilayer substrate technologies due to impedance

mismatching problems, crosstalk effects, leakage losses, unwanted resonances, dielectric and metal losses, and so on. These issues can be particularly overcome forming interconnections as well wave-guiding structures which can be also used as basic transmission lines of distributed-element passives and actives.
In Fig.1a, an example of a chip-package-board part of a system is shown. Multilayer substrate technologies are realized in the example presented by means of a package and a PCB. An interconnection in the multilayer substrates demonstrated in Fig.1a can be divided into blocks, having their specific characteristics, as shown in Fig.1b. These blocks are represented by planar transmission lines, bumps and vias for the electrical channel shown. One can generalize such building blocks by two groups - horizontal and vertical interconnections - as exhibited in Fig.2.

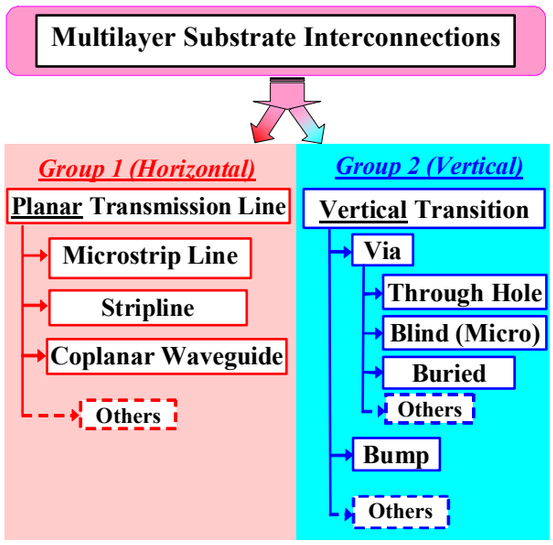


Fig. 2. A generalization of interconnections in a chip-package-board system

To design horizontal interconnections of a high electrical performance, planar transmission lines have been usually used because these structures can provide operation on one (fundamental) mode (for an example, TEM or Quasi-TEM), which has well-defined propagation constant and characteristic impedance, in a wide frequency band. That is why, short and long transmission lines have been used in high-frequency and high-speed systems. Besides that, planar transmission lines in the substrates serve not only as interconnected circuits but also as forming blocks of distributed passive and active components. Consequently, electrical study of planar transmission lines and different functional devices based on these lines has been widely and deeply presented in numerous literatures published (for an example, see comprehensive books (Hoffmann, 1987; Gupta et al., 1996), as for planar transmission lines).
In this chapter, attention will be attracted to the second group of interconnections (see Fig.2) in multilayer substrates, that is, vertical transitions.
Reasons why it will be concentrated on these structures are as following.
Firstly, it can be explained by a significant increase of the vertical transition role in achieving high electrical performance of signal interconnection paths in multilayer

substrates at microwaves and millimeter waves and a contribution of the vertical transitions to impedance mismatching, crosstalk, energy leakage, and other problems which can be excited due to these structures that can finally lead to the fault of the systems, electromagnetic interference (EMI), and other difficulties.

Secondly, it is attractive to use vertical transitions as forming elements of passives and actives (as for an example, short- or open-circuited stubs for filters) and in such way to reduce considerably their dimensions due to:

1) Three-dimensional (3-D) design;

2) Providing an approach to move a functional area for a component to a vertical transition region (see Fig.3).

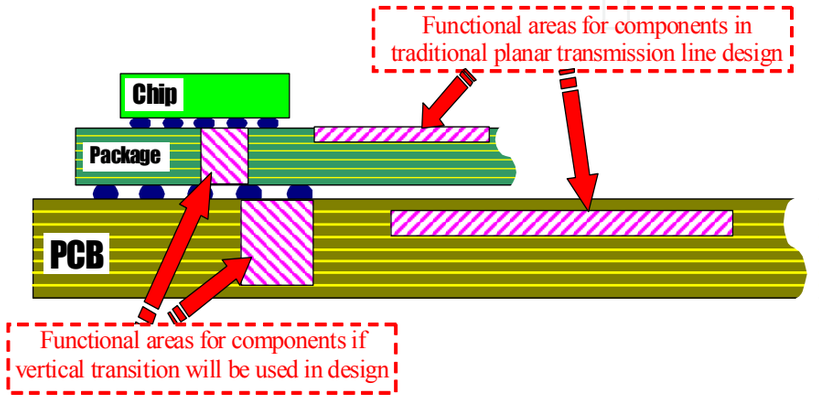


Fig. 3. Approach for miniaturization of a chip-package-board system by means of the use of vertical transitions as forming blocks of a component

2. Shield Via as Vertical Transmission Lines for Multilayer Substrates

Consider vias, as representative structures of vertical transitions, which serve usually to connect planar transmission lines disposed at different conductor layers of multilayer substrates. At microwave and millimeter wave bands, structures similar to a single signal via have poor-defined wave guiding properties and, as a result, they have increasing leakage losses with the growth of the frequency. That is why at these frequencies, propagation constant and characteristic impedance cannot be defined using traditional inductance and capacitance.

As an illustrative example, in Fig.4, the peak of the *E*-field at 10 GHz calculated by a three-dimensional full-wave technique (Weiland, 1996) in a horizontal cross-section between conductor planes of a multilayer substrate comprising the single signal via is shown. As one can see, if the single signal via is placed in the multilayer substrate, then it becomes an effective source of the parallel plate mode excitation. It acts like an antenna exciting parallel plate modes between conductor planes. As a result, such via structure leads to a dramatic reduction of the electrical performance of a whole interconnection due to in-substrate parallel plate-mode resonances and, as their consequence, signal integrity, power integrity and EMI problems. In Fig.5, an impact of the parallel plate-mode resonances on the electrical characteristics of the via is shown by means of the insertion loss. As one can see, the electrical performance of the via dramatically degrades at higher frequencies (in present example, starting from about 2GHz).

Electrical characteristics of vertical transitions can be improved by progressing from through-hole (see Fig.6a) to blind, counter-bored and buried via technologies explained respectively in Figs.6b, 6c and 6d. In these cases, stub effect (Laermans et al., 2001; Kushta et al., 2003) can be removed providing an improvement of signal transmission channel parameters, and the signal via conductor length can be shortened providing a reduction of coupling and radiating areas.
However, in spite of such advancements problems emphasized above remain at microwaves and millimeter waves.

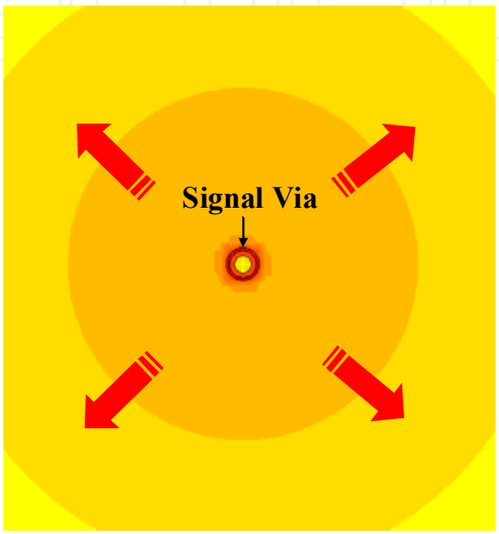


Fig. 4. Simulated peak of the *E*-field taken at 10GHz in a cross-section of a multilayer substrate comprising a single signal via

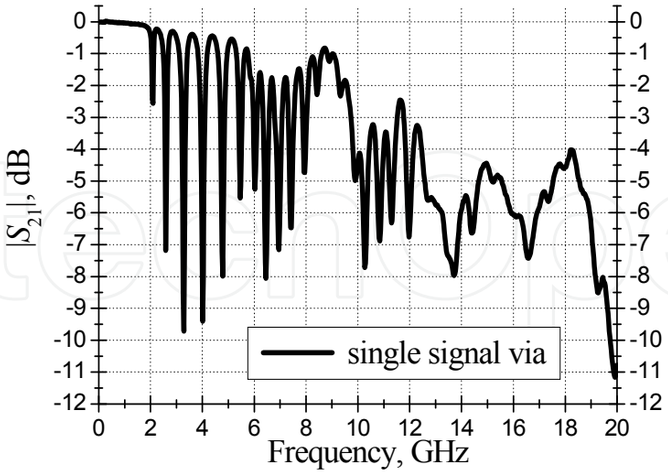


Fig.5. Experimental data for the insertion loss of the single signal via in the multilayer substrate

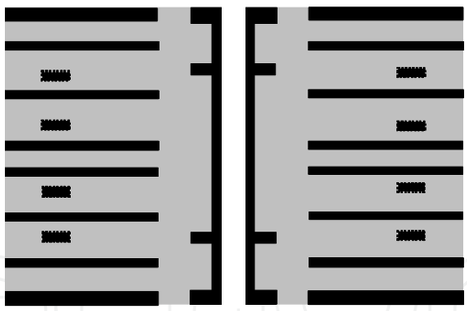


Fig. 6a. Cross-sectional view of through-hole via

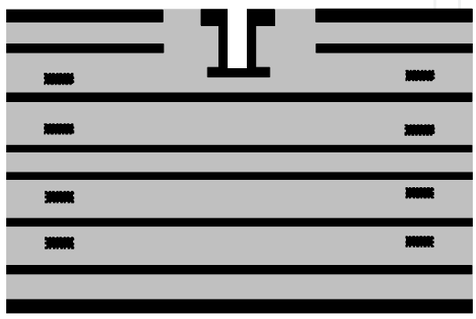


Fig. 6b. Cross-sectional view of blind via

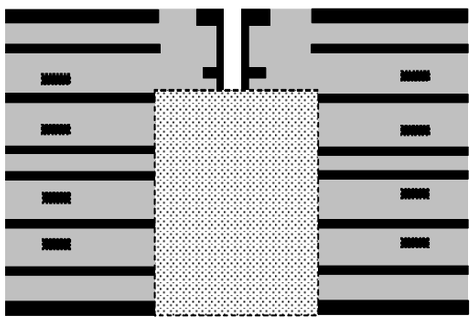


Fig. 6c. Cross-sectional view of counter-bored via

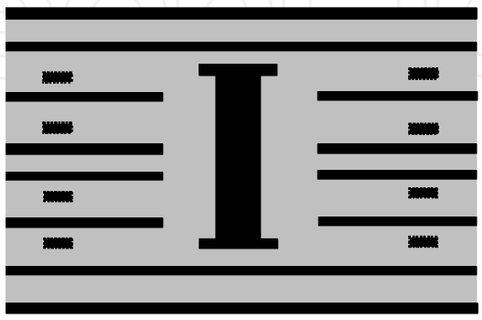


Fig. 6d. Cross-sectional view of buried via

Thus, it comes to be clear that vertical transitions including via structures become an important element in design of high-frequency and high-performance interconnections and components grounded on multilayer substrate technologies.

A solution proposed to provide a high-performance vertical transition in a multilayer substrate is based on forming a shield via as a result of the conjoint use of signal and ground vias. In this case, a specific coaxial waveguide can be formed in the vertical direction of the multilayer substrate (Pillai, 1997; Tarvainen, 2000; Kushta et al. 2002).

Following distinctive examples show advanced characteristics for the shield via compared with the single signal via case. In Fig.7, simulated peak of the *E*-field for the shield via obtained in the same way as for Fig.4 is presented for the identical dimensions of the substrate. As one can see, electromagnetic energy propagating through the shield via is disposed between signal and ground vias. This effect leads to a considerable improvement of the electrical performance for signaling as shown in Fig.8 by means of measured insertion losses (photo of the shield via experimental pattern is in Fig.9). In Fig.8 electrical characteristics of the single via are also given for comparison.

It is well known, to estimate leakage losses in a wide frequency band, *S*-parameters can be used and as for example by means of such equation:

$$Leakage\ Loss, \% = (1 - |S_{11}|^2 - |S_{21}|^2) \cdot 100 , \quad (1)$$

where $|S_{11}|$ is the return loss and $|S_{21}|$ is the insertion loss.

In Fig.10, simulated leakage losses for single signal via and shield via with the same parameters as for Figs.4 and 7 are presented. As one can see, the application of the shield via suppresses leakage losses in considered frequency band. It also means that EMI problems can be considerably reduced by the use of such vias in electronics design (Kushta et al., 2004; Kushta & Narita, 2004).

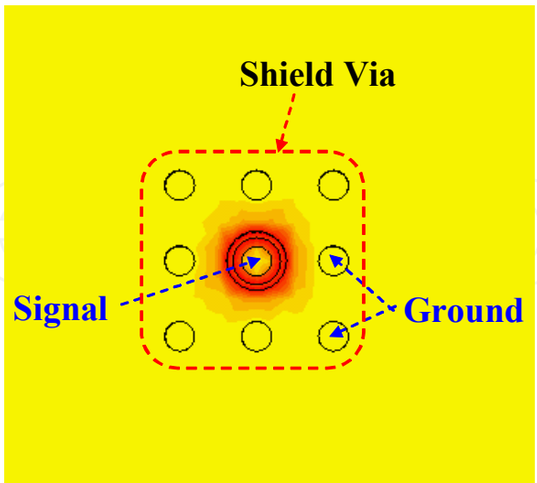


Fig. 7. Simulated peak of E-field taken at 10GHz in the cross-section of the multilayer substrate comprising a shield via

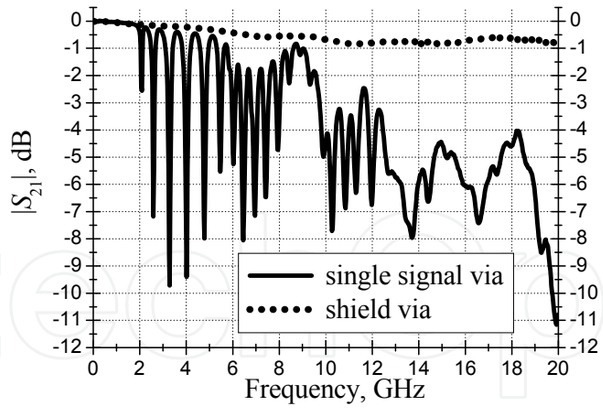


Fig. 8. Experimental data for the insertion loss of both the shield via and the single signal via in the multilayer substrate

Consider leakage effect on the electrical performance of both single and shield via structures in which a digital signal is propagating. In Fig.11, the pulse transmitted through such via structures is shown. As one can see in this figure, signal transmitted through the single signal via has not only higher insertion loss but also higher deformation of the pulse shape that is one of the most important issues in high-speed signaling because, in this case, it is necessary to apply additional techniques like pre-emphasis.

Fig. 9. Photo of the shield via formed by signal and ground vias conjointly

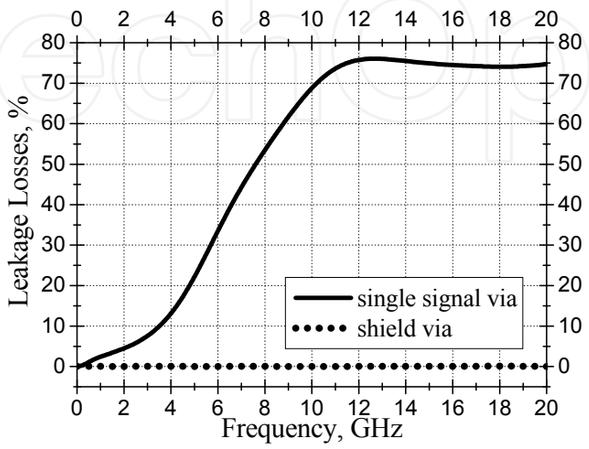


Fig. 10. Simulated leakage losses for via structures calculated according to Eq.1

On the other hand, forming the shield via in the multilayer substrate gives a possibility for a considerable improvement of the electrical performance of the vertical transitions. As follows from Fig.11, the shield via provides significantly lower loss, if it is compared with single signal via case. Moreover, the pulse shape (especially, the width for the signal transmitted) is considerably better for the shield via.

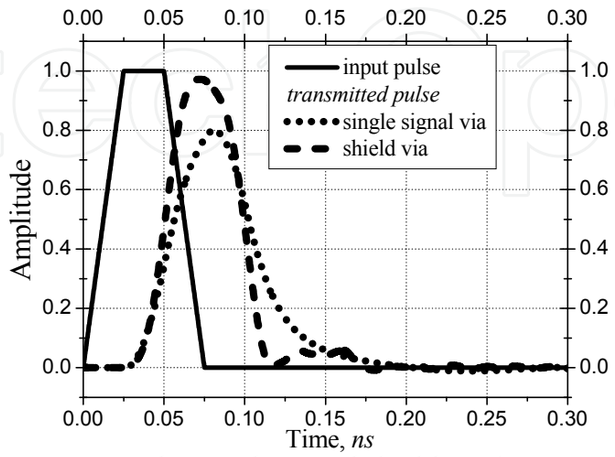


Fig. 11. Signal propagation in single signal via and shield via (transmission)

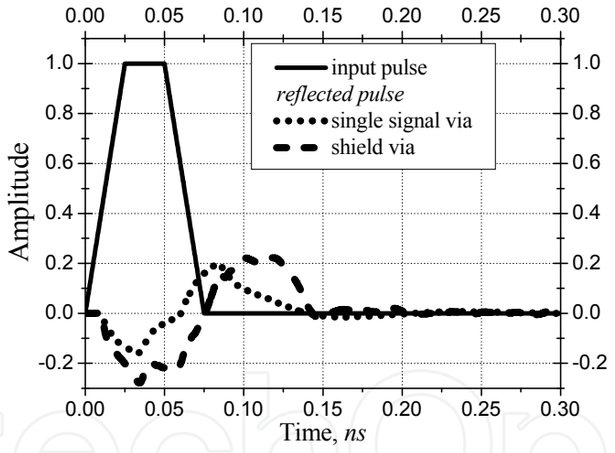


Fig. 12. Signal propagation in single signal via and shield via (reflection)

However, as follows from Fig.12, the amplitude of the reflected pulse is large enough for both via structures. That is why, providing characteristic impedance controlling in a wide frequency band is another important issue to implement the shield vias in real substrates and to achieve their electrical performance similar to that as in planar transmission lines. Therefore, an appropriate physical model showing mechanisms affecting on the electrical characteristics of such type of vertical transitions has to be defined.

Consider the shield via as in Figs.13a and 13b. This structure is formed in an 8-conductor layer substrate. Corrugated coaxial waveguide model (Kushta et al., 2002; Kushta et al., 2004) is proposed to describe physical processes in the shield via. In this model, ground vias are replaced by continuous and smooth conductive surface which acts as an outer

conductive boundary and the signal via serves as an inner conductive boundary of such coaxial waveguide. Also in the model, conductive plates from conductive layers of the multilayer substrate disposed between inner and outer conductive boundaries are considered as specific corrugations of the outer conductive boundary. The corrugated coaxial waveguide model for the shield via shown in Figs. 13a and 13b is presented in Figs.14a and 14b.

In consequence, the outer conductive boundary of such corrugated coaxial waveguide model can be characterized as a surface for which the surface impedance can be approximately defined as:

$$Z_s \approx 120\pi \cdot i \cdot \sqrt{\frac{1}{\varepsilon}} \cdot \tan\left(\frac{2\pi \cdot f}{c} d \cdot \sqrt{\varepsilon}\right) \tag{2}$$

where d is the corrugation depth defined as $d = \left(D_r - d_{cle,r} - d_{gr}\right)/2$, f is the frequency and c is the velocity of light in free space. Note that Eq.(2) is valid under following conditions:

$$H_{i,j} << \lambda, \tag{3}$$

where λ is the shortest wavelength in the isolation material of the multilayer substrate in considered frequency range; $H_{i,j}$ is the distance between i-th and j-th conductor planes; $j = i + 1$.

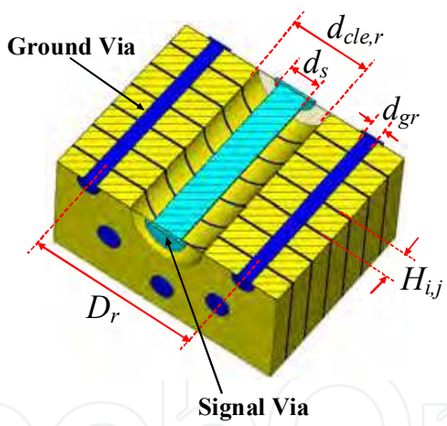


Fig. 13a. Cross-sectional view of shield via

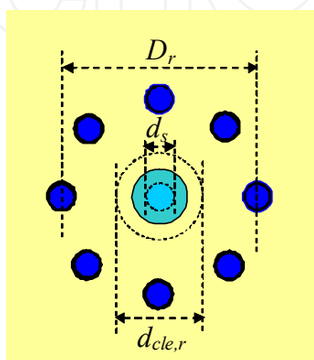


Fig. 13b. Top and bottom views of shield via

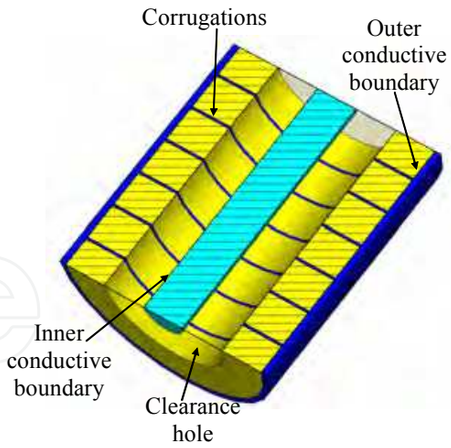


Fig. 14a. Cross-sectional view of corrugated coaxial waveguide model

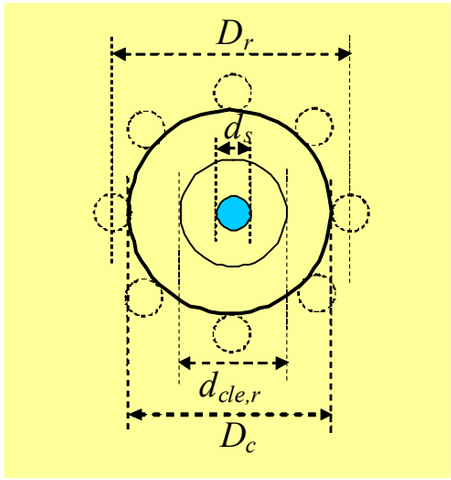


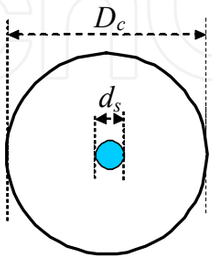
Fig. 14b. Top and bottom views of corrugated coaxial waveguide model

Eq.2 gives a simplified physical mechanism which can explain signal propagation in the shield via. In particular, if corrugations in the coaxial waveguide model are large enough, then the surface impedance of the outer conductive boundary is dependent on the frequency. It means that broadband matching of the shield via with other interconnected circuits having usually approximately constant (or weakly frequency-dependent) characteristic impedance is a difficult problem.
Thus, to provide a broadband high-performance operation of the shield via it is necessary to decrease such the corrugations as much as possible. If this condition will be satisfied, then an approximate equation for the surface impedance can be written as follows:

$$Z_s \approx 0 . \tag{4}$$

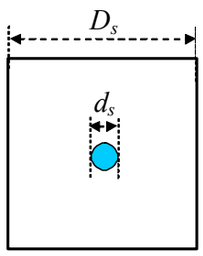
The surface impedance defined according to Eq.4 corresponds to the smooth conductive boundary and, in this case, signal propagation in the shield via can be considered as in a corresponding coaxial waveguide.

As a validation of this coaxial waveguide model, consider two types of shield vias in the multilayer substrate. The first type comprises the outer conductive boundary of a round arrangement of ground vias. The second type is consisted of ground vias with a square arrangement. From coaxial transmission line theory (Wheeler, 1979), there are known analytical formulas for the characteristic impedance of round and square coaxial waveguides. In Figs.15a and 15b, expressions for these coaxial waveguides are presented under the drawing of the corresponding structure by Equations (5) and (6), respectively.



$$Z_r \approx 60 \cdot \sqrt{\frac{\mu}{\varepsilon}} \cdot \ln\left(\frac{D_c}{d_s}\right) \tag{5}$$

Fig. 15a. Cross-section view of round coaxial waveguide and its characteristic impedance



$$Z_{sq} \approx 60 \cdot \sqrt{\frac{\mu}{\varepsilon}} \cdot \ln\left(\frac{1.0787 \cdot D_s}{d_s}\right) \tag{6}$$

Fig. 15b. Cross-section view of square coaxial waveguide and its characteristic impedance

As follows from these equations, which are defined for the coaxial transmission lines with continuous and smooth inner and outer conductive boundaries, the characteristic impedance will have the same magnitude for round and square cases if the diameter of outer boundary of the round transmission line and the side of the square transmission line will satisfy the following identity:

$$D_c \approx 1.0787 \cdot D_s \,. \tag{7}$$

It should be noted that Eq.7 is valid if other parameters of round and square coaxial transmission lines such as the diameter of the inner conductor and constitutive parameters (such as relative permittivity, ε and relative permeability, μ) of the isolating material are the same.

So, first of all, a validation of the coaxial waveguide model will be provided in such manner. If this model is appropriate for the shield via, then identity (7) will be satisfied for shield

vias with round and square arrangements of ground vias around the signal via. To verify this feature, round and square shield vias with $D_c = 3.2mm$ and $D_s = 2.967mm$ have been considered. Cross-sectional views of these via structures are presented in Figs.16a and 16b.

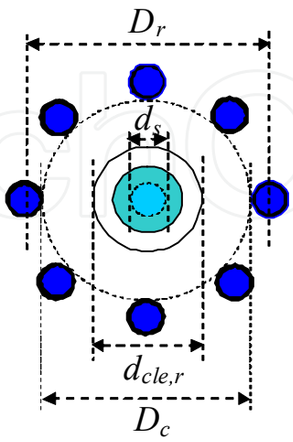


Fig. 16a. Shield via with round arrangement of ground vias

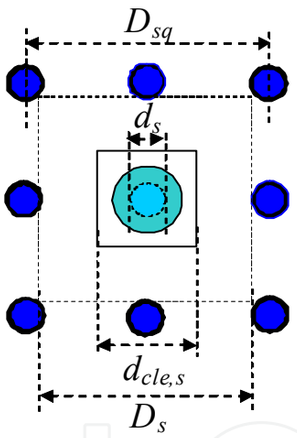


Fig. 16b. Shield via with square arrangement of ground vias

Other dimensions of aforementioned shield via structures are as following (see Fig.17): $d_{pad} = 0.95mm$, $d_{cle,r} = 1.65mm$, $d_{cle,s} = 1.53mm$ and $d_s = 0.65mm$. The shield via structures have been embedded in the substrate which consists of eight copper planar conductor layers isolated by FR-4 material with the relative permittivity of $\varepsilon = 4.17$ and loss tangent of $\tan\delta = 0.023$ as assumed in simulations. Spaces between planar conductor layers as shown in Fig.17 are: $H_1 = 0.2mm$, $H_2 = 0.385mm$ and $H_3 = 0.24mm$; the thickness of conductor planes embedded in the substrate is $t = 0.035mm$; the thickness of top and bottom conductor planes is $t_t = t_b = 0.055mm$.

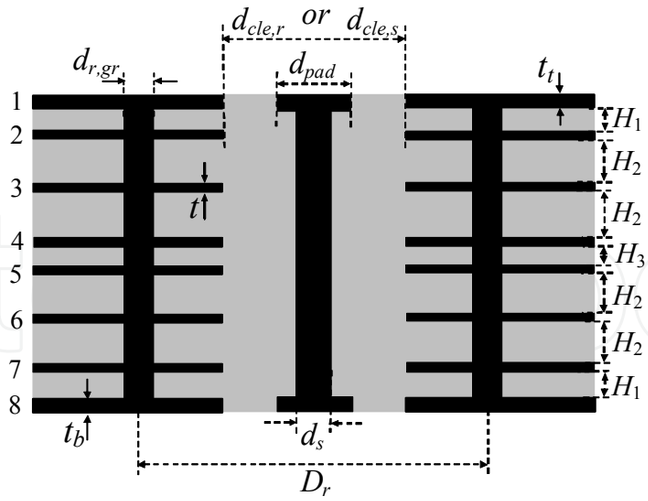


Fig. 17. Vertical cross-section view of shield via in 8-conductor-layer substrate

In Figs.18a and 18b, magnitudes of simulated *S*-parameters for two shield vias with round ($D_c = 3.2mm$) and square ($D_s = 2.967mm$) arrangements of the ground vias in the 8-conductor-layer substrate are presented. As follows from simulated *S*-parameter data shown in these figures, structures with round and square arrangements of ground vias having transverse dimensions defined according to Eq.7 demonstrate practically the same electrical performance in considered frequency band. It means also that the characteristic impedance in structures presented is the same one and, as a result, aforementioned shield vias are practically equivalent.

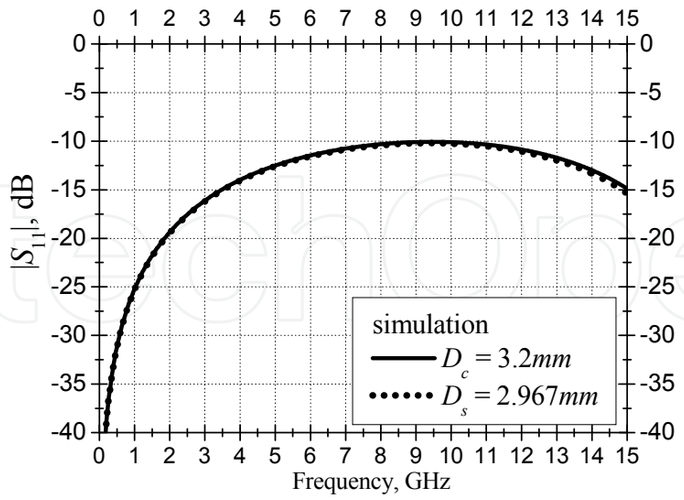


Fig. 18a. Simulated return losses for two shield vias with round and square arrangements of ground vias

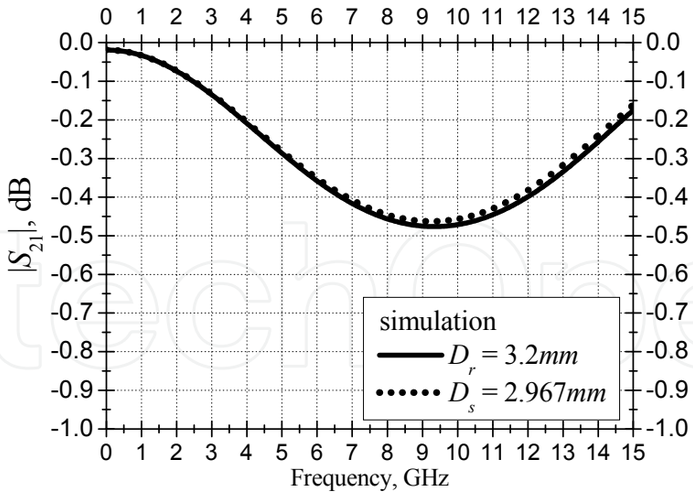


Fig. 18b. Simulated insertion losses for two shield vias with round and square arrangements of ground vias

Simulated results presented in Fig. 18a and 18b serve a proof of a simplified mechanism for signal propagations in the shield via formed by signal and ground vias conjointly as in the corresponding coaxial waveguide with smooth and continuous conductive boundaries. This consideration gives a way to define the characteristic impedance of the shield via in the multilayer substrate that is important to design well-matched interconnected circuits using multilayer substrate technologies.

Note that the corrugation depth for considered round and square coaxial waveguides is the same due to the appropriate choice of the clearance hole form and dimensions. In these cases, the round shield via has the round clearance hole, while the square shield via has the square clearance hole. Also, dimensions of the clearance holes are defined according to Eq.7.

Above-mentioned data have been obtained by three-dimensional full-wave simulations which usually give an adequate description of electromagnetic processes in a test structure. However, each theoretical model is idealized one, which does not include the frequency dependency of board isolating material, roughness and tolerances of shapes of conductive surfaces, and so on. That is why the experimental study of test structures serves not only as an evidence of their theoretical models but also gives a real wide-frequency band behavior of the structures studied.

In following Fig.19a and 19b, measured magnitudes of *S*-parameters for the shield vias whose simulated data are respectively presented in Figs. 18a and 18b are shown and demonstrate the electrical behavior similar to their simulation models. As follows from theoretical and experimental data, characterization of the shield vias in the multilayer substrate as specific coaxial waveguides is a vital and useful approach to design high-frequency and high-speed electrical vertical transitions.

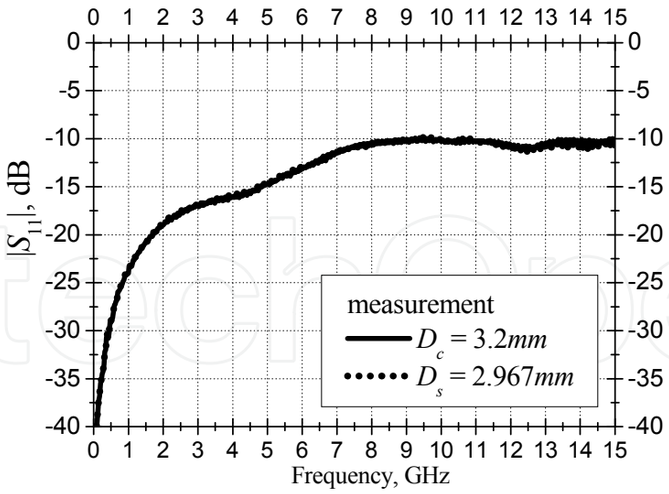


Fig. 19a. Measured return losses for two vertical transitions with round and square arrangements of ground vias

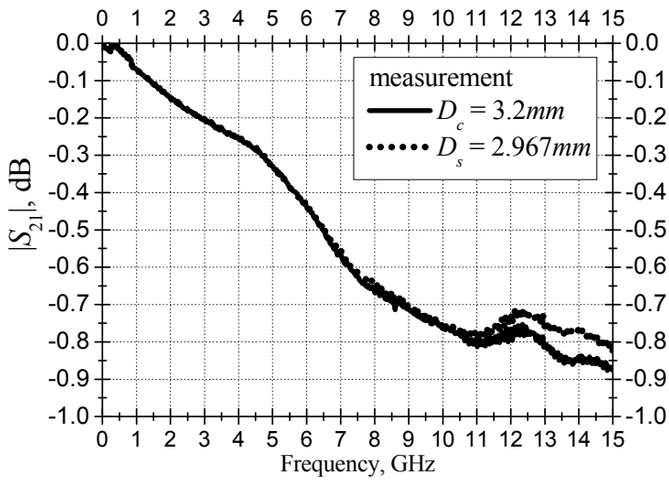


Fig. 19b. Measured insertion losses for two equivalent vertical transitions with round and square arrangements of ground vias

As another verification of the corrugated coaxial waveguide model and also as recommended design steps based on the application of this model, an effect of the distance between signal and ground vias on the electrical performance of the shield via is presented. Two square arrangements of ground vias having $D_s = 2.04mm$ and $D_s = 2.967mm$ (other parameters are the same as in aforementioned cases, except that the clearance hole has the side $d_{cle,s} = 1.16mm$) have been considered here that approximately corresponds characteristic impedances calculated according to Eq.6 as $Z_{sq} \approx 36Ohms$ and $Z_{sq} \approx 47Ohms$. Measurement data for these shield vias are shown in Figs.20a and 20b. Note that top and bottom parts of the shield vias considered were connected to 50*Ohms* coaxial cables. As follows from figures presented the highest electrical performance in all frequency band (up to 15*GHz*) is achieved

for the shield via with $D_s = 2.967mm$. This shield via is better matched to $50Ohm$ cables that is an indirect validation of the coaxial waveguide model. However this is only one important point of the physical model presented because corrugations are another its key point.
Thus, as next, the clearance hole effect on the electrical performance of the shield via is shown that is associated with the corrugation depth in the physical model presented. Measurement data for two shield vias with different dimensions of the clearance hole are demonstrated in Fig.21a and 21b.
The shield vias have the same dimensions and are embedded in the same 8-conductor-layer substrate, as in above-mentioned examples. In considered shield vias, clearance holes have the square form with the side of $d_{cle,s} = 1.53mm$ and $1.16mm$ and for both shield vias $D_s = 2.967mm$. As one can see increasing the clearance hole dimensions leads to a considerable improvement of the electrical performance of the shield via in the wide frequency band.

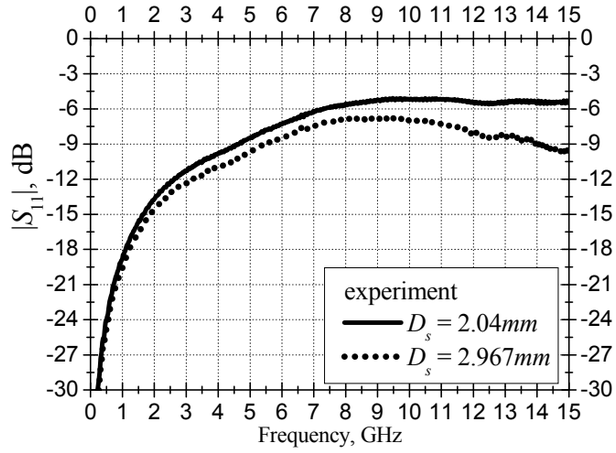


Fig. 20a. Measured return losses for shield vias with square arrangements of ground vias (effect of distance between signal and ground vias)

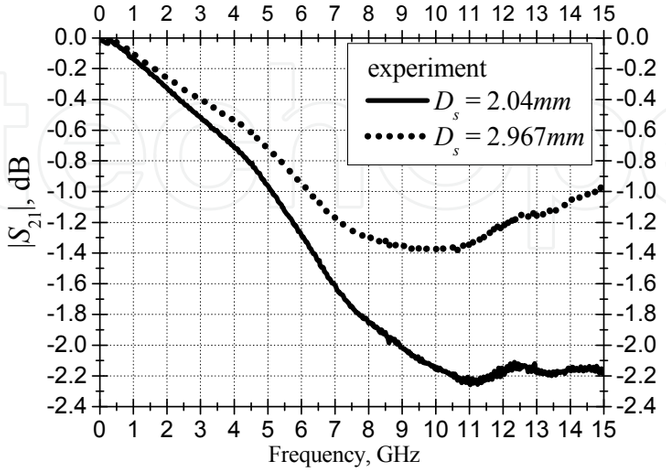


Fig. 20b. Measured insertion losses for shield vias with square arrangements of ground vias (effect of distance between signal and ground vias)

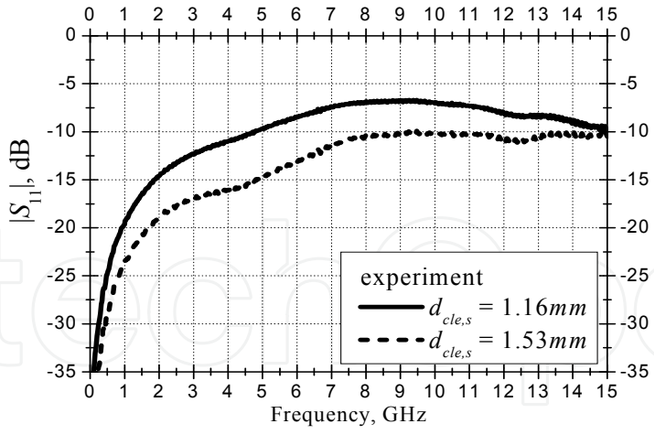


Fig. 21a. Measured return losses for shield vias with square arrangements of ground vias (clearance hole effect)

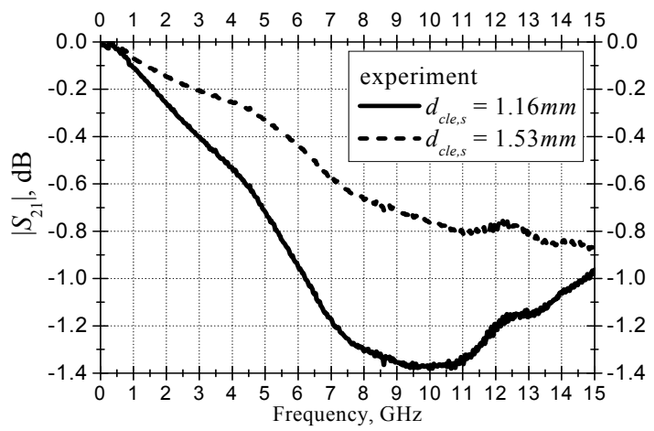


Fig. 21b. Measured insertion losses for shield vias with square arrangements of ground vias (clearance hole effect)

As a result of these considerations, two main points can be categorized as a basis which can provide a high-performance vertical transition in the form of the shield via. They are obtained as following from the corrugated coaxial waveguide model given here.

1) Signal via transversal dimensions and distance between signal and ground vias in a shield via have to be chosen in such way to provide a required characteristic impedance calculated according to an appropriate coaxial transmission line corresponding to the shield via.

2) A clearance hole has to provide minimal corrugations of the ground plates in the coaxial wave guiding channel.

As one can see, in presented examples, cases when signal is propagating from the top to the bottom of the multilayer substrate are considered. However in real applications, the shield via has to be connected to a planar transmission line disposed at a conductive layer of a multilayer substrate. And this connection can not be decided in a simple way at microwaves and millimeter waves and, that is why, it becomes an important issue. In following paragraph, a technique to provide a high-performance transition from the shield via to the planar transmission line will be shown.

3. Broadband Trasition from a Shield Via Structue to a Planar Transmission Line in a Multilayer Substrate

Thus, development of a vertical transition itself is not enough to provide a high-performance interconnection at microwaves and millimeter waves. It is important to match such vertical transition with other interconnected ciruits (Kushta & Harada, 2008), including a planar transmission line as for an example.

In Figs.22a and 22b, cross-sectional views of a shield via in a 14-conductor-layer substrate are shown. The electrical performance of the via structure is strongly-dependent on the shape and dimensions of the clearance hole as it has been shown above.

In real design, dimensions of the clearance hole can be big enough due to a large distance between the signal via and ground vias which conjointly with the radius of the signal via and constitutive parameters of an isolating material in the multilayer substrate provide controlling the characteristic impedance in the shield via. In the case of connection of the shield via to a planar transmission line such clearance hole can excite characteristic impedance mismatching problems that will be shown in following example.

Consider the model presented in Figs.22a and 22b in which the shield via is connected to a stripline disposed at the 12th conductor layer of the 14-conductor-layer substrate. The shield via has such dimensions: $d_s = 0.6mm$; $d_{pad} = 1.2mm$; $d_{cle,r} = 1.4mm$ or $d_{cle,r} = 3.4mm$; $d_{gr,r} = 0.3mm$.

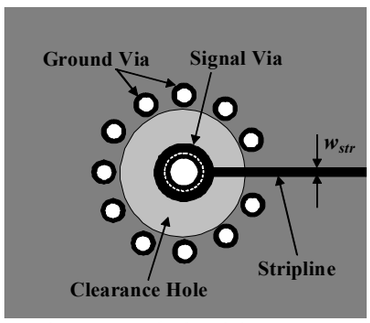


Fig. 22a. Horizontal cross-sectional view of shield via in multilayer substrate taken in the position of stripline

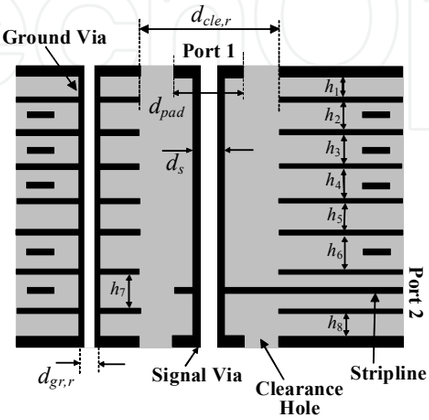


Fig.22b. Vertical cross-sectional view of shield via in multilayer substrate

Note that two dimensions of the clearance hole are considered here. The multilayer subsrate formed by PCB technologies consists of fourteen copper planar layers isolated by the FR-5 material of the relative permittivity of $\varepsilon = 3.78$ as assumed in simulations. Spaces between planar conductor layers (see Fig.22b) are: $h_1 = h_8 = 0.14mm$; $h_2 = h_3 = 0.335mm$; $h_4 = 0.56mm$; $h_5 = 0.15mm$; $h_6 = h_7 = 0.335mm$. The thickness of conductor planes embedded in the PCB is 0.035*mm*; the thickness of top and bottom conductor planes is 0.055*mm*. The signal conductor in the shield via is connected to the stripline by means of the pad having the same diameter, $d_{pad} = 1.2mm$, as via pads at top and bottom conductor layers. The width of the stripline is $w_{str} = 0.14mm$ providing the characteristic impedance of about 50*Ohms*.
Here, both TDR (Time Domain Reflectometry) and *S*-parameter data obtained by the use of the 3-D full-wave electromagnetic simulator are presented.
As input signal, the Gaussian pulse, shown in Fig.23, has been applied to stimulate a test model. Note the width of applied pulse is short (about 40*ps* at the 0.5-amplitude level). This corresponds a high-speed data transmission system.
Characteristic impedance in time domain is calculated according to following well-known equation:

$$Z(t) = \frac{1+\rho(t)}{1-\rho(t)} \cdot Z_0 \,, \tag{8}$$

where Z_0 is the characteristic impedance of input and output ports of the test structure and $\rho(t)$ is the reflection coefficient from the test model taken in time domain.

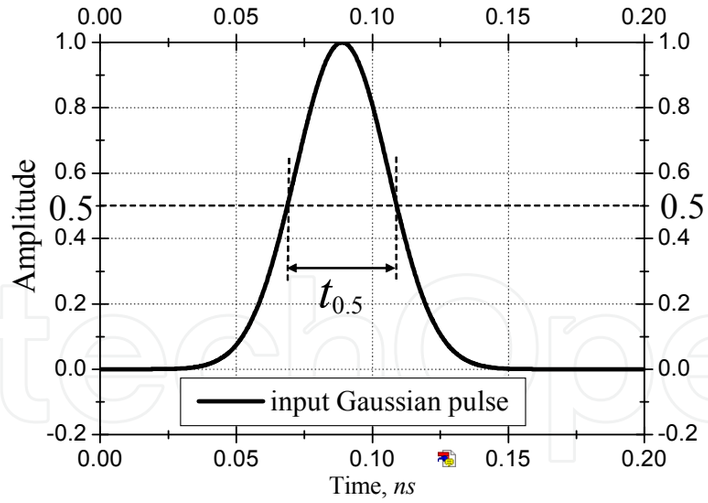


Fig. 23. Input Gaussian pulse used in simulations

In Fig.24, simulated results of the characteristic impedance are presented for models of two different clearance holes: The first is typical clearance hole defined by a technological process to provide a non-contact fabrication of the signal via and conductor layers in the PCB (for this case, $d_{cle,r} = 1.4mm$); The second is an optimized clearance hole ($d_{cle,r} = 3.4mm$) obtained according to the corrugated coaxial waveguide model presented.

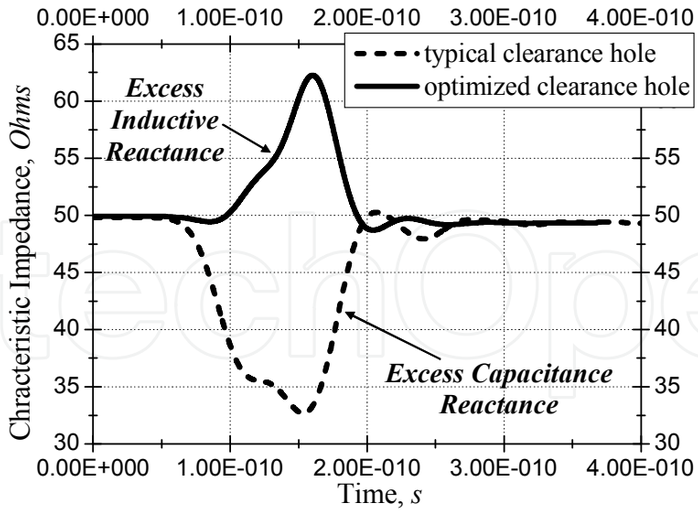


Fig. 24. Characteristic impedance in time domain for the test models

As one can see, a large impedance mismatching for the model comprising the shield via with the typical clearance hole is excited by an excess capacitance reactance due to coupling between the signal via and conductor planes of the PCB.

Optimized clearance hole removed the effect of excess capacitive reactance and considerably improved the electrical performance of the model as it can be traced from simulated *S*-parameter data presented in Figs.25a and 25b.

In spite of a considerable improvement of the interconnection comprising the shield via with the clearance hole optimized, another problem is appeared in the transition from the signal via to the stripline. This is impedance mismatching due to excess inductive reactance (see Fig.24) which is originated by the strip segment disposed between the signal via pad and the stripline. This segment acts as a flat wire inductor for which the characteristic impedance can be approximately represented by the following formula:

$$Z_w \approx iX_w = 2\pi \cdot f \cdot L \,, \tag{9}$$

where X_w is the inductive reactance of the strip, f is frequency, and L is the inductance of the strip segment.

To provide the characteristic impedance matching in the transition from the signal via pad to the planar transmission line in a multilayer substrate, a method to compensate the excess inductive reactance of the strip segment in the area of the clearance hole has been developed. Basis of this method can be traced by a block diagram shown in Fig.26, in which an additional capacitance reactance, $X_{add} = -1/2\pi fC_{add}$, is introduced to reduce or to suppress the effect of the excess inductive reactance of the strip segment.

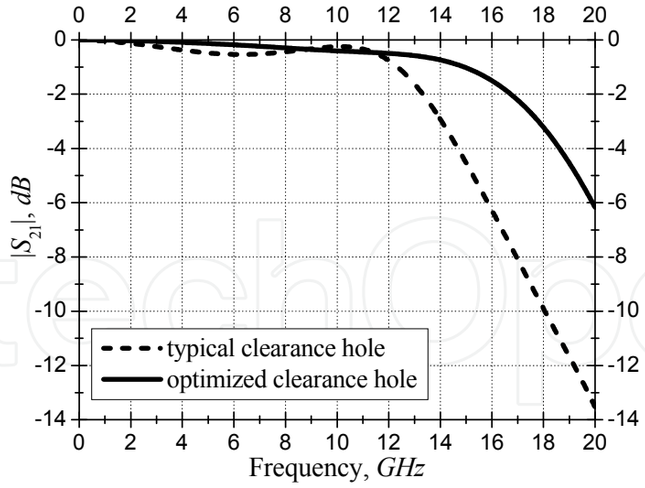


Fig.25a. Simulated insertion loss for the model shown in Figs.22a and 22b

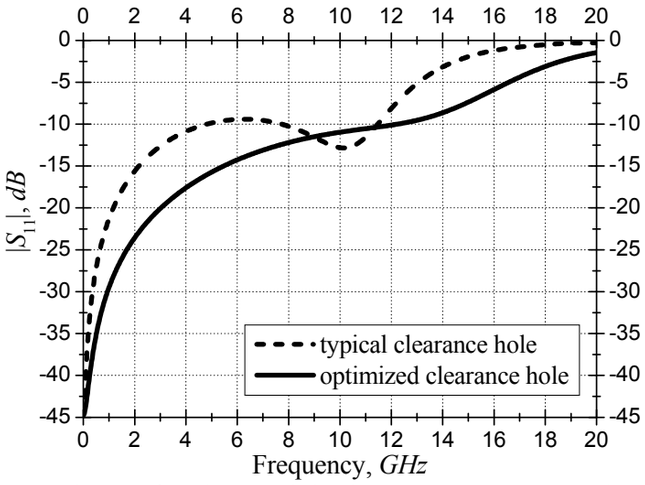


Fig.25b. Simulated return losses for the models shown in Figs.22a and 22b

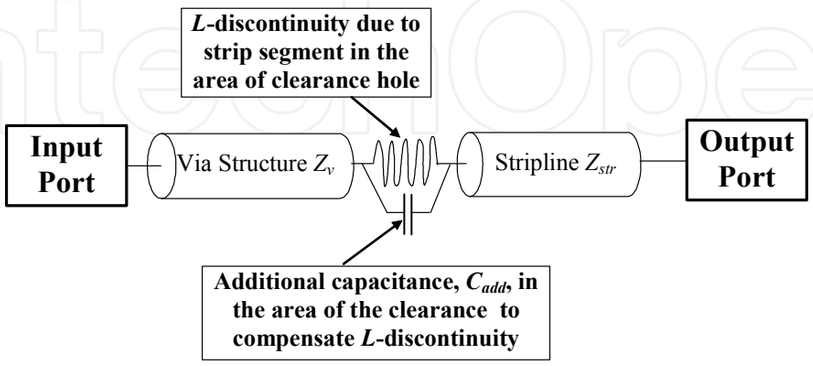


Fig.26. Block diagram of signal propagation in the model shown in Figs.22a and 22b

The additional capacitance can be obtained by forming a transition from the signal via pad to the stripline as the liner taper of the strictly-defined length. Note that the taper length, in this case, is an important parameter to control the magnitude of the additional capacitance and, as a result, the characteristic impedance matching in the considered model. In Fig.27, the horizontal cross-section view is presented for the same model as in Figs.22a and 22b, but only here a linear taper is formed as the transition from the signal via pad to the stripline. The dimensions of the via-stripline structure and parameters of the PCB are the same as for Figs.22a and 22b.

The effect of the taper length is presented in Fig.28 by means of TDR data. In this figure, four characteristic cases of via-to-stripline transitions are presented: The first is the model without application of the compensating method; The second is the transition formed as the linear taper for which the length is equal to the radius of the clearance hole; The third is the optimal taper length application; The fourth is the transition in which a long taper is used.

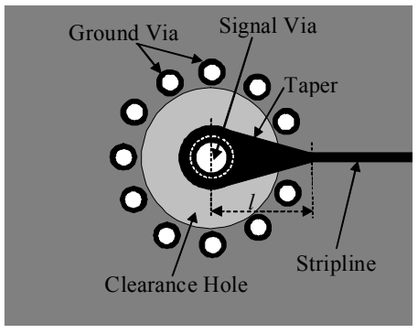


Fig. 27. Horizontal cross-sectional view of shield via in multilayer board taken in the position of stripline.

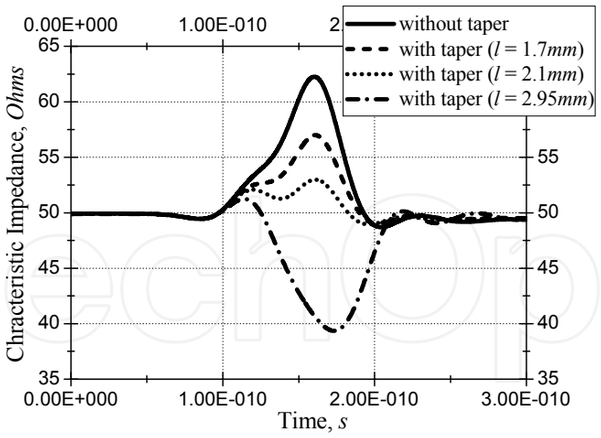


Fig. 28. Characteristic impedance in time domain

As follows from this figure, a good impedance matching (within 5*Ohms* or 10% of the nominal value) is achieved by the use of the linear taper having the length of l=2.1*mm*. Note that this length is larger than the radius of the optimal clearance hole used in the via structure.

On the one hand, the taper with the length equal to the radius of the clearance hole shows the higher excess inductive reactance than indicated nominal value (50*Ohms*). On the other hand, the long taper (2.95*mm* for presented test structure) leads to a high excess capacitance reactance.

Thus, a key point to realize a high-performance transition from the via pad to the planar transmission line is not only the use of the compensating part in the form of a linear taper but also its strictly-defined length as follows from data demonstrated in Fig.28.

Such result can be also traced by means of magnitudes of *S*-parameter data presented in Fig.29a and 29b in the frequency band up to 20*GHz*. These figures shows that the model with the linear taper of the optimal length (*l*=2.1*mm*) has the highest electrical performance compared with other transitions used.

To verify simulated results, experimental patterns of the same models disposed in the FR-5 multilayer board have been designed. In the measurement system, the SMA connectors have been used to provide the connection of the test model and a vector network analyzer. In Fig.30, a block diagram of the experimental patterns is presented.

In Fig.31, photo of bottom view of the test model is demonstrated. Also in Fig.32, photo of the total view of the top side of experimental patterns is shown.

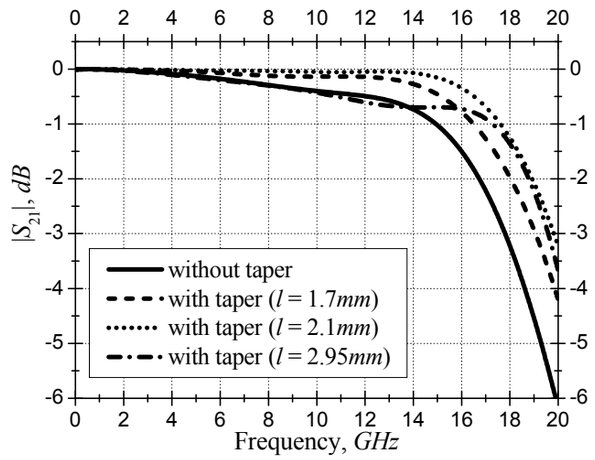


Fig. 29a Simulated insertion loss for test models

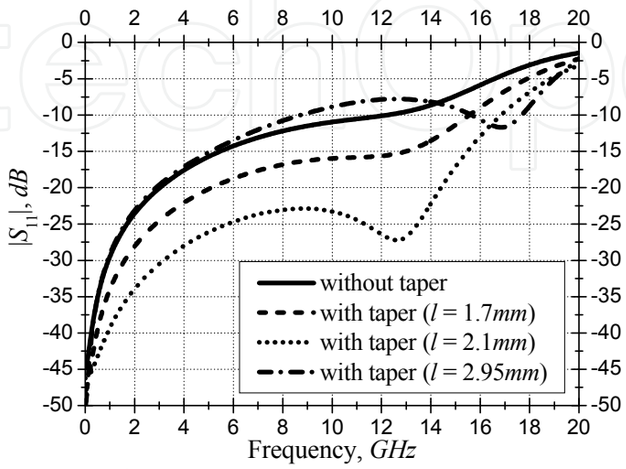


Fig. 29b Simulated return loss for test models

In Fig. 33 and 34, measured time-domain responses from the test models without the compensating technique application and with the taper optimized are respectively presented.

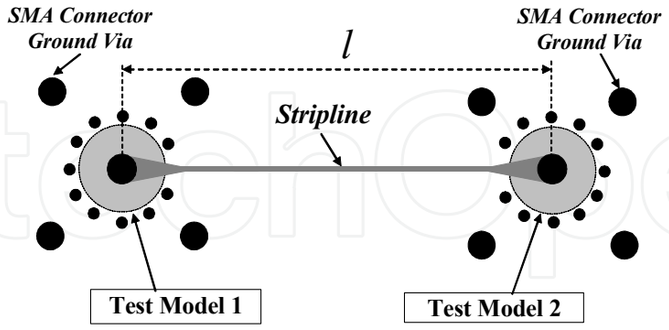


Fig. 30. Block diagram of experimental pattern

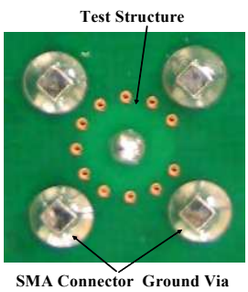


Fig. 31. Photo of experimental pattern (bottom view) of the test model

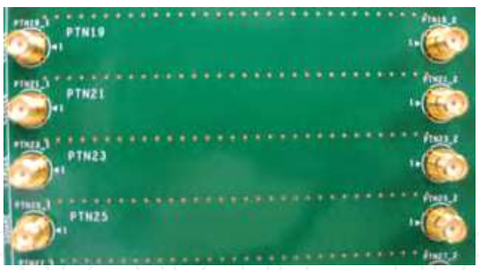


Fig. 32. Photo of experimental patterns (top view) of test models

As one can see in Fig. 33, measured TDR data demonstrate impedance mismatching up to 63*Ohms* in the area of the connection of the shield via having the characteristic impedance of about 50*Ohms* and the 50*Ohms* stripline. Also, presented measurement results are in a good agreement with the simulated data demonstrated in Fig.28.

Experimental data shown in Fig.34 make an approval of effectiveness of the use of the taper of the strictly-defined length to compensate the excess inductive reactance excited in the area of the clearance hole of the via-to-stripline transition. Thus, the use of the linear taper of l=2.1*mm* leads to impedance matching within ±10% of the nominal value 50*Ohms* (see Fig.34) that is corresponding to simulation data.

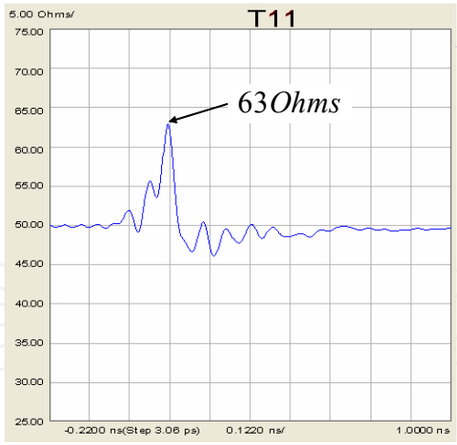


Fig. 33. Characteristic impedance in time domain for the test model without application of linear taper between signal via pad and stripline

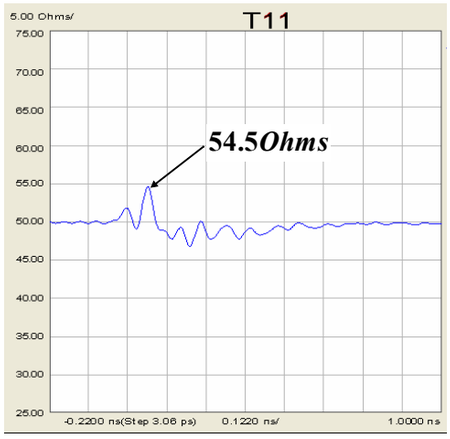


Fig. 34. Characteristic impedance in time domain for the test model with application of optimal linear taper (l=2.1mm) between signal via pad and stripline

Compensating method to improve impedance matching between a via structure and a planar transmission line disposed in a multilayer substrate is presented here. This method is a powerful technique to obtain high-performance electrical interconnections in high–speed multilayer substrates in which a liner taper of the strictly-defined length between the signal via pad and the planar transmission line is used to compensate the excess inductive reactance and to achieve required impedance matching.

4. Bandpass and Bandstop Filter Design Using Shield Via Approach

Two above-mentioned sections serve a good basis for development of high-performance interconnections and can be applied in high-frequency and high-speed multilayer substrates of present and next-generation communication and computing equipment.
Key point of this paragraph is a promotion of an approach using shield vias presented as a basis for providing miniaturization of both systems and components. Positioning of these directions is shown in Fig.35.

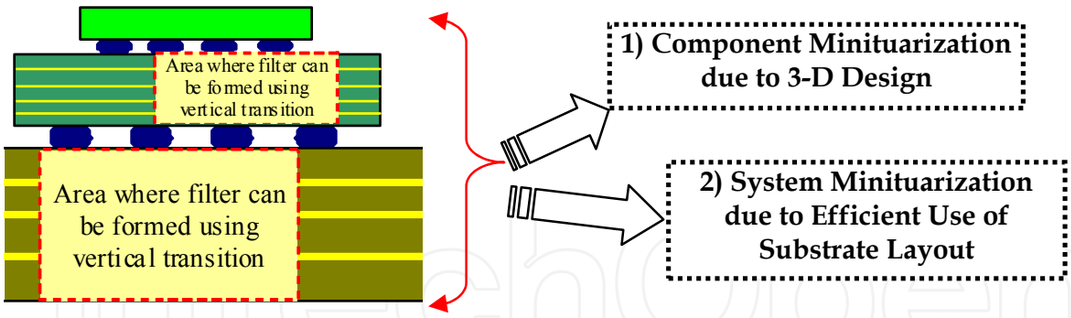


Fig. 35. Target of development of a component by means of the use of a shield via

So, we will start directly from an interconnected circuit which has been developed to realize the approach (Kushta et al., 2005; Kushta & Harada, 2008). Characteristic feature of this configuration is shown in Fig.36.

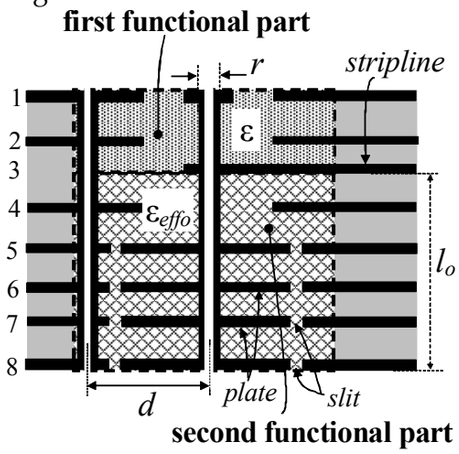


Fig. 36. A combined via structure in a multilayer substrate to form an open-circuited stub

First of all, a combined via structure, which includes two functional parts, is a distinguishing point. Consider each functional part in details.

The first functional part of the composite via structure is extended in the vertical direction from the top conductor layer to the signal conductor layer (where a stripline is disposed) of the multilayer substrate (see Fig.36). This functional part, formed as a shield via segment, provides impedance-matched low-loss signal transmission between signal pad disposed at the top conductor layer and stripline formed at signal conductor layer (third conductor layer in the structure presented). Its design can be made on the basis of the corrugated coaxial waveguide model given here.

The second functional part is extended in the vertical direction from the signal conductor layer to the bottom conductor layer. This functional part of the combined via structure serves to obtain a resonant stub. The resonant stub, besides the signal via surrounded by ground vias, comprises conductive plates connected to the signal via and separated from ground conductors by isolating slits.

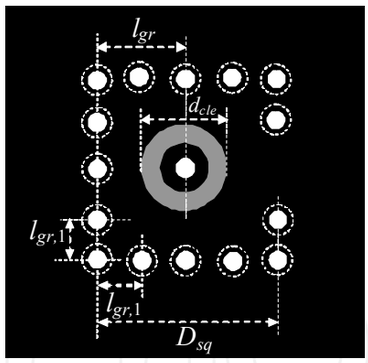
Each functional part of the combined via can be characterized as a transmission line with appropriate characteristic impedance and propagation constant.

Electromagnetic properties of the first functional part can defined by means the characteristic impedance $Z_1 = f(r, d, \varepsilon)$ and propagation constant $\beta_1 = \frac{\omega}{c} \cdot \sqrt{\varepsilon}$, wherein $Z_1 = f(r, d, \varepsilon)$ shows a dependency of the characteristic impedance on transverse dimensions of the signal via, *r*, distance between the signal via and ground vias, *d*, and relative permittivity of an isolating material filling in the multilayer substrate, ε; ω is the angular frequency, *c* is the velocity of light in free space.

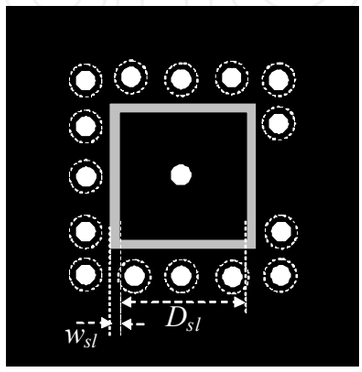
For the second functional part, the characteristic impedance and propagation constant can be represented as following: $Z_2 = f(r, d, \varepsilon_{eff})$ and $\beta_2 = \frac{\omega}{c} \cdot \sqrt{\varepsilon_{eff}}$, wherein, besides dimensional dependency for the characteristic impedance similar to the first functional part, the second functional parameters are a function of ε_{eff} which is dependent on dimensions and form of the conductive plates connected to the signal via, the distance between these conductive plates in the vertical direction, and the relative permittivity of the isolating material filling in the multilayer substrate.

Thus, by means of the combined via structure, we have obtained a cost-effective approach to design a miniaturized stub in which the resonant frequency is dependent on the stub length, l_0, and ε_{eff} , which can be much higher (!) than the relative permittivity of the substrate isolating material and in such way providing compactness of a filter using such stub.

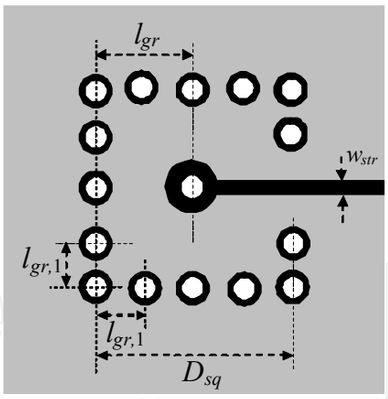
Consider a representative example of the combined via structure used to form the open-circuited stub for which top, bottom and cross-sectional views are shown in Figs.37a, 37b, 37c and 37d.



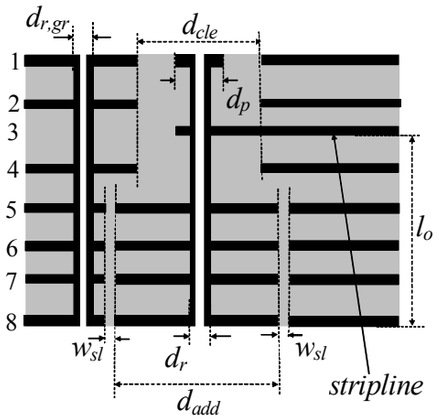
a) Top view



b) Bottom view



c) Horizontal cross-sectional view at signal layer



d) Vertical cross-sectional view

Fig. 37. Open-circuited stub formed by combined via structure in 8-conductor-layer PCB

Here, the stub is formed as a part of the shield via between the stripline disposed at the third conductor layer and pad formed at the bottom conductor layer of an 8-conductor-layer PCB Copper planar conductor layers of this PCB are isolated by the FR-4 material with the relative permittivity of $\varepsilon = 4.17$ as assumed in simulations. Arrangement of ground vias in the shield via has a square contour. Dimensions of the shield via (see Figs.37a, 37b, 37c, and 37d) are as following: $d_r = 0.65mm$, $d_{cle} = 1.65mm$, $d_p = 0.95mm$, $d_{r,gr} = 0.25mm$, $l_{gr} = 1.66mm$, $l_{gr,1} = 0.83mm$, $D_{sq} = 3.32mm$.

Conductive plates connected to the signal via to control the resonance frequency of the stub by means ε_{eff} have a square form with side of $d_{add} = 1.1mm$. The plates are separated from ground plates at the conductor layers by isolating slits of $w_{sl} = 0.2mm$.

Total thickness of the PCB including all conductor layers is 1.847*mm*. The thickness of the conductor layers is as follows: 0.062*mm* for layer 1; 0.069*mm* for layer 8; 0.035*mm* for layers 2, 3, 4, 5, and 6. The distance between conductor layers is as follows: 0.146*mm* is between layers 1 and 2; 0.123*mm* is between layers 2 and 3; 0.138*mm* is between layers 3 and 4; 0.677*mm* is between layers 4 and 5; 0.138*mm* is between layers 5 and 6; 0.138*mm* is between layers 6 and

7; and 0.146*mm* is between layers 7 and 8. Width of the stripline, w_{st}, at the third layer is 0.19*mm*.

In simulations, the same 3-D full-wave electromagnetic field solver has been used. Electromagnetic properties of such open-circuited stub are studied by means of *S*-parameter matrices in the frequency band up to 20*GHz* and are presented in Fig.38. Note that in these simulations signal is propagating between the pad of the combined via structure at the top conductor layer and the end of the stripline embedded in the PCB. From presented results the bandstop effect of the open-circuited stub at the central frequency of about 8*GHz* is clearly traced. This example demonstrates a possibility to form a filter using such open-circuited stub as a building block. The resonance frequency, f_{ro}, of the open-circuited stub can be defined as following:

$$f_{ro} = \frac{c}{4 \cdot \sqrt{\varepsilon_{effo}} \cdot l_o}, \tag{10}$$

where l_o is the length of the stub (or the second functional part in the vertical direction) as shown in Fig.37d.

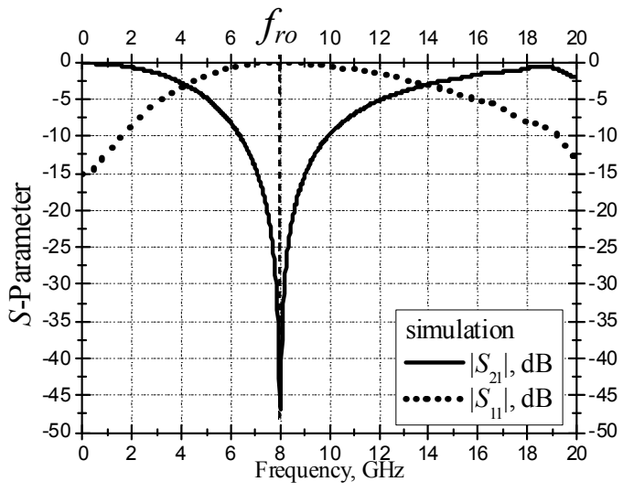


Fig. 38. Simulated insertion ($|S_{21}|$-parameter) and return ($|S_{11}|$-parameter) losses for open-circuited stub in 8-conductor-layer PCB

In the similar manner, a short-circuited stub can be obtained by means of another combined via structure in a transition from this via structure to a stripline as presented in Fig.39. In this case, the pad of the second functional part disposed at the bottom conductor layer is connected to the ground plane. Magnitudes of *S*-parameters for such configuration are demonstrated in Fig.40. Dimensions of the via structures, conductor plates connected to the signal via, stripline, and PCB are the same as for the aforementioned open-circuited stub case. Shown data demonstrate the bandpass effect with the central resonance frequency about 13*GHz*. This resonance frequency can be defined for this structure as following:

$$f_{rsh} = \frac{c}{4 \cdot \sqrt{\varepsilon_{effs}} \cdot l_{sh}}, \tag{11}$$

It is important to note that $\varepsilon_{effo} \neq \varepsilon_{effs}$, because different number of conductive plates is used to form the effective medium in short-circuited and open-circuited stubs. As one can see from Figs. 38 and 40, conductive plates connected to the signal via are powerful parameter to control resonance characteristics of both open- and short-circuited stubs.

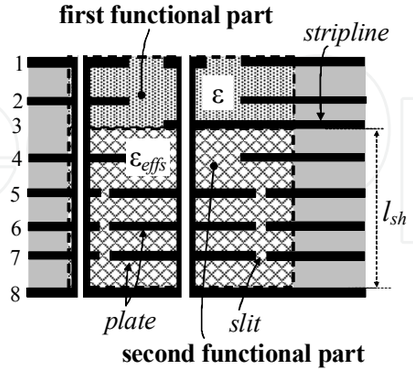


Fig. 39. A combined via structure in a multilayer substrate to form a short-circuited stub

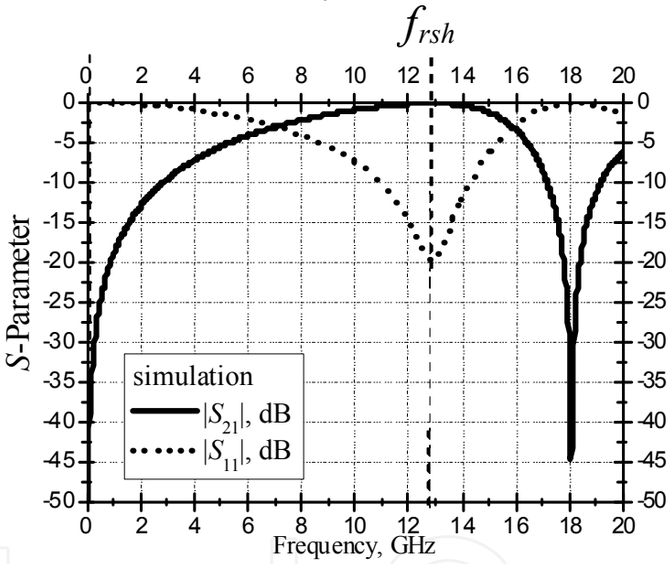
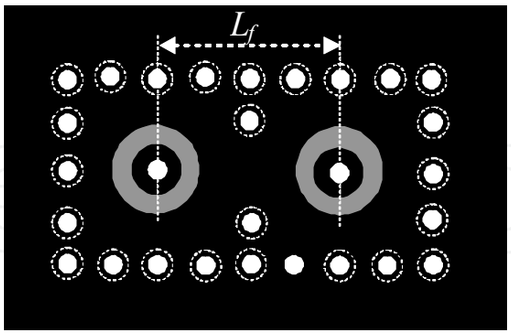


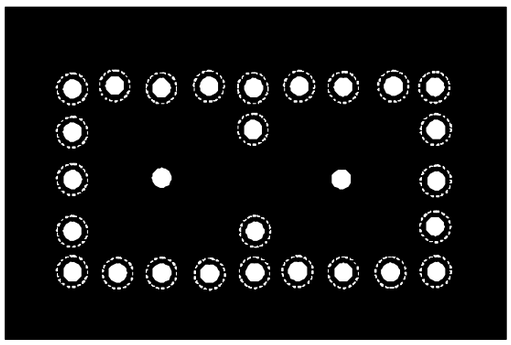
Fig. 40. Simulated insertion and return losses for short-circuited stub

As the next step, it will be shown here that the combined via structures can be effectively used to form high-performance filtering components. In Figs.41a and 41b, 41c and 41d, top and bottom views, horizontal and vertical cross-sectional views of a bandpass filter are shown, respectively. This filter is designed by the use of two identical combined via structures (discussed above) forming short-circuited stubs in the 8-conductor-layer PCB. Photographs of an experimental pattern of such bandpass filter are presented in Fig.42. Dimensions of the shield via, conductive plates connected to the signal vias, isolating slits, stripline connecting two signal vias, and PCB are the same as for the combined via structure forming aforementioned short-circuited stub. The distance between the centers of signal via conductors, L_f, is 3.32*mm*. Input and output ports of the filter are at the pads of the signal vias as shown in Fig.41d.

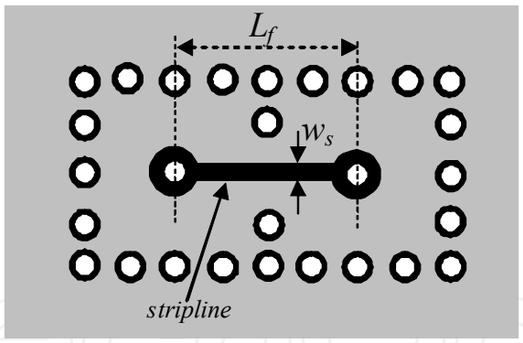
Simulated data of magnitudes of *S*-parameters for the considered bandpass filter in the 8-conductor-layer PCB are shown in Fig.43. In this figure one can define clearly-expressed bandpass properties of the filter in the frequency band from about 9*GHz* to 15*GHz*.



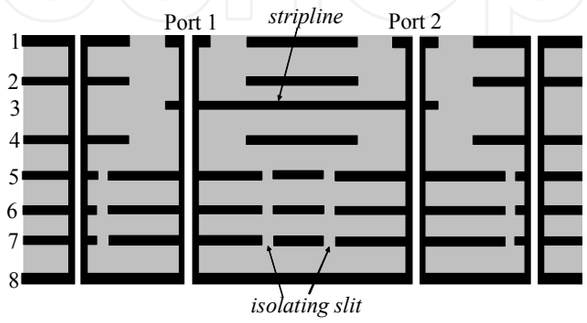
a) Top view



b) Bottom view



c) Cross-sectional view at signal layer



d) Cross-sectional view

Fig. 41. Bandpass filter in 8-conductor-layer PCB

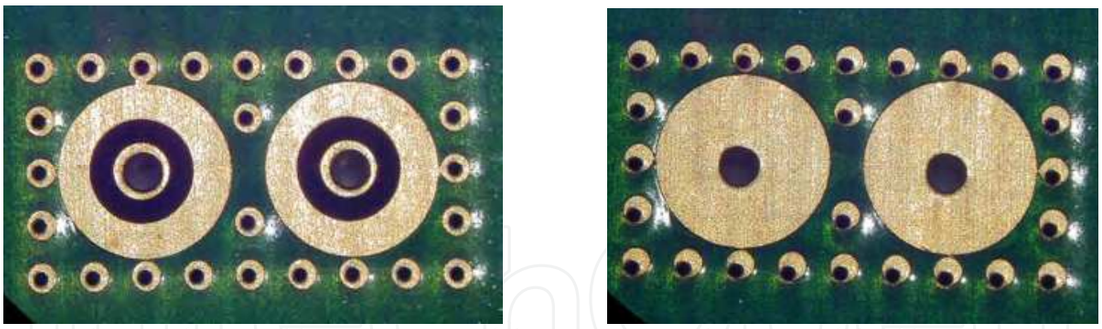


Fig. 42. Photos of top and bottom views of the experimental pattern of the filter

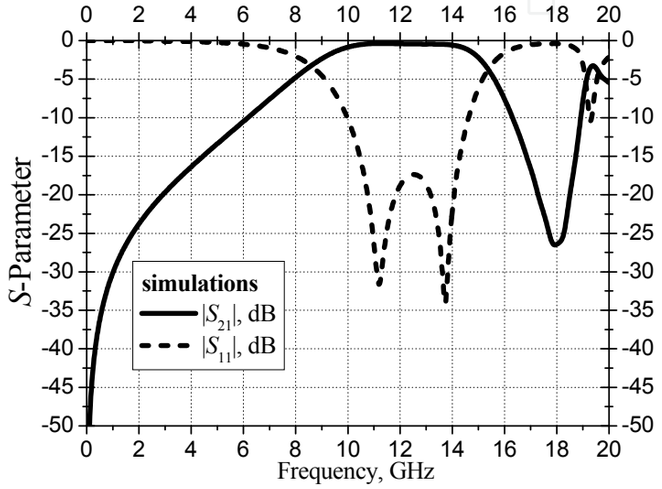


Fig. 43. Simulated insertion and return losses for bandpass filter formed by two short-circuited stubs

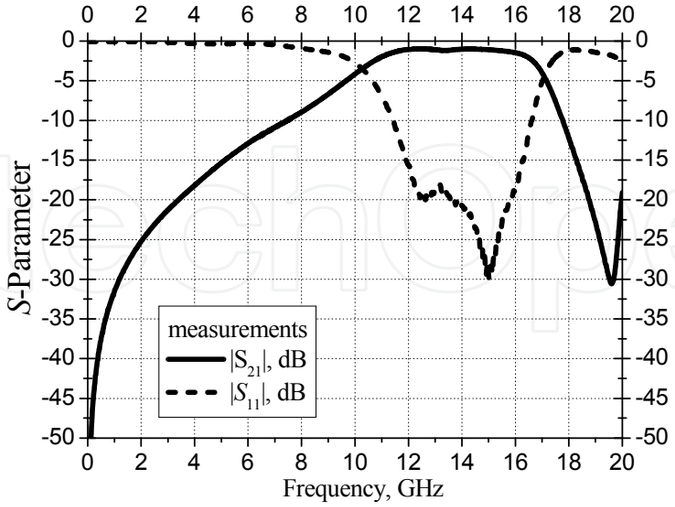


Fig. 44. Measured insertion and return losses for bandpass filter formed by two short-circuited stubs

Experimental verification of the bandpass filter presented and proposed 3-D approach are shown in Fig.44. In this figure, measured data for the filter having the same dimensions as for Fig.43 are presented. These data demonstrate similar bandpass characteristics and are in a good agreement with the simulation results.

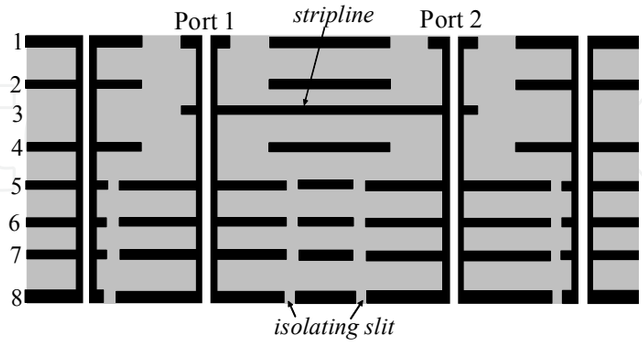


Fig. 45. Cross-sectional view of filter formed by two open-circuited stubs

Another type of filters can be obtained if open-circuited stubs will be used instead of short-circuited ones. Cross-section view of such filter is presented in Fig.45.
In Fig.46, simulated magnitudes of *S*-parameters are shown. This filter demonstrates clearly-expressed bandstop properties with the central frequency of about 8*GHz*.
As a validation of simulated results, in Fig.47, measured data for the filter are presented. As one can see, these data are corresponding to simulation with a good accuracy, including the central frequency.

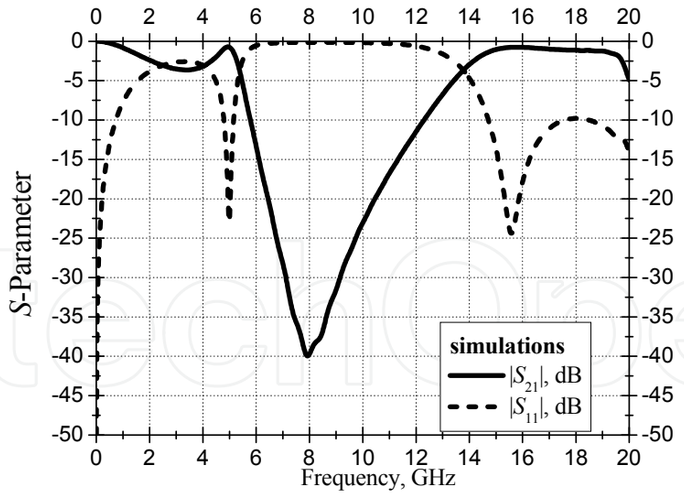


Fig. 46. Simulated insertion and return losses for bandpass filter formed by two short-circuited stubs in 8-conductor-layer PCB

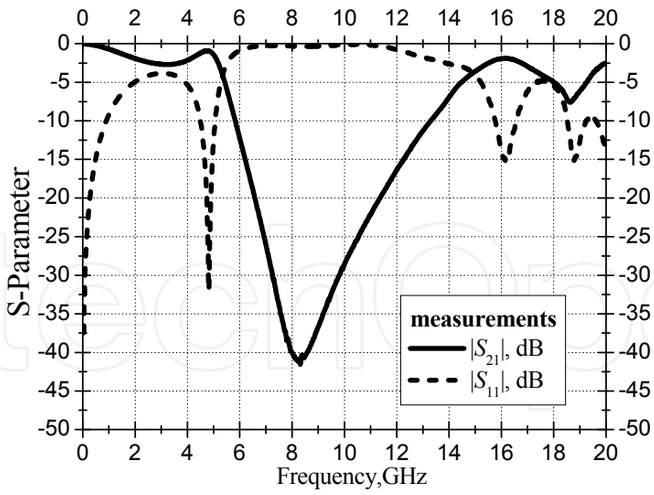


Fig. 47. Measured insertion and return losses for bandpass filter formed by two short-circuited stubs in 8-conductor-layer PCB

Developed approach can be applied to obtain a multipole filter. In Fig.48, a compact four-pole bandpass filter is presented. This filter consists of four identical short-circuited stub elements (as in two-pole filter) connected by the stripline. In Fig.49, simulated *S*-parameters for the filter are shown. As one can see, the increase of quantity of stub elements can control bandpass characteristics. In present example, it leads to sharpening the pass band compared with the two-pole filter.

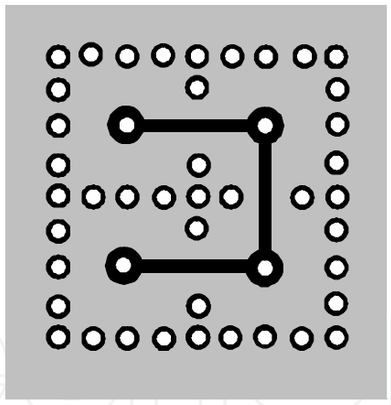


Fig. 48. Cross-sectional view at the signal layer of the bandpass filter formed by four short-circuited stubs in 8-conductor-layer PCB

Thus, these examples of the bandpass and bandstop filters demonstrate applicability of presented approach to design compact and cost-effective filtering components using shield vias in a multilayer substrate.
Required frequency band and desired characteristics of the filter can be achieved by an appropriate choice of dimensions and quantity of the short-circuited or open-circuited stubs. Also, an optimization of the parameters of the filter can be provided by the determination of an appropriate distance between the stubs. Such design techniques will be studied and presented in the future in details.

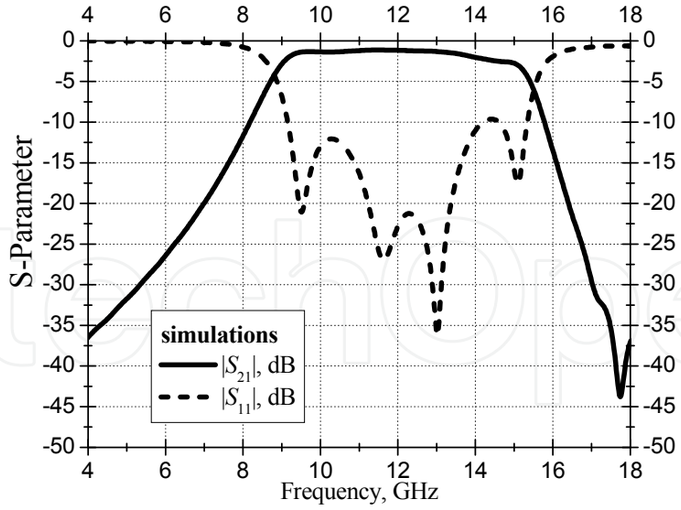


Fig. 49. Simulated insertion and return losses for bandpass filter formed by four short-circuited stubs in 8-conductor-layer PCB

5. Conclusion

In this chapter, advantages of shield vias disposed in a multilayer substrate at the higher frequencies have been shown. These structures have low leakage losses, well-controlled characteristic impedance and definite propagation constant. Presented physical model for the electromagnetic behavior of the shield via is consistent with results obtained by simulations and measurements and can be used for optimum design of vertical transitions in multilayer substrates for high-speed and high-frequency applications. Moreover, vertical transitions demonstrating the electrical performance similar to planar transmission lines can be obtained in multilayer substrate structures.

Also, a powerful 3-D approach to design filtering components using shield vias is presented here. A distinguishing point of this approach is a combined via structure comprising two functional parts. The first functional part is responsible for low-loss signal transmission in a wide frequency band and can be design by means of the corrugated coaxial waveguide model presented here for shield via. The second functional part serves to form a compact short-circuited or open-circuited resonant stub acting as a building block of a filter and comprises conductor plates connected to the signal via to control characteristic impedance and propagation constant in this functional part. Simulation and measurement data for bandpass and bandstop filters presented demonstrate applicability of the approach to design compact and cost-effective filters for highly integrated systems at microwave and millimeter waves with an improved EMI performance.

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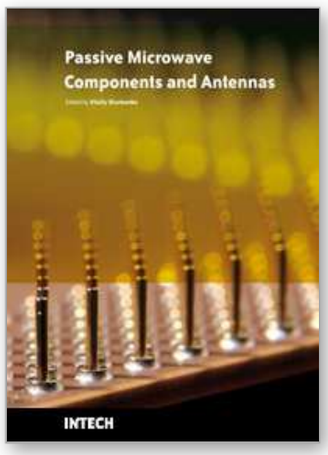

Passive Microwave Components and Antennas

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Modelling and computations in electromagnetics is a quite fast-growing research area. The recent interest in this field is caused by the increased demand for designing complex microwave components, modeling electromagnetic materials, and rapid increase in computational power for calculation of complex electromagnetic problems. The first part of this book is devoted to the advances in the analysis techniques such as method of moments, finite-difference time- domain method, boundary perturbation theory, Fourier analysis, mode-matching method, and analysis based on circuit theory. These techniques are considered with regard to several challenging technological applications such as those related to electrically large devices, scattering in layered structures, photonic crystals, and artificial materials. The second part of the book deals with waveguides, transmission lines and transitions. This includes microstrip lines (MSL), slot waveguides, substrate integrated waveguides (SIW), vertical transmission lines in multilayer media as well as MSL to SIW and MSL to slot line transitions.

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