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Technology CAD of Nanowire FinFETs

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1. Introduction

The potential applications of semiconductor nanowire (NW) field-effect transistors as potential building blocks for highly downscaled electronic devices with superior performance are attracting considerable attention. In the area of Technology CAD (TCAD) of nanowire FinFETs, it is fair to say that there have been very little or no reports are available in the literature on TCAD modeling of nanowire FinFETs. This chapter presents a detailed framework for virtual wafer fabrication (VWF) including both the device design and the manufacturing technology.

Technology computer aided design is now an indispensable tool for the optimization of new generations of electronic devices in industrial environments. In recent years, non-classical MOS devices such as nanowire FinFETs have received considerable attention owing to their capability of suppression of short channel effects, reduced drain-induced barrier lowering and excellent scalability. Different methods have been reported for the fabrication of silicon nanowires. The novel device designs need three-dimensional (3-D) process and device simulations. Nanowire FinFETs being nonplanar are inherently three-dimensional (3-D) in nature. Sentaurus process tool (3-D process simulation) has been used to study suitability of technology CAD for FinFET process development and the simulation results will be presented in this Chapter. TCAD predictability FinFETs having 25 nm gate lengths with nitride cap layer and fabricated using a conventional CMOS like process flow for novel strain-engineered (process-induced strain) nanowire have been described in detail. Effects of process-induced strain on the performance enhancement of nanowire FinFETs have been discussed.

Sentaurus Device simulator has been used to study electrical characteristics by solving self-consistently five partial differential equations (Poisson equation, electron and hole continuity equations, electron energy balance equation, and the quantum potential equation).The detail of device simulation for FinFETs will be presented. A compact model serves as a link between process technology and circuit design. As FinFETs are predicted to be used in RFIC applications, flicker noise in FinFET becomes very important and modeling of noise in FinFETs will also be described. Hot-carrier induced degradation behavior of nanowire FinFETs and extraction of SPICE parameters essential for circuit analysis and design will be described.

2. Importance of TCAD

For the past four decades, the performance of very large scale integrated (VLSI) circuits and cost-per-function has been steadily increased by geometric downscaling of MOSFETs.

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Advanced transistor structures, such as multiple-gate (MuG) or ultra-thin-body (UTB) silicon-on-insulator (SOI) MOSFETs, are very promising for extending MOSFET scaling because short channel effect (SCE) can be suppressed without high channel doping concentrations, resulting in enhanced carrier mobilities. In recent years, non-classical MOS devices such as FinFETs have received considerable attention owing to their capability of suppression of short channel effects, reduced drain-induced barrier lowering and excellent scalability.

The Ω-FinFETs have unique features such as high heat dissipation to the Si substrate, no floating body effect, and low defect density, while having the key advantages of the silicon-on-insulator (SOI)-based FinFETs characteristics. The Ω-FinFET has a top gate like the conventional UTB-SOI, sidewall gates like FinFETs, and special gate extensions under the silicon body. The Ω-FinFET is basically a field effect transistor with a gate that almost covers the body. However, the manufacturability of this type of device structures is still an issue. Many different methods have been proposed to fabricate these devices but most of them suffer from technical challenges mainly due to the process complexity.

Strained-Si technology is beneficial for enhancing carrier mobilities to boost Ion. Both electron and hole mobilities can be improved by applying stress to induce appropriate strain in the channel, e.g., tensile strain for n-channel MOSFETs and compressive strain for p-channel MOSFETs (Maiti et al., 2007). Effect of strain on mobility can be understood by considering the stress induced changes in the complicated electronic band structures of Si. The novel device designs increase the need for three-dimensional (3-D) process and device simulations. FinFET is a nonplanar device and are inherently three-dimensional (3-D) in nature. Therefore, for FinFETs, any meaningful process or device simulation must be performed in three dimensions. Synopsys tools SProcess/SDevice address this need (aSynopsys & bSynopsys, 2006).

2.1 Process simulation

The FinFET process flow used in process simulation is similar to the flow presented by F.-L. Yang *et al.* (Yang et al., 2002). Process flow used is summarized as follows:

1. Fin patterning and threshold voltage implant
2. Gate oxidation, In-situ N+poly gate deposition and patterning
3. nMOS S/D extension implantation
4. Spacer formation
5. S/D implantation

i. Contact formation

As the Sentaurus Process ([a]Synopsys, 2006) is designed as a simulator that works independently of the dimensionality of the structures to be simulated, the process flow was executed by a sequence of three tool instances as discussed above. During the process flow execution, intermediate structures are saved for subsequent use by Sentaurus Process. Sentaurus Process loads the intermediate geometries generated by Sentaurus Structure Editor and performs the implantation and diffusion steps associated with each intermediate structure. The starting material is a (100) FDSOI wafer with a top silicon layer thickness of 25 nm. The top silicon layer has initially a uniform boron concentration of ~5.5x1018 cm^{-3}. The Fin height used in simulation was up to 50 nm, and with 12 nm cap oxide. Channel doping is performed to adjust nMOS Vt using ion implantation. To relieve the etch damage; a sacrificial oxide is removed before gate oxidation. 25 Å thermal oxide is grown and in-situ

heavily doped N+ poly-silicon is deposited. After gate plasma etch, the source/drain extension implantation is simulated followed by annealing simulation.
The activation/annealing are simulated by Sentaurus Process using the pair diffusion model. For the 3-D Ω-FinFET simulation, analytic implantation model is used. For the point defects, the appropriate model is activated. For the activation, the solid solubility model is used. To capture the influence of the nonequilibrium point-defect concentrations on the diffusivity of the dopants (phosphorus, arsenic, and boron), the advanced pair-diffusion model is used. It has been observed that during the annealing process, boron is redistributed in a complex fashion. The arsenic extension implant introduces a large amount of interstitials, which during the annealing diffuse quickly to the surface, where they recombine. As boron diffuses only as boron interstitial pairs, boron is transferred to the surface in this process. Due to small volume in the channel Fin, a limited amount of boron is available and, therefore, the boron pileup at the surface in the extension area is accompanied by a corresponding depletion of boron in the center of the channel fin in the extension area. Composite spacer of silicon oxide and nitride is deposited and etched anisotropically with final thickness of ~ 32 nm. Heavily doped N^+ and P^+ junction are made with Phosphorous

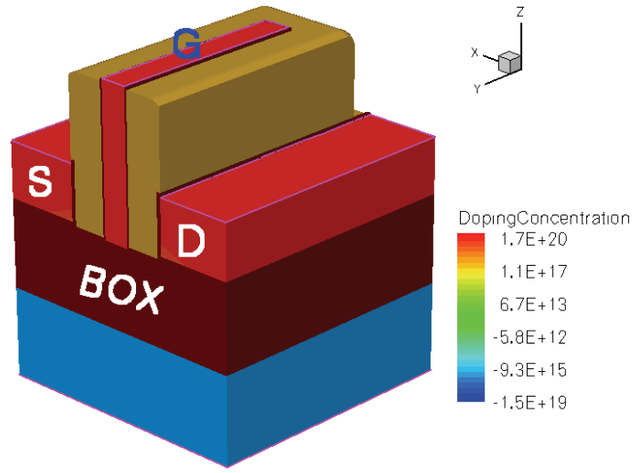

Fig. 1a. Device structure after process simulation.

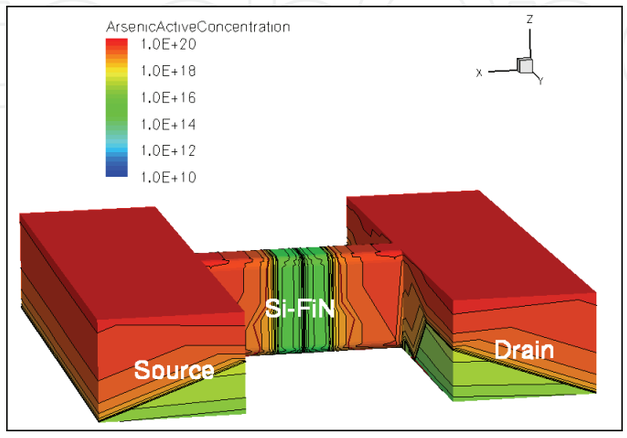

Fig. 1b. Arsenic distribution inside the Strained-Si Fin.

and Boron implantation. Thermal anneals above 1000°C are used for dopants activation. The process was completed by standard metal contact formation. Fig. 1-2 show some process simulated results for 25 nm gate length FinFETs. Silicon-Fin is fabricated on buried-oxide (BOX) and consecutively capped with nitride (Si_3N_4). A tensile process induced strain has been evolved in the Fin, during thermal process.

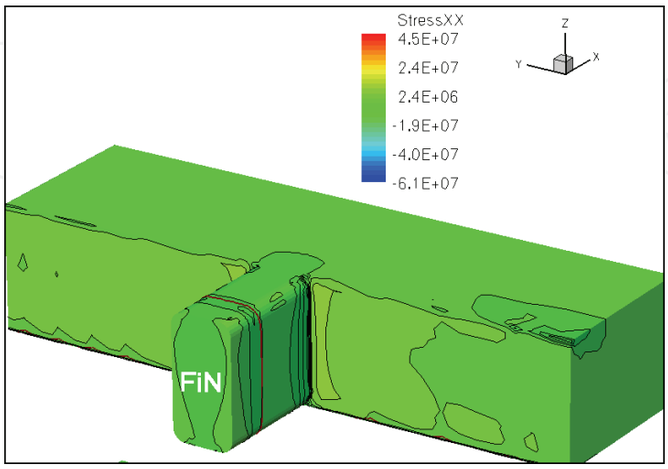

Fig. 2. Stress (ε_{xx}) distribution in channel for Ω-FinFET.

2.2 Device simulation

In advanced deep submicron MOS device structures, transport models must be used. Also the channel–gate oxide interface must be resolved to a very high level of accuracy. The finite-element mesh must also resolve the very steep gradients of the inversion layer. Accordingly, Noffset3D is used to remesh the Ω- FinFET for the device simulations. Also for the Ω-FinFET structure considered here, the body may not be fully depleted. Therefore, the continuity equations for both electrons and holes must be solved simultaneously. The very short gate length of 25 nm mandates the use of the hydrodynamic transport model. Further, the thin oxide thickness (2.4 nm) and relatively high body doping level (~5.5x1018 cm^{-3}) require the consideration of quantization effects. Unlike other approaches to model quantization effects such as 1-D Poisson–Schrödinger and the modified local-density approximation (MLDA), the density gradient model is also applicable to nonplanar 3-D structures. Thus, in simulation, advanced quantization model (density gradient model) is used. Within the density gradient model, an additional partial differential equation is solved to determine the effective quantum potential. For the 3-D FinFET, Sentaurus Device solves self-consistently five partial differential equations (Poisson equation, electron and hole continuity equations, electron energy balance equation, and the quantum potential equation). In device simulation, the I_{ds}–V_{gs} characteristics for a low-drain bias and high-drain bias are simulated and relevant electrical parameters, such as threshold voltages and drain current are extracted.

2.3 Results and discussion

Fig. 3 shows the I_{ds}-V_{gs} characteristics for the device with the strained cap layer and relaxed cap layer. The ON-state Ids of~ 0.42 and ~0.38 mA/μm are obtained for strained and unstrained-Si Ω-FinFET, with OFF-state Ids < nA at an operating voltage of 1.0 V ($|V_{gs}$ −

V_{th}| = 0.96 V and |V_{ds}| = 1.0 V). A slight V_t shift of approximately 15 mV is due to the strain-induced effect on bandgap. One can expect much higher drive currents by further reducing the channel length and gate oxide thickness. Despite the use of a 2.4 nm thick gate oxide, strained-Si Ω-FinFET exhibits near ideal S.S. (~64 mV/dec) and low DIBL (~20 mV/V).

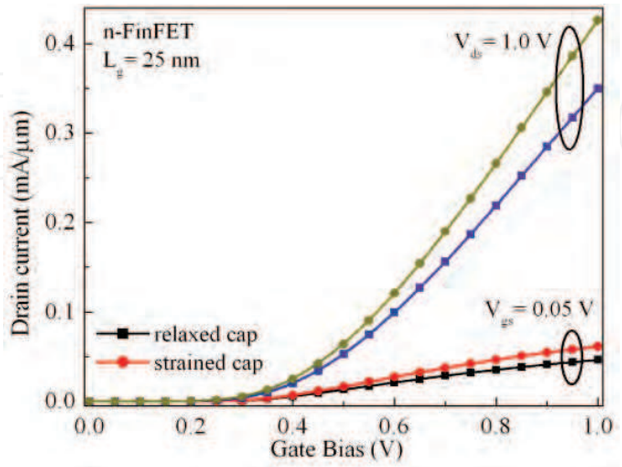

Fig. 3. I_d-V_{gs} characteristic of FinFETs at V_{ds} = 0.05 V and 1.0 V with stressed nitride cap layer and relaxed cap layer.

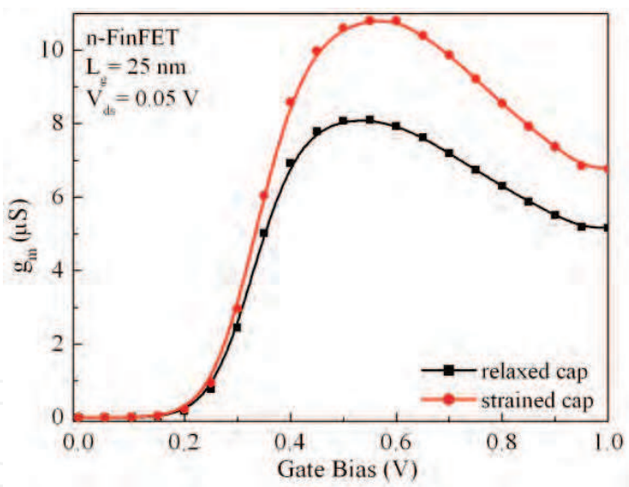

Fig. 4. Comparison of simulated transconductance for both FinFET.

Fig. 4 shows the $g_m(dI_{ds}/dV_{gs})$ variation as a function of gate bias for both devices. Ω-FinFETs shows the peaking in gm value due to mobility dependence on gate-field which is well known for the bulk FET devices. The main reason is the electron confinement due to strain near surface where surface roughness scattering of the carriers at high gate fields (with reduced carrier mobility) leads to the peaking in gm. For strained-Si Ω-FinFET, a 30% higher g_m than reference transistor is observed.

Fig. 5 compares the I_{ds}-V_{ds} characteristics for the devices with a highly tensile cap layer and a relaxed cap layer. The Ω-FinFETs with a highly tensile stress cap layer shows improvement of the saturation current I_{dsat} of approximately 13% compared to the device

with the relaxed cap layer. The stress that originates from oxidation and other processing steps has a minor effect on the carriers transport.

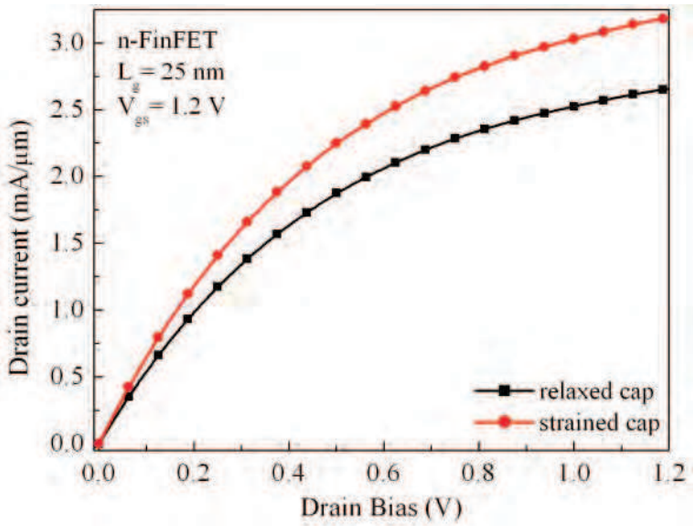

Fig. 5. I_{ds}-V_{ds} characteristics of FinFETs at V_g = 1.25 V with strained cap layer and relaxed cap layer

Summary of transistor parameters in comparison with conventional (Si only) FinFET is shown in Table 1. It is observed that simulated transistor performances (subthreshold swing and gate delay) of the Ω-FinFETs are significance.

Type	Bulk-Si FinFET	Strained-Si FinFET
Threshold voltage (mV)	434	381
Ion (μA/μm)	700	853
Ioff (nA/μm)	1.13	2.02
Subthreshold swing (mV/decade)	62.77	64.55
DIBL (mV/V)	26	20

Table 1. Comparison of transistor parameters with conventional FinFET.

3. Hot carrier degradation in nanowire (NW) FinFETs

Hot-carrier induced phenomena are of great interest due to their important role in device reliability ([b]Maiti et al., 2007). High energy carriers (also known as hot carriers) are generated in MOSFETs by high electric field near the drain region. Hot carriers transfer energy to the lattice through phonon emission and break bonds at the Si/SiO_2 interface. The trapping or bond breaking creates oxide charge and interface traps that affect the channel carrier mobility and the effective channel potential. Interface traps and oxide charge also affect the transistor parameters, such as, the threshold voltage and drive currents. Several workers have reported the results of their investigation on hot-carrier effects on the performance of p-MOS transistors (Pan., 1994; Heramans et al., 1998). It has been shown that the degradation of p-MOS transistors is caused by the interface state generation and hole trapping in the gate oxide from the hot-carrier injection. Reliability assurance of analog

circuits requires a largely different approach than for the digital case. It is generally accepted that injected and trapped electrons dominate the degradation behavior. In this work, we describe a physics based coulomb mobility model developed to describe Coulomb scattering at the Si-SiO_2 interface and implement in device simulator. Hot-carrier induced current and subsequent degradation in nanowire (NW) Ω-FinFETs are investigated using simulation and validation with reported experimental data. The influence of the hot carriers on the threshold voltage and drive currents is examined in detail for nanowire Ω-FinFETs.

3.1 Quasi-2D coulomb mobility model

The silicon (Si)–silicon dioxide (SiO_2) interface in nanowire (NW) Ω-FinFETs shows a very large number of trap states. These traps become filled during inversion causing a change of conduction charge in the inversion layer and increase the Coulomb scattering of mobile charges. Owing to the large number of occupied interface traps, Coulomb interaction is likely to be an important scattering mechanism in nanowire (NW) Ω-FinFET device operation, resulting in very low surface mobilities and may be described by a quasi-2D scattering model. The coulomb potential due to the occupied traps and fixed charges decreases with distance away from the interface. So, mobile charges in the inversion layer that are close to the interface are scattered more than those further away from the interface; therefore, the Coulomb scattering mobility model is required to be depth dependent. We assume that the electron gas can move in the x-y plane and is confined in the z direction. Electrons are considered confined or quantized if their deBroglie wavelength is larger than or comparable to the width of the confining potential. The deBroglie wavelength of electrons, given by $\lambda = \hbar / \sqrt{2m^* k_B T}$, is approximately 150Å at room temperature, where as the thickness of the inversion layer is typically around 50Å to 100Å. Thus, one may justify treating the inversion layer as a two dimensional electron gas. The scattering from charged centers in the electric quantum limit has been formulated by Stern and Howard (1967). We consider only the p-channel inversion layer on Si (100) surface where the Fermi line is isotropic and calculate the potential of a charged center located at (r_i, z_i). Using the image method, we get

$$V_i(r,z) = \frac{e^2}{4\pi\varepsilon_0 \tilde{k}\sqrt{(r-r_i)^2 + (z-z_i)^2}} \tag{1}$$

where $r^2 = x^2 + y^2$, z = 0 corresponds the Si/SiO_2 interface. z > 0 is in silicon whereas z < 0 is in the oxide. Where $\tilde{k} = (k_{Si} + k_{ox})/2$ for z < 0, and ε_o is the permittivity of free space. We assume parabolic sub bands with the same effective heavy-hole mass, m^*. Since inversion layer electrons are restricted to move in the x-y plane, they would only scatter off potential perturbations that they see in the x-y plane. Therefore, we are only interested in determining the potential variations along that plane. To do so, one needs to calculate the two dimensional Fourier transforms of the potential appearing in Eqn. (1). The hole wave functions are then given by

$$\psi_{i,k}(r,z) = \frac{1}{\sqrt{A}}\xi(z)e^{ik.r} \tag{2}$$

where i represent the subband index and $k=\left(k_x,k_y\right)$ is the two-dimensional wavevector parallel to the interface. $\xi(z)$ is the quantized wave function in the direction perpendicular to the interface, E_i its corresponding energy and $r=(x,y)$. We denote the area of the interface by A. The effective unscreened quantum potential for holes in the inversion layer in the electric quantum limit in terms of the 2D Fourier transform is given by

$$v(q,z_i)=\frac{e^2}{2\tilde{k}\varepsilon_0 q}\iint \xi_i(z)\xi_j(z)e^{-q.|z-z_i|}dz \tag{3}$$

We now consider the effect of screening due to inversion layer electrons on Coulombic scattering. Screening is actually a many-body phenomenon since it involves the collective motion of the electron gas. Using the Coulomb screening we get,

$$v(q,z_i)=\frac{e^2}{2\tilde{k}\varepsilon_0(q+q_s)}\iint \xi_i(z)\xi_j(z)e^{-q.|z-z_i|}dz \tag{4}$$

Where $q_s=\frac{e^2}{2\tilde{k}\varepsilon_0}\iint \xi_i(z)\xi_j(z)e^{-q.|z-z_i|}dz$ one obtains the scattering rate using Fermi's golden rules,

$$S(q,z_i)=\frac{2\pi}{\hbar^2}\left(\frac{e^2}{2\tilde{k}\varepsilon_0(q+q_s)}\iint \xi_i(z)\xi_j(z)e^{-q.|z-z_i|}dz\right)^2\delta\left(E_k-E_{k'}\right) \tag{5}$$

where $\hbar$ is Planck's constant. E_k and $E_{k'}$ denote the initial and final energies of the mobile charge being scattered. Scattering of inversion layer mobile charges takes place due to Coulombic interactions with occupied traps at the interface and also with fixed charges distributed in the oxide. Defining the 2D charge density $N_{2D}\delta(z_i)$ at depth z_i inside the oxide as the combination of the fixed charge N_f and trapped charge N_{it} as

$$N_{2D}(z_i)=\begin{cases}N_{it}+N_f(0), & z_i=0\\ N_f(z_i), & z_i<0\end{cases} \tag{6}$$

Using the above approximation, one obtains the total transition rate. Since, Coulombic scattering is an elastic scattering mechanism, the scattering rate or equivalently the inverse of the momentum relaxation time is then calculated as

$$\frac{1}{\tau_m}=\frac{1}{(2\pi)^2}\cdot\frac{2\pi}{\hbar^2}\left(\frac{e^2}{2\tilde{k}\varepsilon_0}\right)^2\int\left(\frac{1}{(q+q_s)}\iint \xi_i(z)\xi_j(z)e^{-q.|z-z_i|}dz\right)^2\delta\left(E_k-E_{k'}\right)(1-\cos\theta)\delta k \tag{7}$$

Using the above relaxation time, one obtains the mobility of the i-th subband as,

$$\mu_i=\frac{e}{m^*}\frac{\int\sum_i \tau_m\varepsilon\frac{\partial f_0(\varepsilon)}{\partial\varepsilon}d\varepsilon}{\int\varepsilon\frac{\partial f_0(\varepsilon)}{\partial\varepsilon}d\varepsilon} \tag{8}$$

The average mobility, $\bar{\mu}$, is then given by

$$\bar{\mu} = \frac{\sum_i p_i \mu_i^2}{\sum_i p_i \mu_i} \tag{9}$$

where p_i is the hole concentration in the i th subband. Taking into the different scattering mechanism and using the Matthiessen's rule one obtains the total mobility μ.

3.2 Mobility model implementation

The Coulomb scattering mobility model has been implemented in Synopsys Sentaurus Device simulator. To activate the mobility model appropriate mobility values were defined in the fields of the parameter file. Simulation data for the drain current (I_{ds}) versus gate voltage (Vgs) curves match the experimentally measured results very well (Singh et al., 2005). Fig. 6 shows the I_{ds}-V_{gs} characteristics of the simulated p-type nanowire Ω-FinFET with a 10 nm-thick, and 100 nm-long Si-fin as the channel body. At room temperature, the devices show high ON-current (I_{ds} at V_{ds} = Vgs = 1.1 V) of ~0.68mA/μm, V_{th} ~ 0.2 V, and subthreshold swing (SS) of ~68 mV/dec. Low drain-induced barrier lowering (DIBL) of ~10 mV/V is obtained, with $I_{ON}/I_{OFF} > 10^7$ at room temperature. These results are similar to those reported for nanowire Ω-FinFETs by Singh et al. (Singh et al., 2005).

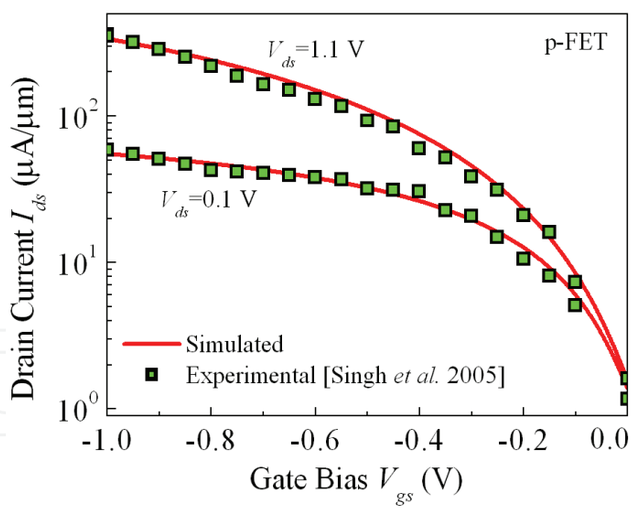

Fig. 6. Gate bias dependence of drain current for nanowire Ω-FinFETs (both simulated and experimental) (after [b]Maiti et al., 2008).

3.3 Results and discussion

Fig. 7 shows a lower drain current for Ω-FinFETs which underwent hot carrier stressing (compared to unstressed devices). Degradation in drain current indicates that hot-carrier induced positive charges are localized near the drain end.

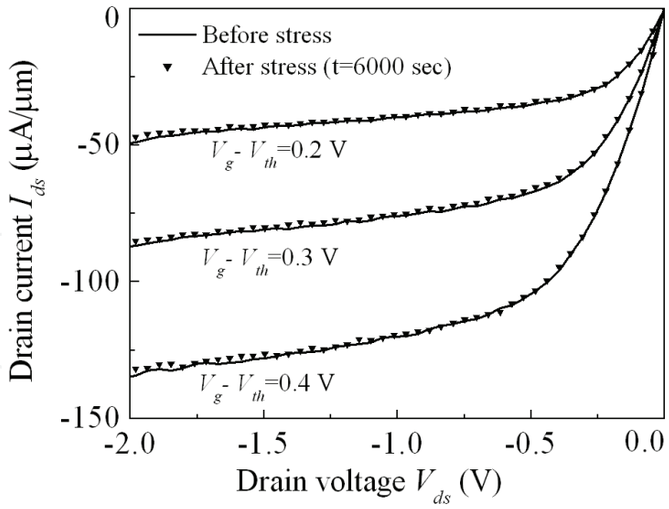

Fig. 7. Degradation of drain current under DC stress (after [b]Maiti et el., 2008).

Fig. 8 shows the threshold voltage V_{th} shift with increasing stress time. The threshold voltage V_{th} shift indicates that net positive charges exist at the gate dielectric interface as a result of hole trapping. As the lateral electric field near the drain increases in short channel devices, electron-hole pairs are generated by impact ionization. These generated holes have energies far greater than the thermal-equilibrium value and are the hot holes. In surface-channel of Ω-FinFETs, hot holes are injected into the gate oxide via hot-carrier injection (HCI), resulting in the formation of dangling silicon bonds due to the breaking of silicon-hydrogen bonds and lead to the interface traps generation (Hu et al., 1985). The charge trapping in interface states causes a shift in threshold voltage and the decrease of transconductance, which degrades the device properties over a period of time.

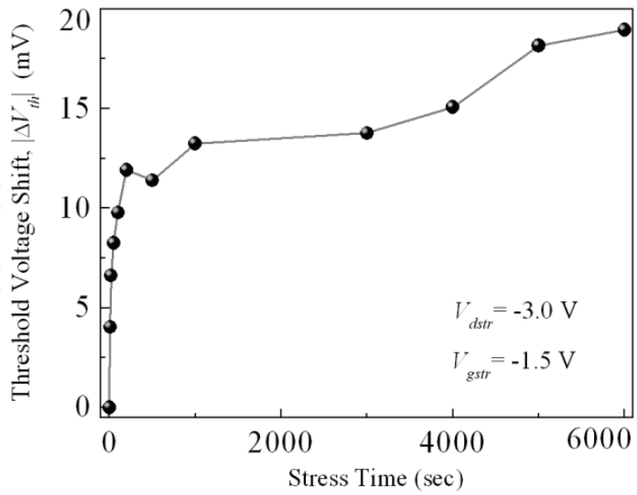

Fig. 8. Threshold voltage V_{th} shift with increasing stress time indicating an accumulation of negative charges due to electron trapping at the Si/SiO_2 interface (after [b]Maiti et el., 2008).

The hot-carrier lifetime measurements were performed and the typical I_{dsat} degradation as a function of stress time is plotted in Fig. 9. The I_{dsat} degradation is consistent with V_{th} shift.

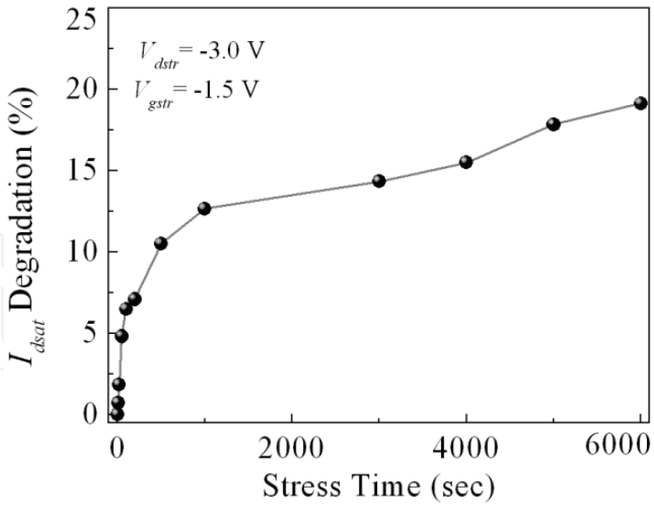

Fig. 9. I_{dsat} degradation as a function of stress time. Hot carrier lifetime in nanowire Ω-FinFETs after stressing for a given I_{sub}/I_d (after [b]Maiti et el., 2008).

4. Spice modeling of silicon nanowire FETs

In this section we will discuss the spice model of silicon nanowire FETs. This section presents the fully depleted BSIMSOI modeling of low power n- and p-MOS nanowire surrounding gate field-effect transistors (SGFETs), extraction of distributed device parasitics, and measuring the capabilities of these FETs for high-speed analog and RF applications.

4.1 Intrinsic SPICE modeling of nanowire FETs

SPICE models of n- and p-MOS SGFETs are created by fully depleted BSIMSOI parameters and are listed in Table 2. These parameters are optimized to ensure input and output I–V characteristics of 10 nm channel length and 2 nm radius SGFETs (Hamedi-Hagh & Bindal, 2008).

The distributed parasitic RC components across the intrinsic SGFET transistor are modeled for n- and p-MOS transistors, as shown in Fig. 10 and (b), respectively.

C_{gsx} is the parasitic capacitance between metal gate and the concentric source and C_{gsy} is the parasitic capacitance between metal gate and the source contact. The resistor rg accounts for the effective gate resistance at high frequencies caused by the distributed gate-oxide channel. The resistance R_g accounts for two parallel gate contacts. C_{dsx} is the parasitic capacitance between intrinsic drain and source contacts and C_{dsy} is the parasitic capacitance between drain and source interconnects. Resistors R_{sx} and R_{sy} represent source contacts and resistors R_{nw} and R_{pw} represent overall concentric n-well and p-well resistances from intrinsic source to extrinsic source contacts of n- and p-MOS SGFETs, respectively. C_{gdx} is the parasitic capacitance between gate contact and the intrinsic drain and C_{gdy} is the parasitic capacitance between gate and drain interconnects. The resistor R_d represents the drain contact of the transistor. The effective resistor r_g is given by

$$r_g = \frac{1}{12}\left(R_s \frac{2\pi R}{L}\right) \tag{10}$$

Parameters	Values
Channel Length (L)	10 nm
Channel Radius (R)	2 nm
Gate Oxide Thickness (t_{ox})	1.5 nm
Channel Doping Concentration (n_{ch})	1.5e+19 cm^{-3}
Substrate Doping Concentration (n_{sub})	1.0e+11 cm^{-3}
Threshold Voltage (V_{th0})	0.26 V (nMOS) -0.28 V (pMOS)
Mobility (U_0)	1000 $cm^2/V.s$ (nMOS) 300 $cm^2/V.s$ (pMOS)
Parasitic Resistance Per Unit Area (R_{dsw})	130Ω.µm (nMOS) 360Ω.µm (pMOS)
Saturation Velocity (V_{sat})	≈2e+06 cm/s
Subthreshold Region Offset Voltage (V_{off})	0.06 V
Channel Lenth Modulation (P_{clm})	25
Primary Output Resistance DIBL Effect (P_{diblc1})	1.02e-06
Secondary Output Resistance DIBL Effect (P_{diblc2})	1
Primary Short Channel Effect on V_{th} (D_{vt0})	3.8
Secondary Short Channel Effect on V_{th} (D_{vt1})	2.75
Short Channel Body Bias Effect on V_{th} (D_{vt2})	0 V^{-1}
Primary Narrow Width Effect on V_{th} (D_{vt0w})	0
Secondary Narrow Width Effect on V_{th} (D_{vt1w})	7.25e+07
Narrow Width Body Bias Effect on V_{th} (D_{vt2w})	0.34 V^{-1}
Subthreshold Region DIBL Coefficient (Eta_0)	0.008
Subthreshold Body Bias DIBL Effect (Eta_b)	0.174 V^{-1}
DIBL Coefficient Exponent (D_{sub})	1
Source/Drain to Channel Coupling Capacitance (C_{dsc})	1.373e-10 F/cm^2

Table 2. List of BSIMSOI model parameters of SGFETs (after Hamedi-Hagh & Bindal, 2008).

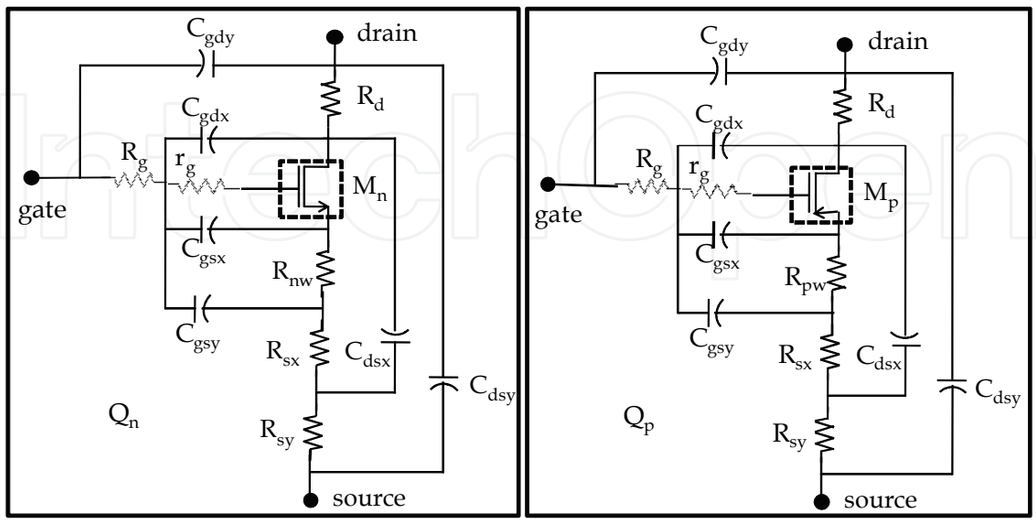

Fig. 10. Distributed parasitic components across. (a) Intrinsic n-MOS, M_n . (b) Intrinsic p-MOS, M_p , SGFETs (after Hamedi-Hagh & Bindal, 2008).

which is equal to the effective gate resistance of the planar transistors with signals applied to both ends of the gate. The distributed SGFET parasitic components are listed in Table 3(a) and (b) for resistors and capacitors, respectively.

Resistors	Values
r_g	10 Ω
R_g	110 Ω
R_{nw} (R_{pw})	2.3 (3.4) k Ω
R_{sx}	100 Ω
R_{sy}	100 Ω
R_d	70 Ω

(a)

Capaqcitors	Values
C_{gsx}	3 aF
C_{gsy}	1 aF
C_{gdx}	0.5 aF
C_{gdy}	0.8 aF
C_{dsx}	0.5 aF
C_{dsy}	0.8 aF

(b)

Table 3. List of SGFET parasitic (a) resistors (b) capacitors (after Hamedi-Hagh & Bindal, 2008).

4.2 Extrinsic SPICE modeling of nanowire FETs

S parameters are obtained by sweeping the frequency from 1 MHz to 10^3 THz and using ports with Z_0 = 1 kΩ internal resistances to ensure stability. The transistors are biased with V_{ds} = 1 V and V_{gs} = 0.5 V to yield the maximum transconductance and to ensure a high power gain. The S_{22} (output return loss) is a measure of the transistor output resistance and S_{21} (forward gain) is a measure of the transistor voltage gain. Due to similar dimensions, n- and p-MOS SGFETs have very similar parasitic components, while the g_m and rout of n- and p-MOS transistors differ from each other. Therefore, it is expected that S_{22} and S_{21} of the n- and p-MOS transistors deviate from each other, while S_{11} (input return loss) and S_{12} (reverse gain) of transistors match more closely. The two important figure of merits for RF transistors are the maximum frequency of oscillation (f_{max}) and the unity current- gain cut-off frequency (f_T). The f_{max} is obtained when the magnitude of the maximum available power gain (G_{max}) of the transistor becomes unity and f_T is obtained when the magnitude of the current gain (H_{21}) of the transistor becomes unity. The G_{max} and H_{21} of the transistor, under simultaneous conjugate impedance-matching conditions at input and output ports, are expressed in terms of S-parameters as (Hamedi-Hagh & Bindal, 2008)

$$G_{\max} = \frac{S_{21}^2}{\left(1 - S_{11}^2\right)\left(1 - S_{22}^2\right)} \tag{11}$$

and

$$H_{21} = \frac{S_{21}}{\left(1 - S_{11}\right)\left(1 + S_{22}\right) + S_{12}S_{21}} \tag{12}$$

The f_{max} and f_T of n- and p-MOS SGFETs are 120 THz, 36 THz and 100 THz, 25 THz, respectively. All SPICE results indicated the potential use of nanowire FETs in high-speed and low-power next-generation VLSI technologies.

5. Process-compact SPICE modeling of nanowire FETs

In this section, we present a simulation methodology for nanowire FinFETs which allow the flow of pertinent information between process and design engineers without the need for disclosing details of the process. Compact SPICE model parameters are obtained using parameter extraction strategy as a polynomial function of process parameter variations. As a case study, SPICE models are used to identify the impacts of process variability in inverter circuit with nanowire FinFETs.

In advanced technology nodes (< 45 nm), process variations and defects are largely dominating the ultimate yield. The sources of the process variations and defects must be identified and controlled in order to minimize the yield loss. Technology CAD (TCAD) is a powerful tool to identify such root causes for yield loss. TCAD tools are used to study device sensitivities on process variations. Currently, TCAD is heavily used in device research and process integration phases of technology development. However, a major trend in the industry is to apply TCAD tools far beyond the integration phase into manufacturing and yield optimization. In this section, linking of process parameter variations (via DoE) with the electrical parameters of a device through Process Compact Model (PCM) is also demonstrated.

Towards extended TCAD, in process modeling, generally a systematic design of experiments (DoE) run is performed. DoE experiments can be systematically set up to study the control over process parameters and arbitrary choice of device performance characteristics. The models developed from DoE are known as process compact models (PCMs) which are analogous to compact models for semiconductor devices and circuits. PCM may be used to capture the nonlinear behavior and multi-parameter interactions of manufacturing processes (Maiti et al., 2008). SPICE process compact models (SPCMs) can be considered as an extension of PCMs applied to SPICE parameters. By combining calibrated TCAD simulations with global SPICE extraction strategy, it is possible to create self consistent process-dependent compact SPICE models, with process parameter variations as explicit variables. This methodology brings manufacturing to design, so that measurable process variations can be fed into design [borges06]. To design robust circuits using strain-engineered MOSFETs, the effect of process variability on the circuit model parameters examined in detail.

5.1 Process compact models: An overview

Process compact models (PCMs) methodology consists of TCAD simulations, using the process and device models that are calibrated to silicon, and process-dependant compact SPICE model extraction (see Fig. 11). The parameter extraction is performed using the parameter extraction tool Paramos (cSynopsys, 2008), which interfaces with TCAD or experimental data and directly generates process-aware SPICE models. The process-aware SPICE models allow designers to account for process variability and to develop more robust designs.

Process compact models:

Capture the process–device relationships between the process parameters and device performance of a semiconductor manufacturing process.

1. Are robust, fast to evaluate, and can be embedded into other environments such as PCM Studio, spreadsheet applications, and yield management systems.
2. Are analogous to device compact models, which capture electrical behavior and can be derived from measurements or simulations.

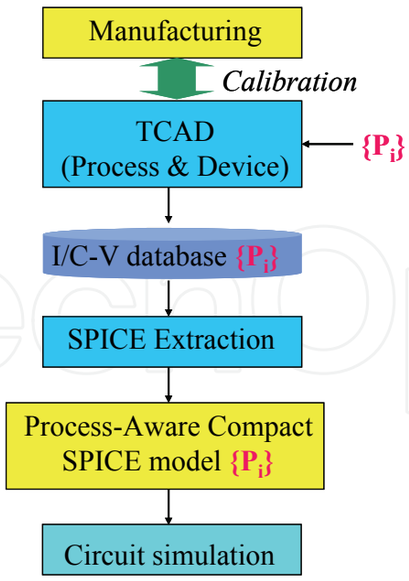

Fig. 11. Compact SPICE model extraction and validation methodology.

SPICE process compact models (SPCMs) can be considered as an extension of PCMs applied to SPICE parameters. Using a global extraction strategy, available from the Synopsys tool Paramos, pertinent compact SPICE model parameters are simultaneously obtained as a polynomial function of process parameter variations. The extraction procedure is performed using Paramos, which will deliver an XML file containing the extracted SPICE model parameters. This methodology brings manufacturing to design, so that measurable process variations can be fed into design. Additionally, design sensitivity to process can be fed back to manufacturing so that product dependent process controls can be performed. Here the chosen SPICE model parameters (Y_i) are extracted as an explicit polynomial function of normalized process parameter variations ($\tilde{P}_j$) as shown in Eqn. 13. Process parameter variations are normalized with respect to the corresponding standard deviation of the parameter as shown in Eqn. 14. Such a normalization process enables the encryption of proprietary information like the absolute values of the process parameters.

$$y_i = y_i^0 + \sum_j \sum_{n=1}^{N} a_{ij}^n \tilde{p}_j^n \tag{13}$$

Where, Y_i - Nominal value of the *i-th* model parameter, j is the *j-th* process parameter, N is the highest order of polynomial, a_{ij}^n is the process coefficient of *j-th* process parameter for the *i-th* SPICE model parameter and for order n of the polynomial, $\tilde{p}_j$ is the normalized process parameter defined as,

$$\tilde{p}_j = \frac{p_j - p_j^0}{\sigma_j} \tag{14}$$

Where, p_j is the *j-th* value of the process parameter, p_j^0 is the nominal value of the *j-th* process parameter, σ_j is the standard deviation of the *j-th* process parameter. Here we represent the BSIM4 SPICE model parameters as quadratic function of process parameters.

This model is easily scalable to higher orders of polynomial (N) for higher accuracy of extraction (Tirumala et al., 2006). Current extraction strategy of the SPICE model parameters involves extraction of nominal SPICE parameters $\left(y_0^i\right)$ followed by extraction of process coefficients $\left(a_{ij}^n\right)$ and re-optimized nominal values of SPICE parameters $\left(y_0^i\right)$.

5.2 Process-aware SPICE parameter extraction

To extract the model parameters, process and device simulations were first performed using typical CMOS process flow. The model parameters extracted are for the nominal process conditions and various drawn gate lengths. One of the SPICE parameters, namely voltage (V_{th}), as a function of process parameters has been extracted. In order to validate the compact SPICE model, for a given set of process conditions and device bias states, I-V curves obtained from TCAD simulations are compared with those obtained from Paramos using process-dependant compact SPICE model card. Fig. 12 shows the current-voltage characteristics. The dots show the TCAD simulation data, and the solid lines show the electrical characteristics generated by global SPICE model.

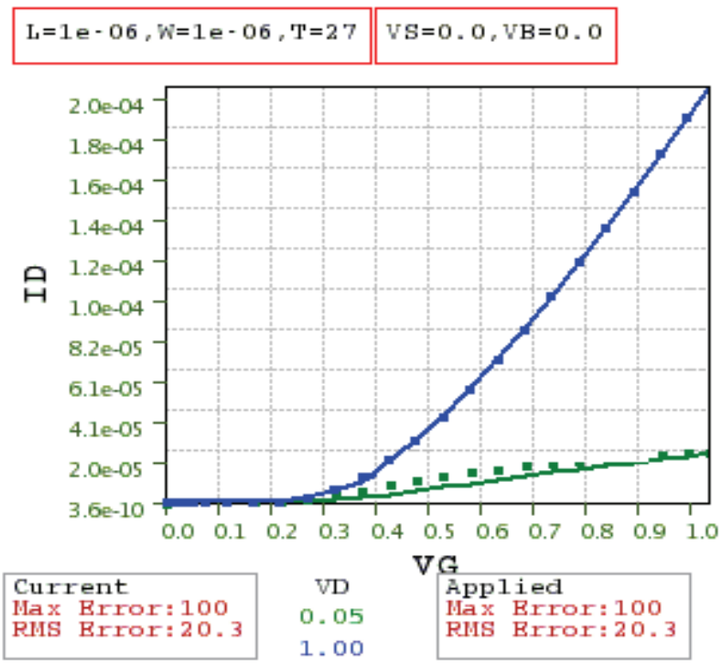

Fig. 12. Current–voltage characteristics.

As an example, SPICE model parameter of threshold voltage (V_{th}) extracted as an explicit polynomial function of normalized process parameter variations (P_i^n) as shown in Eqn. 14.

$$V_{th} = V_{th0} + \sum\sum a_i^n P_i^n \tag{15}$$

Where, V_{th0} is the nominal value of threshold voltage, i is the i^{th} value of the process parameter, a_i^n process coefficient of i^{th} process parameter for the SPICE model parameter and for order n of the polynomial, and P is the normalized process parameter. Such a normalization process (P) enables the encryption of proprietary information like the

absolute values of the process parameters. BSIMSOI SPICE model parameters as quadratic function of process parameters have been considered. This model is easily scalable to higher orders of polynomial (n) for higher accuracy of extraction. The SPICE model parameter such as threshold voltage (V_{th}) involves extraction of nominal SPICE parameters (V_{th0}) followed by extraction of process coefficients a_i^n and re-optimized nominal values of SPICE parameters (V_{th0}). Threshold voltage model for strain-engineered nMOSFETs have been obtained using first order polynomial as function of gate length (L_g) and oxide thickness (T_{ox}) as

$$V_{th} = V_{th0} + \left(L_g - \alpha_1\right).\beta_1 + \left(T_{ox} - \alpha_2\right).\beta_2$$

and corresponding threshold voltage Eqn.

$$V_{th} = 0.27 + (Lg-90)/45*0.088032 + (t_{ox}-0.055)/0.01*0.0231 \quad (16)$$

Here, spice parameters are represented as first order polynomial function of process parameter variations. Threshold voltage parameter generated by the global SPICE model, shows the maximum error is approximately 12% and the root-mean-square (RMS) error is approximately 5%. These results show that the global model can be used to predict the electrical behavior of the devices in the absence of process variability.

6. Noise in silicon nanowire Fin-FET

This section deals with the noise in silicon nanowire FinFETs (SNWFinFETs). The noise of a device is the result of the spontaneous fluctuations in current and voltage inside the device that are basically related to the discrete nature of electrical charge. Noise imposes limits on the performance of amplifiers and other electronic circuits. Si nanowire transistors (SNWTs) have also been widely studied as chemical and biochemical sensors ([a]Zhang, 2007; [b]Zhang, 2008 & Stern, 2007). Biosensing by SNWTs is based on the pronounced conductance changes induced by the depletion of charge carriers in the silicon body when the charged biomolecules are bound to its surface. The high noise level in the depletion (subthreshold) region may lead to reduced signal-to-noise ratios in these sensors (Wei, 2009). In this section Low-frequency noise (LFN) in SNWTs has been demonstrated in the subthreshold region.

6.1 Low frequency noise measurements

The standard noise measurement set-up included an E5263A 2-channel high speed source monitor unit, a SR 570 low noise amplifier (LNA) and a 3570A dynamic signal analyzer. Here, E5263A 2-channel high speed source monitor unit provided the necessary gate-source and drain-source biases as shown in Fig. 13. The minute fluctuations in the drain-source voltage were amplified to the measurable range using low amplifier. The output of the amplifier is fed to 35670A dynamic signal analyzer that performs the fast Fourier transform on the time domain signal to yield the voltage noise power spectral density (S_V) in the 1-100 kHz range after correcting for amplifier gain. In order to obtain a stable spectrum, the number of averages was set at 40 and a 90% sampling window overlap was used for optimal real time processing. A computer interface was provided to control the dynamic signal analyzer and automate the noise data collection.

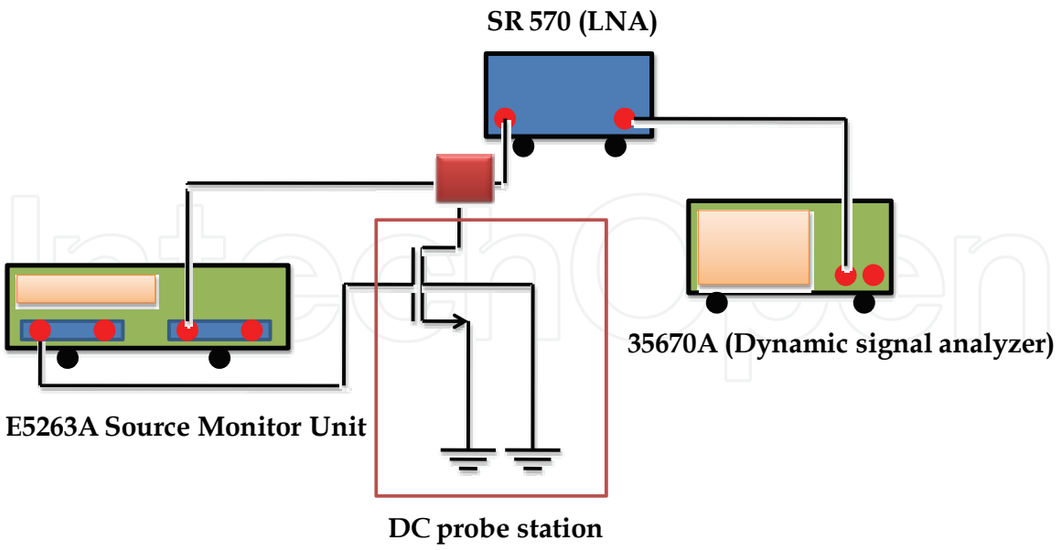

Fig. 13. Low frequency noise measurement system.

6.2 Low-frequency noise

Fig. 14 shows the frequency dependence of the measured drain-current noise spectral density S_v of 100 nm p-type SNWFinFETs, biased at V_{ds} = −50 mV at different gate bias. The S_v extracted at f = 600 Hz of each curve is shown in the inset. The dispersion of the noise spectral density is due to randomly distributed oxide traps, the lattice quality and mobility variations of the ultrascaled dimension of SNWFinFETs.

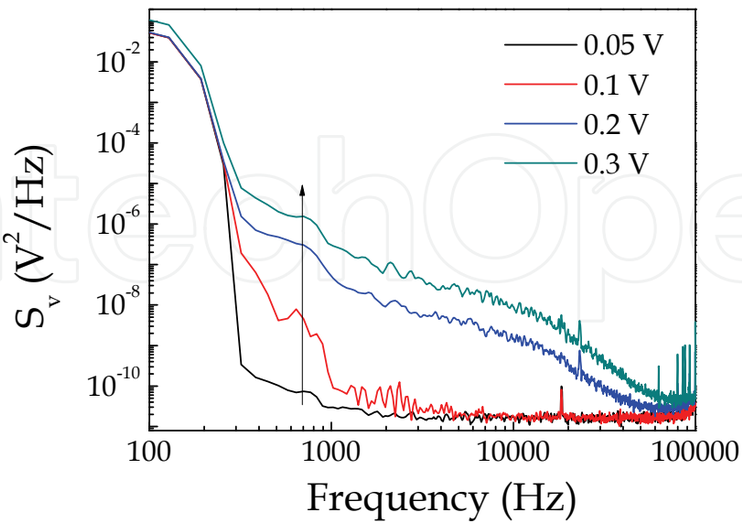

Fig. 14. Drain–current noise spectral density S_v of p-type SNWFinFETs with L = 100 nm biased at V_{ds} = −50 mV at different gate bias (V_{gs}).

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Nanowires

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This volume is intended to orient the reader in the fast developing field of semiconductor nanowires, by providing a series of self-contained monographs focusing on various nanowire-related topics. Each monograph serves as a short review of previous results in the literature and description of methods used in the field, as well as a summary of the authors recent achievements on the subject. Each report provides a brief sketch of the historical background behind, the physical and/or chemical principles underlying a specific nanowire fabrication/characterization technique, or the experimental/theoretical methods used to study a given nanowire property or device. Despite the diverse topics covered, the volume does appear as a unit. The writing is generally clear and precise, and the numerous illustrations provide an easier understanding of the phenomena described. The volume contains 20 Chapters covering altogether many (although not all) semiconductors of technological interest, starting with the IV-IV group compounds (SiC and SiGe), carrying on with the binary and ternary compounds of the III-V (GaAs, AlGaAs, GaSb, InAs, GaP, InP, and GaN) and II-VI (HgTe, HgCdTe) families, the metal oxides (CuO, ZnO, ZnCoO, tungsten oxide, and PbTiO3), and finishing with Bi (a semimetal).

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