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Advanced RF MOSFET´s for microwave and millimeter wave applications: RF characterization issues

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1. Introduction

The communication industry has always been a very challenging and profitable market for semiconductor companies. The new communication systems are today very demanding; they require high frequency, high degree of integration, multi-standards, low power consumption, and they have to present good performance under harsh environment. The integration and power consumption reduction of the digital part will further improve with the continued downscaling of technologies. The bottleneck for further advancement is the analog front-end. Present-day transceivers often consist of a three or four chip-set solution combined with several external components. A reduction of the external components is essential to obtain a lower cost, power consumption and weight, but it will lead to a fundamental change in the design of analog front-end architectures. The analog front-end requires a high performance technology, like GaAs or silicon bipolar transistors, with devices that can easily achieve operating frequencies in the GHz range. For a digital signal processor, a small device feature size is essential for the implementation of complex algorithms. Therefore, it appears that only the best submicron CMOS technology is suitable for a feasible and cost-effective integration of the communication systems.
This last decade MOS transistors have reached amazingly high operation speed and the semiconductor community has noticed the Radio Frequency possibilities of such mainstream devices. Silicon-on-Insulator (SOI) MOSFET technology has demonstrated its potentialities for high frequency reaching cutoff frequencies close to 500 GHz for nMOSFETs and for harsh environment (high temperature, radiations) commercial applications.
From its early development phase till recent years, SOI has grown from a mere scientific curiosity into a mature technology. Partially Depleted (PD) SOI is now massively serving the 45-nm digital market where it is seen as a low cost - low power alternative to bulk silicon. Fully depleted (FD) devices are also widely spread as they outperform existing semiconductor technologies for extremely low power analog applications.

In this chapter, we are going to present the current state-of-the-art of advanced MOS transistors for microwave and millimeter wave applications. The importance of an accurate RF small-signal equivalent circuit of MOSFETs to properly design RF circuits is pointed out. Based on several experimental and simulation results the RF characterization issues of such advanced field effect transistors will be detailed. Several characterization techniques to extract an accurate small-signal equivalent circuit of MOSFET will be described.

2. Historical trend

The microelectronics area has gone through great developments during these last decades. The beginning of electronics technology can be situated in the beginning of the 20th century when the vacuum triode and pentode were developed. Since then, many applications have started to appear in several fields especially in communications: the radio and TV systems were developed.

The first step on the conception of solid state electronics devices was made by Lilingfiel (Iwai & Ohmi, 2002). He theoretically proposed a device called "Device for Controlled Electric Current". This theoretical device used the electric field generated across a dielectric film in order to control the flux of electrons between two electrodes called source and drain. The control terminal was called gate. Such device was not physically built because the technological possibilities did not allow its fabrication.

Some years later the first transistor was invented in the laboratories of the Bell Telephone Co. in 1947. This was a point-contact transistor made on germanium (Shockley, 1976). In 1958, Jack Kilby developed the first integrated circuit (IC). He integrated few devices on germanium to build a phase-shift oscillator, demonstrating the feasibility to integrate several devices in a semiconductor sample (Kilby, 1976). One year later, Robert Noyce developed a new technology and in fact a new conception of the IC´s. This new technology was called "The planar technology" and was a revolutionary technology for microelectronics (Kilby, 1976).

Additionally in the 1950´s and 1960´s, many successful efforts were made looking for fabrication on reliable silicon Bipolar Junction Transistor´s (BJT´s). This promotes the growing of digital applications thanks to the called Transistor-Transistor Logic (TTL). At the same time, analog applications look for the use of BJT´s in order to replace the vacuum triodes and pentodes. In fact, the first transistor with cut-off frequencies in the order of 1 GHz was developed in 1958-1959 based on germanium (Schwierz & Liou, 2001). At that time the community established that devices for high frequencies applications needed high carrier mobility and thus the silicon and germanium technologies were replaced by the III-V semiconductor technologies. Thus, in the 1960´s different III-V based transistors with very high cut-off frequencies began to appear (Mead, 1966). In 1966, the first field-effect transistor based on GaAs was developed, this was a MESFET device which revolutionized the RF world (Schwierz & Liou, 2001).

Fig. 1 indicates the evolution of the record frequencies as a function of time (Schwierz & Liou, 2001) from the 1960´s to the end of the century. As we can see in the late 90´s the InP based transistors showed amazing cut-off frequencies near to 1 THz.

In the late 60´s, the first silicon MOS transistor (MOSFET) was developed (Kahng, 1976). Due to its low carrier mobility, the silicon transistors were not considered for very high frequency applications but mainly for digital circuits**.** The n-MOS and p-MOS logic

technologies gained the attention of the digital community and a few years later the development of the CMOS technology revolutionized the digital applications. This technology allowed the development of the first microprocessors and high density memories (Iwai & Ohmi, 2002). In 1974, R. Denard established a new procedure with two objectives in mind: (i) increase the operation velocity of the MOSFETs and (ii) the integration density of the ICs (Denard *et al*., 1974).

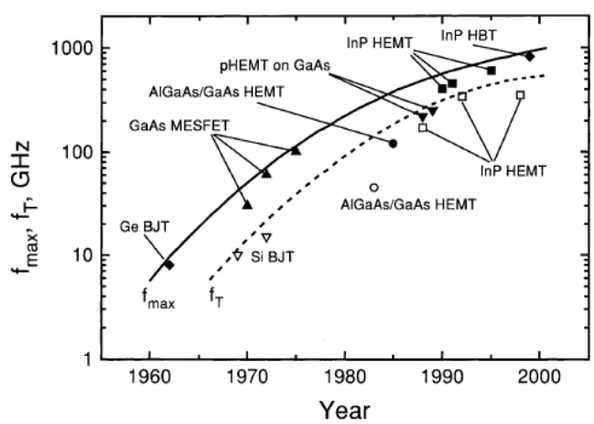


Fig. 1. Evolution of the record frequencies from 1960 to the end of the last century (Schwierz & Liou, 2001).

The downscaling of the MOSFET dimensions is the major way to reach both objectives. This has been the gold rule of microelectronics in the last three decades (Iwai, 2009). Thanks to downscaling, the digital electronics evolved enormously, in fact the integration density passed from hundreds of devices to millions of devices in the same silicon area and the microprocessors clock frequencies increased from a few MHz to the GHz range, through the fabrication of MOSFETs with channel lengths from 10 μm to the current transistors with 65 nm (Iwai, 2009). Fig. 2 shows the evolution of the CMOS technology in the last decades (Iwai, 2009).

3. Development of high frequency MOSFET´s

As established before, the MOS technology evolved enormously in the last decades allowing the development of very high performance circuits for digital applications. This evolution has been guided by the downscaling procedure (Iwai & Ohmi, 2002). Thanks to this, the channel length of the MOSFETs has been shrunk from 10 μm down to 65 nm.
In recent years the RF community started to notice the potentialities of those devices and many efforts started to appear in order to optimize the RF performance of the MOSFETs. Due to the channel length reduction, the cut-off frequencies of the MOSFETs have grown enormously in such way that deep-submicron devices start to present values higher than 400 GHz (Schwierz & Liou, 2007).
Since then, many efforts began to look for the optimization of the MOSFETs for very high frequencies operation. Thanks to those researches, it was found that very important facts limiting the high performance at very high frequency are the series extrinsic resistances,

especially the gate resistance (Schwierz & Liou, 2007). Fig. 3 shows the evolution cut-off frequencies (f_t and f_{max}) from the early 90´s to the present (Schwierz & Liou, 2007).

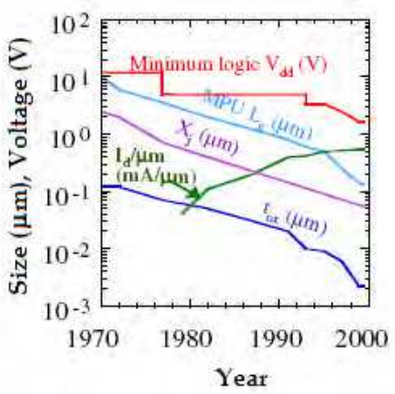


Fig. 2. Evolution of the main MOSFET parameters, gate length (L_g), junction depth (X_j), oxide thickness (t_{ox}), normalized drain current ($I_d/\mu m$) and minimum logic voltage (V_{dd}) in the CMOS technology (Iwai, 2009).

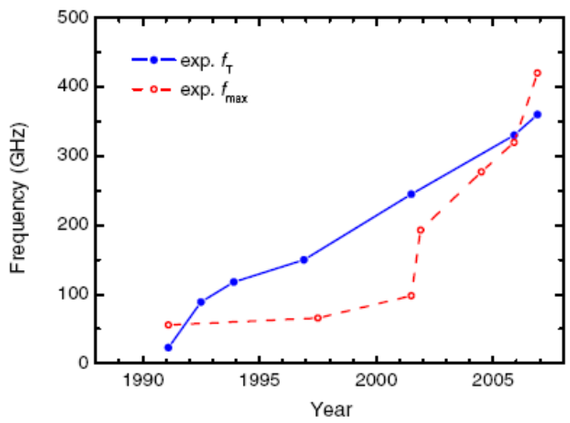


Fig. 3. Cut-off frequencies of MOSFETs, from early 90´s to the present time (Schwierz & Liou, 2007).

As we can see in Fig. 3, the high frequency performance has recently grown amazingly and the current MOS transistors can present record frequencies higher than 460 GHz.
Since the cut-off frequencies are inversely proportional to the channel length, cut-off frequencies as high as 1 THz can be expected for gate length in the order of 10 nm (Schwierz & Liou, 2007) as presented in Fig. 4.

3.1 Toward the Terahertz transistor

The standard MOS transistor is fabricated over a silicon substrate, however as the channel length is shrunk beyond 100 nm, some electrical degradations start to appear. Those effects include the loss of the gate electrostatic control on the carrier flow along the channel and they are called short channel effects, SCE (Colinge, 1991).

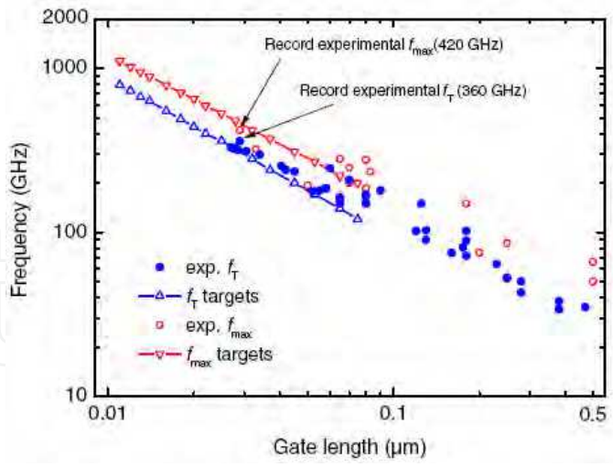


Fig. 4. Dependence of the cut-off frequencies of MOSFETs as a function of the channel length (Schwierz & Liou, 2007).

In order to keep a good electrostatic control of the channel by the gate and thus reduce the short-channel effects, Silicon-on-Insulator technology appears as a solution of great interest. Additionally, thanks to the buried oxide (BOX) underneath the transistor area, the source and drain capacitances to the silicon substrate are strongly reduced. The decrease of the capacitive coupling between the active silicon area of the transistor and the substrate contributes to the reduction of the parasitic capacitances and then the improvement of the high frequency capabilities of MOSFETs.

To reduce the SCE in nanometer scale MOSFETs, multiple-gate architectures (MuGFET) emerge as one of the most promising novel device structures, thanks to the simultaneous control of the channel by more than one gate. The idea of the double-gate (DG) MOSFET was first experimentally proven by J.-P. Colinge in 1990 (Colinge, 1990). Starting by the FinFET (Hisamoto *et al.*, 2000), other types of multiple-gate SOI MOSFETs have been introduced these last years (Cristoloveanu, 2001), (Tao Chuan Lim, 2009).

Additionally, new technologies like strained-silicon MOSFETs (s-Si MOSFETs) (Thompson, 2005) or Schottky barrier MOSFETs (SB MOSFETs) (Valentin *et al.*, 2008) appear as very interesting alternatives to replace the conventional bulk-technology and also promising devices for the TeraHertz era.

Theoretical analyses have proven that double-gate transistors (DG-MOSFETs) can reach cut-off frequencies as high as a few THz as shown in Fig. 5.

Some challenges must be solved in order to reach these projections. From a technological point of view, many efforts must be done to fabricate reproducible and feasible devices with channel length lower than 20 nm and engineers must figure out how to reduce as much as possible the access resistances and capacitances to the active useful area of the tiny transistor. Additionally, adequate modelling and characterization techniques are quite necessary to accurately simulate the device behaviour.

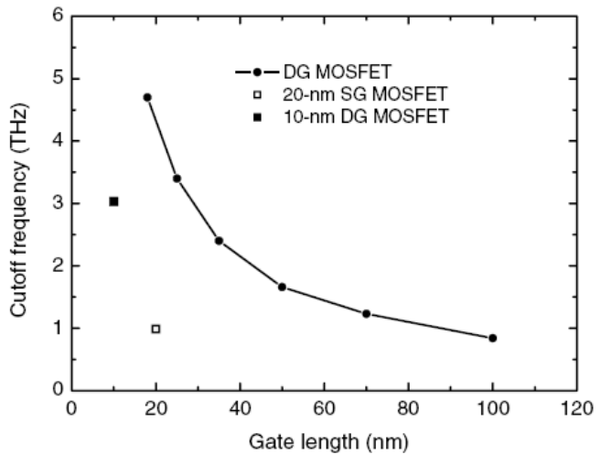


Fig. 5. Dependence of the cut-off frequencies of MOSFETs as a function of the channel length for DG-MOSFETs (Schwierz & Liou, 2007).

4. RF Modelling and characterization

The modelling and characterization of MOS transistors at very high frequencies is of first importance and is made by the measurement of the scattering (*S*-) parameters. In general, there are two kinds of models: Polynomial and Physical-based small-signal models.

- Polynomial models: Those models describe the behaviour of the MOSFET as black boxes and usually require mathematical optimization routines. They are relatively easy to obtain but they do not give information about the physical nature of the transistors.
- Physical-based small-signal models: These models describe the behaviour of the MOSFET as equivalent electrical lumped circuits. The elements have a physically based origin but they are not easy to extract from the measurements.

The knowledge of the physically based small-signal equivalent circuit is very important because they are useful to determine circuit design methodologies or the influence of each parameter on the dynamic performance. In the following sections, a general equivalent circuit of MOS Transistor is presented.

4.1 Useful effect

The useful effect of a MOSFET is the modulation of the current (labelled as I_{ds}) flowing through the channel from the source terminal (S) to the drain terminal (D), by a control of the voltage applied on the gate terminal (G). Electrically this behaviour can be represented by a current controlled source connected between S and D terminals, while the control voltage is applied between the G and S terminals (V_{gs}). The current source is defined by the intrinsic transconductance (g_{mi}). Fig. 6 represents the equivalent circuit of the MOSFET considering only the useful effect.

The intrinsic transconductance can be mathematically expressed as:

$$g_{mi} = \left.\frac{\partial i_{ds}}{\partial v_{gs}}\right|_{v_{ds}=const} \tag{1}$$

4.2 Quasi-static model

The quasi-static regime is defined when an applied small signal varies sufficiently slowly that the carriers inside the transistor can follow it instantaneously. Additionally in the MOSFET, there are some influences from one terminal to the others. In such way that a small increment of the voltage applied on one terminal will produce a variation of the charge associated to the others. Fig. 7 shows the reduced scheme of the MOSFET when it is DC biased and an additional small signal is added to the gate terminal with a value δV_g. Such a voltage increment produces an increase of the channel charge represented by δQ. This charge increment is associated to both source and drain terminals noted as δQ_s and δQ_d, respectively.

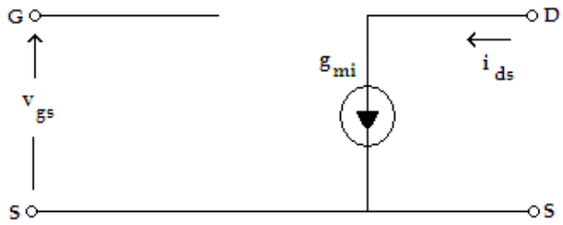


Fig. 6. Equivalent circuit for the useful effect of a MOSFET.

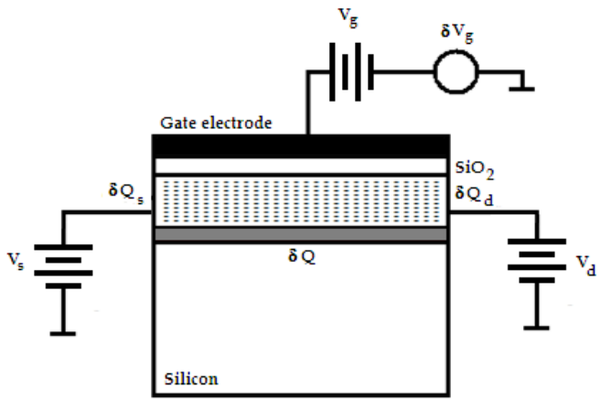


Fig. 7. Reduced scheme of a MOSFET showing the channel effect produced by a small increment of voltage applied on the gate terminal.

Those effects can be included in the equivalent small-signal model as capacitances due to the charge increment related to a voltage change. The capacitances between the source, drain and gate are defined by:

$$C_{gdi} = -\left.\frac{\partial q_g}{\partial v_d}\right|_{v_{gs}=const} \quad C_{dgi} = -\left.\frac{\partial q_d}{\partial v_g}\right|_{v_{gs}=const} \tag{2}$$

$$C_{gsi} = -\left.\frac{\partial q_g}{\partial v_s}\right|_{v_{gd}=const} \qquad C_{sgi} = -\left.\frac{\partial q_s}{\partial v_g}\right|_{v_{gd}=const}$$

$$C_{dsi} = -\left.\frac{\partial q_d}{\partial v_s}\right|_{v_{gs}=const} \qquad C_{sdi} = -\left.\frac{\partial q_s}{\partial v_d}\right|_{v_{gs}=const}$$

It is interesting to note that in general those capacitances are not reciprocal. For instance, if we consider a MOSFET biased in saturation, an increment on the drain voltage will not produce any change on the gate terminal, because of the pinch-off condition (Colinge, 1991) and thus $C_{gdi} = 0$. On the other hand, a small change on the gate voltage will produce a variation on the channel charge density and a drain current change which will lead to an associated drain charge change and therefore $C_{dgi} \neq 0$. Thus, under this condition we have $C_{gdi} \neq C_{dgi}$. This non-reciprocal effect can be modelled by adding an imaginary part to the transconductance called transcapacitance (C_{mi}). Thus, the transadmitance (Y_{mi}) is defined as:

$$Y_{mi} = g_{mi} - j\omega C_{mi} \tag{3}$$

Usually, the transcapacitance can be neglected for relatively low frequencies, however for very high frequencies it must be considered in order to accurately describe the MOSFET behaviour.
Additionally, the transistor acts as a real current source and thus it has a specific output conductance, defined by:

$$g_{di} = \left.\frac{\partial i_{ds}}{\partial v_{ds}}\right|_{v_{gs}=const} \tag{4}$$

Finally, the equivalent small-signal circuit will be modified as presented in Fig. 8, where all the parameters are bias dependent as equations (1-4) clearly indicate.

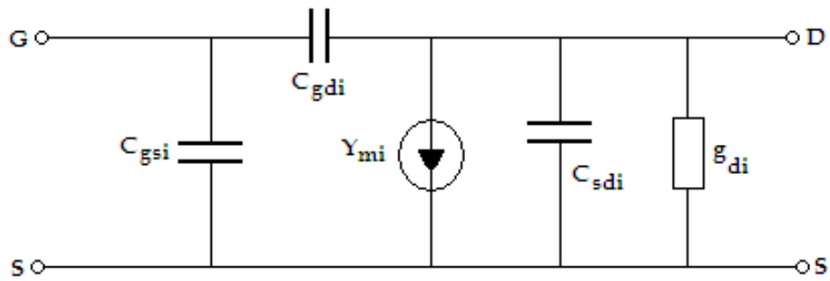


Fig. 8. Equivalent circuit of the quasi-static model of a MOSFET.

4.3 Non-Quasi-static model

As the operation frequency of the MOSFET increases, there will be a moment when the small-signal applied varies so fast that the charges inside the device cannot follow it anymore. In other words, at very high frequencies the charges will show inertial

phenomena, producing a delay between the applied signal (stimulus) and the charge redistribution in the channel (response). This delay cannot be modelled simply by the use of a capacitance effect.
The above phenomenon will be observed if the frequency exceeds the upper limit of validity of the quasi-static model presented in the previous section. Tsividis established this limit as proportional of $1/L^2$, where L is the transistor channel length (Tsividis, 1987).
One way to model the transistor under the non-quasi-static regime is to split the transistor into several small sections as Fig. 9 shows. The length of each section is chosen in such manner that the quasi-static model is valid in each section. The combination of the models for all sections will be valid for the whole device at the frequency of interest.

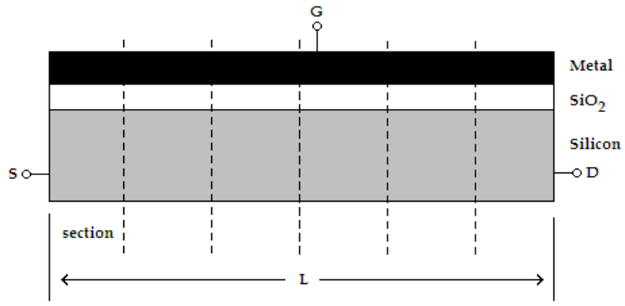


Fig. 9. MOS transistor split up in several sections along its channel.

However, this procedure is difficult to use due to the complexity of the analysis of several combined equivalent circuits and because if we change the frequency of analysis it is necessary to redefine the device subdivision. Another way to analyze the non-quasi-static regime is by the introduction of new elements in the equivalent circuit. The delay along the channel can be represented by the use of intrinsic series resistances connected between the gate and the drain (R_{gdi}) and between the gate and the source (R_{gsi}). Furthermore, the delay from the moment where the signal is applied to the gate and the moment at which the effect is transferred to the channel can be modelled by a complex transconductance, as represented in Fig. 10.

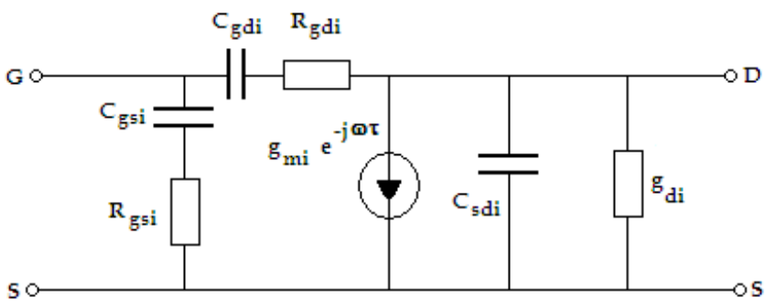


Fig. 10. Small-signal equivalent circuit of MOSFET under non-quasi-static condition.

This equivalent circuit can be represented by the admittance (Y-) matrix given by:

$$Y_{\pi i} = \begin{bmatrix} j\omega\left(\frac{C_{gsi}}{1+j\omega R_{gsi}C_{gsi}} + \frac{C_{gdi}}{1+j\omega R_{gdi}C_{gdi}}\right) & -j\omega\left(\frac{C_{gdi}}{1+j\omega R_{gdi}C_{gdi}}\right) \\ \frac{g_{mi}\cdot e^{-j\omega\tau}}{1+j\omega R_{gsi}C_{gsi}} - j\omega\left(\frac{C_{gdi}}{1+j\omega R_{gdi}C_{gdi}}\right) & g_{di} + j\omega\left(C_{sdi} + \frac{C_{gdi}}{1+j\omega R_{gdi}C_{gdi}}\right) \end{bmatrix} \quad (5)$$

4.4 Extrinsic model

In previous sections we established the equivalent circuit model under quasi-static and non-quasi-static regimes. Those models take into account only the intrinsic part of the transistor which is bias and geometry dependent. However, the structure of the MOSFET itself is surrounded by some parasitic effects originating mainly from the contacts and interconnections that must be considered in order to accurately describe its overall behaviour. Such parasitic extrinsic elements are in general bias independent.

4.4.1 Extrinsic capacitances

Various extrinsic capacitances are associated to the physical structure of the transistor, as shown in Fig. 11. The extrinsic capacitances are associated to the gate, drain and source terminals. The gate-drain (C_{gde}) and gate-source (C_{gse}) capacitances originate from the parallel combination of: (i) the overlap regions due to the diffusion of source and drain doping atoms underneath the thin gate oxide and (ii) the fringing electric field from the gate electrode to the source and drain regions. The drain-to-source capacitance (C_{dse}) corresponds to a proximity capacitance due to the coupling effects through the substrate.

The *Y*-matrix of the small-signal equivalent circuit presented in Fig. 12 is defined as:

$$Y_{\pi} = Y_{\pi i} + Y_e \quad (6)$$

$$\text{Where } Y_e = \begin{bmatrix} j\omega\left(C_{gse} + C_{gde}\right) & -j\omega C_{gde} \\ -j\omega C_{gde} & j\omega\left(C_{dse} + C_{gde}\right) \end{bmatrix}$$

4.4.2 Extrinsic resistances and inductances

The doped source and drain semiconductor regions are characterized by a certain resistivity which, due to the geometry, will relate to access resistance values. Additionally, the transistor must be connected to the external world using metal lines. Those interconnection lines also introduce some series resistances with the intrinsic channel of the transistor. Finally, the contact between the metal lines and the doped semiconductor regions is characterized by a contact resistance which also contributes to the total parasitic resistances. Fig. 13 represents a top view of the transistor with the distributed extrinsic resistances.

Due to the interconnection lines the transistor structure might present some inductive effect at each electrode. Fig. 14 presents the small-signal equivalent circuit of the MOSFET including the all the intrinsic and extrinsic lumped elements. It is worth noting that due to the small size of the advanced MOSFETs the series extrinsic inductances are very small and can even be neglected for optimized layout.

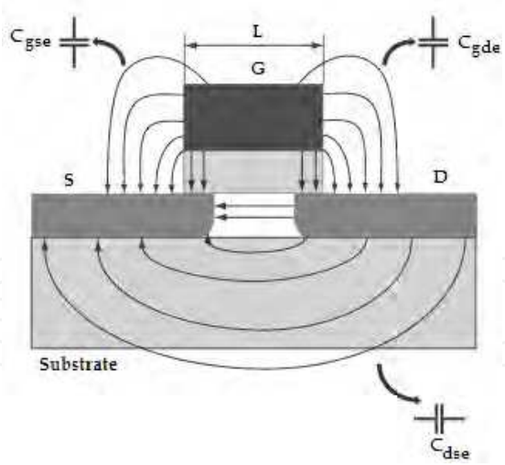


Fig. 11. Extrinsic capacitances associated to the physical structure of the MOS transistor.

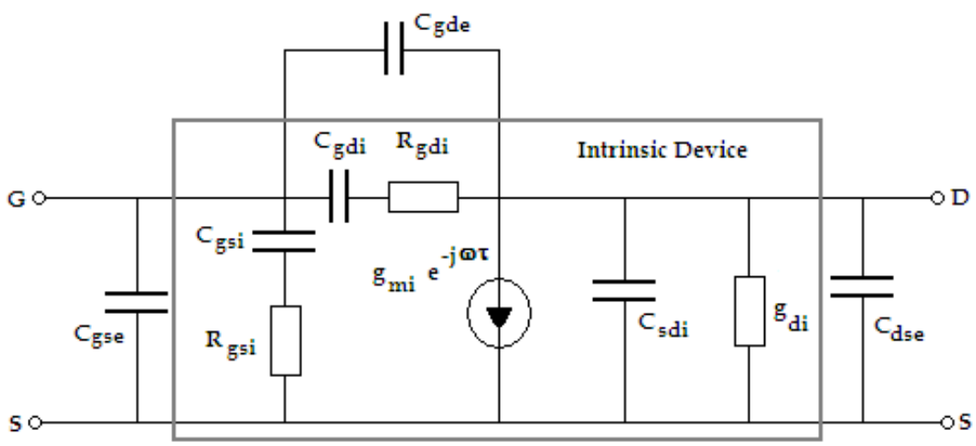


Fig. 12. Non-quasi-static intrinsic model including the extrinsic capacitances.

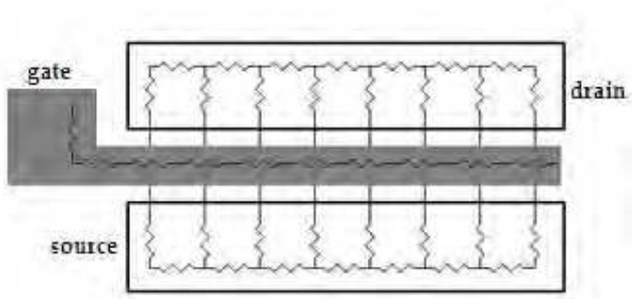


Fig. 13. Extrinsic series resistances distributed in the physical transistor structure.

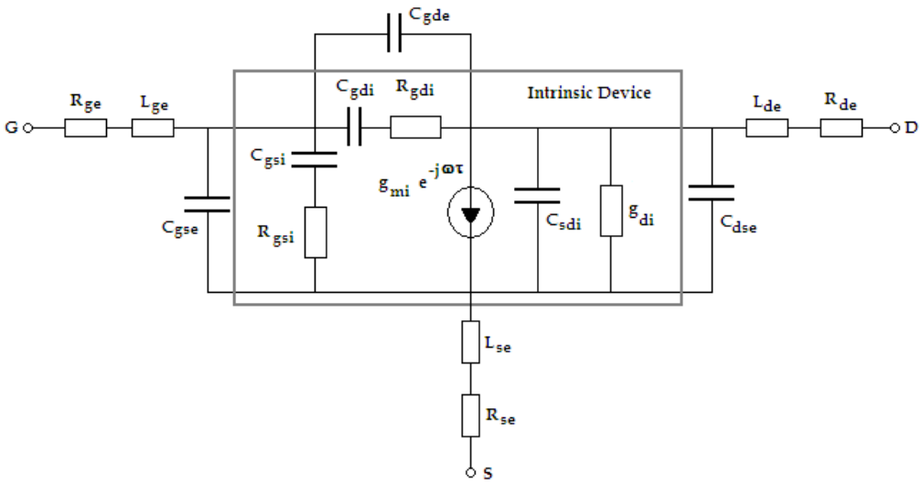


Fig. 14. Non-quasi-static small-signal equivalent circuit for a MOSFET including all intrinsic and extrinsic lumped elements.

The impedance (Z-) matrix of the whole circuit presented in Fig. 14 can be mathematically represented by:

$$Z_{\Sigma} = Y_{\pi}^{-1} + Z_e \tag{7}$$

$$\text{Where: } Z_e = \begin{bmatrix} (R_{ge} + R_{se}) + j\omega(L_{ge} + L_{se}) & R_{se} + j\omega L_{se} \\ R_{se} + j\omega L_{se} & (R_{de} + R_{se}) + j\omega(L_{de} + L_{se}) \end{bmatrix}$$

4.5 Access parameters

In order to characterize the MOSFET over a wide frequency band, it must be embedded into planar transmission lines and the most common ones are the coplanar-waveguide (CPW) presented in Figure 15. Those feed lines will of course introduce some additional series and parallel lumped elements at the input and output of the transistor under test.

Several procedures called de-embedding techniques are proposed in the literature (Cho & Burk, 1991) to withdraw those lumped elements related to the CPW structure. However, in the real scheme the de-embedding is not perfect and thus some access parasitic elements still remain at the input and output of the device.

For this reason the remaining parasitic access elements (Z_{ga}, Z_{da}, Y_{ga}, Y_{da}, Y_{gda}) must be included in the equivalent circuit model as presented in Fig. 16.

The mathematical representation of the complete small-signal equivalent circuit presented in Fig. 16, needs two steps, first it is necessary to add the access impedances to the Z_{Σ} matrix and second the access admittances must be added. Thus we have:

$$Z_{\sigma} = Z_{\Sigma} + Z_a \tag{8}$$

$$\text{Where } Z_{\alpha} = \begin{bmatrix} Z_{ga} & 0 \\ 0 & Z_{da} \end{bmatrix}$$

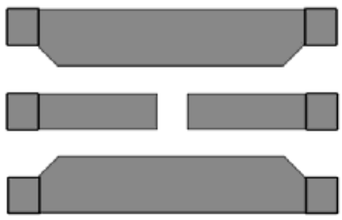


Fig. 15. Coplanar-waveguide structure.

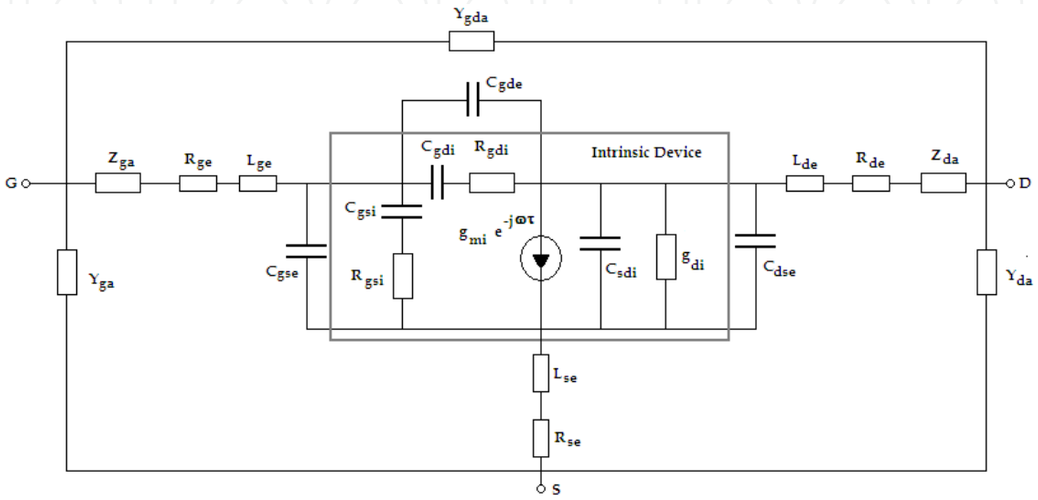


Fig. 16. Complete small-signal equivalent circuit of a MOSFET embedded in a CPW structure.

And finally:

$$Y_\mu = Z_\sigma^{-1} + Y_a \tag{9}$$

$$\text{Where } Y_\alpha = \begin{bmatrix} Y_{ga} + Y_{gda} & -Y_{gda} \\ -Y_{gda} & Y_{da} + Y_{gda} \end{bmatrix}$$

Thus, Y_μ matrix represents the admittance parameters of the whole equivalent circuit of the MOS transistor. At the present time, the technology facilities are robust enough that the test structures used for the de-embedding procedures can adequately remove the access parasitic elements. Thus, for well optimized advanced transistors and de-embedding structures (open, short, lines, load), the access elements can be well withdrawn from the measured device under test.

5. Small-signal extraction procedure

As we mentioned above, the current technology is able to produce test structures to properly de-embed access lines. Thus, the extraction of the elements forming the equivalent circuit of the MOSFET as presented in Fig. 14 proceeds as follows:

- First, the extrinsic resistances and inductances are extracted and the matrix Z_e is constructed;
- Secondly, the Y_π^{-1} matrix is de-embedded from equation (9);
- Thirdly, the extrinsic capacitances are extracted and the matrix Y_e is defined;
- Finally, the matrix $Y_{\pi i}$ is de-embedded from equation (8) and the intrinsic parameters are determined.

In general, the philosophy of the RF extraction methods is to bias the MOSFET under specific bias conditions in order to reduce the complexity of the equivalent circuit and thus obtain the direct extraction of the elements of the equivalent circuit.

5.1 Extraction of the series extrinsic resistances and inductances

There are several methods to extract the series extrinsic resistances. In general, they can be divided in two groups: (i) the methods which rely on DC measurements, and (ii) the methods that require RF measurements.

The RF methods allow determining independently the three series resistances R_{se}, R_{de} and R_{ge}. The most widely used RF methods to extract the extrinsic series resistances have been proposed in the literature by (Lovelace *et al*., 1994), (Torres-Torres *et al*., 2003), (Raskin *et al*., 1998) and (Bracale *et al*., 2000).

It is worth to mention that some of those RF methods require the extraction of intermediate parameters before the series resistances extraction (Pascht *et al*., 2002) and other methods require complex mathematical optimization routines (Lee *et al*., 1997). Such characteristics make them more sensitive to measurement noise and difficult to apply. For that reason, we are going to focus on the previously mentioned methods which are briefly described here below.

5.1.1 Lovelace´s method

For this method the MOSFET is biased in depletion and under the quasi-static regime, i.e. with $V_{gs} << V_T$ and V_{ds} = 0 V. Under these bias conditions the intrinsic lumped elements vanish (Lovelace *et al*., 1994). Thus, the transistor can be represented by the simplified equivalent circuit shown in Fig. 17.

From the above equivalent circuit, the real parts of the impedance relationships can be written as:

$$\begin{aligned} \mathrm{Re}(Z_{11} - Z_{12}) &= R_{ge} \\ \mathrm{Re}(Z_{12}) = \mathrm{Re}(Z_{21}) &= R_{se} \\ \mathrm{Re}(Z_{22} - Z_{12}) &= R_{de} \end{aligned} \tag{10}$$

Thus, the series extrinsic resistances can be extracted at very high frequency from a plot of the corresponding real part of the impedance relationship as a function of the frequency.

On the other hand, the imaginary part of the impedances follows the next relations:

$$\begin{aligned} \omega\,\mathrm{Im}(Z_{11} - Z_{12}) &= \omega^2 L_{ge} + C_A \\ \omega\,\mathrm{Im}(Z_{12}) = \omega\,\mathrm{Im}(Z_{21}) &= \omega^2 L_{se} + C_B \end{aligned} \tag{11}$$

$$\omega \mathrm{Im}(Z_{22} - Z_{12}) = \omega^2 L_{de} + C_C$$

Where C_A, C_B and C_C are values dependent on the extrinsic capacitances C_{gse}, C_{gde} and C_{dse}. Thus, a plot of the corresponding imaginary part of the impedance relationship multiplied by ω *vs*. the second power of ω gives a linear function where the slope of such a plot corresponds to the respective series inductance.

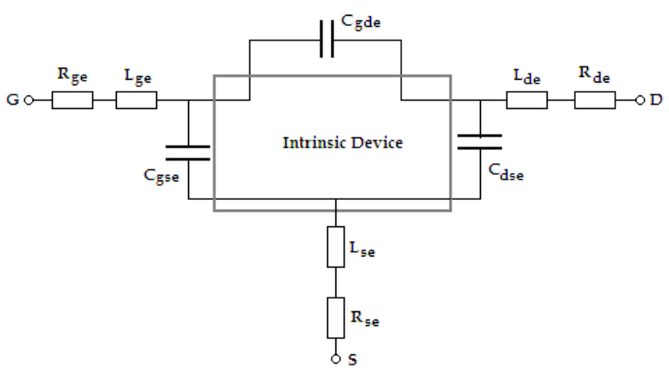


Fig. 17. Small-signal equivalent circuit under depletion regime: V_{gs} << V_T and V_{ds} = 0 V.

5.1.2 Torres-Torres´ method

For this method the MOSFET is biased in inversion and under quasi-static regime, i.e. with V_{gs} > V_T and V_{ds} = 0 V. Under these bias conditions the intrinsic transconductance (g_{mi}) vanishes. Additionally, the authors neglect the effect of the extrinsic series inductances, for that reason the equivalent circuit is simplified as presented in Fig. 18.

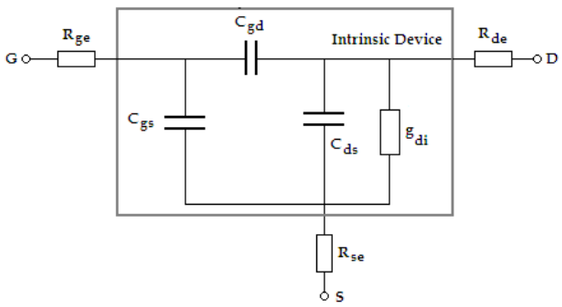


Fig. 18. Small-signal equivalent circuit under inversion regime: V_{ds} = 0 V and V_{gs} > V_T with C_{gs} = C_{gsi} + C_{gse}, C_{gd} = C_{gdi} + C_{gde} and C_{ds} = C_{sdi} + C_{dse}.

Under these bias conditions, the authors establish that the real parts of the impedances follow the following relationships (Torres-Torres *et al.*, 2003):

$$\begin{aligned} \mathrm{Re}(Z_{11}) &= R_{ge} + R_{se} + A/2 \\ \mathrm{Re}(Z_{12}) &= R_{se} + A/2 \\ \mathrm{Re}(Z_{22}) &= R_{de} + R_{se} + A \end{aligned} \tag{12}$$

where $A = \frac{R_{ch}}{1+\omega^2 C_x R_{ch}^2}$, $C_x = C_{ds} + \frac{C_{gs}C_{gd}}{C_{gs}+C_{gd}}$ and $R_{ch} = \frac{1}{g_{di}}$

In order to determine the extrinsic series resistances it is necessary to know the values of R_{ch} and C_x. From the imaginary part of Z_{22} we have:

$$-\frac{\omega}{\mathrm{Im}(Z_{22})} = C_x\omega^2 + \frac{1}{C_x R_{ch}^2} \tag{13}$$

Thus, a plot of $-(\omega/Im(Z_{22}))$ gives a linear function respect to ω^2 where the slope corresponds to C_x and the intercept corresponds to $1/C_xR_{ch}^2$. Once those values are determined, the extrinsic series resistances can be obtained from equation (12).

5.1.3 Raskin´s method

This technique biases the MOSFET in saturation or at the bias point of interest, with $V_{gs} > V_T$ and $V_{ds} > V_{gs} - V_T$ and under quasi-static regime. Under this condition, the device is asymmetric and its equivalent circuit is as shown in Fig. 19.

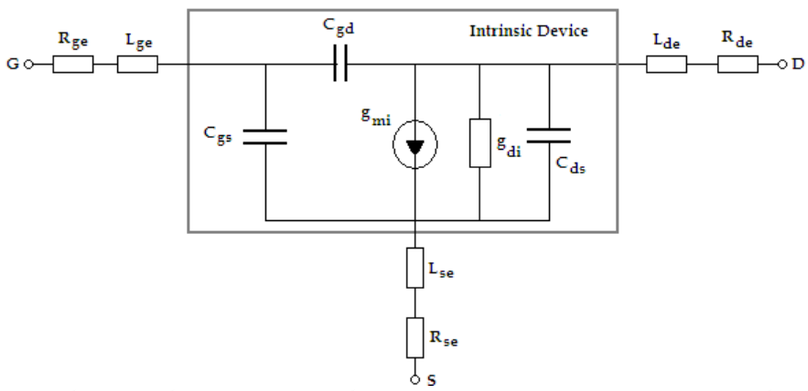


Fig. 19. Small-signal equivalent circuit under saturation regime: $V_{gs} > V_T$ and $V_{ds} > V_{gs} - V_T$.

The real parts of *Z*-parameters can be expressed as (Raskin *et al.*, 1998):

$$\mathrm{Re}(Z_{12}) = R_{se} + \frac{A_s}{\omega^2 + B} \tag{14}$$

$$\mathrm{Re}(Z_{22} - Z_{12}) = R_{de} + \frac{A_d}{\omega^2 + B}$$

$$\mathrm{Re}(Z_{11} - Z_{12}) = R_{ge} + \frac{A_g}{\omega^2 + B}$$

Thus, the extrinsic series resistances R_{ge}, R_{se} and R_{de} are obtained, respectively, by using the parametric plots of the forms $\{\mathrm{Re}[Z_{\sigma\pi 11}(\omega)], \mathrm{Re}[Z_{\sigma\pi 21}(\omega)]\}$, $\{\mathrm{Re}[Z_{\sigma\pi 12}(\omega)], \mathrm{Re}[Z_{\sigma\pi 21}(\omega)]\}$ and $\{\mathrm{Re}[Z_{\sigma\pi 22}(\omega)], \mathrm{Re}[Z_{\sigma\pi 12}(\omega)]\}$.

5.1.4 Bracale´s method

For this method the MOSFET is biased in inversion and under quasi-static regime, i.e. with V_{gs} > V_T and V_{ds} = 0 V. Under these bias conditions the intrinsic transconductance (g_{mi}) vanishes. Also, since V_{ds} = 0 V the device becomes symmetric which implies C_{gs} = C_{gd} = C. Thus, the equivalent circuit is simplified as shown in Fig. 20.

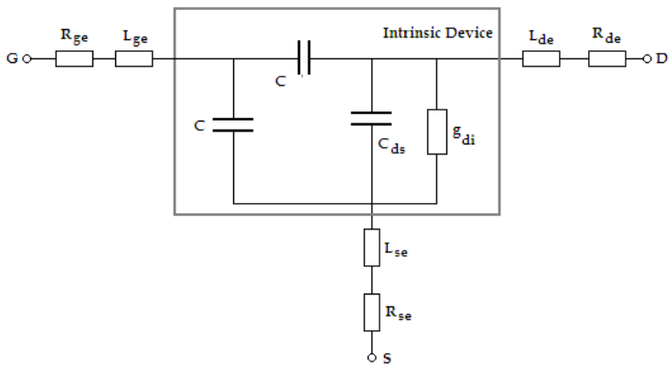


Fig. 20. Small-signal equivalent circuit under inversion regime: V_{gs} > V_T and V_{ds} = 0 V.

Considering that $C + 2CC_{ds} << 2g_{di}/\omega$ and a constant mobility (Bracale *et al.*, 2000) for each applied V_{gs}, the real parts of *Z*-parameters are related to the equivalent circuit elements as:

$$\begin{aligned} \mathrm{Re}(Z_{22} - Z_{12}) &= R_{de} + \frac{1}{2K(V_{gs} - V_T)} \\ \mathrm{Re}(Z_{12}) &= R_{se} + \frac{1}{2K(V_{gs} - V_T)} \\ \mathrm{Re}(Z_{11} - Z_{12}) &= R_{ge} + \frac{1}{4K(V_{gs} - V_T)} \end{aligned} \tag{15}$$

Where $K = \mu(W/L)C_{ox}$, μ and C_{ox} are, respectively, the carrier mobility and the normalized gate oxide capacitance, and W, L, the width and length of the MOS transistor channel, respectively.

Finally, the series resistances are determined by the intercept of a plot representing the real parts of the *Z*-parameters *vs.* the inverse of the gate overdrive ($1/(V_{gs} - V_T)$).

On the other hand, the imaginary parts of the Z-parameters are given by:

$$\mathrm{Im}(Z_{22} - Z_{12}) = L_{de} + \frac{C + 2C_{ds}}{4K^2} \frac{1}{(V_{gs} - V_T)^2}$$

$$\mathrm{Im}(Z_{12}) = L_{se} + \frac{C + 2C_{ds}}{4K^2}\frac{1}{(V_{gs} - V_T)^2} \tag{16}$$

$$\mathrm{Im}(Z_{11} - Z_{12}) = L_{ge} + \frac{C_{ds}(C + 2C_{ds})}{4CK^2}\frac{1}{(V_{gs} - V_T)^2} - \frac{1}{2C\omega^2}$$

Thus, L_{de} and L_{se} are obtained by the intercept of a plot of the corresponding Z-parameter imaginary part *vs.* $(1/(V_{gs} - V_T))^2$. For the case of L_{ge}, two steps are needed: (i) a linear regression of $Im(Z_{11}\text{-}Z_{12})$ *vs.* ω^2 is required for different V_{gs} values and (ii) a new linear regression of each intercept of the step (i) *vs.* $(1/(V_{gs} - V_T))^2$. The intercept of the second step will give the corresponding L_{ge} value.

5.1.5 Tinoco´s method

Recently, we showed that the Lovelace, Torres-Torres and Raskin´s methods are quite sensitive to *S*-parameters measurement noise, for that reason a small noise signal mixed with the scattering parameters will disturb the extraction procedure enough to reduce the accuracy on the extracted lumped parameters (Tinoco & Raskin, 2008). On the other hand, the Bracale´s method is more robust in terms of noise, however it cannot accurately extract the resistance values. Thus, we established a new extraction procedure of the extrinsic series resistances based on the Bracale´s method (Tinoco & Raskin, 2009) but considering that the carrier mobility varies with Vgs and that the transistor is not perfectly symmetric.Under those new assumptions, the real parts of the *Z*-parameters are expressed as:

$$\begin{aligned}
\mathrm{Re}(Z_{22} - Z_{12}) &= R_{de} + \frac{1}{(\alpha^{-1} + 1)}\frac{L}{W\mu_0 C_{ox}}\left(\theta + \frac{1}{V_{gs} - V_T}\right) \\
\mathrm{Re}(Z_{12}) &= R_{se} + \frac{1}{(\alpha + 1)}\frac{L}{W\mu_0 C_{ox}}\left(\theta + \frac{1}{V_{gs} - V_T}\right) \\
\mathrm{Re}(Z_{11} - Z_{12}) &= R_{ge} - \frac{1}{(\alpha + \alpha^{-1} + 2)}\frac{L}{W\mu_0 C_{ox}}\left(\theta + \frac{1}{V_{gs} - V_T}\right)
\end{aligned} \tag{17}$$

Where $\alpha = C_{gs}/C_{gd}$ is defined as the symmetry coefficient and θ is the mobility degradation coefficient (Tinoco & Raskin, 2009).

The mobility degradation factor θ can be determined measuring an array of transistors characterized by different channel lengths (*L*-array) following by a two-step procedure as mentioned below:

i. A linear regression of dV_{ds}/dI_{ds} *vs.* $1/(V_{gs} - V_T)$ for each device in order to determine the intercept (β) and the slope (m) parameters;
ii. A linear regression from the function β *vs.* m for the different channel lengths of the *L*-array is then traced to determine θ, as detailed in (Tinoco & Raskin, 2009).

Additionally, the α parameter can be obtained from:

$$\alpha = \frac{\mathrm{Im}(Z_{22} - Z_{12})}{\mathrm{Im}(Z_{12})} \tag{18}$$

Therefore, the correct series resistance can be obtained by the Bracale´s method but applying the corrections related to the carrier mobility change with the applied gate voltage (θ) and the asymmetry of the device under test (α) (Tinoco & Raskin, 2009).

5.2 Extraction of the extrinsic capacitances

Once the series resistances and inductances are extracted, the matrix Z_e is constructed and removed from the Z_Σ matrix according to equation (7). Then, the extrinsic capacitances can be removed using the MOSFET biased in depletion with V_{ds} = V_{gs} = 0 V. Under this condition, the equivalent circuit is shown in Fig. 21.
From that equivalent circuit, extrinsic capacitances can be obtained from the imaginary parts of the admittance parameters, and they are given by:

$$\begin{aligned} C_{gse} &= \frac{\mathrm{Im}(Y_{11} + Y_{12})}{\omega} \\ C_{gde} &= -\frac{\mathrm{Im}(Y_{12})}{\omega} \\ C_{dse} &= \frac{\mathrm{Im}(Y_{22} + Y_{12})}{\omega} \end{aligned} \tag{19}$$

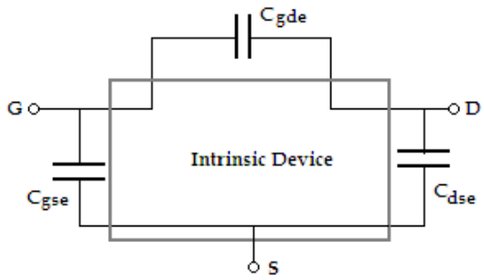


Fig. 21. Equivalent circuit under depletion bias condition after withdrawing the extrinsic series resistances and inductances.

5.2 Extraction of the intrinsic parameters

After extracting the extrinsic capacitances, the intrinsic matrix ($Y_{\pi i}$) can be determined by equation (6). From this matrix, the intrinsic parameters can be obtained from the following expressions.

$$C_{gsi} = \frac{1}{\omega\,\mathrm{Im}\left(1/\left(Y_{11} + Y_{12}\right)\right)}$$

$$C_{gdi} = -\frac{1}{\omega\,\mathrm{Im}\left(1/Y_{12}\right)}$$

$$
\begin{aligned}
C_{dsi} &= \frac{\mathrm{Im}(Y_{22}+Y_{12})}{\omega} \\
R_{gdi} &= -\mathrm{Re}(1/Y_{12}) \\
R_{gsi} &= \mathrm{Re}\left(\frac{1}{Y_{11}+Y_{12}}\right) \\
g_{di} &= \mathrm{Re}(Y_{22}+Y_{12}) \\
g_{mi} &= -\left|\frac{Y_{21}+Y_{12}}{Y_{11}+Y_{12}}\right| \cdot \frac{1}{\mathrm{Im}(1/(Y_{11}+Y_{12}))} \\
\tau &= \frac{1}{\omega}\arctan\left\{\frac{\mathrm{Im}\left[(Y_{21}-Y_{12})/(1+j\omega R_{gsi}C_{gsi})\right]}{\mathrm{Re}\left[(Y_{21}-Y_{12})/(1+j\omega R_{gsi}C_{gsi})\right]}\right\}
\end{aligned}
\tag{20}
$$

6. Figures of merit (FOM´s) for high frequency transistors

Three very important figures of merit (FOM´s) are commonly considered to describe the high frequency performance of MOSFETs: the cut-off frequency of the current gain (f_T), the maximum oscillation frequency (f_{max}) and the minimum noise figure (NF_{min}).
The cut-off frequency f_T can be defined as the frequency when the current gain decreases to 1 (0 dB). The current gain is related to the H_{21} parameter and is defined as the ratio of the output current to the input current. Based on the small-signal equivalent circuit presented in Fig. 14, f_T can be defined by the following expression:

$$
f_T = \frac{g_{mi}}{2\pi}\frac{1}{(C_{gs}+C_{gd})\cdot(1+g_{di}R_{se})+C_{gd}g_{mi}R_{se}} \tag{21}
$$

As we can see from (21), f_T is strongly reduced by the extrinsic source resistance. In the literature, the intrinsic cutoff frequency, f_c, which measures the intrinsic ability of a field effect transistor (FET) to amplify high frequency signals is also defined.

$$
f_c = \frac{g_{mi}}{2\pi}\frac{1}{C_{gs}} \tag{22}
$$

The maximum oscillation frequency is defined as the frequency at which the device still provides power in a stable operation. f_{max} can be defined as:

$$
f_{\max} = \frac{f_T}{2\sqrt{2\pi\cdot f_T R_{ge}C_{gd}+g_{di}\cdot(R_{ge}+R_{se}+R_{gsi})}} \tag{23}
$$

As we can see from (23), f_{max} is directly correlated to f_T and is strongly affected by the gate and source extrinsic resistances.

Another important FOM is the minimum noise figure (NF_{min}). The main application of the transistors, in general, is to amplify the signal present at its input terminal. However, the signal is mixed with noise from several sources, one of them is the transistor itself. Thus, the noise introduced by the MOSFET must be as low as possible in order to assure good amplification performance.
NF_{min} can be defined as the signal-to-noise ratio at the input divided by the signal-to-noise ratio at the output of the transistor and is expressed in dB.

$$NF_{\min} = 10\log\left(\frac{P_{Si}/P_{Ni}}{P_{So}/P_{No}}\right) \tag{24}$$

Where P_{Si} and P_{So} are the signal power at the input and output, respectively, and P_{Ni} and P_{No} are the noise power at the input and output, respectively.

7. Results of high frequency MOSFET´s

Recently, we analyzed by simulation the ability and robustness of the above mentioned methods to extract the extrinsic series resistances (Tinoco & Raskin, 2009) of various advanced MOSFETs.
ELDO software has been used to simulate the *S*-parameters of Partially-Depleted (PD) SOI n-MOS transistors with a channel length of 0.13 μm. The BSIM3SOI model, version 3.11, from ST Microelectronics, Crolles, France, is considered. The intrinsic core of the MOSFET is connected with lumped series resistances R_{se}, R_{de} and R_{ge} and a noise signal is added to the simulated ideal *S*-parameters in order to emulate the noise floor of a Vectorial Network Analyzer (VNA), which corresponds to the most critical noise source.
Table I shows a summary of the resistances extracted using the different methods presented in Section 5.1 for simulated transistors with and without noise.

Method	Extracted series resistances without noise			Extracted series resistances with noise		
	R_{se}	R_{de}	R_{ge}	R_{se}	R_{de}	R_{ge}
Lovelace	2.82	2.94	5.05	---	---	---
Torres-Torres	2.84	2.93	5.1	6.0	6.2	3.5
Raskin	2.89	2.95	5.04	3.75	5.7	5.51
Bracale	4.3	3.95	4.4	4.28	3.97	4.39
Tinoco	2.79	2.89	5	2.79	2.9	5.01
Used in simulations	3	3	5	3	3	5

Table 1. Summary of the extracted series resistances in Ω (Tinoco & Raskin, 2009).

As we can see from Table 1, the Torres-Torres and Raskin´s methods give very different values for the simulations with noise signal added to the *S*-parameters. In the Lovelace´s case, the noise disturbs enough the parameters that it makes impossible to determine the resistance values. On the other hand, the Bracale´s method is more robust in terms of noise, however it cannot adequately determine the values used in simulations. This problem is adequately corrected by the Tinoco´s method (Tinoco & Raskin, 2008).

Recently, we applied the Bracale´s and mobility correction established by the Tinoco´s series resistances extraction procedures on triple gate multifingered FinFETs with 50 gate fingers, 6 fins per finger and different channel lengths and widths. FinFETs are fabricated on a SOI wafer with 60-nm Si film on 145-nm of buried oxide, with <100> and <110> Si planes for top and lateral channels, respectively. From DC measurements a value of θ = 0.3 V^{-1} was extracted. Table II summarizes the aspect ratio of the measured FinFETs as well as the extracted series resistances using both extraction methods.

Measured FinFETs			Extracted Series Resistances							
			Bracele's Method				Tinoco´s Method			
Label	L (nm)	W_{fin} (nm)	R_{se} (Ω)	R_{de} (Ω)	R_{ge} (Ω)	R_{sd} (Ω)	R_{se} (Ω)	R_{de} (Ω)	R_{ge} (Ω)	R_{sd} (Ω)
Fin1	60	27	4.75	7.77	5.66	12.52	4.08	7.1	5.99	11.18
Fin2	60	27	4.9	8.14	8.7	13.05	4.22	7.46	9.05	11.68
Fin3	60	92	0.86	2.92	11.13	3.78	0.58	2.63	11.27	3.21
Fin4	60	93	0.47	2.53	6.42	3	0.41	2.48	6.44	2.9
Fin5	79	27	5.22	7.94	7.05	13.16	4.42	7.14	7.45	11.56
Fin6	106	27	6.41	9.23	11.7	15.65	5.42	8.24	12.21	13.66
Fin7	106	53	1.14	4.14	31.46	5.29	0.42	3.42	31.8	3.85
Fin8	106	53	1	3.97	31.26	4.97	0.22	3.2	31.6	3.42
Fin9	280	27	8.04	10.3	4.39	18.34	6.11	8.39	5.35	14.47
Fin10	280	27	7.95	10.2	3.23	18.17	6.1	8.33	4.2	14.4
Fin11	920	34	0.71	4.96	58.2	5.68	0.11	4.36	58.5	4.48

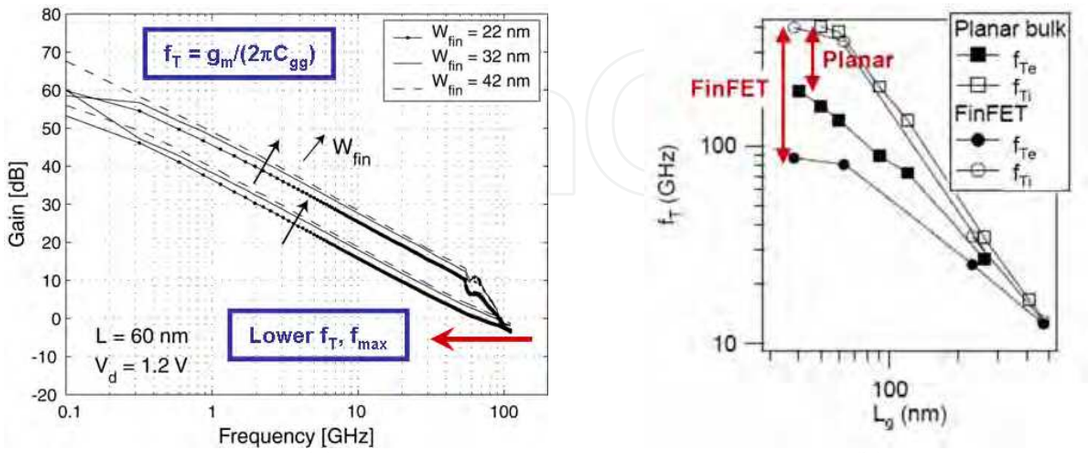
Table 2. Summary of the experimental results for various FinFETs and the extracted series resistances (Tinoco & Raskin, B, 2009).

Using the extracted extrinsic resistances presented in Table II, we have demonstrated in (Tinoco & Raskin, B, 2009) the importance of using the Tinoco's method to accurately extract a wideband small-signal equivalent circuit. Those results highlight the importance of accurate and reliable RF characterization techniques to design wideband ICs.

As mentioned in the introduction, another important objective of developing accurate high frequency characterization techniques is the possibility to deeply analyze the dynamic behavior of the transistor and then identify the main high frequency limitations of a particular technology. As an example, using the developed RF characterization techniques presented in Section 5.1, the RF performance of FinFETs with various geometries (fin width, W_{fin}, channel length L_g) has been deeply analyzed. The current gain ($|H_{21}|$) as a function of frequency which yields the device cut-off frequency (f_T) is presented in Fig. 22a for FinFETs characterized by different fin widths. Unfortunately, we can observe a reduction of the cutoff frequency with the shrinkage of W_{fin}. This degradation is mainly related to the increase of the source and drain resistances with the thinning down of the fin width (Raskin, 2009).

Fig. 22b presents the extracted RF cutoff frequencies of planar and FinFETs devices as a function of channel length. The so-called intrinsic (f_{Ti}) and extrinsic (f_{Te}) cutoff frequencies stand, respectively, for the current gain cutoff frequency related to only the intrinsic lumped parameter elements (g_{mi}, g_{di}, C_{gsi} and C_{gdi}) and the complete small-signal equivalent circuit (including the parasitic capacitances, C_{gse} and C_{gde}, as well as the series resistances R_{se}, R_{de}, and R_{ge}). It is quite interesting to see that both devices present similar intrinsic cutoff frequencies (around 400 GHz for a channel length of 60 nm) but the extrinsic cutoff

frequency, f_{Te} , of FinFET (90 GHz) is nearly twice lower than the one of the planar MOSFET (180 GHz) (Raskin, 2009), (Subramanian, 2008). This demonstrates that unfortunately the parasitic elements in the case of FinFETs are relatively more important than in the case of planar MOSFETs.



(a) (b)

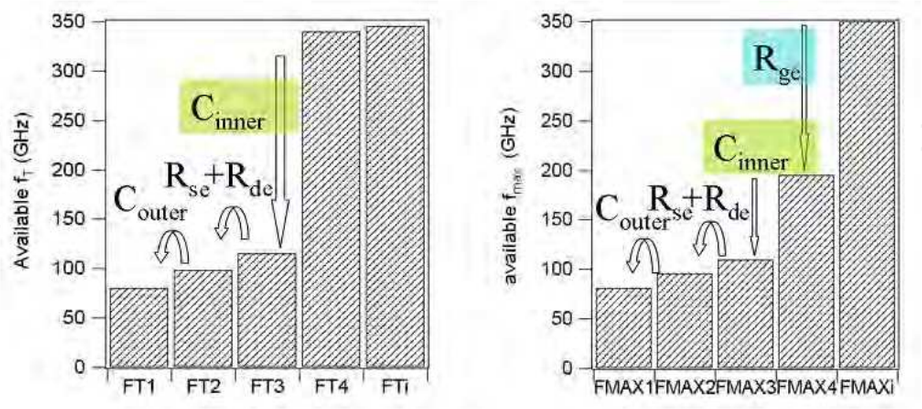
Fig. 22. (a) Current gain and maximum available power gain *vs.* frequency for a 60 nm-gate length FinFET for various fin widths (W_{fin}). (b) Extracted intrinsic (f_{Ti}) and extrinsic (f_{Te}) current gain cutoff frequencies for a planar single gate MOSFET and a FinFET as a function of the channel length (Raskin, 2009), (Subramanian, 2008).

Again, thanks to the RF extraction techniques it was possible to analyze the relative importance of each lumped equivalent elements on the FinFET high frequency electrical behaviour. Indeed, based on a wideband analysis, the lumped small-signal equivalent circuit parameters are extracted from the measured *S*-parameters. Fig. 23 shows the relative impact of each parasitic parameter on the cutoff frequency (f_T, Fig. 23a) and maximum frequency of oscillation (f_{max}, Fig. 23b) in the case of a 60 nm-long FinFET. As expected from the expressions (21)-(23) the gate resistance has an important impact on f_{max} whereas f_T is unchanged. The sum of fringing capacitances C_{inner} directly linked to the FinFET three-dimensional (3-D) architecture has a huge impact on both cutoff frequencies. In fact, f_T and f_{max} drop down, respectively, by a factor of 3 and 2. Finally, the source and drain resistances as well as the parasitic capacitances related to the feed connexions outside the active area of the transistor slightly decrease both cutoff frequencies. Based on that analysis, it is quite clear that the fringing capacitances inside the active area of the FinFET are the most important limiting factor for this type of non-planar multiple gate transistor (Raskin, 2009), (Subramanian, 2008).

Finally, Fig. 24 shows the variations of the minimum noise figure NF_{min} and the available associated gain G_{ass} as a function of the DC drain current density at 10 GHz for three different channel lengths. G_{ass} is the available gain of the transistor when it is matched for minimum noise figure NF_{min}. The minimum noise figure decreases with the gate length, this variation is strongly linked to the increase of the intrinsic cutoff frequency when the gate length decreases, due to the g_{mi} increment.

In (Raskin, 2008), we demonstrated that the noise performance of FinFETs are mainly degraded by the important fringing capacitance (C_{gd}) related to their 3-D and multifin

structure. However, a minimum noise figure of 1.35 dB could still be obtained with an associated available gain of 13.5 dB at 10 GHz for V_{dd} = 0.5 V. This result is quite encouraging to bring solutions for future low-power RF systems.



(a) (b)

Fig. 23. Analysis of the relative impact of each lumped extrinsic parameters on (a) the cutoff frequency (f_T) and on (b) the maximum frequency of oscillations (f_{max}) for a 60 nm-long FinFET (Raskin, 2009), (Subramanian, 2008).

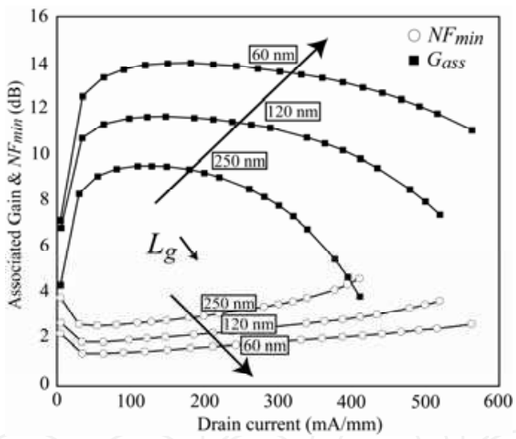


Fig. 24. Associated gain and minimum noise figure *vs*. normalized drain current at V_{dd} = 1 V for FinFETs of various gate lengths, having a total width of 68.4 µm, N_{finger} = 50 and W_{fin} = 32 nm.

7. Conclusions

This chapter summarizes the current status of the MOSFETs for very high frequency applications. It also establishes the small-signal equivalent circuit for MOSFETs under quasi-static and non-quasi-static regimes. An efficient extraction method for the intrinsic and extrinsic lumped elements of the MOSFET electrical model has been presented and applied to various advanced MOS devices. Thanks to the development of accurate wideband characterization techniques, the static and dynamic (up to high frequencies) electrical behaviour of advanced MOSFETs can be modelled for supporting RF ICs designs but also

deeply analyzed to understand the limitations of present technologies and thus to pave ways to technological optimizations and innovations.

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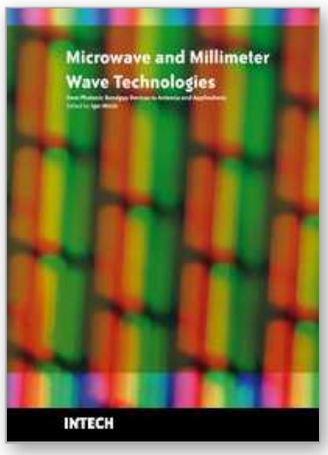

Microwave and Millimeter Wave Technologies from Photonic Bandgap Devices to Antenna and Applications

Edited by Igor Minin

ISBN 978-953-7619-66-4
Hard cover, 468 pages
Publisher InTech
Published online 01, March, 2010
Published in print edition March, 2010

The book deals with modern developments in microwave and millimeter wave technologies, presenting a wide selection of different topics within this interesting area. From a description of the evolution of technological processes for the design of passive functions in milimetre-wave frequency range, to different applications and different materials evaluation, the book offers an extensive view of the current trends in the field. Hopefully the book will attract more interest in microwave and millimeter wave technologies and simulate new ideas on this fascinating subject.

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

Julio C. Tinoco and Jean-Pierre Raskin (2010). Advanced RF MOSFET´s for Microwave and Millimeter Wave Applications: RF Characterization Issues, Microwave and Millimeter Wave Technologies from Photonic Bandgap Devices to Antenna and Applications, Igor Minin (Ed.), ISBN: 978-953-7619-66-4, InTech, Available from: http://www.intechopen.com/books/microwave-and-millimeter-wave-technologies-from-photonic-bandgap-devices-to-antenna-and-applications/advanced-rf-mosfet-s-for-microwave-and-millimeter-wave-applications-rf-characterization-issues

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