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Broadband GaN MMIC Power Amplifiers design

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1. Introduction

Monolithic microwave integrated circuits (MMIC) based on gallium nitride (GaN) high electron mobility transistors (HEMT) have the advantage of providing broadband power performance (Milligan et al., 2007). The high breakdown voltage and high current density of GaN devices provide higher power density than the traditional technology based on GaAs. This allows the use of smaller devices for the same output power, and since impedance is higher for smaller devices, broadband matching becomes easier.

In this chapter, we summarise the design procedure of broadband MMIC high power amplifiers (HPA). Although the strategy is quite similar for most semiconductors used in HPAs, some special considerations, as well as, experimental results will be focused on GaN technology.

Apart from design considerations to achieve the desired RF response, it is essential to analyse the stability of the designed HPA to guarantee that no oscillation phenomena arises. In first place, the transistors are analysed using Rollet's linear K factor. Next, it is also critical to perform nonlinear parametric and odd stability studies under high power excitation. The strategy adopted for this analysis is based on pole-zero identification of the frequency response obtained at critical nodes of the final circuit (Barquinero et al., 2007).

Finally, to avoid irreversible device degradation, thermal simulations are required to accurately predict the highest channel temperature and thermal coupling between transistors.

2. AlGaN/GaN HEMT Technology

First of all, MMIC GaN technology has to be evaluated. High power GaN devices operate at high temperature and high-dissipated power due to the high power density of performance. Therefore, the use of substrates with high thermal conductivity like the silicon carbide (SiC) is preferred.

GaN technological process is still immature and complex. However, gate lithography resolution lower than 0.2 μm and AlGaN/GaN epi-structures on 100-mm SiC substrates are already available (Milligan et al., 2007).

Wide band gap semiconductors such as GaN and SiC are very promising technologies for microwave high power devices. The advantages of these materials over conventional semiconductors, GaAs and Si, include high breakdown field (E_g), high saturation electron velocity (v_{sat}), and high thermal conductivity. GaN/AlGaN high electron mobility transistors (HEMTs) offer even higher power performance due to the higher carrier sheet density and the higher saturation velocity of the bidimensional electron gas channel (2DEG) compared to SiC metal semiconductor field effect transistors (MESFETs). The diagram in Fig. 1 summarizes GaN-HEMT properties and its benefits.
This technology has demonstrated a power density of 30 W/mm using devices with dimensions of 0.55x246 μm² at 4 GHz when biased at 120 V (Wu et al., 2004).

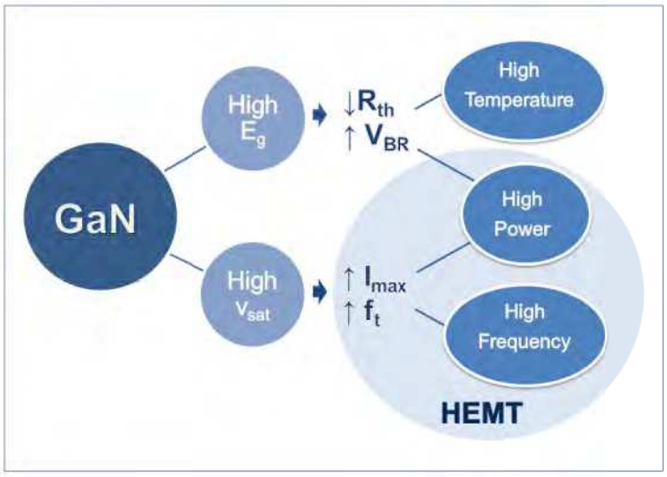

Fig. 1. GaN HEMT properties and benefits.

In a HEMT the conduction channel is confined to the interface between two materials with different band gap. This region known as 2DEG has very few ionized impurities to scatter the electrons, resulting in a very high mobility device. AlGaN/GaN heterostructures have a high sheet carrier density in the 2DEG interface without intentional doping of the structure. The spontaneous and piezoelectric polarization effects are the key factors for the charge distribution in the AlGaN/GaN HEMT (Ambacher et al., 2000).

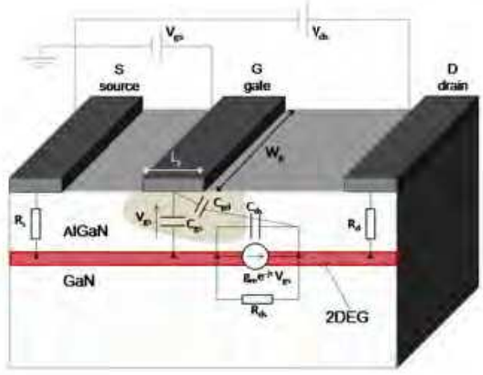

Fig. 2. AlGaN/GaN HEMT model.

The model of a HEMT that shows the small-signal parameters and the 2DEG channel is depicted in Fig. 2. Source and drain ohmic contact, as well as Schottky gate can be observed. The gate voltage (V_{gs}) controls the current (I_{ds}) that flows between the source and the drain. When V_{gs} reaches pinch-off voltage the electrons below the gate are depleted and no current can flow from drain to source.

Since AlGaN/GaN HEMTs for HPA applications work under high power conditions, non-linear models have to be used to simulate the transistor performance. The success of the design depends on the precision of the model fitting. A widely used approach is based on Angelov analytical expressions (Angelov et al., 1992). The model parameters are extracted from load pull, S-parameters, and pulse IV measurements. For instance, the nonlinear current source is characterized fitting DC and pulsed IV-measurements. The voltage controlled gate-source and gate-drain capacitance functions (C_{gs} and C_{gd}) are determined from bias dependent hot-FET S-parameter measurements. Finally, the parasitic elements of the HEMT model are extracted with cold-FET S-parameters measured from pinch-off to open channel bias conditions. The high temperature performance of GaN-HPAs demands the use of electro-thermal models (Nuttinck et al., 2003). Otherwise, power estimation will be too optimistic in CW operation.

The design methodology evaluated in this chapter is based on the experience reported by the design of several 2-6 GHz HPAs. The active devices used are 1-mm gate-periphery HEMTs fabricated using AlGaN/GaN heterostructures and gate length (L_g) technology of 0.5 µm from Selex Sistemi Integrati S.p.A foundry (Costrini et al., 2008) within Korrigan project (Gauthier et al., 2005). The HEMT cells consist of 10 fingers, each with a unit gate width (Wg) of 100 µm. The maximum measured oscillation frequency (f_{max}) of these transistors is about 39 GHz.

A considerable dispersion between wafers is still observed because of GaN technology immaturity. Table 1 shows the main characteristics (device maximum current I_{dss}, pinch-off voltage V_p, breakdown voltage V_{bgd}, C_{gs}, sheet resistance R_s and contact resistance R_c) of two wafers fabricated for the 2-6 GHz HPAs (wafer 1 and 2) and the wafer used for extracting the nonlinear electrical models (wafer 0) for the 1st-run designs. From the results in Table 1, an important deviation between the model and the measurements is expected. For instance, Cgs mismatch will produce a poor S11 fitting.

Wafer	I_{dss} mA/mm	V_p (V)	V_{bgd} (V)	C_{gs} (pF/mm)	R_s (Ω/sq)	R_c (Ωmm)
Wafer 0	972	-6.4	>70	3.2	355	0.44
Wafer 1	794	-4.7	50	2.24	456	0.47
Wafer 2	567	-2.7	71	2.88	440	0.36

Table 1. GaN wafers comparison.

Regarding passive technology, the foundries provide microstrip and coplanar models for typical MMIC components such as transmission lines, junctions, inductors, MIM capacitors and both NiCr and GaN resistors.

3. Design

The design process of a broadband HPA is described in this section. Special attention should be paid on broadband matching network synthesis and device stability.

3.1 Amplifiers Topology

The first step in an HPA design is to choose the most appropriated topology to fulfil design specifications. Single or multi-stage topology will be used depending on the gain target. In order to achieve high output power, several devices must be combined in parallel.

The classical combination topologies are the balanced and the corporative HPA. Balanced structures are made with λ/4-lines, which become quite large in designs below X-band. Furthermore, multi-stage approach for broadband design will enlarge the circuit even more. On the other hand, the corporate topology based on two-way splitters seems to be a more versatile solution for broadband designs. It can be designed with compact lumped broadband filters in frequencies below X-band while transmission lines can be used at higher frequencies.

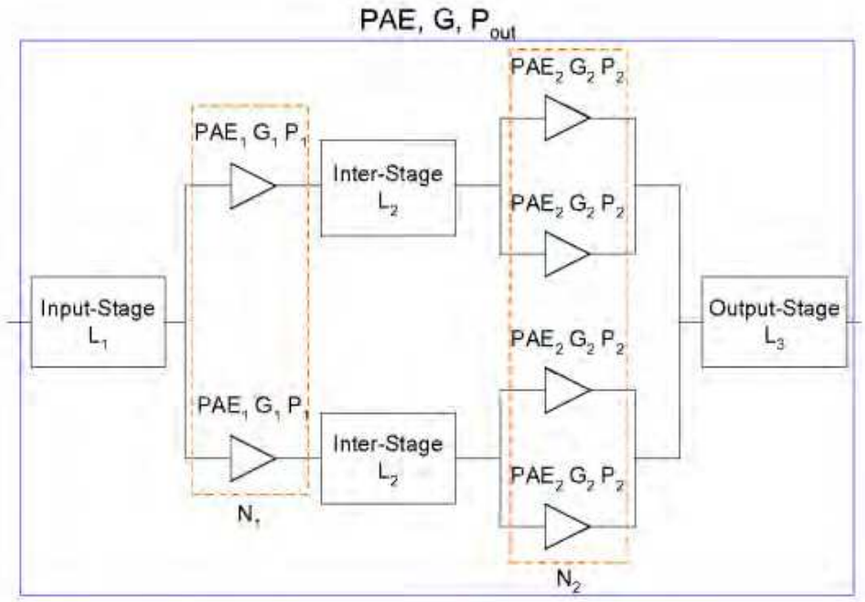

Fig. 3. Two-stage corporative topology amplifier.

The two-stage corporative topology, such as the one in Fig. 3, is widely used to design HPAs, because it offers a good compromise between gain and power. Note that the first stage consists of two unit cells which drive the output stage, composed of four equal cells. This power amplifier has three matching networks: input-, inter-, and output-stage. The labels displayed in Fig. 3 represent the loss of each matching network (L_i), the number of combined cells (N_i), the power added efficiency (PAE_i), the gain (G_i), and the output power (P_i) at the i^{th}-stage.

Output stage loss, L_3, is critical to the HPA output power ($P_{out}=N \cdot P_{HEMT} \cdot L_3$). Besides, network loss has to be minimised mainly in the output network, because it is essential to maximise power added efficiency (PAE_{total}). Equation (1) is used to calculate PAE_{total} of a corporative topology with 2^n transistors at the output stage. The representation of equation (1) in Fig. 4 confirms the higher influence of L_3 in PAE_{total}.

$$PAE_{total} = \frac{PAE_1 PAE_2 (L_1 L_2 L_3 G_1 G_2 - 1)}{PAE_1 L_1 L_2 G_1 (G_2 - 1) + PAE_2 L_1 (G_1 - 1)} \quad (1)$$

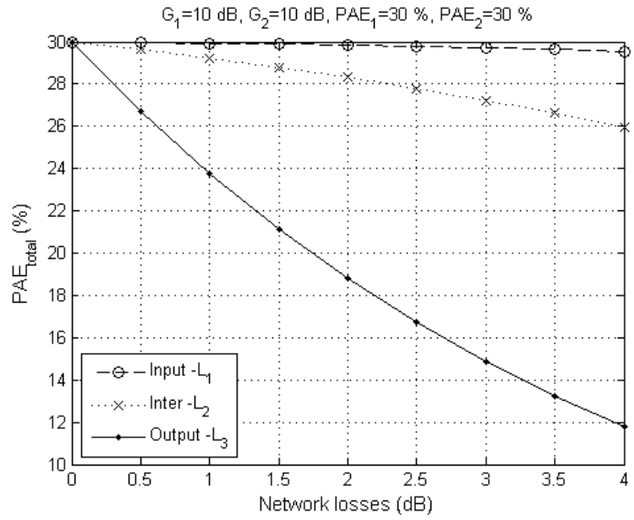

Fig. 4. PAE_{total} versus input-, inter-, and output-stage network loss. To analyse the influence of each network the loss of the other networks are set to 0 dB.

High efficiency operation is especially important for power devices, because thermal issues can degrade the amplifier performance. Dissipated power (P_{dis}) is inversely proportional to the HPA efficiency, see equation (2).

$$P_{dis} \approx P_{out} \cdot ((PAE_{total})^{-1} - 1) \tag{2}$$

P_{dis} and temperature increase (ΔT) are related in equation (3) through the thermal resistance (R_{th}). This parameter gives an idea of the thermal flow through a material or a stack of materials from a hot spot to another observation point. Therefore, R_{th} depends on the thermal conductivity of the materials and the final HPA set-up.

$$\Delta T = P_{diss} R_{th} \tag{3}$$

3.2 Unit transistor cell

The unit transistor cell size selection is based on a compromise between gain and power, because large devices have higher power, but lower gain (Walker, 1993). Moreover, input and output impedances decrease for larger devices, making the design of broadband matching networks difficult. The lack of power of small devices can be solved by combining several devices in parallel. It is worth noting that the complexity of the design increases with the number of cells to be combined.

Once the transistor size is selected, the available unit cells have to be evaluated at different bias operating conditions (Snider, 1967). The optimum operation class of a power amplifier depends on the linearity, efficiency or complexity of the design specifications. In the conventional operation classes, A, B, AB and C, the transistor works like a voltage controlled current source. On the contrary, there are some other classes, such as D, E and F, where amplifier efficiency improves by working like a switch. In the diagram of Fig. 5, different operation classes have been represented, indicating the IV-curves, the load-lines and the

conduction angle (Φ) of each one. The conduction angle defines the time that the transistor is in the on-state.

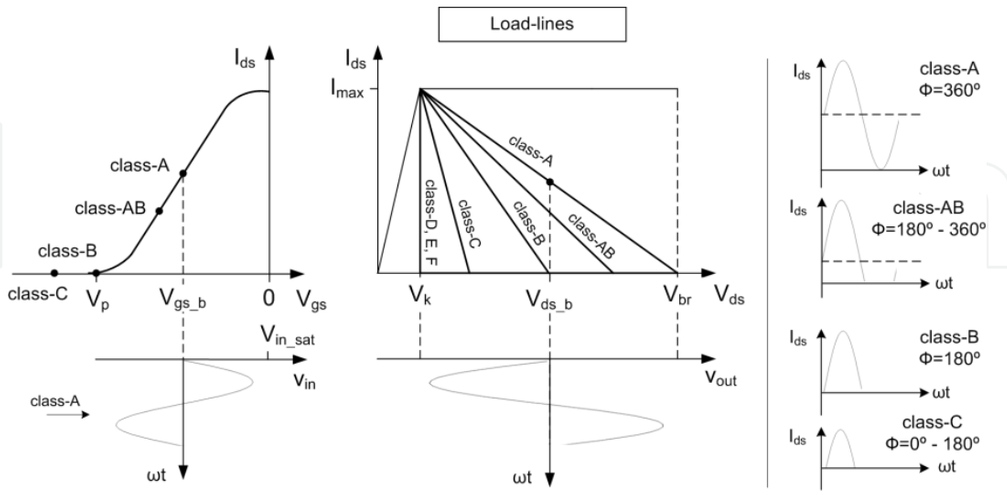

Fig. 5. HPA bias operation classes.

The maximum drain efficiency ($\eta=P_{out}/P_{dc}$) and the maximum output power of a transistor versus the conduction angle can be calculated under ideal conditions, as shown in Fig. 6, where the knee voltage (V_k) is assumed to be 0 V and RF compression is not considered. This representation shows that drain efficiency is inversely proportional to Φ, and that output power is almost constant between class AB and class A. Class-AB operation quiescent point at $30\%I_{max}$ provides simultaneously maximum power and a considerable high drain efficiency, therefore this seems to be an optimum bias point.

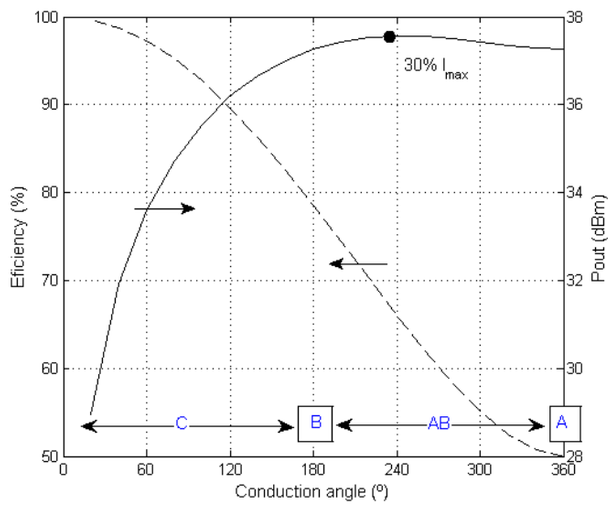

Fig. 6. Output power and drain efficiency versus the conduction angle (Φ) calculated for V_{ds}=25V and I_{max}=850mA.

Given an operation class, the RF power drive determines the actual drain efficiency. Efficiency and linearity are opposite qualities. Therefore, a compromise has to be assumed depending on the HPA design application.

3.3 Unit cell stabilization

An in-depth analysis of the stability is necessary to guarantee that no oscillation phenomena arise. Firstly, the transistors are analysed using the classical approach for linear stability based on the Rollet's (Rollet, 1962) formulas over a wide frequency band. This theorem stands that the transistor is unconditionally stable if the real part of the impedance at one port is positive ($Re(Z_{ii}) > 0$) for any real impedance at the opposite port. The Rollet's K factor as a function of the two-port network inmitance parameters ($\gamma ii = Zii = Yii$) is the following:

$$K = \frac{2Re(\gamma_{11})Re(\gamma_2) - Re(\gamma_{12}\gamma_{21})}{|\gamma_{12}\gamma_{21}|} > 1 \tag{4}$$

The easiest way to increase K to achieve K>1 is increasing the input impedance of the transistor. This can be done by adding a frequency dependent resistance (R_{stab}) at the transistor input port: $Z'_{11}=Z_{11}+R_{stab}$. Stability can also be improved with a resistor at the transistor output, but this would reduce the maximum output power. The series stabilization resistance can be calculated from equation (5).

$$R_{stab} = \frac{K|Z_{12}Z_{21}| + Re(Z_{12}Z_{21})}{2Re(Z_{22})} - Re(Z_{11}) \tag{5}$$

Another useful way to write R_{stab} is as a function of the small-signal parameters of the transistor:

$$R_{stab} = \frac{2\omega C_{ds}C_{gs}(K-1) + C_{gd}g_m K}{2\omega C_{gd}g_m(C_{gd} + C_{gs})} \tag{6}$$

Parallel RC networks in series with the transistor gate make it possible to synthesize R_{stab} in a wide frequency band, see Fig. 7.

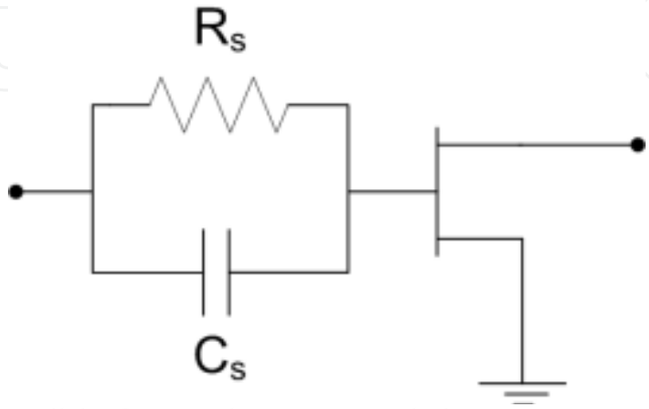

Fig. 7. Stabilization parallel RC networks in series with the transistor gate.

As an example, we take an unstable transistor (K<1) at frequencies under 12.5 GHz. The ideal stabilization resistance to make this transistor unconditionally stable (with K=1.2) at any frequency is plotted in Fig. 8 (left). In the same plot, the R_{stab} traces obtained with two different RC networks have been included. The new K factor (K_{new}) recalculated taking into account the cascade of the series RC networks and the transistors are represented in Fig. 8 (right).

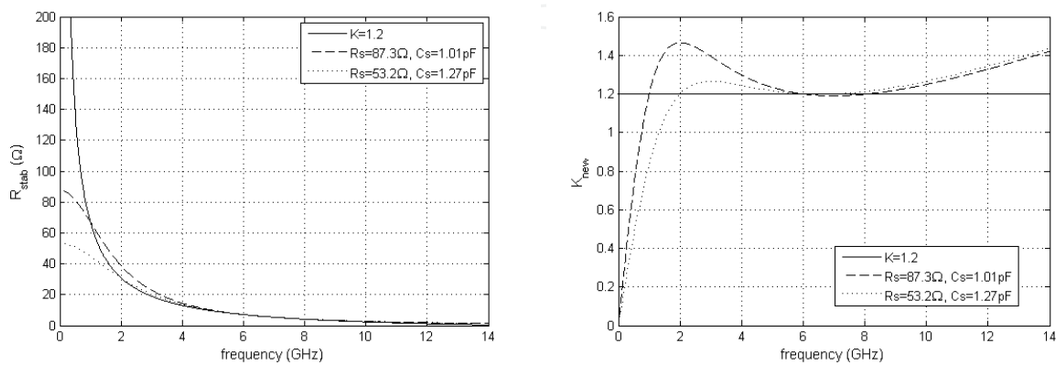

Fig. 8. R_{stab} and K_{new} calculated with an ideal network for K=1.2 and two different RC networks.

RC networks cannot be used to stabilize a transistor at low frequencies because the resulting resistor becomes too large or the capacitor too small to be feasible in MMIC technology. Therefore, off-chip stabilization networks are sometimes required to avoid the use of big components in the chip. Another solution is to add a parallel resistor (R_p) in the internal stabilization network. This resistor can be included in the gate bias path (L_b) as depicted in Fig. 9. L_b should be chosen high enough to have no influence in the frequency band of the design.

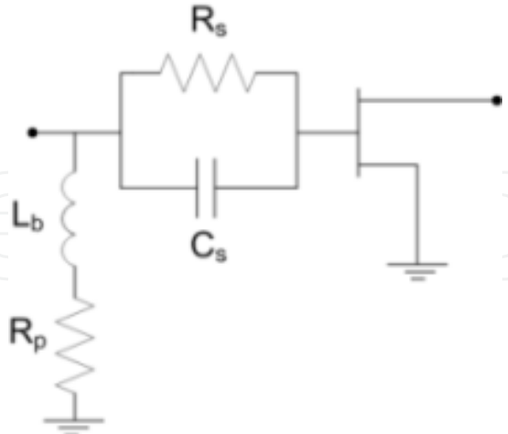

Fig. 9. Combination of a parallel RC networks in series with the transistor and a parallel resistor in the bias path to achieve unconditional stability at any frequency.

In Fig. 10 it is shown the comparison between K_{new} calculated with the series RC network of Fig. 7 and the network of Fig. 9 that combines a series and a parallel resistor. The last solution makes the transistor unconditionally stable even at low frequencies.

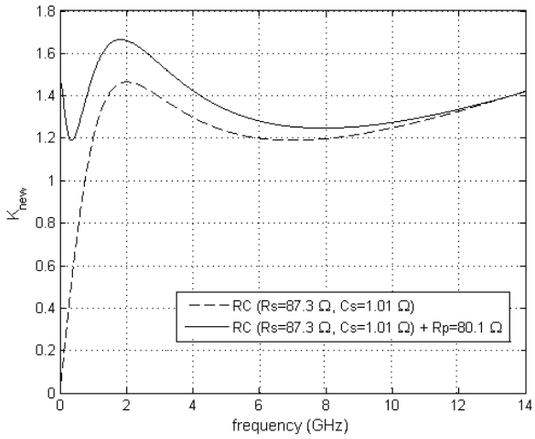

Fig. 10. K_{new} obtained with a single RC networks and with the combination of an RC network and a parallel resistor at the gate bias path.

As Fig. 8 shows, the stabilization networks introduce dissipative loss decreasing with frequency, what also contributes to compensate the device gain slope. The maximum available gain (MAG) after stabilization is obtained as:

$$MAG = \left|\frac{Z_{21}}{Z_{12}}\right|\left(K_{new} - \sqrt{K_{new}^2 - 1}\right) \tag{7}$$

The comparison between the original MAG of the transistor and the MAG obtained with the proposed stabilization networks is shown in Fig. 11.

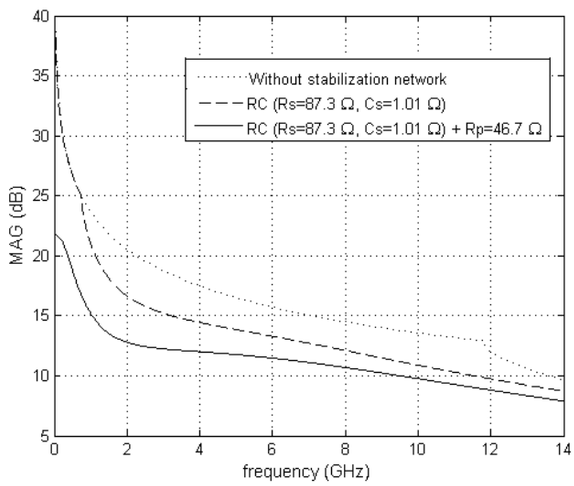

Fig. 11. Comparison of the transistor MAG without any stabilization network and with both a single RC networks and the combination of an RC network and R_p.

RC networks are also used to prevent parametric and out-of-band oscillations (Teeter et al., 1999).

3.4 Networks synthesis

The HPA matching networks (input-, inter-, and output-stage) are synthesized from filter theory and implemented with both lumped elements and transmission lines. These networks are designed to provide optimum impedances at the transistor output and conjugated matching at its input, as well as, matching the HPA input and output to 50 Ω. Stabilization networks and DC bias networks have to be included and considered in the synthesis process.

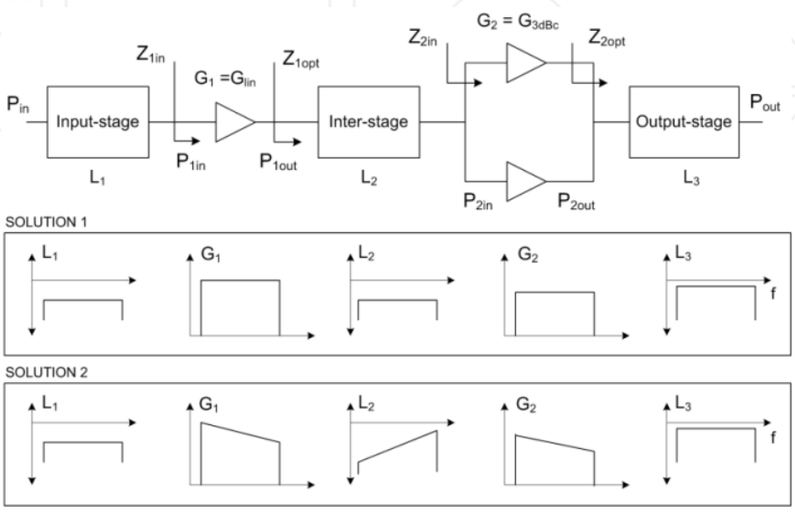

Fig. 12. Two-stage HPA design process.

Two different strategies can be followed in the HPA design as indicated in the diagram in Fig. 12; in the first solution, the transistor and the gain equalization network are considered a single block and the matching networks have to be designed with a flat frequency response. This approach is easily adopted when the stabilization network introduces frequency dependent loss. In the second solution, gain compensation is performed by the inter-stage matching network.

The following steps describe the HPA design process:

- Firstly, the transistor optimum loads for maximum power (Z_{2opt}) are calculated using load-pull techniques. The most precise method to obtain the optimum loads is by means of load-pull measurements. However, load-pull measurement equipment is expensive and, the measurement process could be tedious and long for broadband design, because many load measurements are required. If nonlinear models of the transistor are available, load-pull simulation could be done in CAD simulators. The accuracy of this option depends on the precision of the nonlinear models. When only the transistor lineal-model and the IV-curves are available, the load-pull contours have to be estimated by the Cripps method (Cripps, 1983).
- Next, the output-stage network has to be designed. This network transforms Z_{2opt} to the 50 Ω impedance of the HPA output-port and combines the power of the 2nd-stage transistors. The drain DC-bias is included in this network and it is done through a parallel inductance of a value calculated to provide the imaginary part of Z_{2opt} at the design centre frequency. Network loss (L_3) must be minimised, mainly in this output-stage because it is critical to maximise power and PAE.

- Later, the inter-stage network loads are calculated; firstly, the input impedance of the second-stage transistors loaded with the output-stage network (Z_{2in}); secondly, the optimum loads for maximum gain at the first-stage transistors (Z_{1opt}). It is important to calculate the impedances at the expected high power working conditions.
- Then, the inter-stage network is designed to synthesize the optimum loads for the first-stage (Z_{1opt}) and to match the second-stage input (Z_{2in}). The design complexity of this network is higher because two complex impedances have to be matched over a broad frequency bandwidth. Moreover, if it is required, the transistor gain roll-off should be compensated by frequency dependent losses in this network (L_2). This can be done with a RC network, as it was described in section 3.3. First-stage drain DC-bias is also done through a parallel inductance that provides the imaginary part of Z_{1opt} at the design centre frequency.
- Finally, the input-stage network is designed to match the HPA-input of 50 Ω to the first-stage transistors input (Z_{1in}). In this case, the input impedance of the transistors is also calculated loading them with the inter- and output-stage networks.

The matching networks can be designed as two-port networks. Anyhow, it is worth noting that the input impedance has to be scaled by the number of transistors to be combined (N). Then, the network can be transformed into a (N+1)-port network. The transformation is done by dividing the two-port network in different sections and scaling them depending on the branching level in the power combination (or division) network. Fig. 13 shows a diagram where the transformation process is schematized.

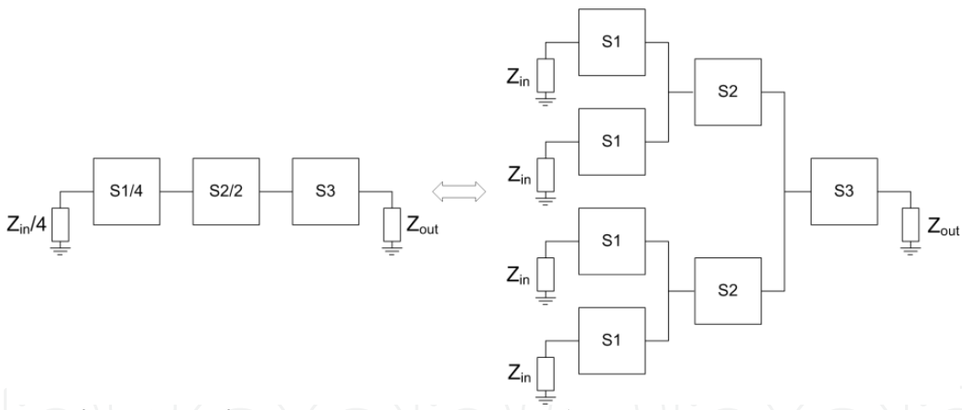

Fig. 13. Transformation of two-port to N-port networks.

4. Global stability analysis

Multistage HPAs are prone to parametric oscillations that are function of the input-power drive. The origin of these instabilities is the nonlinear capacitance of the transistor input impedance, which varies with the input-drive. Odd-mode oscillations are also frequent due to the presence of multiple active elements and the circuit symmetry. Subharmonic oscillations at $f_{in}/2$, where f_{in} is the input signal frequency, are very common in transistors due to the nonlinear capacitance nature. However, spurious oscillations at non-harmonically related frequency f_a are also observed.

Two-port network techniques cannot be applied for HPA stability analysis due to the existence of multiple feedback loops. The standard harmonic-balance (HB) simulators used

for HPA design do not include tools for high-power stability analysis either. Fortunately, there are several techniques that perform a nonlinear stability study based on the circuit linearization around the large-signal steady state obtained with HB. The method proposed by Mons (Mons et al., 1999) is rigorous and complete, but it requires the verification of the Nyquist stability criteria for every nonlinear element, what becomes tedious in complex circuits. From the design process point of view, faster stability analysis is preferred. Therefore, it is proposed a technique based on the insertion of an external small-signal perturbation in a circuit node. This way, it is possible to obtain the closed-loop transfer function provided by the impedance calculated at the observation node in a certain frequency range. Pole-zero identification of the resultant transfer function is used to verify the stability of the circuit (Jugo et al., 2003). This study can be done in both small-signal and large-signal conditions. Different observation nodes must be considered to ensure the detection of masked instabilities, because of pole-zero cancellation in certain nodes. At least, an analysis per each HPA stage is required.

Parametric simulations at different working conditions are advisable to see the evolution of critical poles. If any complex conjugated poles cross to the right half plane an oscillation is detected.

In circuits with N active devices, N modes of performance coexist. There are N-1 odd-modes and one even-mode simultaneously. For instance, in the second-stage of the HPA in Fig. 3, three odd-modes and one even-mode coexist. However, due to the symmetry, two odd-modes are equivalent, so only the odd-modes [+ - + -] and [+ + - -], and the even-mode [+ + + +] have to be studied. Using different perturbation configurations, the stability of each mode can be determined by means of the pole-identification technique. Instead of a single perturbation generator, one generator at the input of each transistor is introduced and the phase of the perturbation signals is shifted 180º depending on the excitation mode (Anakabe et al. 2005).

In Fig. 14, the frequency responses of an even-mode (left) and an odd-mode [+ - + -] (right) are depicted. Both responses have been obtained at the same operating conditions (P_{in}=19dBm, f_{in}=4GHz, V_{ds}=26V and V_{gs}=-4.2V), and it can be seen that the odd-mode presents a resonance at $f_{in}/2$ that indicates the presence of a possible subharmonic oscillation. This means the transfer function may have poles with positive real part.

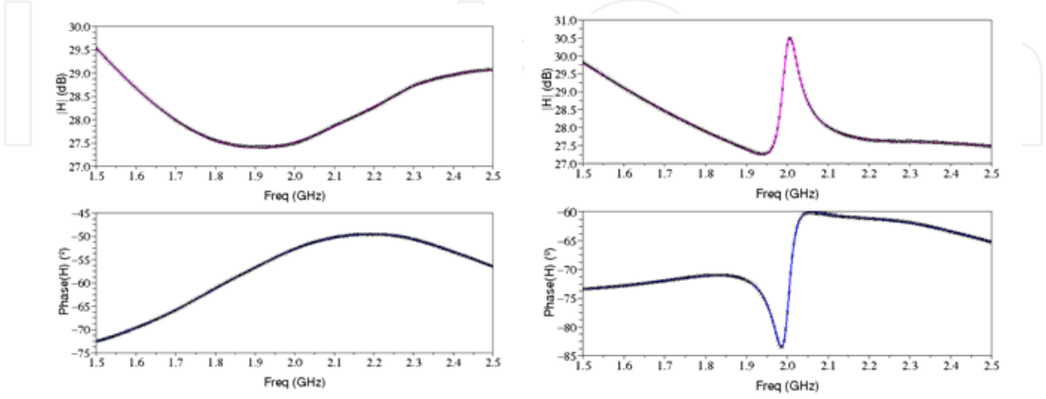

Fig. 14. Closed-loop transfer function calculated with even-mode [+ + + +] (left) and odd-mode [+ - + -] (right) excitation. The HPA operation conditions are P_{in}=19dBm, f_{in}=4GHz, V_{ds}=26V and V_{gs}=-4.2V

Once an oscillation is found, the instability margin has to be determined through a parametric study about the critical operation conditions. Frequency and power of the input signal, as well as the HPA DC-bias (V_{ds} and V_{gs}) are common parameters that affect stability. The evolution with frequency and V_{ds} of the poles at $f_{in}/2$ corresponding to the frequency response in Fig. 14 are represented in Fig. 15. The HPA is unstable between 3.97 GHz and 4.03 GHz at V_{ds} = 26 V.

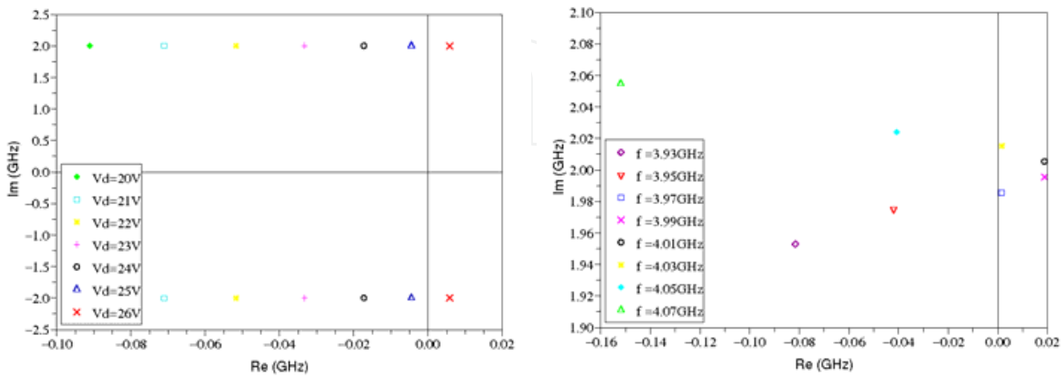

Fig. 15. Evolution of the poles at $f_{in}/2$ versus V_{ds} (left) and f_{in} (right). The HPA initial operation conditions are P_{in}=19dBm, f_{in}=4GHz, V_{ds}=25V and V_{gs}=-4.2V

Once the stability nature has been determined, the HPA circuit has to be corrected to avoid oscillations that may invalidate the design. Usually, the instability is cancelled using notch filters (like RC networks (Teeter et al., 1999)) at the oscillation frequency or resistors to add loss in the oscillation feedback loop. For instance, resistors between the transistors (R_o) can be added to prevent odd-mode oscillations, see Fig. 16.

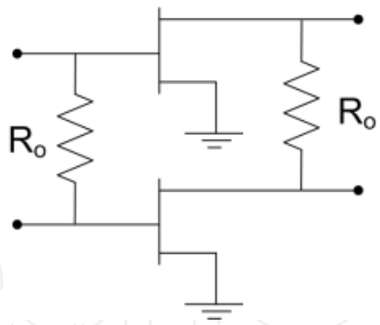

Fig. 16. Resistors to prevent odd oscillations.

5. Thermal characterization

Thermal characterization with different techniques is of crucial interest in GaN-HPAs, because it is still necessary to analyse the influence of the high power dissipated in this leading technology (Nuttinck et al., 2003).

Thermal resistances, R_{th}, at different working conditions can be calculated with commercial software like COMSOL Multiphysics (FEMLAB) or Ansys. The simulations can be performed for the unit transistor cell to obtain the maximum channel temperature (T_{chann}),

or for the final HPA to characterize the thermal coupling between the transistors. Fig. 17 shows the thermal resistance of a unit transistor cell of 1mm, and the results for an HPA with 8x1mm transistors at the output-stage. The simulation has been performed in ideal conditions and taking into account the real mounting fixture of the device on a cooper carrier.

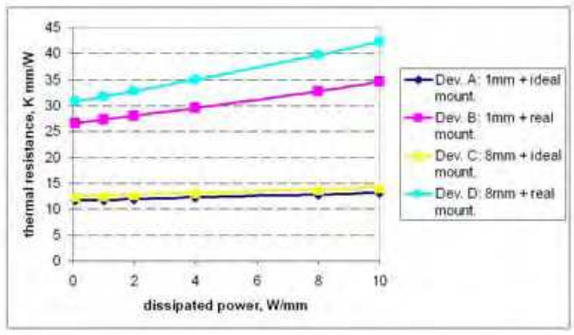

Fig. 17. Comparison between the simulated thermal resistance of a 1mm-transistor and of an HPA with 8x1mm transistors at the output-stage, in ideal and real mounting conditions.

R_{th} in the range of 13.5 ºC/W has been obtained at 6W dissipated power (P_{dis}) for the ideal mounting of the 1mm-transistor. From these calculations, an estimated gradient (ΔT) around 81ºC is expected between the channel and the backside temperature. However, the real assembly increases R_{th} to 32 ºC/W, which means a temperature gradient of 192 ºC. Thus, we see that a test fixture mounted on a cooling platform is necessary in order to provide the amplifier with a proper heat dissipation system.

6. Broadband HPA examples

Two fully monolithic broadband HPAs with an output-stage active periphery of 4 mm and 8 mm are presented in the photos of Fig. 18. They have been fabricated at Selex Sistemi Integrati S.p.A.

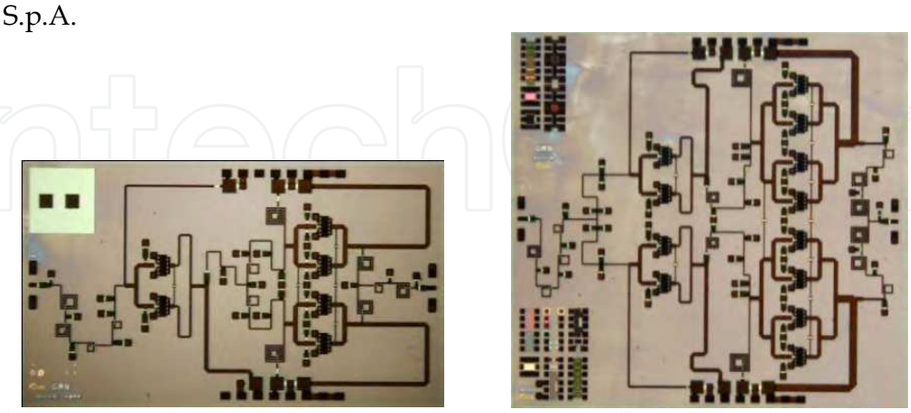

Fig. 18. Photograph of the 4 mm (left) and 8 mm (right) HPAs. The chip size is 6.6x3.7 mm² and 6.6x 6.0 mm², respectively.

Several MMIC HPAs were characterized in CW and pulsed conditions. All chips were tested at drain-source voltage, V_{ds}, from 20 to 25 V and I_d=30%Imax.

Typical measured small-signal gain and input return loss of the 4 mm-HPA are shown in Fig. 19. Over the 2-6 GHz frequency range, gain was about 18 dB and the input return loss was lower than -7 dB. Simulated results are also shown for comparison. Mismatch between simulated and measured input return loss exists because the transistor model was extracted from a previous wafer and the technological process is still in development.

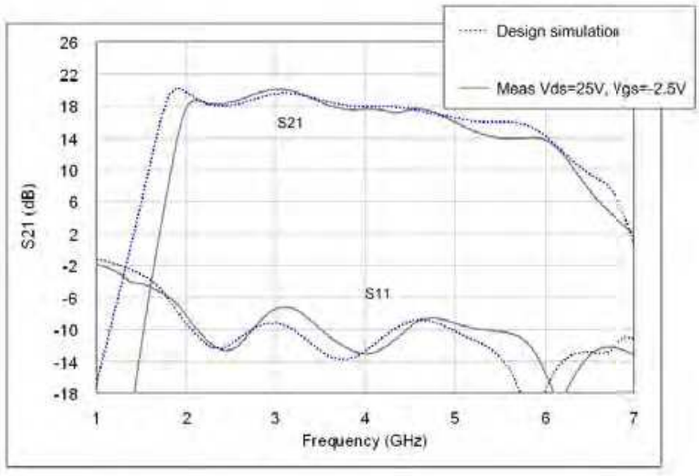

Fig. 19. Comparison of gain and input return loss measurements and simulation of the 4mm-HPA.

Pulsed and CW characterization of the 8mm-HPAs from two different wafers (see Table 1) at 4.5 GHz and V_{ds}=25V are shown in Fig. 20. The pulsed measurements were performed with short pulses of 20 µm length and 1% duty cycle. The HPA from Wafer 1 exhibited higher output power in pulsed-mode, whereas the power capacity in CW is similar. Saturation power is about 15 W in CW with better than 20% PAE and, reaching 26 W and 25% in pulsed-mode.

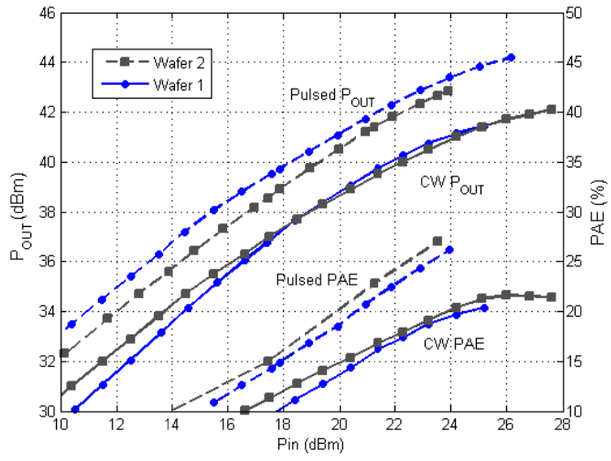

Fig. 20. CW and pulsed output power and PAE versus input power of the 8mm- HPA from Wafer 1 and Wafer 2 at 4.5 GHz, V_{ds}=25 V and 30%I_{DSS}.

Typical broadband performance of both 4mm-HPA and 8mm-HPA in CW and pulsed-mode is shown in Fig. 21. Pulsed measurements in the lower frequency band are not available because the set-up works above 3 GHz. The 4mm-HPA has greater than 40 dBm (2.5 W/mm) output power in 50% of the band in CW, and greater than 41.4 dBm (3.5 W/mm) in pulsed conditions. On the other hand, the 8mm-HPA delivers 41.2 dBm (2 W/mm) in CW and 44 dBm (3.5 W/mm) in pulsed-mode. Thermal problems are more significant for the 8mm-HPA in CW.

To characterise the power degradation due to thermal heating, the HPAs have been measured in pulsed-mode at different duty cycles and pulse lengths. The duty cycle has higher influence than the pulse length in the HPA performance. The results of this analysis with a pulse length of 100 µs are depicted in Fig. 22. The output power and PAE at V_{ds}=20 and 25 V are shown for both HPAs. As expected, the power and efficiency degradation is higher for the 8mm-HPA. This device losses approximately 40% of the power capacity from 1% to 50% duty cycle, while the 4mm-HPA falls only 30%.

There is still margin to increase CW power if the test-jig is improved to reduce its thermal resistance.

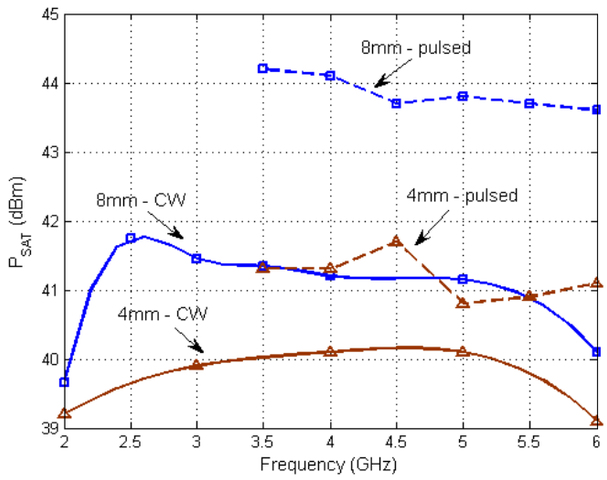

Fig. 21. CW and pulsed output power versus frequency of both 4mm-HPA and 8mm-HPA at V_{ds}=25 V and 30%I_{DSS}.

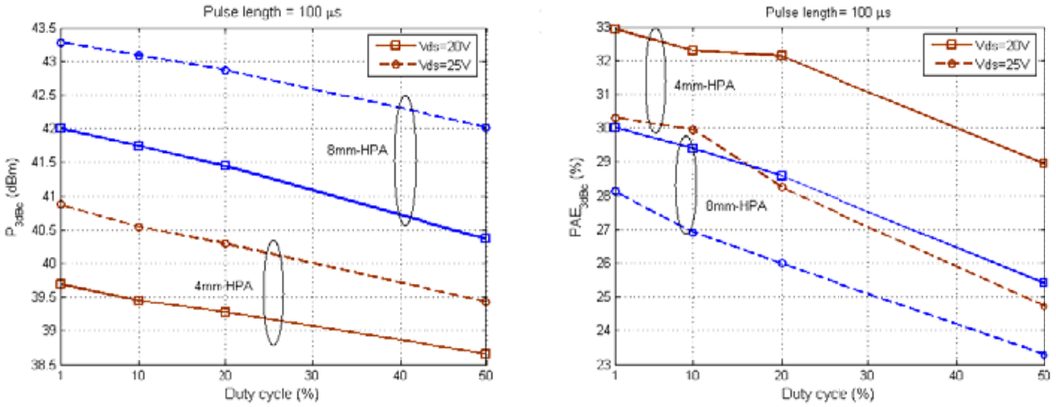

Fig. 22. Output power and PAE versus duty cycle of both 4mm-HPA and 8mm-HPA. Measurements with pulses of 100 µs length at V_{ds} =20, 25 V and 30%I_{DSS}.

7. Conclusion

This chapter makes a brief introduction of the GaN-HEMT technological process development. Based on this technology, it is established a design procedure for broadband high power amplifiers. The design is focused on the synthesis of the matching and stabilization networks of a two-stage amplifier. It is highlighted the need for nonlinear stability analysis to avoid parametric and odd-mode oscillation. Thermal characterization is also critical due to the high power dissipated in high power GaN devices. Finally, we present the analysis of results of two broadband HPA demonstrators.

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