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A Complete Practical Ultra wideband Test Bed in X-Band

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1. Introduction

Design of an UWB system has several challenges some of which are not shared with more traditional narrowband systems [David et al.,2005]. Also the multifunction test bed is designed and implemented to receive, change and transmit multiple simultaneous independent RF signals, including communications, Radar and Electronic Warfare (EW) [Gregory et al.,2005; Blair et al.,1998]. It is important that this test bed includes of an ultra wideband white Gaussian noise generator and delay lines circuits, so it is capable to test, evaluate and calibrate many types of systems especially with radio receivers [Askari et al.,2008(a); Askari et al.,2008(b)]. In summary this test bed will be used for evaluating communication systems performance by allowing an operator to add a controlled amount of thermal noise to a reference signal and determine the effect of noise on system performance, such as BER [Mattews,2006]. Also, a delay line is used to delay a signal by certain time while minimizing the distortion caused by crosstalk, dispersion and loss [Hohenwarter et al.,1993]. With those capabilities this test bed can be used as a Gaussian modulating signal source to mimic real conditions such as Rayleigh fading and other simulated models. In ECM applications, High power amplified noise modules can be used to produce many types of interferenc for RF systems such as RADARs. Also for RADAR applications, it can be useful for effects of target amplitude fluctuations, beam shape, missed detections, false alarms, target maneuvers, pulse compression, track loss, Stand Off Jammer (SOJ) broadcasting wideband noise and targets attempting range gate pull off (RGPO) [Blair et al.,1998]. In Noise application, Noise Figure measurement, Bandwidth, Linearity, Inter-modulation, Frequency Response and Impulse Response of a DUT can be measured [Gupta,1975; Upadhyaya,1998]. In Encryption application, an electrical thermal noise source is more random than anything else in nature. It can also be used for Continuous Monitoring of System Performance for Built In Test Equipment (BITE)[Robbins,2004].

In this chapter design and implementation of a practical reconfigurable communication system including an additive ultra wide band white Gaussian noise and delay lines in X-band from 6 to 12 GHz with other necessary microwave parts as the test bed are introduced. The challenges that affect the design of a custom CW/pulsed UWB

architecture is discussed, also design and implementation procedures of all microwave parts such as ultra wideband amplifiers, dividers, switches, drivers, gain controllers, generators, filters, delay components, bias tee, transitions and etcetera are presented.

2. Transceiver general descriptions

Transceiver is short for *transmitter-receiver*, a device that both receives, process and transmits signals. Fig.1 shows a general block diagram of a transceiver test bed with important sections. Important sections of a tranceiver is front end, intermediate receiver, programmable delay , white gaussian noise, driver and control. The specific goals are to achieve a test bed in X-band from 6GHz to 12GHz with the following specifications.
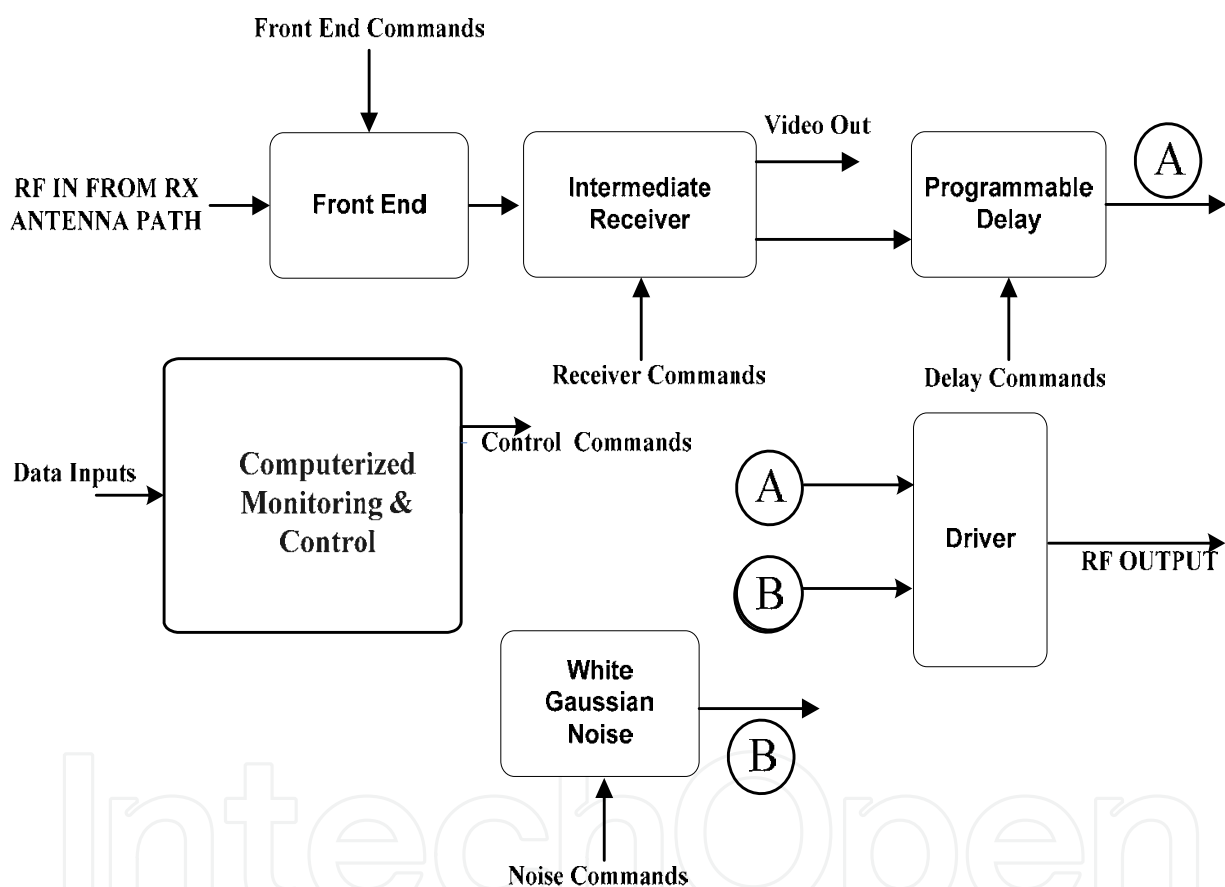
Fig. 1. General transceiver test bed with important sections

Frequency Range: 6-12 GHZ
Pulse Duration: 100 nsec to CW
CW or Pulse Transmitter Output: 25 dBm
Sensitivity:-45 dBm in a 100 nsec pulse
Delay Mode & Gain Control
CW Rejection with Operator Command: 30dB
Programmable Control Commands from Control & Monitoring Section
Fault Generation

Wide Band White Gaussian Noise in 6-12GHz
Blanking switch isolation: 55dB
Narrow Band White Gaussian Noise bandwidth: 20 ~ 40 MHz
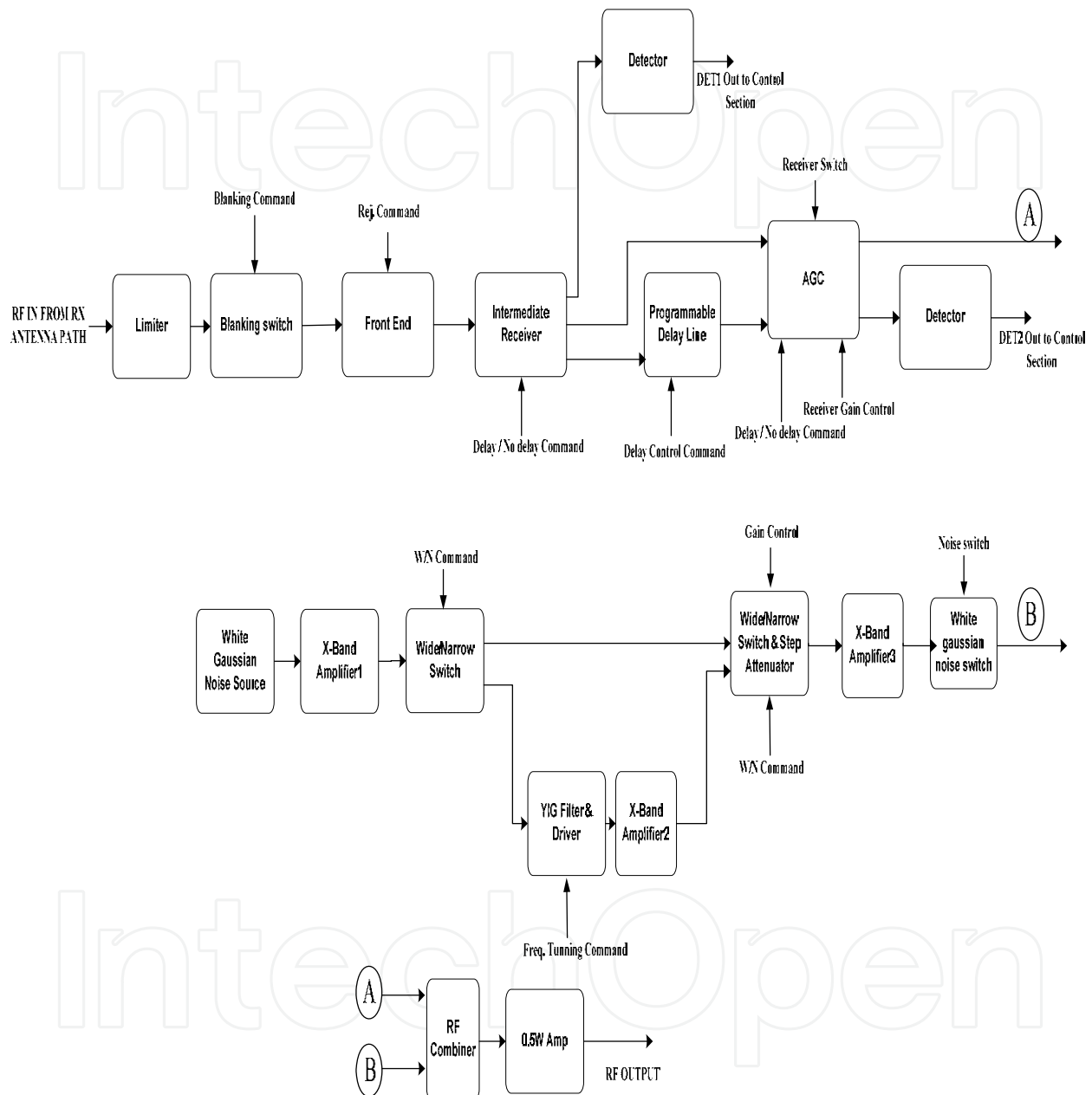Fig. 2 shows the complete block diagram that encompasses all desired specifications.

Fig 2. complete block diagram of the test bed

3. Design procedure

To achieve a transceiver test bed with desired specifications, each component of block diagram should have specific features which are discussed in the following.

3.1 The limiter

Limiter is an optional circuit that allows signals below a specified input power to pass unaffected while attenuating the peaks of stronger signals that exceed this input power and is used to protect receiver from strong signals. ACLM4616 from *Advanced Control Components* is used as a limiter. According to the datasheet and the experimental results the specifications of this component are represented in table 1.

Frequency Range (GHZ)	Part Number	Peak Input Power (Watts)	CW Input Power (Watts)	Flat Leakage (CW Power) (dBm)	Insertion Loss (dB) (Experimental)	Maximum VSWR
6-18	ACLM4616F	100	2	13	0.3 ~ 1.2	2.2:1

Table 1. Specifications of ACLM4616F according to the datasheet and the experimental results

3.2 The blanking switch

The RF signal from limiter is entered to the blanking switch. This switch is used to protect the receiver from specified signals by the suppression command. S1D2018A5 from *Herotek* is a circuit that switches the RF input by the TTL control input. According to the datasheet and the experimental results, the specifications of this component are represented in table 2.

Model	Insertion Loss(dB) (Experimental)			Min Isolation(dB) (6-12 GHz) (Experimental)	Max VSWR
	0.5-2GHz	6-12GHz (Exp.)	12-18GHz		
S1D2018A5	-	1.5-2.5	2.5	65	2:1

Table 2. Specifications of S1D2018A5 according to the datasheet and the experimental results

3.3 The front end section and circuit design

RF front end is a generic term for everything in a receiver that sits between the antenna and the intermediate receiver stage. For most architectures, this part of the receive chain consists of a matching circuit allowing all the received energy from the antenna to get to the next stage. All important specifications such as maximum gain and flatness in frequency response in all attenuation levels have been solved in this section. The final experimental result is a front end block with max 8 dB of gain, 31.5dB attenuation and 2dB of flatness in frequency bandwidth of 7-11GHz. In this section, a low noise amplifier, a band-pass filter (BPF) to reject out-of-band signals and a variable attenuator to cancel or control input signal power (if needed) are used. The block diagram of front end board is shown in fig 3.
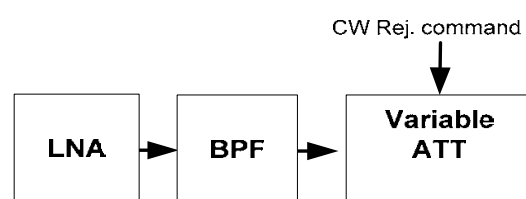

Fig. 3. Front end block diagram

The sub circuits specifications of this board are mentioned below:

- Low noise amplifier

The LNA is used to set the receive sensitivity of the receiver by offering high gain and low noise figure. Because in this design the input signals are mentioned strong enough, so the noise figure is not very important. *Agilent Technology's* 6-18GHz MMIC, AMMP5618 is used as a low noise amplifier to amplify the input signal power and improve the system MDS and compensate the filter loss.

- Band pass filter

A compensated Chebychev filter with 0.5dB ripple and 9GHz center frequency and 5GHz bandwidth is designed to maximize the MDS of system and minimize the out of band interference. To achieve maximum bandwidth and better second order response due to implementation on micro-strip technology and feasibility of micro-strip fabrication, the Edge-Coupled BPF with tapped input and output is used. This parallel arrangement gives relatively large coupling for a given spacing between resonators, and thus, this filter structure is particularly convenient for constructing filters having a wider bandwidth than other structures [Askari et al.,2008(a); Hong&Lancaster,2001].

- Variable attenuator

The variable attenuator is used to cancel CW signal (if needed) and also to control the variations of output power and gain of front end from 0.5 to 31.5 dB with 0.5dB step. *Hittite* DC-13GHz attenuator, HMC424LH5 is used as a variable attenuator to decrease the signal power by 0.5 dB LSB Steps to 31.5 dB.

After combining sub circuits together and optimizing by ADS (Advanced Design System 2005) simulation, the final structure is achieved. For feasibility of implementation, the filter section is implemented on a micro-strip laminate with lower permittivity and the other sections are implemented on a laminate with higher permittivity. The BPF is fabricated on *Rogers-5880* and other parts of block design are fabricated on *Rogers-6010* microstrip board.

All footprints, lines and ground planes of final design are simulated and optimized in EM simulator of ADS.

After implementing all parts together, the final circuit was achieved and tested. Fig. 4-a shows the photograph of front end block and fig. 4-b shows the experimental results S21 vs. frequency with 0,2,6,14,30 dB attenuation.
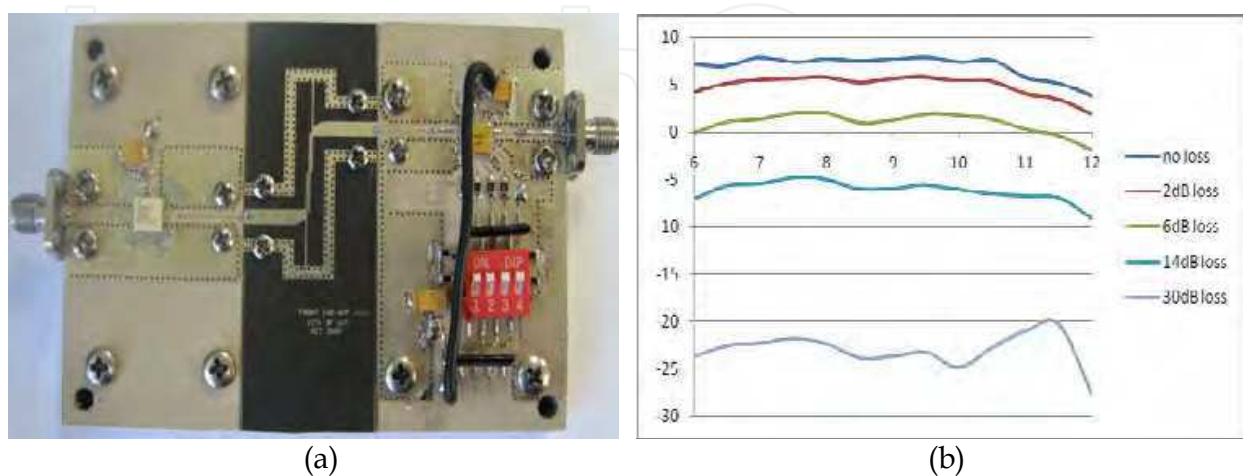

(a)   (b)

Fig. 4. (a) Photograph of front end block (b) experimental results S21 vs. frequency with 0,2,6,14,30 dB attenuation.

3.4 The intermediate receiver section and circuit design

The front end board output signal is entered to the intermediate receiver section. As it was shown in fig.2 this section is used to produce three RF output signals. So, a divider is necessary to divide the input signal to the detector path and delay-no delay path. The signal in the detector path is amplified and sent to a BPF and then is sent to a RF envelope detector to make the video signal. The other signal is sent to a switch after amplifying to select between two paths, delay or no delay with a command.

The main important challenge in this section is amplifying and dividing the ultra wide band RF signal to three paths with preservation of flatness in overall frequency response.

The block diagram of intermediate receiver board is shown in fig. 5. In this design, divider, amplifier (#2), BPF and switch are used.
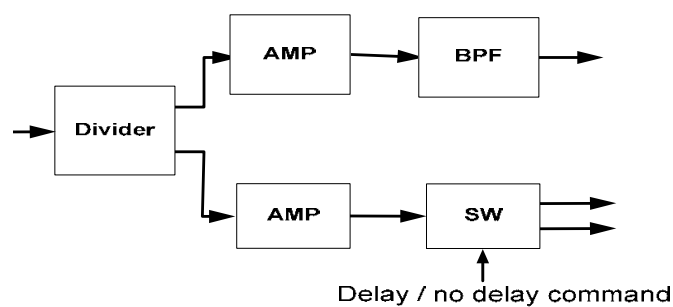

Fig. 5. Intermediate receiver block diagram

The sub circuits' specifications of this board are discussed in the following:

- Divider :

A wide band divider is necessary to divide signal to the detector path or delay-no delay path. All important specifications such as insertion loss and flatness in frequency response have been solved in this section. For this purpose, two types of compensated Wilkinson dividers are supposed and finally a double stage compensated Wilkinson divider with two isolation resistors is selected [Askari et al.,2008(b); Fooks&Zakarevicius,1990]. After simulation and optimization by ADS, the final structure for this part is obtained. Fig. 6-a shows the final layout of this divider which is designed and implemented on a Rogers-5880 microstrip board. Fig. 6-b shows the photograph of divider.

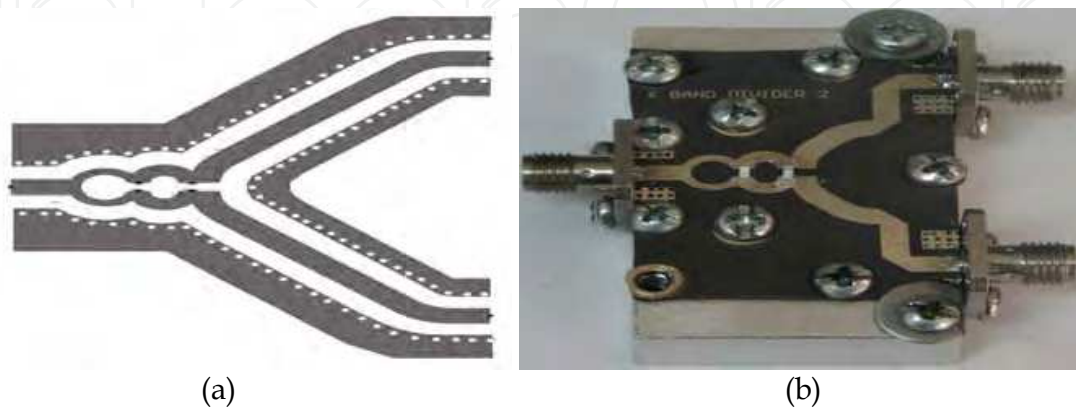(a)   (b)

Fig. 6. (a) Divider layout   (b) Divider photograph

The first and second resistors (100 ohm and 200 ohm, respectively) are mounted to improve the isolation between output ports up to 20dB. The experimental results, insertion loss and isolation of two ports are shown in fig. 7-a and 7-b. The final experimental result is a divider block with 3dB insertion loss and 1dB of flatness and minimum 20dB isolation in frequency bandwidth of 6-12GHz.

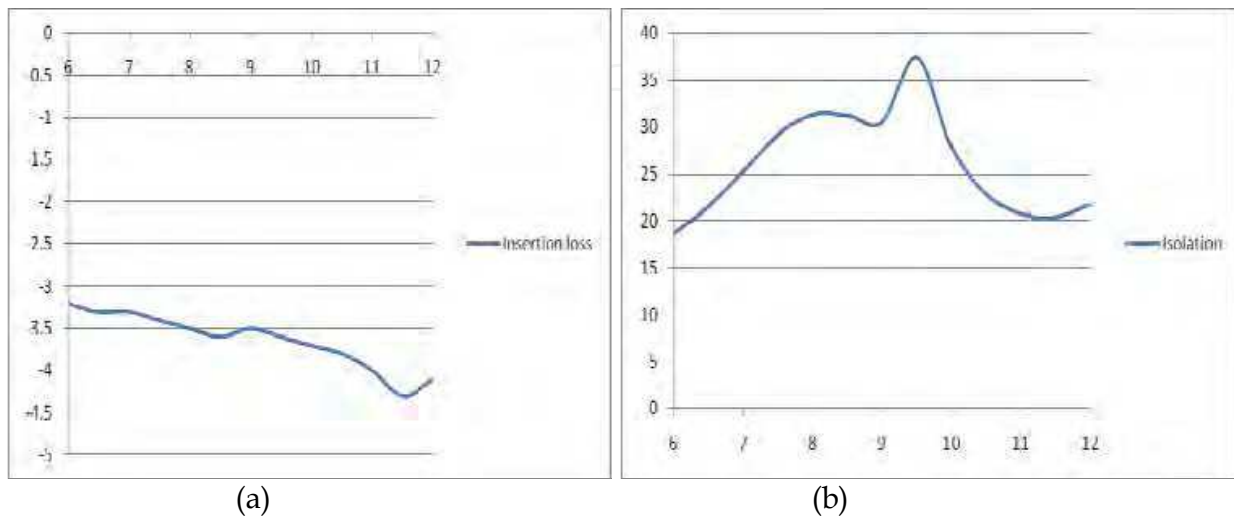(a)   (b)

Fig. 7. (a) Insetion loss vs. Frequency   (b) Isolation vs. Frequency

- amplifier :

To increase the output power signals and to achieve the output signals to the desired power level, after dividing, amplifiers are used in each path. To design a wideband amplifier with flatness in gain, the variations of |S21| have to be compensated. There are many methods to design wideband amplifiers such as reactive matching, lossy matching, balanced matching and matching with negative feedback [Gonzalez, 1997]. In this section, lossy matching combined with reactive matching is used to increase the bandwidth of amplifier and to flatten the gain. One MMIC amplifiers (*Avago Technologies* AMMP-5618) are used in each path. Amplifiers are simulated with Advanced Design System. Each amplifier increases the output power to approximately 13 dB. AMMP-5618 specifications are explained completely in section 3-3.

- Band pass filter :

A third order Chebychev filter with 0.5dB ripple and 9GHz center frequency and 5GHz bandwidth is designed to minimize the interference and to achieve the best detector sensitivity and dynamic range over the desired bandwidth. The BPF is the same as BPF in front end (Edge Coupled BPF), but it is not tapped input and output.

- switch :

To select RF signal to be sent to the delay or no delay path, a high speed switch should be used in the design of intermediate receiver section. *Hittite* GaAs MMIC SPDT non-reflective, DC - 20.0 GHz switch.

After combining subcircuits together and doing simulations and optimizations by considering undesired effects, the final structure is achieved. For feasibility of implementation , the filter section is implemented on a micro-strip laminate with lower permittivity and the other sections are implemented on a laminate with higher permittivity. The BPF is fabricated on *Rogers-5880* and other parts of block design are fabricated on

Rogers-6010 microstrip board. All footprints, lines and ground planes of final design are simulated in EM simulator of ADS.

After implementing all parts together, the final circuit was achieved and tested. Fig. 8-a shows the photograph of intermediate receiver block and fig. 8-b and 8-c show the experimental results. The final experimental result is an intermediate receiver block with a 10dB gain in output to detector over 6.5-11 GHz with 3 dB of flatness, and 8dB gain in output to delay or no delay paths and 3dB of flatness in frequency bandwidth of 6-12GHz.

(a)

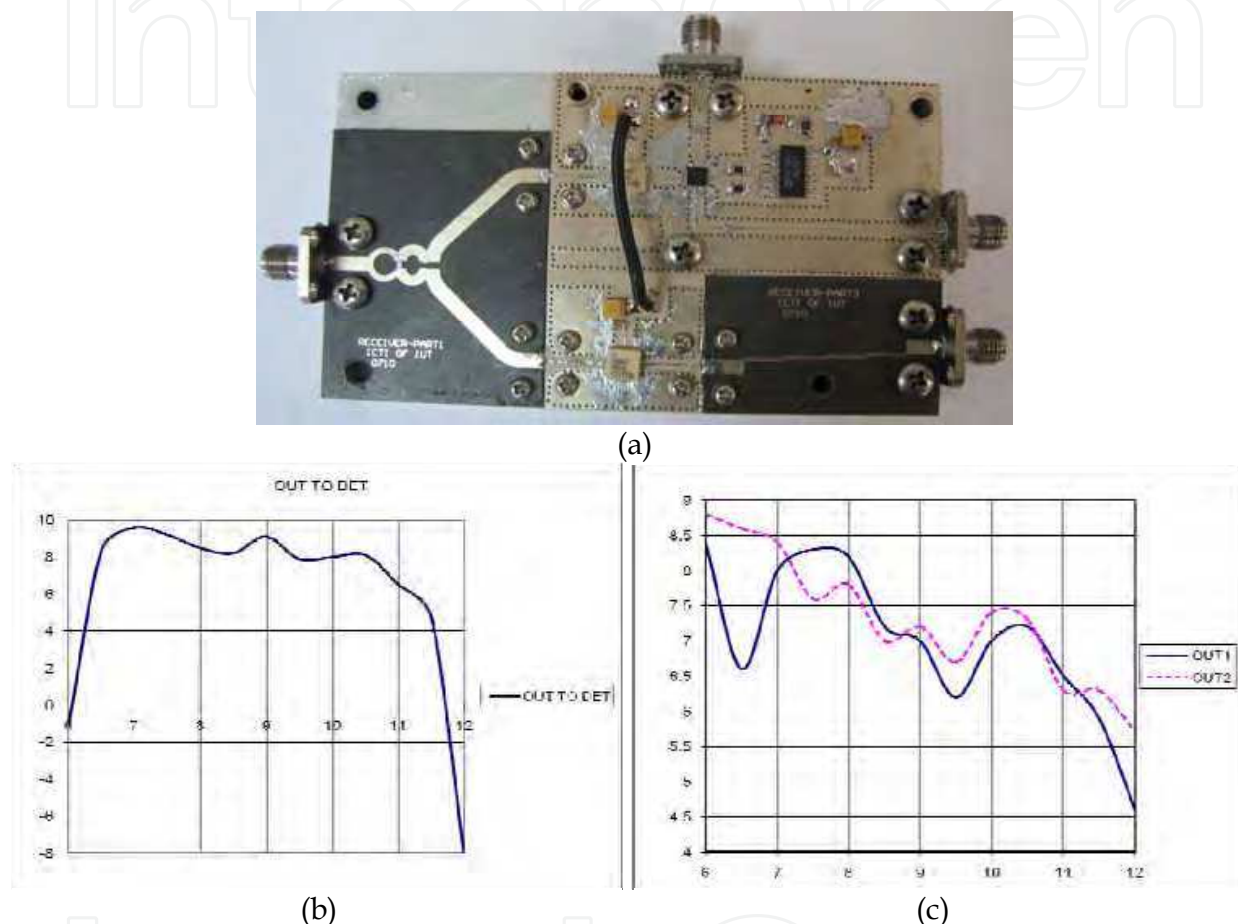(b)   (c)

Fig. 8. (a) Photograph of intermediate receiver block, Experimental result: (b) Insertion loss of output to detector vs. frequency (c) Insertion loss of output to delay and no delay path vs. frequency

3.5 The envelope detector

The output of intermediate receiver (out to detector) is the input of the envelope detector. The detector is used to detect the envelope of RF signal to make the video signal. The detector must have a very fast pulse response and wideband frequency response. ACTP1528N from *Advanced Control Components* is used as a detector.

3.6 The Selective delay section and circuit design

The intermediate receiver board output (output to delay path) is entered to the selective delay section. The selective delay section can make delay to RF signal from 0 to 1500 nsec by

100 nsec steps (the maximum delay can be increased, independently). In this design delay control commands (4bits) are entered to the decoder to make 16 bits commands (b0-b15) and to control the delay of each 100nsec delay block. The structure of 100 nsec delay block will be explained in the following.

The main problems to construct a wide band delay block with more than 10nsec delay are insertion loss and its high variation in overall frequency bandwidth. In this block, design and implementation of a wideband delay circuit in X-band are presented. All important specifications such as insertion loss and flatness in frequency response and free of high order effects in time domain have been solved in this section [Askari et al., 2008(b)].

A delay line is used to delay a signal by certain time while minimising the distortion caused by crosstalk, dispersion and loss. There are many applications for a delay line like phase shifter in phase array radars, pulse compression radars, calibration of microwave altimeter, and loop circuits in ECM circuits [Askari et al.,2008(b); Hohenwarter et al.,1993].

There are a few ways to delay a signal. One of them is Piezoelectric Transducer which converts electromagnetic energy to acoustic energy (and also reconverts acoustic energy back into electromagnetic energy after the energy is delayed in the acoustic crystal). Another way to delay a signal is a CPW transmission line with a superconductor. This can be used as a low loss ultra wide band delay line. To achieve a larger bandwidth, it has to be smaller in size to decrease the undesired effects of resonance frequencies [Hohenwarter et al.,1993; Wang et al.,2003]. Microstrip transmission lines are another way to produce small delay [Lijun et al.,2006] which have high loss and variation of loss over frequency so they can be used for delays less than 12nsec [Hohenwarter et al.,1993]. Like microstrip, coaxial cables are high loss delay lines, but they are better than microstrip or stripline because of less loss and variation of loss [Askari et al.,2008(b)]. It is difficult for coaxial cables and/or microstrip printed circuit board (PCB) delay lines to get a long delay whilst maintaining a small size and low insertion loss over a wide frequency band [Wang et al.,2003].

Fig. 9 shows a block diagram of a 100 nsec delay line which can make delay or cancel it by a TTL command. The goal of this design is achieving a long delay (100nsec) in X-band signal from 6GHz to 12GHz with frequency response variation less than 3dB over frequency bandwidth. It should have selectable delay, VSWR better than 2 and 0dB of overall gain. To achieve desired results, each part of this block diagram should have some specifications which are explained in the following.
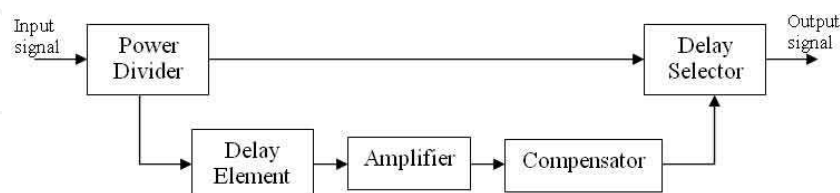

Fig.9. Block diagram of a 100 nsec delay line

- Divider

A wide band divider is necessary to select delay or not. For this purpose, a double stage compensated Wilkinson divider is designed and implemented on a *Rogers-5880* microstrip board that was explained completely in section 3-4.

- Delay Element

In this block, the final solution to make delay is a high precision 18GHz *Huber & Suhner* coaxial cable (S_04272_B). The signal delay of this cable is 4.1nsec/m; so to achieve 100nsec of delay, 24.4m length of it is required.

  • Compensator

Since 24.4m of cable makes a high insertion loss and approximately 8dB linear variation of insertion loss over the frequency bandwidth, a special amplification and structure is needed to compensate these effects. There are different methods to compensate the slope of a frequency response in a circuit. First of all, a lumped network of resistor, capacitor and inductor can be used as an equalizer [Fejzuli et al.,2006; Kurzrok,2004]. The most important problem of these networks is that achieving 8dB linear slope over almost 1-octave is not possible. The next method is to use the out band positive slope of a BPF. This design contains two microstrip lines which are joined together with two different widths and a stub between them. The simulation result of this design is good but the reflection of input and output (S11, S22) makes a mismatch for amplifiers and other parts of the total circuit [Askari et al.,2008(b)]. So, the next important goal in this part is to achieve an absorptive compensator. The last design is an unbalanced Wilkinson divider that is optimized in ADS to make an 8dB positive linear slope for S21 and to have S11 less than -7dB and S22 less than -5dB. Fig. 10-a shows the layout of this compensator in ADS on a *Rogers-5880* microstrip board and Fig. 10-b shows the simulation results of S11, S22 and S21.
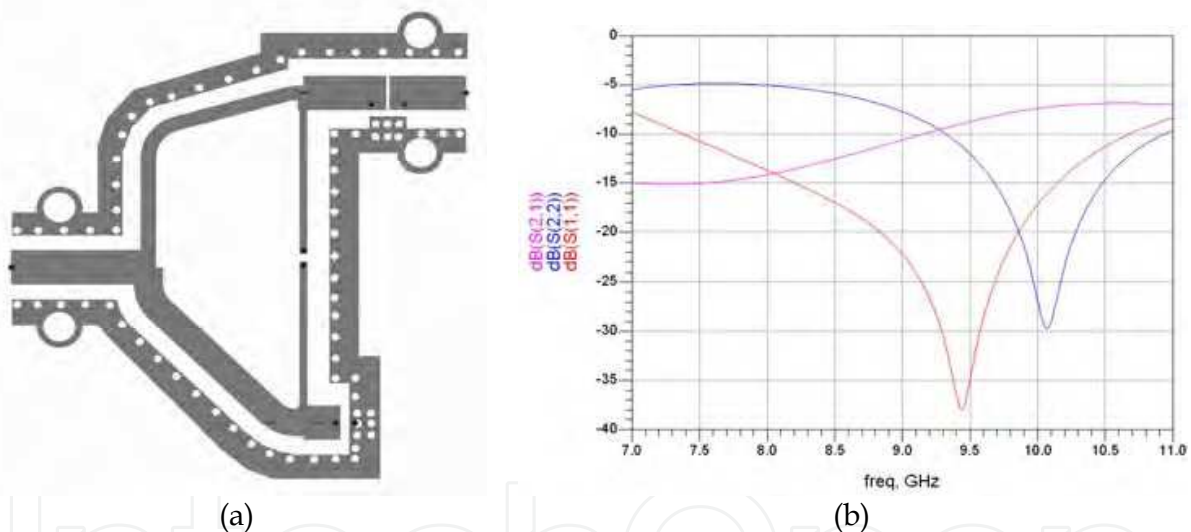

(a)   (b)

Fig. 10. (a) Compensator layout (b) Simulation results: S11, S22, S21

There are two 50ohm resistors for matching of port3 and isolation resistor consequently and a 3dB attenuator is used to improve S22 at the output.

  • Amplifiers

To compensate insertion loss of 24.4m cable and compensator, 36dB gain is necessary to achieve 0dB gain for this block. In this design, two types of MMIC are used. The first one is *Agilent Technology's* 6-18GHz MMIC, AMMP5618 and the next one is *Hittite's* 6-18GHz MMIC, HMC441LC3B.

After combining sub circuits together and optimizing by ADS simulation by considering undesired effects, the final structure is achieved. In the block diagram of Fig. 9, to terminate insertion loss of divider and *Hittite* switch (HMC547LP3) in the output, a 6dB attenuator and

an AMMP Amplifier are required. Except divider and compensator, other parts of block design are on *Rogers-6010* microstrip board.

All footprints, lines and ground planes of final design were simulated in EM simulator of ADS.

After implementing all parts together, the final circuit was achieved and tested. Fig. 11 shows a photo of circuit after mounting. All connectors for this circuit are SMA (stripline) type and the material of fixture is Aluminium. The final experimental result is a delay block with a 100nsec delay, 0dB compensated insertion loss and 3dB of flatness in frequency bandwidth of 7-11GHz and a very good time response without second and third order reflection effects in time domain.

Fig. 11. Photo of 100nsec compensated delay block without cable

To measure the delay of two paths, a pulse modulated RF signal is used and at the output, a detector (ACTP1528N) is used to detect the envelope of RF. Fig.12-a shows the delay of no delay path related to reference pulse (wave form no.1) and Fig.12-b shows the delay of delay path. A 31nsec common delay for both paths is because of gate delay of input switch control circuit so the individual delay is 100nsec. As it is shown in Fig. 12, there is no effect of second and third reflections in time response and a pure response is achieved. The complete discussion of this section has been described by [Askari et al., 2008(b)].
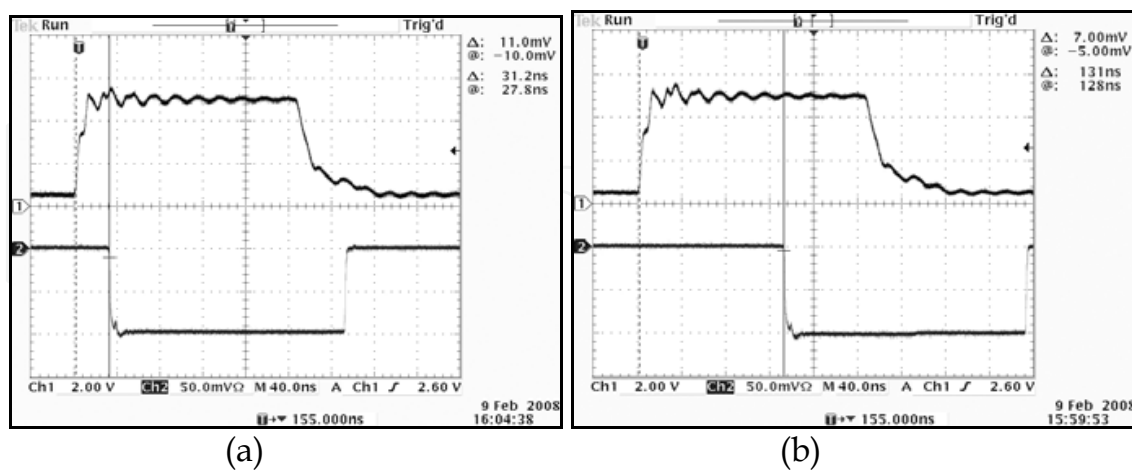

| (a) | (b) |

Fig. 12. Measurement of delay (a) No delay path (b) Delay path

3.7 The AGC section and circuit design

The intermediate receiver board output (output to no delay path) and the selective delay section output are entered to the AGC section and one of them is selected by the delay/no

delay TTL command. This section is used to produce two RF outputs. So, the divider is necessary to divide the selected signal to the detector path and driver path. The signal in the detector path is sent to the detector after amplifying to make the envelope of RF signal detect the probable error and/or to provide an automatic gain control feedback from the control and monitoring section. The signal to the driver path is sent to the amplifier and switch to make RF signal on/off by the TTL receiver switch command. A 6-bit receiver gain control command is used to control the output power variation from 0.5 to 31.5dB with 0.5dB step size.

All important specifications such as fault detector and AGC loop, have been solved in this section. In this design, variable attenuator, divider, amplifier (#3) and switch (#2) are used. The block diagram of AGC board is shown in fig. 13.
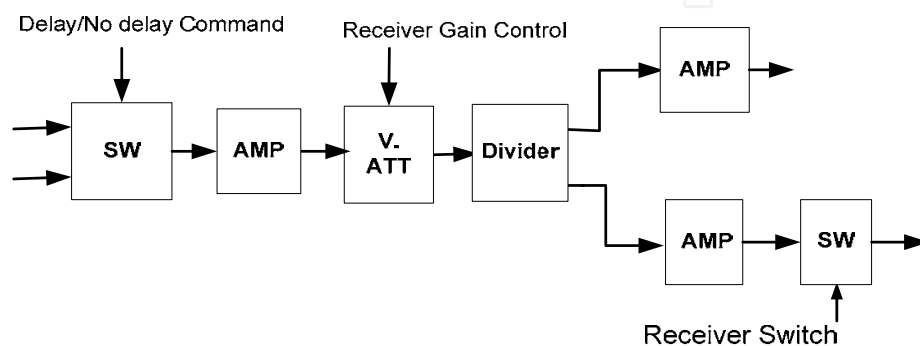

Fig. 13. AGC block diagram

The sub circuits' specifications of this block are mentioned below:

•   Switch (#1,#2) :

Switch #1 selects one of the RF inputs (delay / no delay) by a TTL command and switch #2 is used to make RF output to driver on/off by a receiver switch TTL command. two high speed switches should be used in the design of AGC section. HMC547LP3 is used as a switch that was explained completely in section 3-4.

•   variable attenuator :

To control and decrease input signal to 31.5 dB by 0.5 dB step the input signal is sent to the variable attenuator. HMC424LH5 is used as an attenuator that was explained completely in section 3-3.

•   divider :

A wide band divider is necessary to divide signal to the detector or driver path. For this purpose, a double stage compensated Wilkinson divider is used that was explained completely in section 3-4.

•   amplifier :

To increase the output signals power and to achieve the output signals to the desired power level, amplifiers are used in each path. The first one in the input path is *Hittite's* 6-18GHz MMIC, HMC441LC3B and the others in the output paths are *Agilent Technology's* 6-18GHz MMIC, AMMP5618. Amplifiers are simulated with Advanced Design System.

After combining sub circuits together and optimizing in ADS by considering undesired effects, the final structure is achieved. For feasibility of implementation, the divider section is implemented on a micro-strip laminate with lower permittivity and the other sections are implemented on a laminate with higher permittivity. The divider is on *Rogers-5880* and

other parts of block design are on *Rogers-6010* microstrip board. All footprints, lines and ground planes of final design were simulated in EM simulator of ADS.

After implementing all parts together, the final circuit was achieved and tested. Fig 14-a and 14-b show the experimental results of output to detector and output to driver, gain vs. frequency in different attenuation. The final experimental result is the AGC block with a 18dB gain in output to detector, -16 ~ +16 gain variation in output to driver and 3dB of flatness in frequency bandwidth of 6-11GHz.

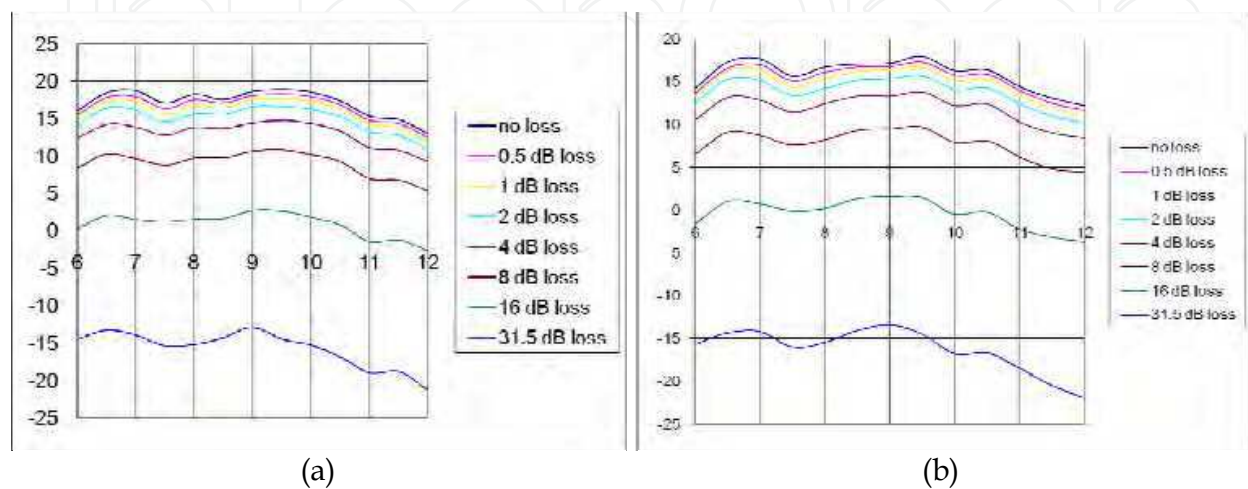(a)   (b)

Fig 14. Experimental result: (a) out to detector, gain vs. frequency in different attenuation (b) out to driver, gain vs. frequency in different attenuation

3.8 noise source

One type of favorite source signal is a white noise signal having a Gaussian PDF. Such a signal has a relatively flat signal spectrum density. White Gaussian noise generators can serve as useful test tools in solving engineering problems. Test and calibration of communication and electronics systems, cryptography and RADAR interfering are examples of noise generator applications. A few of the measurements that can be made with these sources are: Noise Equivalent Bandwidth, Amplitude Response and Impulse Response [Carlson, 2002].

Depending upon how the noise is employed, noise applications are somewhat arbitrarily clustered into many categories which were explained in introduction [Askari et al., 2008(a)].

In this section design and implementation of an X-band noise generator used in identifying the specifications of the communication and electronics systems are described. This noise generator has 4dB bandwidth of 5.5GHz (6-11.5GHz) and 60dB of ENR or -114dBm/HZ of noise density.

Due to internal noise of measurement systems and to overcome the noise floor of these systems for testing DUT, noise generators need ENR of about 60-70dB.

The noise-generator output can be viewed as a collection of sine waves separated by, say, 1-Hz. Each separated frequency "bin" has its own Gaussian amplitude and random phase with respect to all the others. So, the DUT is simultaneously receiving a collection or "ensemble" of input signals. As the spectrum analyzer frequency sweeps, it looks simultaneously at all of the DUT frequencies that fall within the spectrum analyzer's IF

noise bandwidth [Straw,2005].The general block diagram of the noise generator is shown in fig. 15.
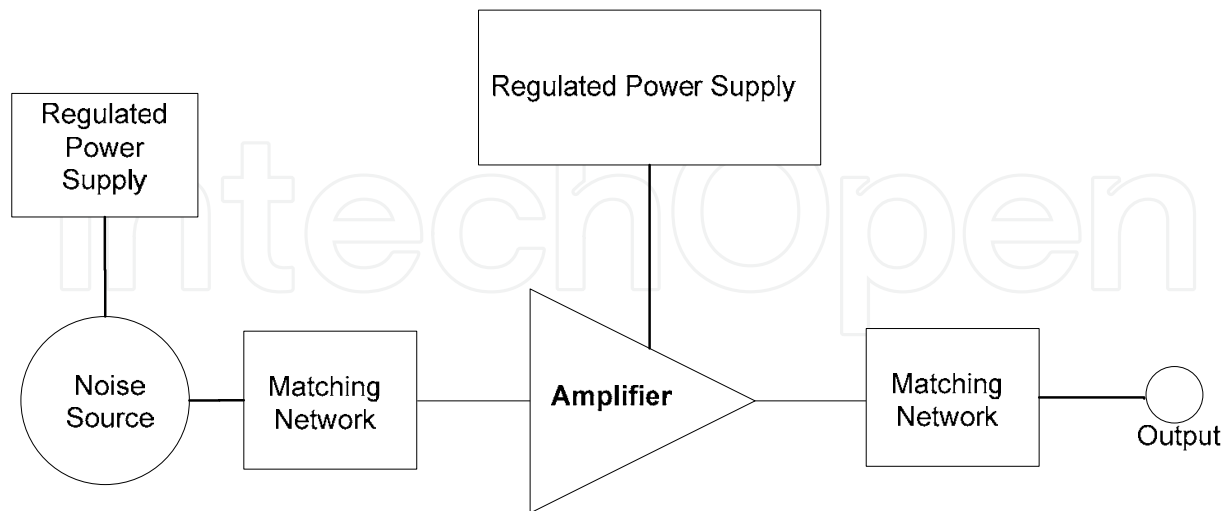

Fig. 15. Noise Generator Block Diagram

The elements of the block diagram are demonstrated in the following sections.

- Noise source

One method of generating white Gaussian noise is to amplify thermal noise in a resistor. The density of the thermal noise is -174dBm/Hz at room temperature. Amplifying the thermal noise to overcome the internal noise of measurement systems in a wide bandwidth isn't an easy problem [Carlson,2002; Motchenbacher & Connelly,1993].

The other method is to use a noise diode with ENR of about 25-35dB. Any Zener diode can be used as a source of noise. If, however, the source is to be calibrated and used for reliable measurements, avalanche diodes specially designed for this purpose are preferable by far. A good noise diode generates its noise through a carefully controlled bulk avalanche mechanism which exists throughout the PN junction, not merely at the junction surfaces where unstable and unreliable surface effects predominate due to local breakdown and impurity. A true noise diode has a very low flicker noise (1/f) effect and tends to create a uniform level of truly Gaussian noise over a wide band of frequencies. In order to maximize its bandwidth, the diode also has very low junction capacitance and lead capacitance [Straw, ,2005]. Insensitivity of power value and frequency response of noise generator due to variation of its parameters such as dynamic resistor of diode, breakdown current of zener diode, load pulling, source pushing and matching network are very necessary in order to design a noise generator and its power supply.

There is noise diode up to 110GHz made by *NOISE/COM*. In this project, the NOISEWAVE NW401 diode is used. It is rated for use from 10MHz to 18GHz, if appropriate construction methods are followed.

In order to maximize the flatness of frequency response, noise source construction methods should aim for Microwave circuit lead length as close to zero as possible as well as minimum inductance in the ground path and the coupling capacitors. The power-supply voltage must be clean, well bypassed and set accurately [Straw,2005].

- amplifier

As mentioned before, noise generators need high ENR (60-70dB) to overcome the noise floor of the measurement instruments. Based on Noise Diode's ENR, up to 40-50dB amplification is needed over the wide bandwidth. Four stage amplifiers are used in this design. MMIC amplifiers (*Avago Technologies* AMMP-5618) are used in each stage. Amplifiers are simulated with Advanced Design System. Matching network and filter are optimized to flatten the gain and decrease the input and output mismatch compared to 50Ω over the desired bandwidth. Also, sensitivity of matching and filter due to dimension variation of filter and matching network are reviewed.

- filter

A third order Chebychev filter with 0.5dB ripple and 9GHz center frequency and 5GHz bandwidth is designed to maximize the output noise density over the desired bandwidth. The filter design is explained completely in section 3-4. For feasibility of implementation based on amplifier selection, the filter section of noise generator is implemented on a micro-strip laminate with lower permittivity and the other sections are implemented on a laminate with higher permittivity.

After prototype design, the total response including amplifiers matching network and filter response are optimized for flat gain and lower return loss.

In order to study the sensitivity of the overall response, variations of dimensions are considered with ±25% tolerances due to variation in implementation process and environmental conditions. The effect of the tolerances in simulation is shown in fig. 16-a and the photo of the implemented noise generator is shown in fig. 16-b.

Moreover, sensitivity simulation was executed for any element in filter and matching network. Although, not all sections of noise generator are optimized because exact model of noise diode doesn't exist.Wideband and narrowband Experimental results of noise generator are shown in fig. 17-a and fig. 17-b. All results are measured by Anritsu MS2665C Spectrum Analyzer.
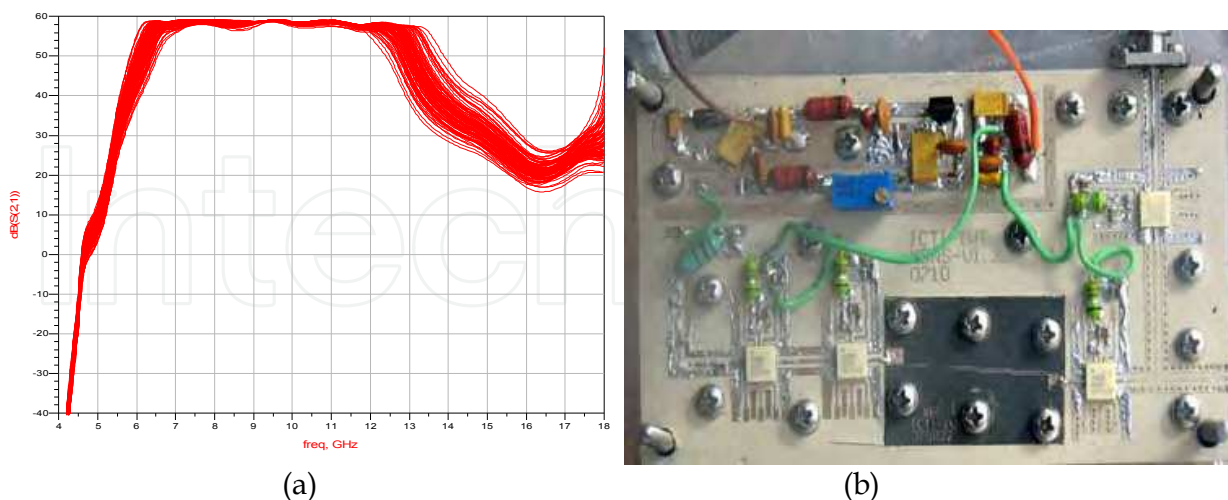

(a)   (b)

Fig. 16. (a) Effect of implementation tolerances (b) Photo of the implemented noise generator
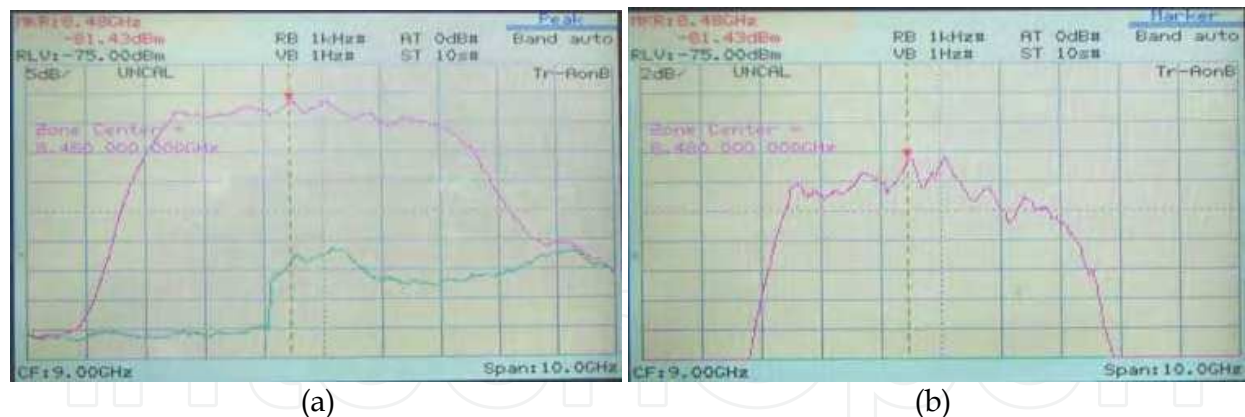
| (a) | (b) |

Fig. 17. (a) Experimental result in wideband comparing to spectrum noise floor (b) Experimental result with more detail

3.9 The X-band Amplifier1, 2, 3

Agilent Technology's 6-18GHz MMIC, AMMP5618 is used as an amplifier to amplify the noise signal power. 3-stage amplifier with AMMP5618 is used in x-band amplifier1 and x-band amplifier2 blocks. 1-stage amplifier with AMMP5618 is used in x-band amplifier3. After simulating and optimizing, the experimental results of 1-stage amplifier gain vs. frequency at -10dBm input power and 3-stage amplifier gain vs. frequency at -40dBm input power is shown in fig. 18.
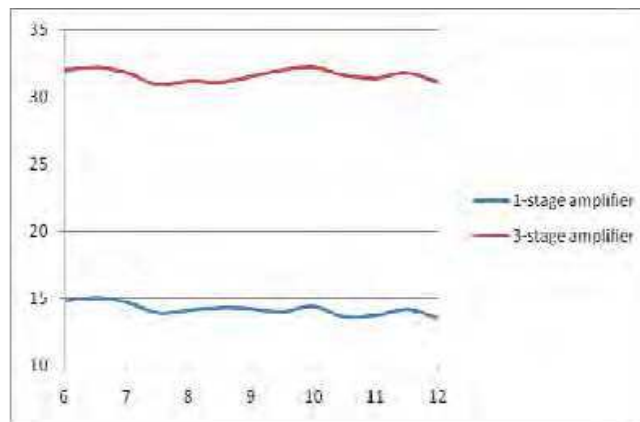

Fig. 18. Gain vs. frequency in 1-stage and 3-stage amplifier

3.10 The Wide/Narrow switch

The amplifier1 output is entered to the wide/narrow selector switch to select the direct path (wide band White Gaussian Noise) or the YIG path (narrow band White Gaussian Noise) by W/N command.
HMC547LP3 is selected as a fast switch that was explained completely in section 3-4.

3.11 YIG Filter & Driver

The output of wide/narrow switch block is entered to the YIG filter block. M979 from *OMNIYIG* is used as a YIG filter. According to the datasheet and experimental results, the specifications of this component are represented in table 3.

Frequency Range (GHZ)	Part Number	Insertion Loss (dB)	Bandwidth @ 3dB (MHz) (Experimental)	Passband Ripple (dB) (Experimental)	Freq. Drift 0 to 60C (MHZ)	OFF RESONANCE ISOLATION (dB) (Experimental)
2-18	M979	6.5	25-60	2.5	13	100

Table 3. Specifications of M979 according to the datasheet

The 6-bit frequency control command is converted to the analog command to control the center frequency of 6~12 GHZ. The photograph of YIG filter and its driver are shown in fig. 19.

Fig. 19. Photograph of YIG filter and driver

3.12 Wide/Narrow Switch and Step attenuator
The narrow and wide white Gaussian noise signals are entered to this block. This section is used to select one of the signals and control the output power gain variation from 0.5-31.5 dB with 0.5dB step. In this design, switch, variable attenuator, amplifier and 3 dB attenuator are used. The block diagram of Wide/Narrow Switch and Step attenuator board is shown in fig. 20.
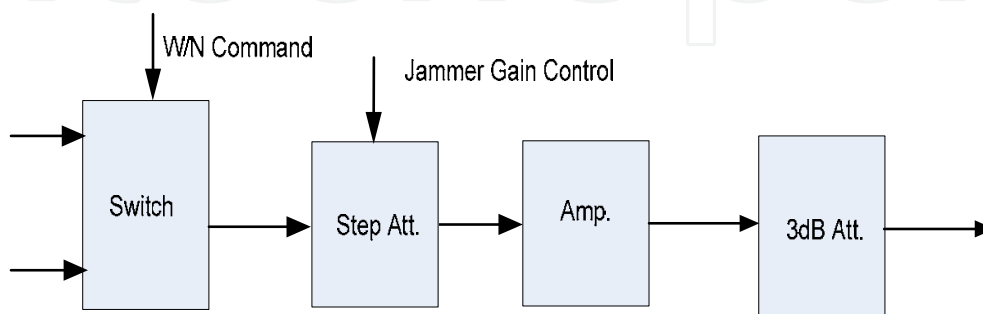

Fig. 20. Wide/Narrow selector Switch and Step attenuator block diagram

After combining sub circuits together and doing simulation and optimization by considering undesired effects, the final structure is achieved. All parts of block design are on *Rogers-6010* microstrip board. All footprints, lines and ground planes of final design were simulated in EM simulator of ADS.

After implementing all parts together, the final circuit was achieved and tested. Fig. 21-a and fig. 21-b show the experimental results gain in different attenuation and isolation vs. frequency. The final experimental result is a Wide / Narrow Switch and Step attenuator block with a 3dB gain and 3dB of flatness in frequency bandwidth of 6-11.5GHz.
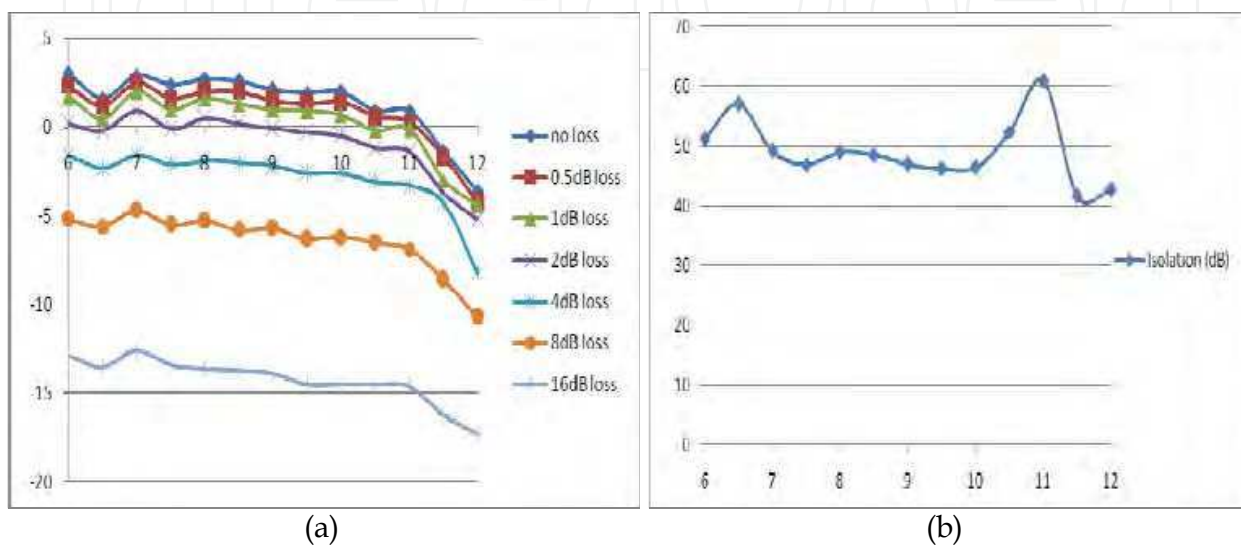

<table>
<tr><td>(a)</td><td>(b)</td></tr>
</table>

Fig. 21. (a) Gain vs. freq. in different attenuation, (b) Isolation vs freq.

3.13 White Gaussian Noise switch

To make RF output to driver with or without WGN a high speed and remarkable on/off isolation switch should be used, HMC547LP3 is used as a switch that was explained completely in section 3-10.

3.14 RF Combiner

The input RF signals from receiver section and WGN can be entered together or alone into the RF combiner section. The Combiner is a circuit that combines the input signals with minimum loss. R2SC-2.0-18.0-sf-1W-L from *Raditek* is used as a combiner. According to the datasheet, the specifications of this component are represented in table 4. The picture of combiner is shown in fig. 22.

Freq. Range (GHZ)	Part Number	Max Insertion Loss (dB)	Isolation (dB)	VSWR In	VSWR Out	Amp. Balance (dB)	Ph. Ang.	Total Power (W)
2-18	R2SC-2.0-18.0-sf 1W-L	3.9	17	1.4	1.4	<+/-0.3	<+/-3^0	1

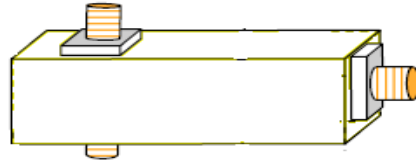Table 4. Specifications of R2SC-2.0-18.0-sf 1W-L according to the datasheet

Fig. 22. Picture of the combiner

3.15 0.5W amplifier

The combiner signal output is entered to the 0.5W amplifier section. This section is used to produce about 0.5w RF output. So, the 0.5W amplifier is necessary in the final RF path and the pre amplifier must be used to produce the sufficient input power. In this design, a pre amp, a 0.5W amplifier, a bias T network and a coupler are used. The block diagram of 0.5W amplifier board is shown in fig 23.
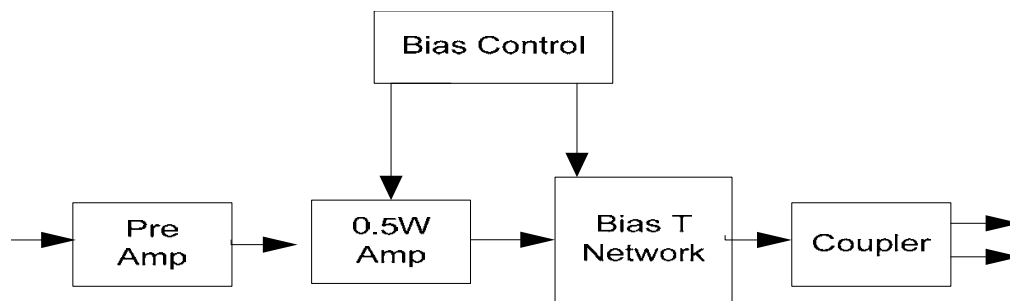

Fig. 23. 0.5W amplifier block diagram

The sub circuits' specifications of this board are mentioned below:

- Pre Amp :

To produce the sufficient input power for 0.5W amplifier the pre amplifier is used. In this design, *Hittite's* 6-18GHz MMIC, HMC441LC3B with 14dB gain and 21.5dB output at 1dB compression point is used as a pre amplifier.

- 0.5W Amp :

To have 0.5w RF output the 0.5W amplifier is used. In this design, *iterra Hittite's* 2-20GHz, iT2008K is used as a 0.5W amplifier.

- Bias Tee Network :

A single-sided butterfly combined with a double-sided ultra wide band butterfly bias tee is used to bias the amplifier that is the broadband model of bias tee [Hong&Lancaster,2001]. After optimizing in ADS by considering undesired effects, the final structure is **Coupler :**

An ultra wide band 15 dB coupler is used to produce a sample RF output to detect probable error for control section. This coupler must have flat insertion loss response and remarkable return loss and 15dB coupling factor in the frequency bandwidth 6~12GHz. After optimizing in ADS by considering undesired effects, the final structure is achieved.

Pre amp is on *Rogers-5880* and the other parts of block design are on *Rogers-6010* microstrip board. The photo of implemented 0.5W amplifier is shown in fig. 24-a and the experimental test result 1dB comp. output vs. frequency is shown in fig. 24-b. The final experimental result is a 0.5W amplifier block with a 25dB output power at 1dB comp. point and 3dB of flatness in frequency bandwidth of 6-13GHz.
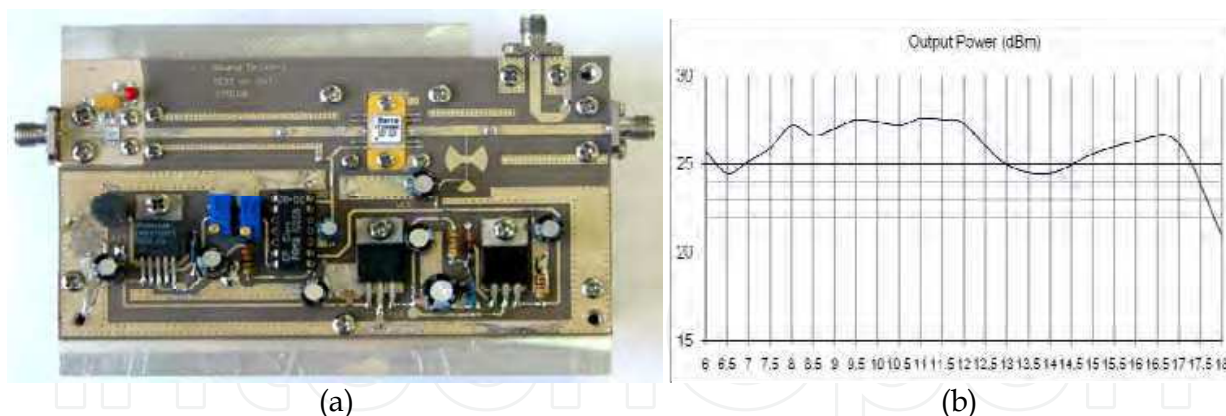
<div align="center">(a)   (b)</div>

Fig. 24. (a) photograph of 0.5W amplifier (b) 1dB comp. output vs. frequency

4. Overall experimental test results

Overall system in different modes is tested and the results are given in the following:

4.1 Transciver in CW mode
The output power levels (dBm) of different blocks in the RF path and the final output (0.5W amp output) and video output (mV) vs. frequency bandwidth are shown in fig. 25.
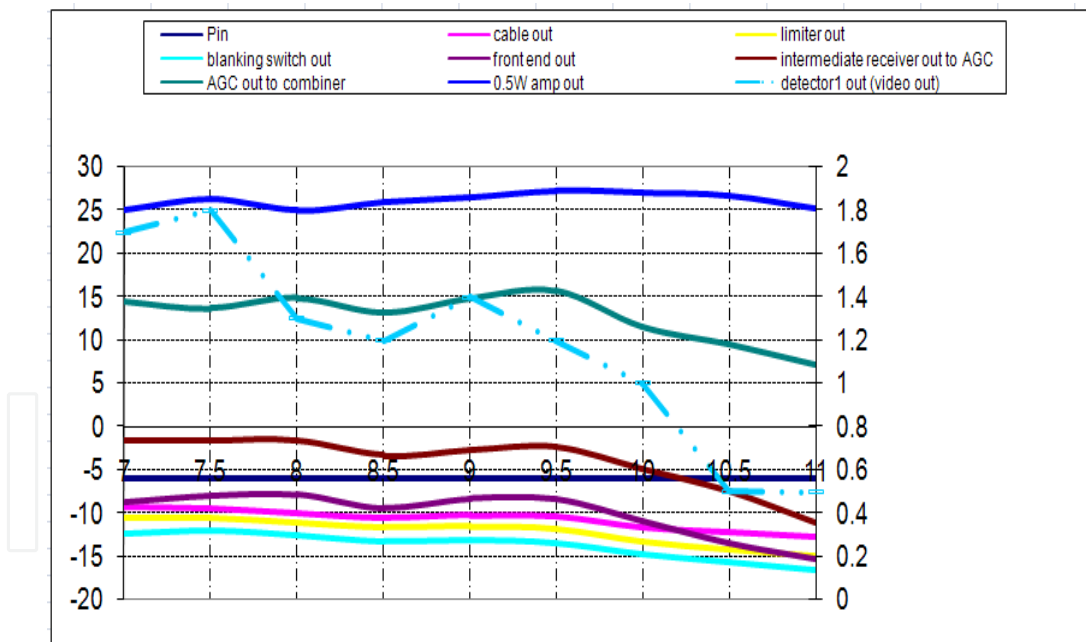

Fig. 25. Output power of different blocks in the RF path and video output vs. frequency

4.2 Transciver in pulse mode
The video output of the receiver and driver sections together in the delay mode is shown in fig. 26. In this fig. the receiver input RF signal is modulated with an RF pulse modulator and the envelope of the driver video output after 100nsec delays is depicted.

Fig. 26. Modulating pulse and video out after 100nsec delay

4.3 Wideband White Gaussian Noise mode

The output of x-band amplifier1 in the Wideband White Gaussian Noise mode path is measured by the spectrum analyzer that is shown in fig. 27. 3dB bandwidth of the noise is approximately 5GHz.

Fig. 27. The experimental results of wide band WGN in output of x-band amplifier1 on the spectrum analyser.

The outputs of noise source, x-band amplifier1, Wide/narrow switch and step attenuator and 0.5W amp are measured by the power meter and the results are given in table 6.

Noise source	-21 dBm
x-band amp1	+8 dBm
Wide/narrow switch and step att.	+4 dBm
0.5W amp	+25.8 dBm

Table 5. Power levels at different block outputs

4.4 Narrowband White Gaussian Noise mode

The output of wide/narrow switch and step att. in narrowband noise selection at two typical center frequency 7GHz and 9.5GHz is measured by the spectrum analyzer that is shown in fig. 28-a and 28-b. 3dB bandwidth of the noise is approximately 40MHz.

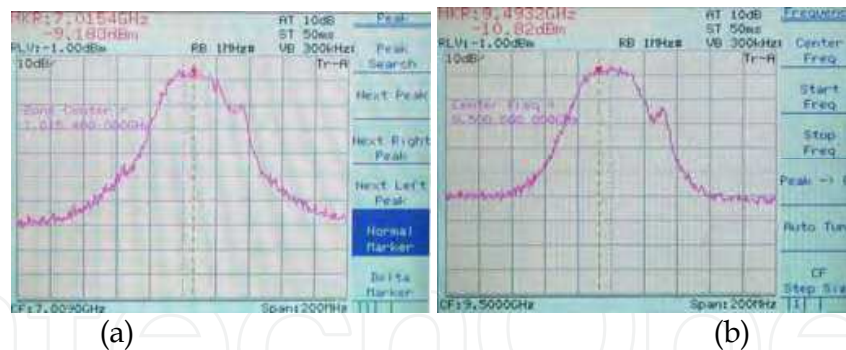(a)   (b)

Fig. 28. The experimental results of narrowband WGN in output of wide/narrow switch and step att. (a) At 7 GHz (b) At 9.5 GHz

The outputs of YIG filter, x-band amplifier2, Wide/narrow switch and step att. and 0.5W amp are measured by the power meter and the results are given in table 6.

YIG Filter	-28dBm
x-band amp2	+5dBm
Wide/narrow switch and step att.	+4dBm
0.5W amp	+25.5dBm

Table 6. Power levels at different block outputs

5. Technical guidelines

There are lots of technical points of view for everyone who is interested in microwave research, especially practical project. In this section some of the most important technical guidelines in transitions, implementations and assembly and test points in x-band are given.

5.1 Transitions

One of the most important effects to decrease the band widths is transition. A transition is an interconnection between two different transmission lines or components that possesses low insertion loss and high return loss. These characteristics can be achieved only through careful matching of the impedances and electromagnetic fields of the two transmission lines. The designs of the signal and ground current paths through a transition are also critical. For a transition to function properly, these paths must often be continuous, in close proximity to suppress radiation, and as short and closely matched in length as possible. Additionally, a good transition should be easy to fabricate, mechanically robust, and insensitive to ambient temperature variations. In this project there are lots of transitions which some of the final results are discussed in the following.

The connection of connector to the microstrip board and a line with 0.58 mm width and 5mm length via the Aluminum box is simulated in HFSS simulator and the best result is obtained in the diameter hole of 2.4mm. The simulation results are shown in fig. 29-a and 29-b and 29-c.

- SMA connectors of Stripline type are selected to be completely tangent with the fixture.

- The connector is connected to the fixture by a 3-mm tapping screw. Through all the stages care should be taken to trim the bulge created at the edge of the hole after tapping on the fixture by a 5- or 6-mm drill bit.

- For the preparation of the connector, the edge of its nipple is broken in the beginning, but a little solder is placed on it and then the back of the connector (the same soldered side) is smoothed with soft sandpaper so that the solder knob on the nipple does not prevent the correct connection of the connector.

- To solder the connector to the line, it is recommended that a little solder be placed at the end of the line, so that after complete connection of the connector by a screw the connection is made by one touch of a 450^0C hot soldering iron over nipple connection.

- with regard to the simulations made in HFSS for the connection of two transmission lines of boards, care should be taken to cover the connection of the two lines (on the two boards) with a little solder and care should also be taken to prevent the formation of any sharp point or crack in its physical shape and the two lines with two widths be connected together in a 3-D taper shape.

- Another method for the connection of the two boards is the use of a 50Ω line separated from a 10.2 board in a bridge manner, but fully stuck to the board.

-Another transition is connections between microstrip transmission lines to the IC pins, for this connection ultra wide band tapering is needed. The best transition is obtained by using microstrip laminate with greater permittivity and the minimum size of tapers from the transmission lines to the IC pins. (In this project *Rogers-6010* microstrip board is used for implementing of ICs).

-Also after simulating the best results of transitions between the capacitors pins and transmission lines are given at 1mm gap and the best result of coupling capacitor value is approximately 1.5pF (from the *Johanson Technology*, with 402 footprints) and also the best results of distance between coupling capacitors and IC pins, In/Out is approximately λ /4.

(a)

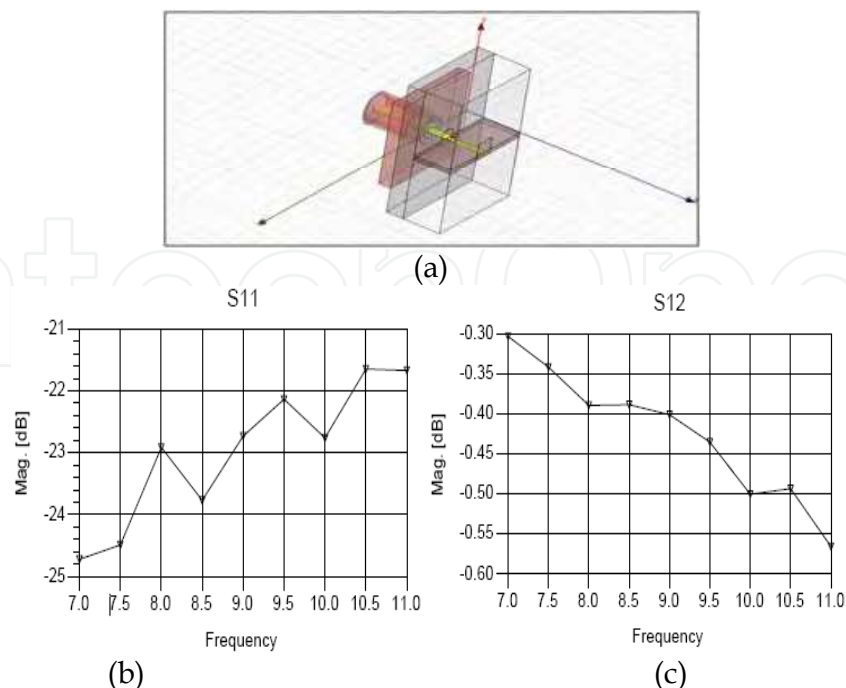(b)   (c)

Fig. 29. (a) HFSS structure of transition between connector to the microstrip board and line via the hole with 2.4mm diameter and simulation results (b) Return loss (c) Insertion loss

5.2 Implementation

- Simulation and experimental results show that the fixture is better than the box for implementing boards in x-band frequency and the fixture in use is made from Aluminum with fully polished surfaces.

- Install the board on the fixture by 3-mm tapping screws. Through all the stages, care should be taken that after tapping on the fixture, the edge of the hole bulges a little which should be trimmed by a 5-mm or 6-mm drill bit.

- Placing two screws at the two sides of each line connected to the connector is a must. The edges of these screws from the transmission line and the edge of the board are 1.5mm and 2.5mm, respectively.

- At the connection of the two 2.2 and 10.2 boards, each is screwed to the fixture by two 2-mm tap screws. The distance of the 2-mm screws from this point to the transmission line and to the side of the board is 1.5mm.

- The size of the fixture should be exactly equal to the total of ε r=10.2 and ε r=2.2 boards.

- A box with the same length and width as the fixture for being placed on the fixture should be designed in a manner that its top has the least height with a view to elements and absorbent.

- using absorbent is very useful to reject unwanted reflections and radiations.

- The wall of the box at the connection of the connector nipple to the line on the board should be vacant as much as the size of a semi-circle with a diameter of 7mm.

5.3 IC assembly

- For mounting the ESD sensitive ICs on the board, care should be taken to use ESD bracelets connected to a large metal plate on which the board is placed. Pincer and needle should be insulated and a special soldering iron be used. In spite of observing all these tips avoid touching the IC pins.

- First, the ground plate and the pins under the IC are coated with a thin layer of tin in a manner that no coarseness is felt on the surface.

- Fill all the holes of the ground under the IC over the board with solder paste by a needle in a manner that the solder paste just covers inside of the holes and not the surface of the ground to produce coarseness.

- With regard to the shaking of the board (to avoid displacement of the IC), the IC should be placed on the desired points precisely then the background under the IC from the back of the board should be heated about 10~20 sec so that smoke rises from under the IC. After rechecking the accuracy of placement, the IC ground should be checked for it firm connection (by shaking the IC with a pincer). The good connection of background is very important in ultra wide band frequency response.

- Then by placing 0.3 mm of tin by a 350~ 400 soldering iron on the footprint beside the IC and pushing it under the IC with the use of a fluxpen, the rest of the pins are mounted.

- After mounting, first check all the pins from the sides of the IC by at least by a magnifying glass and then spray clean the board to avoid stray capacitances.

- Finally the board should be placed upside down on a metal plate and pressed at the two sides of IC. Then the ground behind the IC is heated for 3 to 4 seconds by a 450⁰C soldering iron once again. The use of fluxpen in this stage produces better results.

5.5. Other points

- All simulations in ADS2005 have been done in RF enable mode, also in all simulations in edge of the boards the single ports, and in the middle of the boards, internal ports, have the best coincidence with the experimental results.
- Gnd region around the board and RF path make better isolation and better power ripple in the frequency band. Connection to the bottom of the board in gnd region is made by the vias with 1mm distance from each other.
- Always high precision cable and connectors with good reflection should be used and if a cable or connector is employed in the test, the effect of their drop should be taken into consideration.
- As much as possible, use a connector instead of a cable for testing.

6. Conclusion

In this chapter design and implementation of a practical reconfigurable communication system including an additive ultra wide band white Gaussian noise and delay lines in X-band from 6 to 12 GHz with other necessary microwave parts as the test bed were presented. The challenges that affect the design of a custom CW/pulsed UWB architecture were discussed, also design and implementation procedures of all microwave parts such as ultra wideband amplifiers, dividers, switches, drivers, gain controllers, generators, filters, delay components, bias tee, transitions and etcetera were presented. In the feature works, extending the band width from one octave to one decade has been considered.

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