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Improving Performance and Reliability of MOS Devices using Deuterium Implantation

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1. Introduction

Our advancing information network society is based on various kinds of digital communication systems in which versatile silicon integrated circuits (ICs) are indispensable key components. For the next-generation networking systems, there is need for higher packing density, higher quality and higher speed of ICs. Much effort is needed to improve the quality of thin silicon dioxide (SiO_2) used in submicron metal-oxide-semiconductor (MOS) field-effect transistors (FETs) in ICs. Since MOSFETs with thermal SiO_2 were developed in 1960, SiO_2 has been widely used as a gate insulator in MOSFETs and has played an important role in rapidly advancing IC development.

The quality of the gate insulator or gate oxide is closely related to the control of driving current, which is one of the most important factors for the MOS device. From this point of view, the practical minimum value of gate oxide thickness is below 2 nm at present, and at the same time, defect-free oxide must be prepared for both gate oxide and inter-gate oxide. Many kinds of contaminations from various processes and electrical-stressed-induced-damage on SiO_2 and the Si- SiO_2 interface must be extensively examined and removed.

Progressive silicon complementary MOS (CMOS) IC technologies are also based on reductions in the channel lengths of MOSFETs as well as on reductions in the gate oxide thickness. The reduction in the channel lengths leads to an increase in hot electron generation (for n-channel MOSFETs) owing to an increase in the electric field applied to the channel. The reduction in the gate-oxide film thickness results in an increase in the electric field applied to the thin gate-oxide films. Hot electron generation in short channel MOSFETs is followed by electron trapping in gate oxides on the silicon substrates. The electron trapping in gate oxides is the principal cause of instability for short channel MOSFETs, and electron traps in as-grown oxides need to be studied extensively. At any rate, improvement in the quality and reliability of thin SiO_2 is one of the most important concerns for next-generation MOS IC development.

The central theme of this work is to characterize the electrical reliability of MOS devices related to the nature of thin SiO_2 film. This monograph deals with hydrogen or deuterium process employed in fabrication to improve MOS device's reliability. The process of post-metallization anneal of the wafers at a low temperatures in hydrogen ambient is critical to CMOS fabrication technology to improve MOS device function by passivating the otherwise

electrically active interface traps, but it sets the stage for subsequent hydrogen-related degradation. Recently, an alternative process during which the interface traps are passivated by deuterium instead of hydrogen was demonstrated. This phenomenon can be understood as a kinetic isotope effect. The chemical reaction rates involving the heavier isotopes are reduced, and consequently, under the electrical stress, bonds to deuterium are more difficult to break than bonds to hydrogen. However, it is difficult to identify whether the deuterium could passivate the whole silicon dangling bonds along the gate length. Deuterium diffusion takes place primarily through the silicon oxide (SiO_2) in the MOS system because of the limited permeability of bulk Si, metal, and even poly silicon to deuterium. In the case of large scale ICs, therefore, the ability of deuterium to diffuse within the very thin gate oxide layer may be severely impeded, impacting the large-area devices.

2. Gate Oxide Reliability in MOS System

The microelectronics industry, including the internet and the telecommunications revolutions, owes its success largely to the existence of the thermal oxide of silicon, i.e., silicon dioxide (SiO_2). A thin layer of SiO_2 forms the insulating layer between the control "gate" and conducting "channel" of the transistors used in modern integrated circuits. As circuits are made more dense, all the dimensions of the transistors are reduced ("scaled") correspondingly, so that nowadays the SiO_2 layer thickness is 2 nm or less, and the reliability of such ultrathin oxide layers has become a major concern for continued scaling.

The reliability of SiO_2 , i.e., the ability of thin film of this material to retain its insulating properties while subjected to high electric fields for many years, has always been an important issue and has been the subject of numerous publications over the last 43 years, since the realization that SiO_2 could be used as an insulating and passivating layer in silicon-based transistors. Oxide reliability and the experimental methods for accelerated testing have been the subject of earlier review papers.

For the relatively thick (> 10 nm) oxides used in earlier technologies, the breakdown mechanisms are actually fairly complex, and the detailed understanding of the intrinsic reliability has only come about in the more recent past. When a voltage is applied across the gate oxide, an electron current will flow if the gate voltage (V_g) is high enough and/or the oxide is thin enough. For thick oxides, the current is controlled by Fowler-Nordheim tunneling, while for thin oxides (≤ 3 nm) at voltages below about 3 V (corresponding to the barrier height between n-type silicon and the SiO_2) the current is due to direct quantum-mechanical tunneling. The electrons flowing across the oxide will trigger several processes depending on their energy. The defect generation mechanism at the lower energy process, which dominates at the voltages where present MOSFETs operation, is attributed to hydrogen release from the anode with a threshold gate voltage of about 5 V. As a consequence of the reaction of the released mobile hydrogen, a variety of defects such as electron traps, interface states, positively charged donor-like states, etc., gradually build up to the point where the oxide breaks down destructively.

Low temperature post-metal anneal in hydrogen ambient is imperative from a fabrication standpoint since silicon dangling bonds at the Si/ SiO_2 interface are electrically active and lead to the reduction of channel conductance. Electron spin resonance (ESR) on deep-submicron transistor Si/ SiO_2 interface has in fact identified in the stress-induced P_b defects a spread in the distance between the silicon atom at which the defect is localized and its

nearest neighbors, which would correspond to a spread in the Si-H bond energy. Fig. 1. represents P_b defects at the (100) interface. Such defects appear as the source of interface trapped charges. Thermal activation of hydrogen from the P_b defect at the (111) interface has confirmed a spread in the bond energies of 0.08eV, and the spread of the energies of P_b defects at the (100) interface deems to be twice of that. The passivation process of P_b defects is described by the equation



where P_bH is the passivated dangling bond.

In the case of bulk oxide defects generation, a model considers the interaction of the applied electric field E with the dipole moments associated with oxygen vacancies (weak Si-Si bonds) in SiO_2 . The oxygen vacancies, known as E' centers, generate dominant hole traps during the electrical operation. Fig. 2 shows the E' defect in SiO_2 bulk system. The activation energy required for bond breakage is lowered by the dipolar energy, leading to a quantitative prediction for the field dependence of the activation energy for dielectric breakdown. Allowing for a distribution of energies of the weak bonds could account for a wide range of observations of the temperature- and field-dependence of SiO_2 breakdown times, since the defect which dominates the breakdown process may change depending on stress conditions.

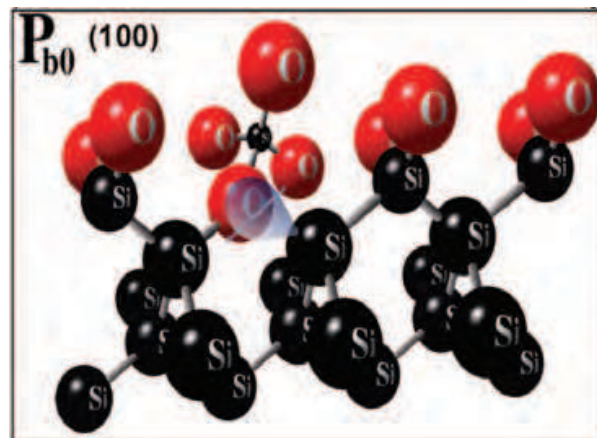


Fig. 1. Oxygen vacancy, P_b center, at the Si/ SiO_2 interface.

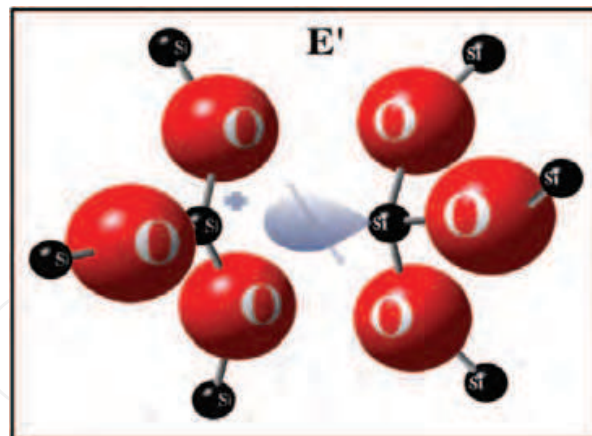


Fig. 2. Oxygen vacancy, E' center, in SiO₂ bulk.

2.1 Hydrogen in Silicon and Silicon Dioxide

The introduction of hydrogen into silicon-based materials is an important step for the fabrication of many electronic devices. Besides hydrogen's ability to relieve network strain and passivate shallow donor states, hydrogen can also passivate electrically active midgap states. The latter are commonly associated with silicon dangling bonds and are found at surfaces, grain boundaries, interfaces, and in bulk silicon. Incorporation of hydrogen during the growth of amorphous silicon (a-Si) films is essential for producing devices such as solar cells. Also, device quality silicon-based transistors are annealed in a hydrogen-rich environment on order to passivate defects at the Si-SiO₂ interface.

A fundamental understanding of the Si-H dissociation process is essential for analyzing and controlling these phenomena. The present calculations build on earlier theoretical work which found that hydrogen interacts strongly with impurities as well as with defects in bulk crystalline and the dangling bond, where Si-H bonds are formed with bond strengths of up to 3.6 eV, similar to those found in silane. Although the energy to take a neutral hydrogen atom from an isolated dangling-bond site to free space is 3.6 eV, the energy to move the hydrogen into a bulk interstitial site is only about 2.5 eV.

Hydrogen exists in abundant quantities in bound forms in the oxide, the polysilicon gate, and the metal interconnects as a result of manufacturing process. Intrinsic defects generate electron-hole pairs and holes react with the bound forms to release mobile hydrogen. Hydrogen can migrate through the oxide as a neutral atom, as a positive ion (proton), or in other form, and reaches at the Si-SiO₂ interface where it reacts and new defects are generated. If the interface is first dry annealed, a process that is known to depassivate defects such as dangling bonds, introduction of H passivates the defects via the reaction



where X stands for a dangling bond and SiH stands for a Si-H bond. If the interface contains H-passivated dangling bonds (SiH), introduction of H may depassivate some of them through the reaction



During device operation electronic defects are created that limit device lifetimes, and hydrogen has been observed to be involved in this degradation process. For instance, hydrogen is known to play a role during hot-electron degradation in silicon-based transistors, as well as during light-induced degradation in a-Si:H solar cells. The created defects are isolated and immobile. Hydrogen desorption from silicon dangling bonds is usually considered to be the dominant mechanism by which interface or bulk defects are created.

There is compelling evidence, however, that introduction of H induces additional defects at or near the interface. These defects can function as oxide traps, interface traps or border traps. Theoretical calculations so far focused on the behavior of hydrogen in bulk SiO₂. A great deal has been learned about the bonding of H in nominally perfect SiO₂ in different charge states and about cracking of H₂ molecules. Theoretical investigations of H at the Si-SiO₂ interface have been lacking, however, because of the enormous complexity of the problem.

2.2. Deuterium Effect in Degradation of MOS Devices

A large body of literature exists on hot electron and hydrogen related degradation of MOS devices. Degradation has been identified to be due to trap generation in the oxide as well as at the Si-SiO₂ interface and the interface to polysilicon gates. While numerous experimental facts of the degradation have found a large variety of explanations, the actual mechanism of the damage has only been cursorily addressed. For damage within the oxide, electron hole defect recombination and the corresponding energy release have been identified as the likely cause. At the Si-SiO₂ interface and the interface with polysilicon it is the release of hydrogen and the creation of dangling bonds that have been identified as causes of MOS device's degradation. However, the actual mechanism as to how the energy of electron-hole recombination or the energy of hot electrons (or holes) creates the defect has not been fully explained. A new large isotope effect of hot electron degradation by using deuterium instead of hydrogen for interface passivation was found.

The isotope effect can be used to distinguish hydrogen related hot electron damage from other mechanisms. It was initially discovered during scanning tunneling microscope (STM) experiments dealing with passivation and de-passivation of silicon surfaces in ultrahigh vacuum (UHV). These experiments showed that it takes a certain number of electrons (typically of the order of 10⁶-10⁸) having a certain energy to remove hydrogen from the (100) silicon surface. The same experiments performed with the isotope deuterium instead of hydrogen required roughly a factor of one hundred more electrons to remove deuterium for electron energies above ~ 4 eV. Recent STM experiments now show that this isotope effect increases dramatically for electron below 4 eV.

Silicon surface is passivated with hydrogen and then selectively de-passivated by STM to form silicon nanostructure patterns that could be used for further chemical processing. In the course of these investigations, it is found that passivations with deuterium are significantly more resistant to STM de-passivation. It takes higher voltages or significantly higher STM current densities to remove a given deuterium atom from the surface than necessary for hydrogen. The isotope effect is of the order of a factor of 100 at high STM voltages and much higher still at lower voltages. Typical measurement of the desorption yield for H and D is shown in Fig. 3. The strong dependence on the STM current is a signature of a process requiring multiple scattering events.

These basic STM experiments led to investigations of hot electron degradation of CMOS devices that were annealed in a deuterium atmosphere. Again a large isotope effect was found with transistor lifetimes being extended by factors of 10-50. Smaller improvements were observed under circumstances of large background hydrogen or reduced deuterium diffusion (e.g., nitride spacers).

The basic desorption mechanism toward which the isotope effect points is the creation (by hot electrons) of vibrational excitations of hydrogen bound to silicon (or polysilicon) at an interface. These vibrations and collisions with electrons having a few electron volts of energy can lead to desorption of the hydrogen, creating atomic hydrogen and a dangling bond. The freed atomic hydrogen subsequently can create further damage. The desorption mechanism itself determines critical energies and current densities and is therefore important for understanding and controlling degradation.

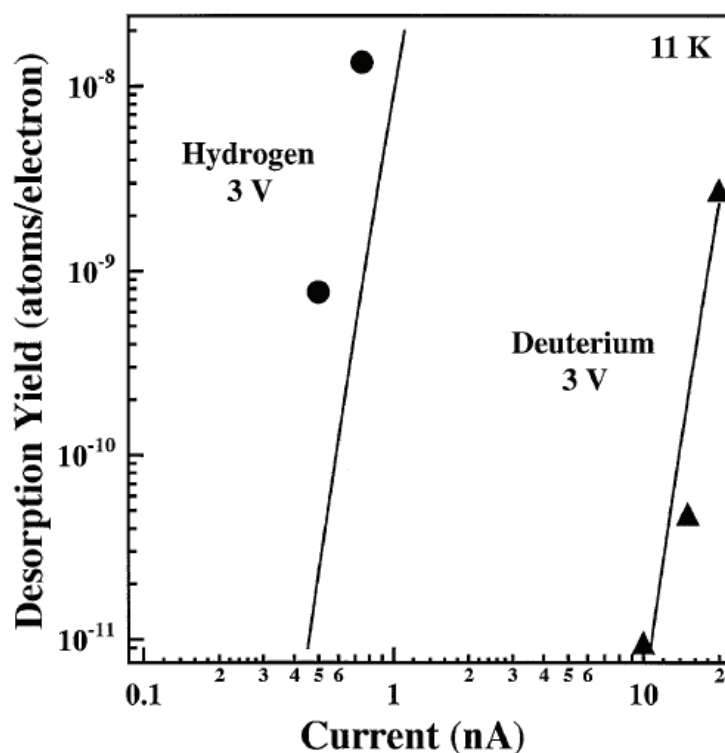


Fig. 3. Comparison of hydrogen and deuterium desorption yields at 3 V and 11 °K as a function of STM current showing an isotope effect and current dependence.

3. Deuterium Implantation in MOS Devices

The passivation with the annealing process is thought to be due to deuterium (D)-terminated, dangling bonds at the silicon surface, reducing interface trap density. This process relies on the diffusion of deuterium to the interface in the entire device area. Deuterium diffusion takes place primarily through the gate oxide, as depicted in Fig. 4, because of the limited permeability of bulk Si, metal, and even polysilicon to hydrogen or deuterium. Room temperature diffusion coefficient through Si is measured to be $\approx 10^{-15}$ cm²/s, compared with $\approx 10^{-11}$ cm²/s in SiO₂. The hydrogen diffusion through the

polysilicon is further retarded at the grain boundaries, as has been demonstrated in a study of thin-film transistors (TFT). In the case of large scale ICs, therefore, the ability of hydrogen to diffuse within the very thin SiO_2 layer may be severely impeded, impacting the large-area devices. This is particularly alarming since it has, in addition, been reported that H_2 permeability in SiO_2 is reduced as the oxide thickness decreases.

Lyding et al. delivered the deuterium to the region of the gate oxide in an oven through thermal diffusion. This causes most of the deuterium to be wasted. In addition, during the sintering process, the deuterium may experience difficulty diffusing through some materials to reach the Si/SiO_2 interface, especially in those cases where several layers of metallization are located between the deuterium gas and the Si/SiO_2 interface.

Deuterium is introduced into the semiconductor devices by implantation in our study, instead of by thermal diffusion as was done by Lyding et al. The implantation may be accomplished at any step of the semiconductor process flow. In general, deuterium implantation is provided so that, during subsequent thermal cycles, the deuterium will diffuse to the gate oxide/silicon interface and become chemically attached to the dangling bonds at the interface, this generally being the Si/SiO_2 or polysilicon/ SiO_2 interface. The energy, dose and defects of the implant are optimized to affect this.

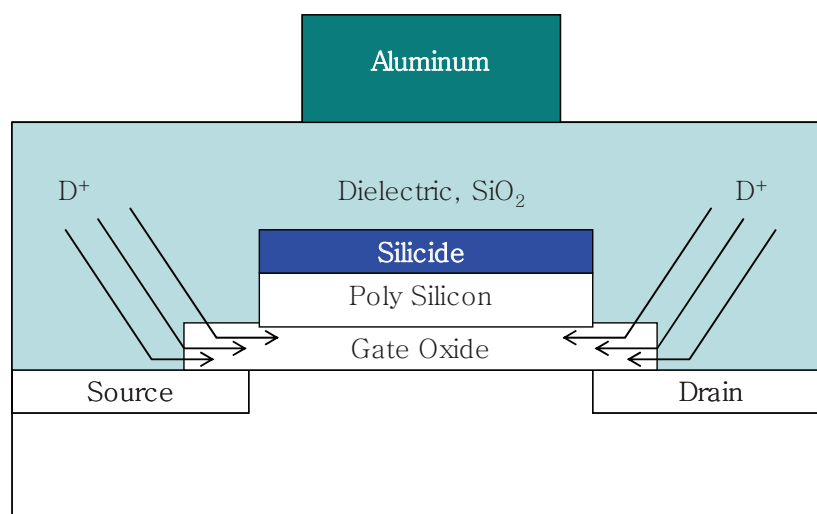


Fig. 4. Schematic of the device structure, indicating the path of D^+ diffusion through gate oxide from the edges of poly-silicon gate.

3.1. Calculation for Ion-Implant Process

There is need for the mathematical calculation for the ion implantation. TRIM(Transport of ions in matter) is Monte Carlo computer program that calculates the interactions of energetic ions with amorphous targets. TRIM is a group of programs which calculate the stopping and range of ions (10 eV ~ 2 GeV/amu) into matter using a quantum mechanical treatment of ion-atom collisions. This calculation is made very efficient by the use of statistical algorithms which allow the ion to make jumps between calculated collisions and then averaging collision results over the intervening gap. During the collisions, the ion and atom have a screened Coulomb collision, including exchange and correlation interactions between

the overlapping electron shells. The ion has long range interactions creating electron excitations and plasmons within the target.

TRIM accepts complex targets made of compound materials with up to eight layers, each of different materials. It calculates both the final 3D distribution of the ions and also all kinetic phenomena associated with the ion's energy loss: target damage, sputtering, ionization, and phonon production. Fig. 5 is the Setup Window for TRIM execution. The window is used to input the data on the ion, target, and the type of TRIM calculation that is wanted. Almost all inputs have online explanations.

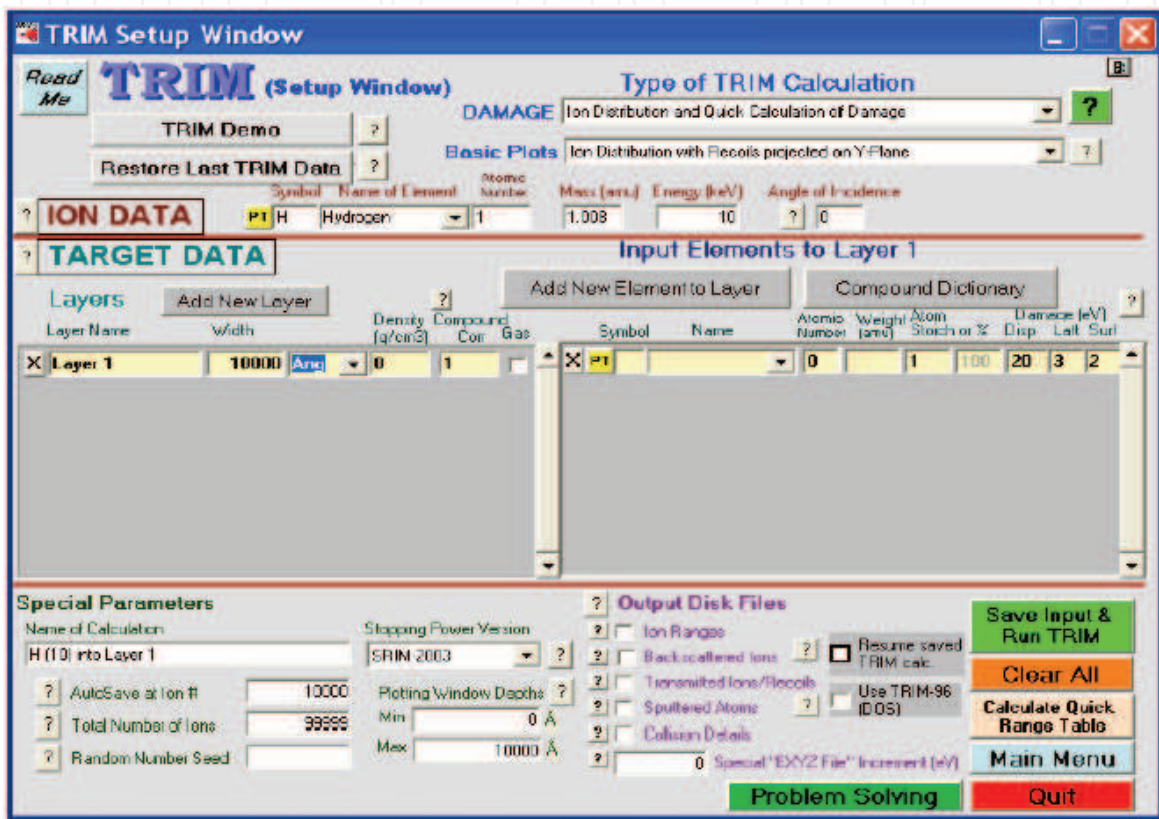


Fig. 5. TRIM Setup Window to calculate ion-implant process.

4. Experimental Results

4.1. Device Fabrication

In our study, both p- and n-MOSFETs were fabricated using standard CMOS processes for various channel lengths and widths down to 0.15 μm . Fig. 6 shows schematic cross section of our n-MOSFET device and experimental set up for the voltage stress measurements. The effective oxide thickness of our devices has a range of 3 ~ 7 nm. The gate oxide films were produced with a conventional furnace in $\text{H}_2\text{-O}_2$ ambient. The hydrogen (H) or deuterium (D) implantation was performed at the back end of the process line (after first metallization) to passivate the defects which spreaded in gate oxide area.

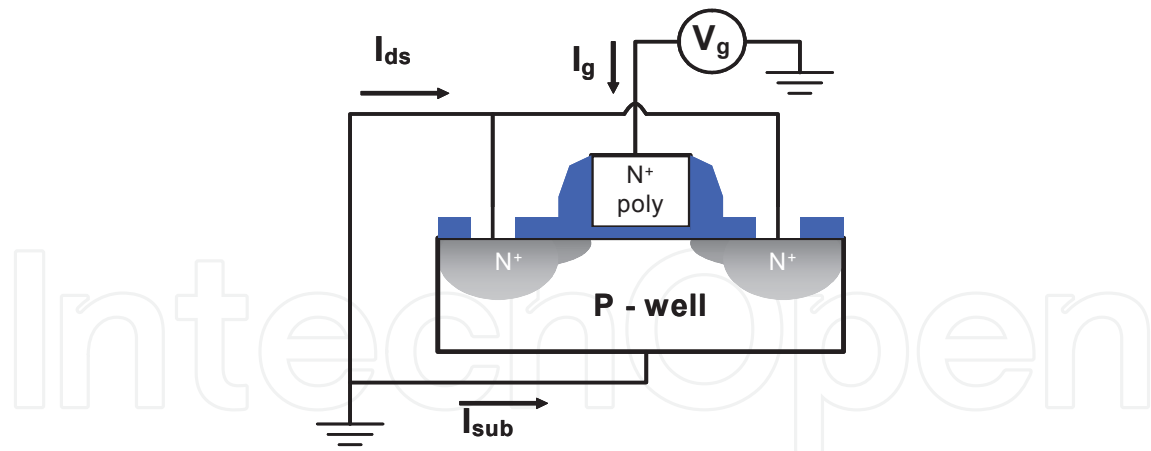


Fig. 6. Schematic cross section of n-MOSFET and experimental setup for the voltage stress measurements.

Transistors from a given wafer were divided into two groups. One group was implanted by H^+ ion with ≤ 60 keV and the other group was implanted by D^+ ion with ≤ 80 keV. Ion dose was fixed at $1 \times 10^{14}/\text{cm}^2$ only for hydrogen implant as referential sample, while in case of deuterium implantation the ion dose have a range from $1 \times 10^{10}/\text{cm}^2$ to $1 \times 10^{16}/\text{cm}^2$ to find optimum process condition. Post-annealing was achieved at 400°C for 30 minutes at N_2 ambient for the whole devices to activate the injected ions and to annihilate damages due to the implant process.

The implantation conditions for each ion were extracted through the computer simulation (TRIM tool). The total thickness from the top of first metal to the bottom of gate oxide was about 700 nm, including aluminum, silicon dioxide, and polysilicon layers, as shown Fig. 7. The control device was also prepared without our implantation processes to compare its electrical properties with those of our processed devices.

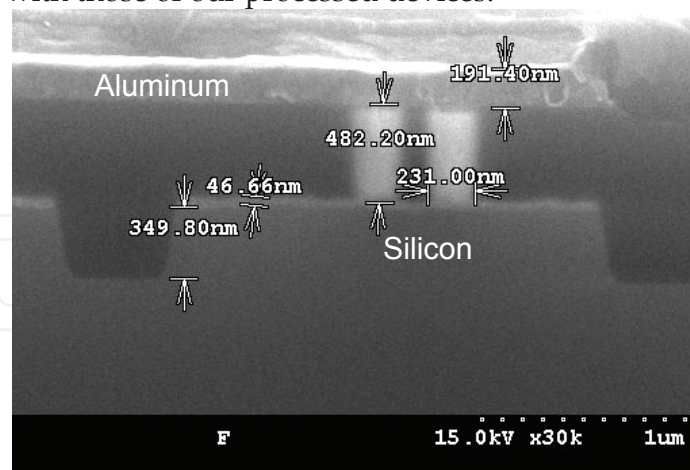


Fig. 7. Cross-section picture for our processed wafer. Two via contacts are shown between silicon substrate and aluminum metal layer.

To investigate the reliability of our devices, the degradation phenomenon such as channel hot carrier injection (HCI), negative-bias temperature instability (NBTI), and stress-induced leakage current have been studied.

A voltage of $V_g = V_d = \pm 3.0$ V was applied to the 3 nm-thick-MOSFET gate at the room temperature to accelerate HCI gate oxide degradation. A source terminal is connected to substrate and grounded. Stress voltages of $V_g = -2.8$ V for NBTI was applied to the p-MOSFET gate at the temperature of 50 ~ 100 °C. The source and drain terminals were connected to the substrate and grounded. For gate oxide leakage current measurements, large area MOSFETs ($W/L = 500 \mu\text{m}/500 \mu\text{m}$) were used to avoid the edge effect. While the constant voltage, $V_g = \pm 3.5$ V, was applied to gate terminal, the gate current was measured simultaneously. The percent shifts (%) of saturation drain current (I_d) and the shift of threshold voltage (ΔV_{TH}) were measured to determine device parameter degradation. The percent shifts (%) of the gate current (I_g) were also monitored to assess gate oxide wear-out.

4.2. Result

The carrier separation experiment was conducted to measure the gate current I_g , the sum of source and drain currents I_{ds} , and the substrate current I_{sub} separately before stress, applying negative polarity of V_g . All currents flowing into the device are taken as positive.

Fig. 8 shows I_g , I_{sub} , and I_{ds} versus sweeping V_g in our p- (a) and n-MOSFET (b) at 100 °C, respectively. In p-MOSFET, the conduction mechanism for three current components indicates that the electron current, when tunneled to the substrate, produces electron-hole pairs by impact ionization from near $V_g = -4.0$ V. The impacted ionized holes flow out through the source/drain; hence, those "hot" holes generate negative I_{ds} . Below $V_g = -4.0$ V, "cold" hole injection from silicon valence band and electron injection from polysilicon valence band become allowed, simultaneously. In n-MOSFET, the trend is quite similar to the case of p-MOSFET. However, I_{ds} measured the electron current and I_{sub} measured the hole current. Near $V_g = -3.5$ V, the increase of I_{sub} tends to slow down, and changes the sign from positive to negative that means the impact ionization could be dominant.

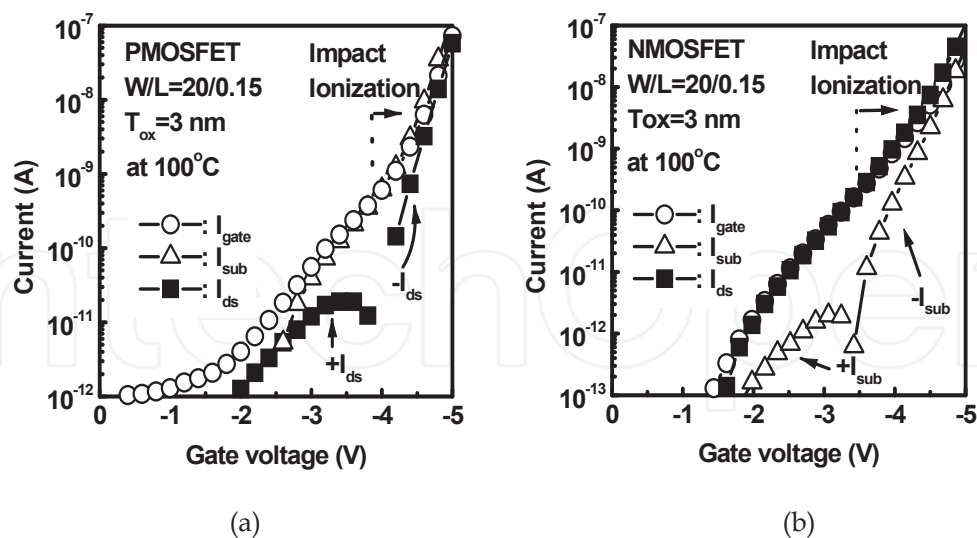


Fig. 8. Carrier separation I-V curves for 3 nm-thick gate oxide devices ($W/L : 20 \mu\text{m}/0.15 \mu\text{m}$) measured in negative bias : (a) p-MOSFET; (b) n-MOSFET.

Before actual ion implantation its optimum condition was estimated through the computer simulation with TRIM. The material stack between aluminum and silicon substrate in our MOS device was composed of SiO₂ [300 nm] / poly-Si [250 nm] / gate oxide [3~7 nm] / Si-substrate. Fig. 9 shows the distribution of ion ranges for deuterium when the incident energy was 30 KeV for SiO₂/poly-Si/Si structure and 85 KeV for Al/SiO₂/poly-Si/Si structure. The each peak was close to the bottom of poly-Si gate, and then deuterium ion would be diffused into the gate oxide area through post-annealing process.

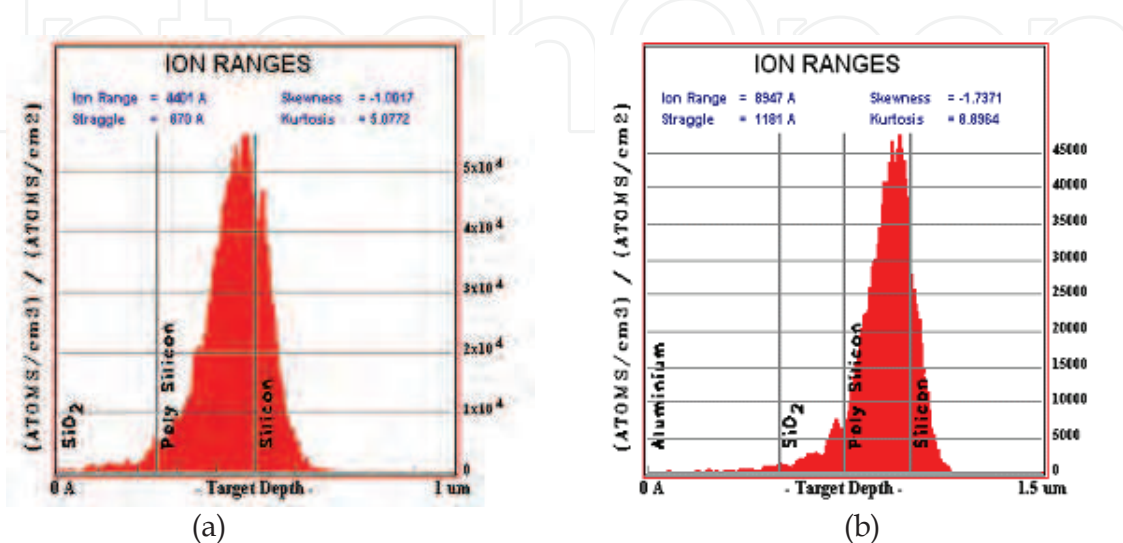


Fig. 9. Ion range calculation with the computer simulation for (a) SiO₂/poly-Si/Si structure and (b) Al/SiO₂/poly-Si/Si structure.

Secondary ion mass spectroscopy (SIMS) measurement of Al/SiO₂/poly-Si/Si structure which was implanted by deuterium on the top Al with 85 KeV energy and 10¹⁶/cm² dose is shown in Fig. 10. The SIMS analysis was done after 400 °C post-annealing process. The deuterium concentrations at the two SiO₂ interfaces are higher than that for aluminium area, indicating also deuterium concentration at the gate oxide region. Consequently, deuterium incorporation in the thin gate oxide (3 ~ 7 nm) was achieved at lower temperature through our implant process.

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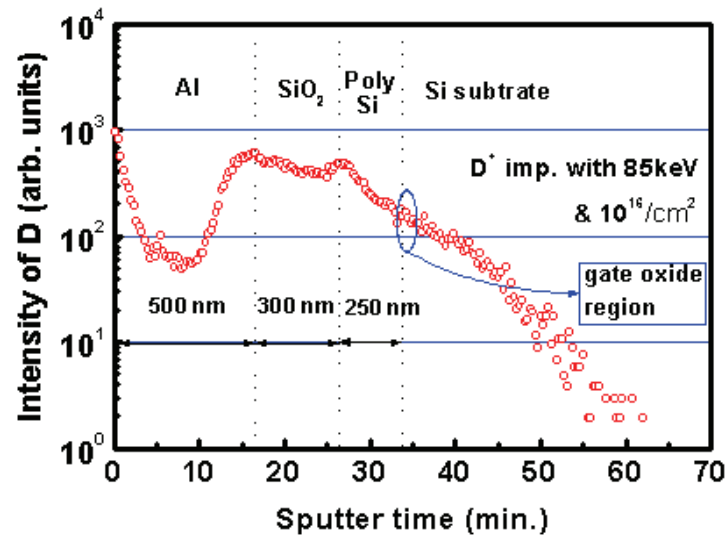


Fig. 10. SIMS analysis for Al/SiO₂/poly-Si/Si structure that was implanted with deuterium ion.

Fig. 11 represents the variation of gate current for both H⁺ and D⁺ implanted p-MOSFETs. The current was measured at the gate terminal while the gate voltage was being swept from 0 to 3 V. The device with deuterium implantation showed a lower gate leakage current for the entire range of sweeping voltages. Because the generation of stress-related bulk-oxide traps is suppressed by deuterium incorporation, we can infer that the isotope effect is valid in our new implant process. Therefore, deuterium implantation might be used to improve the reliability, if the suitable implant condition is obtained.

The normalized gate current is plotted as a function of stress time for p-MOSFETs with 3 nm-thick gate oxides in Fig. 12. The conventional, the hydrogen, and the deuterium-processed devices were stressed at a constant $V_g=3.5$ V voltage. The stress-induced leakage current is considered to be monitor for the defect generation in the gate oxide. From these curves, deuterium process shows fewer defects than hydrogen process, and the gate oxide implanted with deuterium, $1 \times 10^{12}/\text{cm}^2$ dose, generates almost the same number of defects as the gate oxide annealed in H₂. Trap generation rate increases with the deuterium (or hydrogen) concentration in the gate oxide, which is the same result as in the hydrogen or deuterium annealing process.

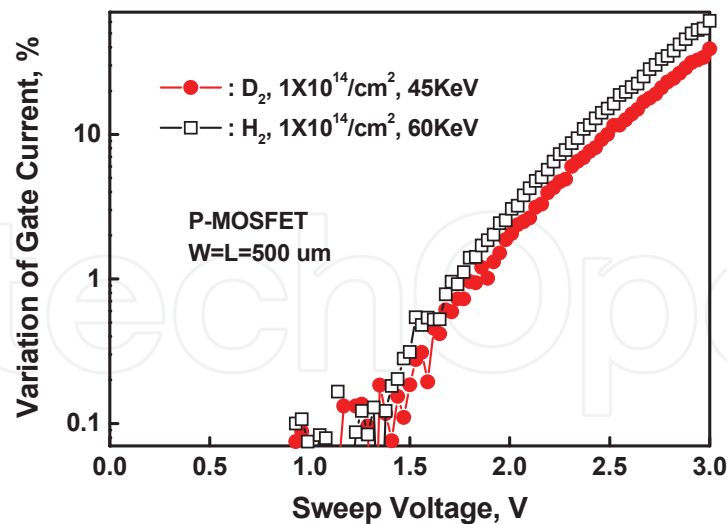


Fig. 11. Change of gate leakage current, after a constant voltage stress ($V_g=3.5$ V), of large-area p-MOSFETs implanted with H_2 and D_2 , respectively.

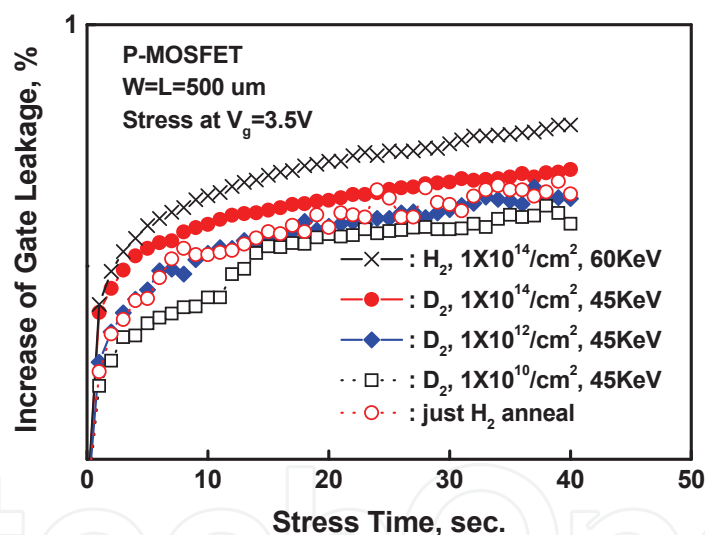


Fig. 12. Gate current transients during constant gate voltage, $V_g = 3.5$ V, for deuterium-implanted p-MOSFETs. These curves represent the evolution of defect generation.

NBTI of p^+ -gate p-MOSFETs has been the most serious issue for the reliability of ultra-thin gate oxide for continuous scaling down of devices. The isotope effect of the NBTI phenomenon was evaluated in our devices. Fig. 13 shows the saturation current and the threshold voltage dependence on the stress-time, respectively, for hydrogen- and deuterium-implanted p-MOSFETs. The degradation of deuterium-incorporated gate oxide is less remarkable than that of conventional gate oxide. Instead of hydrogen, using a deuterium can suppress the hydrogen-related precursors because the bonds to deuterium are more difficult to break than bonds to hydrogen.

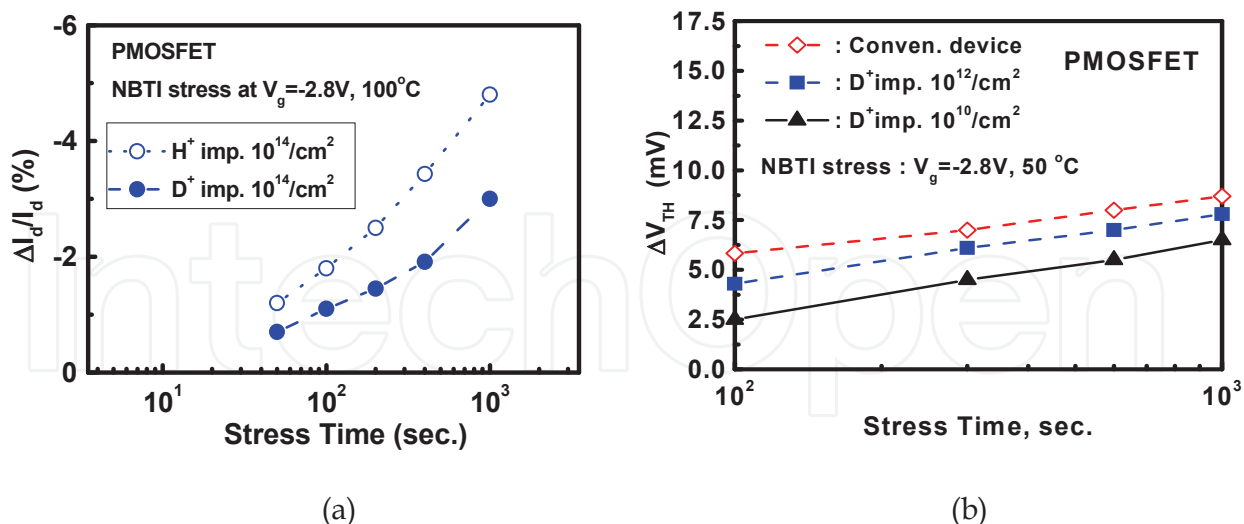


Fig. 13. (a) Decrease of saturation current and (b) variation of threshold voltage depending on NBTI stress time for both hydrogen- and deuterium-implanted p-MOSFETs.

In the channel hot carrier stress test, the Si/SiO₂ interface is degraded by hot carriers that are travelling the device from source to drain. The accelerated stress tests performed on MOSFET typically results in localized oxide damage, which has been correlated to Si/SiO₂ interface trap states. The generation of the interface trap states is due to hot carrier stimulated hydrogen desorption and de-passivation of the silicon dangling bonds. Fig. 14 shows the decrease of the saturation current by HCI stress for hydrogen- and deuterium-implanted MOSFETs. The deuterium-implanted device shows the slight enhancement for both n- and p- types compare to the conventional and the hydrogen-implanted devices. We believe that the incident deuterium atoms were not fully replaced with as-bonded hydrogen atoms at the Si/SiO₂ interface, and the damage area was restricted to the narrow channel area near drain.

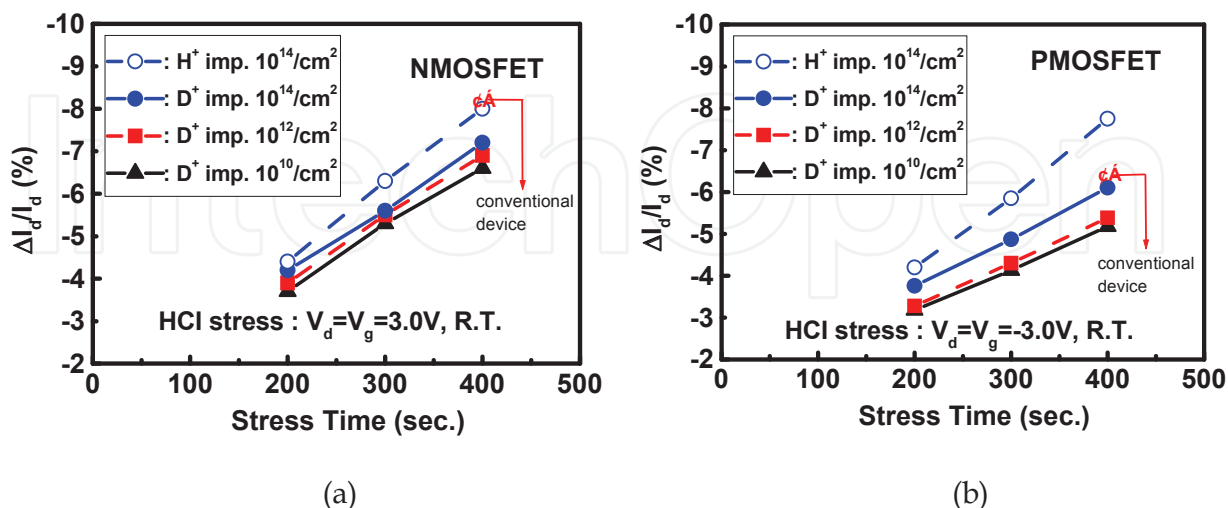


Fig. 14. Decrease of saturation current depending on HCI stress time for both hydrogen- and deuterium-implanted (a) n-MOSFETs and (b) p-MOSFETs.

In case of a large-area capacitor ($100 \times 100 \mu\text{m}^2$), the capacitance-voltage (CV) curve was measured at 1 MHz frequency, as shown in Fig. 15, for the deuterium-implanted n-MOSFETs. A shift of threshold voltage was observed in the deuterium-implanted device, which is related to the interface states density. In addition, there is a reduction in the minimum capacitance, indicating that the net doping in the Si substrate has been decreased. We believe that the difference of threshold voltage between before and after D^+ implantation is due to two different mechanisms. One is the elimination of the interface states by D^+ implantation, while the other is the change in the net doping in the substrate, due to deactivation of channel dopants.

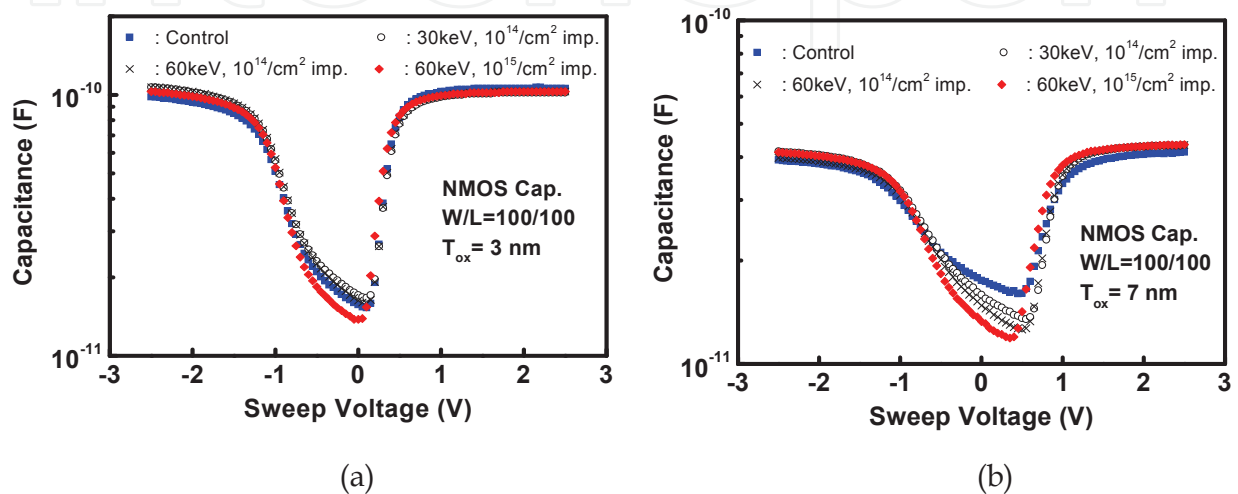


Fig. 15. Variation of CV characteristics for both the control and the deuterium-implanted n-MOSFETs with (a) 3 nm-thick gate oxide and (b) 7 nm-thick gate oxide.

4.3. Discussion and Summary

The generation of charge trapping in the existing precursor is explained by the strained bond model. The strained bonds exist not only at the SiO_2/Si interface but also in the oxide bulk because strain extending 1-3 nm into oxide from SiO_2/Si interface has been observed. When a strained Si-O bond in SiO_2 is broken by a hydrogen ion under the high-pressure and high-temperature hydrogen anneal, structure is rearranged locally to relax the strain, generating a trivalent silicon and a nonbridging oxygen simultaneously. The trivalent silicon acts as a positively charged center after it traps an injected hole. The nonbridging oxygen may act as a neutral electron trap center.

In the annealing process hydrogen or deuterium atom reaches at the gate oxide layer through upper layers, like aluminum, silicon oxide, silicon nitride, and polysilicon, by diffusion mechanism. In case of deuterium annealing, low levels of deuterium could be expected because the silicon nitride or polysilicon layer acts as a barrier to deuterium. Therefore, deuterium bond may not distribute uniformly along the channel area. Non-uniform distribution of deuterium bond tends to lack an isotope effect during electrical stress. By means of our suggested implantation, the deuterium bond could be distributed intentionally in the gate oxide layer.

Fig. 16 illustrates the possible reaction for the generation of oxide traps in the deuterium-implanted n-MOSFETs gate oxide with the energy band diagram. When the deuterium bond

distributes through the gate oxide, two kinds of reactions, the interface and the bulk reaction, may occur independently. The interface reaction involves deuterium release that could produce positive deuterium ions. The deuterium ions bonded with non-bridging atoms in gate oxide bulk react with the energetic electrons or holes. The bond breakage is not accelerated as rapidly, because deuterium is twice as heavy compare to hydrogen, and the dissociation by injected electrons or holes is suppressed. In the process of dissociation the mass of the atom plays a significant role and a large kinetic isotope effect is the consequence.

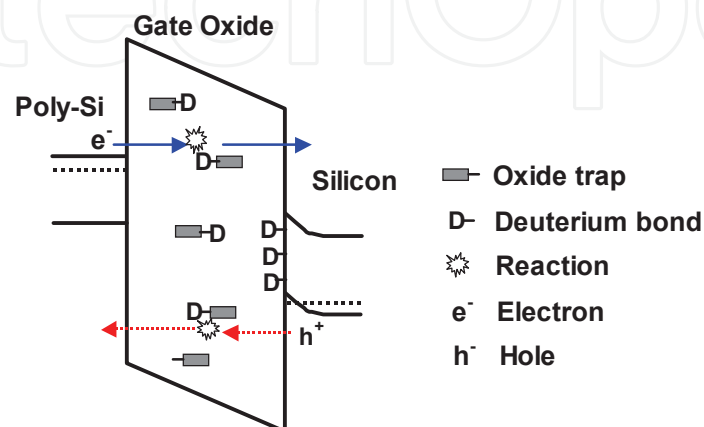


Fig. 16. Illustration for the reaction of injection carriers with the deuterium bonds existing at Si/SiO₂ interface and/or in SiO₂ bulk.

5. Conclusion

In the large-scale transistor structures, where gate oxide thickness of 7 nm and below is used, the post-metallization annealing (PMA) leaves a large number of Si/SiO₂ interface states unpassivated. Furthermore, the un-bonded hydrogen atoms in the SiO₂ is known as the main cause of the device degradation, such as NBTI and HCI. By means of our new method of deuterium implantation at the back-end process, we have improved the gate oxide reliability of MOSFETs, as compared with that of the conventional device. It was found that Si-D bonds (instead of Si-H) play a major role in suppressing the generation of oxide traps in our process. However, when the concentration of deuterium is redundant in gate oxide, excess traps are generated and degrades further the performance. We have suggested the new deuterium implantation process for the reliability of MOSFET, which is compatible with the conventional hydrogen annealing process.

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The main purpose of this book is to describe important issues in various types of devices ranging from conventional transistors (opening chapters of the book) to molecular electronic devices whose fabrication and operation is discussed in the last few chapters of the book. As such, this book can serve as a guide for identifications of important areas of research in micro, nano and molecular electronics. We deeply acknowledge valuable contributions that each of the authors made in writing these excellent chapters.

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