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Single-Electron Circuits for Sigma-Delta Domain Signal Processing

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1. Introduction

Contemporary micro-electronics fabrication technology downsizes electronic circuits to the nanometer scale. In nanometer-scale electronic circuits, physical quantities are quantized and device behaviour is discontinuous. The following three physical phenomena are examples of the quantization and the discontinuity:

Single-electron tunnelling (Grabert & Devoret, 1992): Figure 1(a) shows a physical system consisting of two electrodes and an island. They are capacitively coupled. Suppose that the left gap of the island is so narrow that electrons can tunnel. When voltage V_g is applied to the right electrode and the left electrode is grounded, electrons tunnelled from the left electrode accumulate on the island. The equivalent circuit of the physical system is shown in Fig. 1(b). The two coupling capacitances are denoted by Ct and C_g . Suppose further that capacitances Ct and C_g are small enough to satisfy

$$\frac{e^2}{C_t + C_g} >> k_B T , \tag{1}$$

where e, k_B , and T denote elementary charge, Boltzmann constant, and temperature. The above inequality means that a small number of excess electrons can remain on the island withstanding collision with phonons. Then the negative charge on the island cannot be regarded as continuous any more. As voltage V_g increases, the number n of electrons on the island increases. However, small increase of V_g do not necessarily increase n because of repulsive force between electrons, which is called Coulomb blockade. Figure 1(c) shows the relation between V_g and n. The figure implies that only a single-electron tunnels at a moment.



Fig. 1. Coulomb blockade and single-electron tunneling

Single-flux quantum (Tinkham, 1975): Figure 2(a) shows a superconductive ring in magnetic field *H*. The ring is cooled under its critical temperature. Magnetic flux also exists in the air surrounded by the ring because of diamagnetic current in the ring. Even after magnetic field *H* is switched off, the ring holds magnetic flux ϕ as shown in Fig 2(b). The wave function of electrons distributes so that it satisfies a periodic boundary condition of the ring. The condition quantizes the flux . Figure 2(c) shows the relation between magnetic field *H* and magnetic flux . In the figure, $\phi 0 = h/e$, *h*: Planck constant. This quantization can be seen even if the ring is macroscopic in scale.

Point contact (van Wees et al., 1988): A heterojunction between GaAs-AlAs and GaAs layers makes a two-dimensional electron system as shown in Fig. 3(a). Two electrodes with a *y*-directional gap narrower than mean free path of electrons are made on the surface. When negative voltage V_g is applied to the electrodes, no electron exists under the electrodes and the two-dimensional system is divided into two parts. The gap between the electrodes makes a narrow path of electrons between the two parts. The path is called a point contact. In the contact, wave function of electrons distributes nonuniformly as shown in Fig. 3(b). Then the *y*-directional kinetic energy of electrons is quantized. This quantization also leads to the quantization of the *x*-directional conductance *G* of the electron system. The conductance varies depending on electrode voltage V_g but it takes quantized values as shown in Fig. 3(c).

Like these phenomena, both passive and active nanometer scale devices behave discontinuously and signals are no more continuous in nanometer-scale circuits. In near-future nano-electronics era, although analog signal processing (ASP) based on quantum wave interference (Sols et al., 1989) will find a niche for itself, present type of ASP is considered to be destined to decay.

Nanoelectronic devices are seriously vulnerable to electronic magnetic interferences, atmospheric neutrons, and varying environmental conditions such as temperature. In Nyquist-rate multi-bit digital signal processing (DSP) circuits built of nanoelectronic devices, large surge noise is caused in internal signals and in outputs when the device errors lead to the reversal of the sign-bits or significant bits of the signals. Irregularly structured nanoelectronic circuits are difficult to construct because special technology for nanoscale fabrication such as self-organization of quantum dots cannot be used. Long routing lines among nanoelectronic devices badly affect device behavior because of parasitic components of the lines. Regularly arranged and locally connected cellular array structure is required to

the architecture of nanoelectronic signal processing circuits. Conventional circuit techniques for Nyquist-rate multi-bit DSP do not always satisfy the requirements.



Fig. 3. Quantization of conductance

Pulsed signal processing (PSP) has the potential to grow up to be the new nanoelectronic signal processing. Its signal form is a stream of positive and negative pulses whose average represents signal level, as shown in Fig. 4. As later sections of this chapter will show, PSP will be developed to be an ASP-like signal processing and inherit the properties of ASP. It also will be seen in the later sections that the PSP scheme will solve the above-mentioned problems of Nyquist-rate multi-bit DSP.

Several types of PSP schemes have been proposed in various areas such as communications and controls. Stochastic computing (Gaines, 1969), (Hori et al., 2006) is one of the PSP schemes. Bernoulli sequences used in stochastic computing have uniformly distributed frequency spectra of quantization errors. Pulsed signals with large quantization spacing contain large power of quantization errors. Therefore, the quantization error spectra of Bernoulli sequences are high in signal band. Thus the sequences are not high quality pulse streams. Sigma-delta domain signal processing (SDSP) (Fujisaka et al., 2002), (Fujisaka et al., 2003) is another PSP scheme. Its signal form is sigma-delta (SD) modulated signals (Candy & Temes, 1992) whose quantization error components are small in signal band. Then, compared with stochastic computing, SDSP is a high quality signal processing.

This chapter is devoted to the principles and the design of SDSP circuits with single-electron tunneling (SET) devices (Grabert & Devoret, 1992). The rest of this chapter is organized as follows: In section 2, a basic SD modulation circuit and the characteristics of SD modulated signals are presented. Section 3 describes the concept, architecture and distinctive features of SDSP. In section 4, logic circuits built of SET devices are presented. In section 5, arithmetic and piecewise linear circuit modules for SDSP are built of the logic gates introduced in

section 4. In section 6, linear and nonlinear filters are constructed by using the circuit modules as examples of nanoelectronic SDSP circuits.



Fig. 4. A pulsed signal and its local time average

2. Sigma-Delta Modulation

Sigma-delta modulation (Candy & Temes, 1992) is applied to analog-to-digital and digital-to analog conversions. Figure 5(a) shows first-order SD modulators. The two modulators are equivalent. Although the lower diagram shows the popular structure of the SD modulator, we will use the upper diagram to illustrate the modulation. The block Q in the SD modulator performs one or a few-bit quantization. In this article SD modulated signals are limited to bit-streams of one-bit pulses with height $\pm \Delta/2$, that is $y(n) \in \{\pm \Delta/2, -\Delta/2\}$, Δ : quantization spacing.



The bit-rate f_{SD} of the streams is higher than Nyquist-rate f_N . The ratio f_{SD}/f_N is referred as oversampling ratio (OSR). Let quantization error be defined with the variables in Fig. 5 as

$$e(n) = y(n) - u(n).$$
⁽²⁾

The probability distribution of the error is assumed to be uniform as Fig. 5(b) shows. Then the variance of the error, that is its power, is given by

$$e_{rms}^{2} = \langle e(n)^{2} \rangle = \frac{\Delta^{2}}{12}.$$
 (3)

The first-order SD modulated signal y(n) contains the error in the following difference form:

$$y(n) = x(n-1) + e(n) - e(n-1).$$
(4)

The difference of the error e(n)-e(n-1) is called first-order SD modulation noise. Assume further that the quantization error e(n) is white noise. Then the spectral density E(f) of the SD modulation noise is given by

$$E(f) = e_{rms} \frac{\left|1 - \exp(-j2\pi f/f_{SD})\right|}{\sqrt{f_{SD}/2}} = \Delta \sqrt{\frac{2}{3f_{SD}}} \sin(\pi f/f_{SD}), \quad j^2 = -1.$$
(5)

Figure 5(c) shows the spectral density of the SD modulation noise. The spectrum is low in low frequency band in which signal components locate. Thus SD modulation signals with high OSR are high quality. Conversion of original white noise e(n) to its difference e(n)-e(n-1) is called noise shaping.

Sigma-delta modulators built of nanoelectronic devices have been developed (Yokoyama et al., 2001), (Chibashi et al., 2004). A circuit shown in Fig. 6 is a first-order SD modulator proposed in (Chibashi et al., 2004). It is a continuous-time correspondence to the lower SD modulator in Fig. 5(a). It employs resonant-tunneling diodes (RTD). By exploiting the negative resistance of RTDs, a monostable-bistable transition logic element (MOBILE) (Maezawa, 1994) is composed with a pair of RTDs. A D-type flip flop is built of a MOBILE and an FET transistor. The components of the modulator circuit work in the following way: Transistors Tr1 and Tr2 convert the voltage difference between input *Vin* and *Vout* to a current. Capacitance *C* integrates the current. A D-type flip flop consisting of a MOBILE and transistor Tr3 operates as a quantizer with a unit-delay element. Then, we find that the circuit operates as a SD modulator.



Fig. 6. A first-order sigma-delta modulator using resonant-tunneling diodes

3. Sigma-Delta Domain Signal Processing

As mentioned in section 1, SDSP (Fujisaka et al., 2002), (Fujisaka et al., 2003), (Katao et al., 2007), (Hayashi et al., 2007) is a PSP scheme employing SD modulated signal forms. Figure 7 shows the architecture of Nyquist-rate multi-bit DSP and SDSP systems. In Nyquist-rate multi-bit DSP circuits built of nanoelectronic devices, large surge noise is caused in internal signals and in outputs when transient device errors lead to the reversal of the sign-bits or significant bits of the signals. On the other hand, a few bits of errors in a SD modulated bit-stream slightly decrease its signal quality but do not cause large surge because the signal level is represented by the average of the bit-stream in a time window. Even one transient device error in the sequence controller of Nyquist-rate multi-bit DSP systems causes chain-

reaction errors and leads the systems to failure. In SDSP systems, all the circuit modules are driven by a clock synchronized to the SD modulated bit streams. The modules complete their tasks within each one period of the clock. Thus, unlike conventional processors, SDSP processors need no operation sequence controller. Therefore, SDSP systems never go out of control by transient device errors. The pulsed signal form and the controller-less architecture equip SDSP systems with fault tolerance of transient device errors.



Fig. 7. The architecture of signal processors

Stochastic computing (Gaines, 1969), (Hori et al., 2006) mentioned briefly in section 1 uses binary Bernoulli sequences $x(n) \in \{+\Delta/2, -\Delta/2\}$ as signals. The advantage of stochastic computing is the simplicity of processing circuits. The signal level is represented by

$$\overline{x(n)} = \left\{ \operatorname{Prob}(x(n) = +\frac{\Delta}{2}) - \operatorname{Prob}(x(n) = -\frac{\Delta}{2}) \right\} \frac{\Delta}{2}.$$
(6)

Figure 8(a) shows the probability distribution of the quantization error esc(n) defined by

$$e_{SC}(n) = x(n) - x(n). \tag{7}$$

Then the power of error *esc*(*n*) is given by

$$e_{SC,rms}^{2} = \langle e_{SC}(n)^{2} \rangle = \frac{\Delta^{2}}{6}.$$
 (8)

Because signal x(n) is a Bernoulli sequence, error esc(n) is considered as white noise. Then, the spectral density Esc(f) of esc(n) is given by

$$E_{SC}(f) = e_{SC,rms} \frac{1}{\sqrt{f_{SC}/2}} = \Delta \sqrt{\frac{1}{3f_{SC}}}, \qquad (9)$$

where fsc is the bit rate of the signal x(n). Figure 8 compares spectral density between error esc(n) in stochastic computing and SD modulation noise esD(n) in SDSP. As signal components locate in low frequency band, SD modulated signals have higher quality than Bernoulli sequences. Figure 9 shows the power of the components of esc(n) and esD(n) located in signal band [0, fN]. The power decreases by -3dB and -9dB when OSR is doubled in stochastic computing and SDSP respectively. The figure implies that SDSP can perform higher quality signal processing at lower speed than stochastic computing.



Fig. 9. The quality of signals in stochastic computing and SDSP

4. Logic Circuits based on Single-Electron Tunnelling

Coulomb blockade and single-electron tunneling phenomena mentioned in section 1 make it possible to confine excess n (: integer) electrons in a nanoscale island. Logic gates exploiting the phenomena are introduced in this section. In most of the logic gates, the number of excess electrons in every island of the logic gates is $n \in \{0, 1\}$ or $\{0, -1\}$.

4.1 Linear Threshold Gates

Consider a linear threshold gate (LTG) (Lewis & Coates, 1967) expressed by



The LTG is constructed of SET devices as shown in Fig. 10(a) (Lageweg et al., 2001). The circuit possessing two islands P- and P+ takes the following two states.

State 1: Islands P- and P+ respectively hold one excess hole and one excess electron.

State 0: Both islands P- and P+ hold no excess charge.

When the circuit is in state 1/0, the output level is high/low. In state 0, voltage V_j across the tunneling junction between P- and P+ is given by

$$V_{j} = \sum_{i=1}^{N+} w_{i,+} v_{in,i,+} - \sum_{i=1}^{N-} w_{i,-} v_{in,i,-} + w_{b} V_{b},$$

$$w_{i,+} = C_{\Sigma-}C_{i,+} / C_{r}^{2}, \quad w_{i,-} = C_{\Sigma+}C_{i,-} / C_{r}^{2}, \quad w_{b} = C_{\Sigma-}C_{b} / C_{r}^{2},$$

$$C_{\Sigma+} = C_{b} + \sum_{i=1}^{N+} C_{i,+}, \quad C_{\Sigma-} = C_{o} + \sum_{i=1}^{N-} C_{i,-}, \quad C_{r}^{2} = C_{\Sigma+}C_{j} + C_{\Sigma+}C_{\Sigma-} + C_{j}C_{\Sigma-}.$$
(11)

The circuit gets into state 1 when V_j is greater than critical voltage Vc given by

$$Vc = (C_{\Sigma +} + C_{\Sigma -})e/2C_r^2.$$
(12)

Then it is found that the circuit behaves as LTG described by Eq. (10). The LTG circuits work as Boolean logic gates. A circuit shown in Fig. 10(b) operates as AND or OR gate when its threshold level is set at a high or a low level. A circuit shown in Fig. 10(c) operates as NOR or NAND gate depending on its threshold level. Circuit parameters to make the LTGs operate as various Boolean logic gates are shown in Tab. 1.

4.2 Logic Circuits based on Binary Decision Diagram

A binary decision diagram (BDD) is a directed graph representing a Boolean logic function (Miller et al., 2006). Examples of BDD expression are shown in Fig. 11. All the paths from the top of the graph to terminal-1/0 assign values of variables x_1 , x_2 , ..., x_N that make Boolean function true/false.

Logic circuits based on BDD can also be constructed by using SET devices (Asai et al., 1997). In BDD-based logic circuits, paths are represented by series of islands located like steppingstones. In the logic circuits, a single-electron entered at the top is transferred from one island to another through SET junctions. A basic circuit transferring a single-electron is shown in Fig. 12(a). The circuit is named single-electron pump (Pothier, 1992). Let terminal voltages be fixed at $V_1 = 0$ and $V_2 = 0$. When the two islands hold n_1 and n_2 excess electrons, the electrostatic energy $E(n_1, n_2)$ of the circuit is given by

$$E(n_1, n_2) = \frac{1}{6C_j} \left\{ (n_1 e - C_g V_{g1})^2 + (n_2 e - C_g V_{g2})^2 + ((n_1 + n_2) e - C_g (V_{g1} - V_{g2}))^2 \right\},$$
(13)



Fig. 10. Linear threshold gates built of SET devices

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Parameters	OR	AND	NOR	NAND	4-input AND
Vin High. Vin Low	0V, 16mV				
ю	16mV	16mV	16mV	16mV	16mV
Съ	10.1aF	10aF	9.9aF	10.1aF	9,7aF
Ci	0.1aF	0.1aF	0.1aF	0,1aF	0.1aF
Co	10aF	10aF	10aF	10aF	10aF
Cj	0.1aF	0.1aF	0.1aF	0.1aF	0.1aF

Table 1. Circuit parameters of LTG-based Boolean logic gates

where C_j is the capacitance of the tunneling junctions, C_g is the gate capacitance, and V_{g1} and V_{g2} are the gate voltages. Figure 12(b) shows the region in which energy $E(n_1, n_2)$ becomes low and the two islands can stably hold (n_1, n_2) electrons in (V_{g1}, V_{g2}) -plane. By changing (V_{g1}, V_{g2}) along the circle in Fig. 12(b), a single-electron moves from the left to the right terminal. The node cells in BDD-based logic circuits are built by applying the singleelectron pumps, as shown in Fig. 13. A clocked logic circuit which functions as $f(x_1, x_2, x_3, x_4)$ = $x_1 x_2 + x_3 x_4$ is constructed by connecting the node cells as shown in Fig. 14.





Fig. 12. Single-electron pump



Fig. 13. Single-electron node cell of BDD-based logic circuits (Asai et al., 1997)



Fig. 14. A BDD-based clocked logic circuit (Asai et al., 1997)

4.3 Delay Elements

Delay elements are built by applying the single-electron pumps. Figure 15 shows a unit delay driven by a four-phase clock set. The delay element consists of seven tunneling junctions (Keller et al., 1996). Connecting additional 4(K-1) junctions to the unit delay changes its delay time to K(: integer).

4.4 Pseudo-CMOS Inverter Buffer

Figure 16(a) shows what is called a single-electron transistor and its gate voltage Vg versus drain-to-source current *I*_{DS} characteristic. The current peaks locate between the regions of gate voltage in which the island of the transistor holds integer number of excess electrons stably. The periodic characteristic is called Coulomb oscillation. Figure 16(b) shows a multi-gate single-electron transistor. When $Cg_1 = Cg_2 = Cg$ and $Cg_2Vg_2 = e/2$, its Vg_1 versus *I*_{DS} characteristic shifts by e/2Cg horizontally. Figure 16(c) shows an inverter (Tucker, 1992) consisting of the two two-gate single-electron transistors. Gate bias voltages Vp and Vn are determined so that current *I*_{DS} passes through the upper and the lower transistors at zero and high levels of input voltage respectively. The inverter is used as a buffer since its voltage gain |dVout/dVin| can be greater than 1.0.









Fig. 16. A puseudo-CMOS inverter buffer

5. SET Circuit Modules for SDSP

In this section we will build arithmetic and piecewise linear (PWL) circuit modules (Fujisaka et al., 2002), (Katao et al., 2007), (Fujisaka et al., 2003), (Hayashi et al., 2007) for nanoelectronic SDSP using SET devices. The circuit modules operate on SD modulated signals and shape quantization error into the form of SD modulation noise.

5.1 Arithmetic Circuits

5.1.1 Adder

Figure 17 shows digital SD modulators converting 3-level signals represented by equally weighted two bits x(n), and y(n) into a SD modulated one-bit stream $z_{1/2}(n)$. The two digital SD modulators are respectively described by



Fig. 17. Two SD modulators with equally weighted two-bit input

$$u_{1}(n) = \frac{1}{2} \{x(n) + y(n)\} - e_{1}(n-1),$$

$$z_{1}(n) = Q(u_{1}(n)),$$

$$e_{1}(n) = z_{1}(n) - u_{1}(n),$$
(14)

and

$$u_{2}(n) = x(n) + y(n) - e_{2}(n-1),$$

$$z_{2}(n) = Q(u_{2}(n)),$$

$$e_{2}(n) = z_{2}(n) - u_{2}(n),$$
(15)

where $Q(\bullet)$ denotes two-level quantization. The above two equation systems have the following relations between their variables and outputs:

$$u_2(n) = 2u_1(n), \quad e_2(n) = 2e_1(n), \quad z_2(n) = z_1(n).$$
 (16)

Thus, the signal conversions by the two digital SD modulators are equivalent. When two SD modulated one-bit streams are applied to the inputs of the digital SD modulators, they operate as two-input adders. We will construct a SET circuit described by Eq. (15). Since x(n), $y(n) \in \{+1, -1\}$, the state of the digital modulator and the quantization noise are $u_2(n) \in \{-3, -1, +1, +3\}$ and $e_2(n) \in \{-1, +1\}$. Thus, $u_2(n)$ can be represented by the sum of three binary signals as

$$u_{2}(n) = \sum_{i=1}^{3} u_{2,i}(n), \quad u_{2,i}(n) \in \{+1, -1\}.$$
(17)

The three binary signals $u_{2,i}(n)$, *i*=1,2,3, are given values as shown in Tab. 2. Then, the output can be

$$z_2(n) = Q(u_2(n)) = u_{2,2}(n).$$
(18)

Fig. 18 shows an adder built of the SET gates introduced in section 4 (Katao et al., 2008).



Fig. 18. Block diagram of the adder built of SET devices

5.1.2 Multiplier

Although SD modulation noise does not contain large low frequency components, the direct multiplication of the SD modulated signals generates large low frequency noise components. Pre-filters are necessary to remove SD modulation noise from a multiplier signal and a multiplicand signal. Let a multiplier and a multiplicand be denoted by x(n) and y(n) and let their filtered signals be given by

$$\overline{x(n)} = \frac{1}{N} \sum_{i=0}^{N-1} x(n-i), \qquad \overline{y(n)} = \frac{1}{N} \sum_{i=0}^{N-1} y(n-i).$$
(19)

The filtered signals are no more SD modulated single-bit signals and the multiplication cannot be performed in SD domain. The product of the filtered signals is expanded as the right hand side of the following equation:

$$\overline{x(n)}\,\overline{y(n)} = \frac{1}{N^2} \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} x(n-i)y(n-j).$$
(20)

The expanded product can be computed with exclusive-OR gates and the above-mentioned SD domain adders. Then the product is computed in SD domain. Figure 19 shows an example of SD domain multipliers. When N=2 in Eq. (20), the multiplier is built of SET gates as shown in Fig. 20 (Katao et al., 2008).



Fig. 19. Structure of multipliers for SDSP



Fig. 20. Block diagram of a multiplier built of SET devices

5.1.3 Circuit Simulation of the Arithmetic Circuits

The SD modulated sum and product obtained by the SET arithmetic circuits in Figs. 18 and 20 are shown in the time and frequency domain in Figs. 21 and 22. The results are obtained by circuit simulation with SIMON (Wasshuber et al., 1997). Figure 22 validates that the SET arithmetic circuits have the function of quantization noise shaping. Figure 21 shows the averaged outputs of the SET circuits. As the transient error rate of SET junctions becomes

higher, the circuits increase noise components and decrease signal components in their outputs. However, the circuits never go out of control. The signal-to-noise ratio (SNR) versus SET junction error rate curves of the adder and the multiplier are shown in Fig. 23. It is found from the figure and Eq. (9) in section 3 that the outputs of the arithmetic circuits with the SET junction error rate of 10⁻² have the same signal quality with that of errorless stochastic computing.



Fig. 21. Averaged inputs and outputs of the arithmetic circuits



Fig. 22. Frequency spectra of the outputs of the arithmetic circuits



Fig. 23. Fault tolerance characteristics of the arithmetic circuits: Output SNR versus transient error rate of SET junctions

5.2 Piecewise Linear Circuits

In ASP, PWL modules such as limiters and rectifiers are easily build by using diodes and frequently used. In SDSP as a successor of ASP, PWL modules are required.

5.2.1 Absolute Circuit

There are several methods of computing absolute (ABS) values in SDSP. We will show a method proposed in (Hayashi et al., 2007). The first-order binary SD modulated signals possess the following characteristic:

[Theorem] Let a first-order binary SD modulator be described by

$$y(n) = Q(u(n)) \in \{+1, -1\},\$$

$$e(n) = y(n) - u(n),\$$

$$u(n) = x(n-1) - e(n-1), \quad x(n) \in [-1, +1].$$
(21)

The output bit-stream y(n) is a sequence such that

$$(y(n), y(n-1)) \neq \begin{cases} (-1, -1) & \text{if } x(n) \ge 0, \\ (+1, +1) & \text{if } x(n) \le 0. \end{cases}$$
(22)

[Proof] Consider the SD modulation in the case that $0 \le x(n) \le 1$ and $-1 \le u(m) \le 2$, $n \ge m$. When state u(m) is in

$$0 \le u(m) \le 2,$$

$$-1 \le e(m) = Q(u(m)) - u(m) \le 1.$$
(23)
(24)

Then, from the last equation in Eq. (21), we have

$$-1 \le u(m+1) \le 2.$$
 (25)

When state u(m) is in

$$-1 \le u(m) \le 0, \quad y(m) = Q(u(m)) = -1,$$
(26)

the quantization error is

the quantization error is

$$-1 \le e(m) = Q(u(m)) - u(m) \le 0.$$
(27)

Then,

$$0 \le u(m+1) \le 2$$
, $v(m+1) = O(u(m+1)) = +1$. (28)

From Eqs. (23) to (28), the range of state u(n) is $-1 \le u(n) \le 2$ for $n \ge m$.

From Eqs. (26), (28) and (29), the upper part of the right hand side of Eq. (22) is obtained. The lower part is similarly proved. An ABS circuit for SDSP is shown in Fig. 24. When the sub-circuit consisting of two AND gates and a unit delay detects (y(n), y(n-1)) = (-1, -1), the SR flip flop is cleared and the exclusive-OR gate inverts input x(n). A SET implementation of the ABS circuit is built by using LTG-based Boolean logic gates mainly, as shown in Fig. 25.







Fig. 25. Block diagram of the ABS circuit built of SET devices

5.2.2 Min/Max and Other PWL Circuits

Operation of a Min/Max selector is expressed by ABS operation and addition/subtraction (Li et al., 1999) as



Since ABS and adder modules for SDSP have been developed, the operations given by Eq. (30) can be carried out in SDSP. Figure 26 shows a Min/Max circuit built according to Eq. (30). A Limiter, a dead zone circuit, and a negative resistance whose functions are described in Fig. 27 are built by using other PWL circuits and adders as shown in Fig. 28. SET circuits for these three PWL operations in SDSP can be built by using the adder, ABS, and Min/Max modules.

(29)





Fig. 29. Averaged inputs and outputs of the PWL circuits; (a) inputs to the ABS and Min/Max circuits, (b) output of the ABS circuit, (c, d) the Min and Max outputs, (e) input to the limiter, dead zone circuit, and negative resistance, (f) output of the limiter, (g) output of the dead zone circuit, (h) output of the negative resistance

5.2.3 Circuit Simulation of the PWL Circuits

Results of simulating the ABS, Min/Max, limiter, dead-zone circuit, and negative resistance are shown in Fig. 29.

6. Applications

Filters have been the most important circuits in both analog and digital signal processing, and they will be in SDSP too. In this section, using the SET modules presented in the previous section, we will construct linear and nonlinear filters.

6.1 Linear Filter

To integrate signals in SD domain is not simple because of the bit-stream signal form. Linear filters for SDSP should be constructed not based on lumped analog filters with integrators but based on analog distributed-parameter filters (ADPF) (Mattaei, et al., 1980). ADPFs are built of transmission lines connected directly, or coupled capacitively and/or inductively, as shown in Fig. 30. In some kinds of ADPF, waves propagating on their transmission lines reflect at the junctions between the transmission lines with different characteristic impedances. Interference between incidental and reflected waves effects filtering. In other kind of ADPF, standing waves are generated on the transmission lines. The resonance causes bandpass or bandstop effect.



Fig. 30. Analog distributed parameter filters

Digital wave filters based on ADPFs have been proposed in (Suzuki et al., 2007a & 2007b). Wave propagation on lossless transmission lines are described by

$$\frac{\partial^2 w(x,t)}{\partial t^2} = c^2 \frac{\partial^2 w(x,t)}{\partial x^2},\tag{31}$$

where *c* denotes propagation speed. By the spatial and temporal discretization $x = i\Delta x$, $t = n\Delta t$ with $\Delta x/2\Delta t = c$ and the binary quantization of variable *w*, Eq. (31) is transformed to the following equations.

$$w_{l}(i,n) = w_{L}(i,n) + w_{R}(i,n),$$

$$w_{L}(i,n+1) = w_{L}(i+1,n-1), \quad n : \text{even},$$

$$w_{R}(i,n+1) = w_{R}(i-1,n-1), \quad n : \text{odd},$$

$$w_{L}(i,n), w_{R}(i,n) \in \{+1, -1\}.$$
(32)

The equations mean that the discrete wave w is the sum of binary-quantized waves w_L and w_R traveling left and rightwards. Thus, as shown in Fig. 31, a transmission line is represented by a pair of left and right shift integer delays in digital wave filters. The arithmetic modules presented in section 5 are placed between integer delays to cause wave phenomena corresponding to wave penetration and reflection at a junction of transmission lines and to coupling between transmission lines of ADPFs.

Consider a bandpass digital wave filter corresponding to the ADPF shown in Fig. 30(b). Building blocks for the ADPF are coupled parallel transmission line pairs with open ends. Let the lines of a pair be referred as line 1 and 2.



Fig. 31. Analog transmission line and its binary-quantized discrete model

Waves traveling left and rightward on lines 1 and 2 are denoted by $w_{1,L}$, $w_{1,R}$, $w_{2,L}$, and $w_{2,R}$. Even and odd mode waves propagating left and rightward on the line pair are defined by

$$w_{e,L} = (w_{1,L} + w_{2,L})/2,$$

$$w_{o,L} = (w_{1,L} - w_{2,L})/2,$$

$$w_{e,R} = (w_{1,R} + w_{2,R})/2,$$

$$w_{o,R} = (w_{1,R} - w_{2,R})/2.$$
(33)

Because the even and odd mode waves are different in propagation speed, the line pair has two resonance frequencies. The center frequency and the bandwidth of a bandpass ADPF consisting of the coupled line pairs are determined by the resonance frequencies. A digital model of the coupled line pair is shown in Fig. 32(a). Integer delays IDe/o,L/R representing transmission lines are built as mentioned in section 4. Type-1 adders are the same circuits as the one presented in Fig. 18. Type-2 adders are different from type-1 adders in that the variable $u_{2,2}$ is not fedback. Both types of adders are used to make the coupling phenomena between the lines in the following way: The type-1 adders synthesize even and odd mode waves $w_{e,L/R}$ and $w_{o,L/R}$. The integer delay pairs propagate the two modes of waves. The length of the integer delays in a pair are set differently instead of setting the propagation speed of the even and odd mode waves differently. The type-2 adders reconstruct waves $w_{1,L/R}$, and $w_{2,L/R}$. Reflection at the open ends of the lines of the pair is represented by inputting waves outputted from the type-2 adders to the type-1 adders. A bandpass digital wave filter is constructed by connecting the building blocks like the ADPF, as shown in Fig. 32(b).

Figure 33 shows the frequency response of the bandpass filter with 4 blocks. In each block, the integer delays ID_{0,L/R} on which odd mode waves propagate are three times as long as the integer delays ID_{e,L/R} on which even mode waves propagate. One building block with ID_{e,L/R} of length $0.5 \times l_{ID}$ and ID_{0,L/R} of length $1.5 \times l_{ID}$, $l_{ID} = 64$, is simulated with SIMON. Simulation results are shown in Fig. 34. In the figure, $f_0 = 1/4l_{ID} = 1/256$. Inputs are passed and attenuated in the passband and the stopband as theoretically estimated. Figure 35 shows the signal-to-noise ratio (SNR) versus SET junction error rate curves. In the figure, $OSR = f_{SD}/2f_0 = 2 \times l_{ID}$. The figure shows that the signal quality does not affected by low rate junction error.

6.2 Nonlinear Filter

Nonlinear digital filters are categorized into two main classes, ε filters and order statistic filters (Pitas & Venetsanopoulos, 1990). Order statistic filters permute input series sampled in a time window in ascending or descending order and weight the samples depending on the order. Median filters, mid-range filters, α -trimmed mean filters belong to the class of

order statistic filters. They can remove wide band noise contained in wide band signals without changing the waveform of the signals. For example, median filters effectively remove pulse-shaped noise.



Fig. 33. Theoretical frequency response of the bandpass filter



Fig. 34. Examples of simulation results of the bandpass filter block with SIMON



Fig. 35. Fault tolerance characteristic of the bandpass filter: Output SNR drop versus transient error rate of SET junctions

Figure 36(a) shows the schematic diagram of order statistic filters. They consist of front delay elements, a sorting network permuting input samples, and a weighted sum computation block. In Nyquist rate operation, the delay time of the front delay elements is D=1. Several kind of efficient sorting networks have been proposed. A sorter shown in Fig. 36(b) is what is called an odd-even transposition sorter. A median filter, a mid-range filters, and an α -trimmed mean filter have weight sets ($w_3 = 1$, $w_1 = w_2 = w_4 = w_5 = 0$), ($w_1 = w_5 = 1/2$, $w_2 = w_3 = w_4 = 0$), and ($w_2 = w_3 = w_4 = 1/3$, $w_1 = w_5 = 0$) respectively.



Fig. 36. Order statistic filters

A median filter operating on SD modulated signals was first presented in (Fujisaka et al., 2003). An example of impulse noise suppression by the median filter is shown in Fig. 37. The result is obtained by logic level simulation carried out under the following conditions: The

delay time of the front delay elements is D = 20. The signal component is a sinusoidal wave with amplitude 0.5 and period 10⁴. The positive impulse noise is 20*D* in interval, 0.2*D* in width and +0.4 in height. The negative impulse noise is 35*D* in interval, 0.9*D* in width and - 0.5 in height. The SET circuit of the median filter can be constructed by employing integer delays presented in section 4 as the front delay elements and Min/Max selectors shown in section 5 in the odd-even transposition sorter.



Fig. 37 Average input and output of the median filter

7. Conclusions

This chapter has presented single-electron pulsed signal processing circuits. The pulsed signal processing scheme is like analog signal processing which is considered to decay in the near-future nanoelectronics age. The pulsed signal processing employs high quality and fault-tolerant sigma-delta modulated signal form, which derived the name of signal processing, sigma-delta domain signal processing (SDSP).

The research on nanoelectronic SDSP has just begun. It contains a lot of works to be challenged. First, circuit architecture of local connection style needs to be developed since parasitic capacitors, inductors, and resistors of the wires between nano-electronic devices cause errors in the device operation. The filters presented in section 6 partly take the style.

Secondly, the circuits operating on high-order SD modulated signals need to be developed since high-order SD modulated signal form is useful for high quality and low clock-rate signal processing. Thirdly, massively parallel computing for high performance processing and spatially redundant computing for defect and fault tolerance (Shukla & Bahar, 2004) will be challenged by taking advantage of the small size of SDSP modules. Lastly, new functions and new applications of SDSP will be explored since SDSP systems which are essentially digital systems can be functionally higher than ASP circuits.

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The main purpose of this book is to describe important issues in various types of devices ranging from conventional transistors (opening chapters of the book) to molecular electronic devices whose fabrication and operation is discussed in the last few chapters of the book. As such, this book can serve as a guide for identifications of important areas of research in micro, nano and molecular electronics. We deeply acknowledge valuable contributions that each of the authors made in writing these excellent chapters.

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