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Arithmetic Circuits Realized by Transferring Single Electrons

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1. Introduction

A number of challenges are facing the semiconductor industry, such as increases of power consumption and interconnects delay. The combination of current CMOS technology and novel nanotechnologies like the single-electron technology is a promising approach to solve these problems. Single-electron devices (SEDs) operate by controlling the movements of individual electrons based on the Coulomb Blockade effect (Likharev, 1999). They have potentially small device area and very low power dissipation. Single-electron circuit, in which discrete electrons are used to process information, can be viewed as the ultimate goal of electronic circuits (Ono et al., 2006). Therefore, the single-electron technology is attracting large interest in the last decade. Various single-electron circuit blocks, including memory (Yano, 1994), inverter (Ono et al., 2000), logic gates (Asahi, 1997), multiple-valued logic circuits (Inokawa et al., 2003) and sensors have been proposed and intensively studied. These circuits used the unique characteristic of SEDs and some of them have been proven to have impressive circuit performances.

Most of previous single-electron circuits have similar operation principle with their CMOS counterparts. For example, the single-electron inverter is composed of two single-electron transistors (SETs) with different I_d - V_g characteristics, just like the CMOS inverter (Ono et al., 2000). The input/output signals are represented by node voltages. The only difference is that the operations of SETs require much smaller energy than MOS transistors. We argue that, this scheme does not release the full potential of SEDs. Actually, the single-electron technology would represent a revolution not only in scaling down but also in its physical foundation of the electron charge discreteness devices. The recent development of single-electron turnstile already allows us to accurately control the transfer of single-electrons and at relative high temperature (Nishiguchi et al., 2006). In this chapter, we will show that, by using single-electron transfer devices to manipulate the transfer of single-electrons, it is able to implement smarter arithmetic circuits with very compact structures and impressive circuit performances.

Arithmetic circuits like adder and multiplier are regarded as very critical components in modern information-processing systems. A promising nanoscale adder circuit should have high integration density, low power dissipation and high speed, which is a great challenge. The worst-case propagation delay t_d of a conventional ripple-carry adder is proportional to

its operand length n , so that the operation speed of ripple-carry adder is low. Carry look-ahead adder can reduce t_d to the order of $\log n$, but circuit area are largely increased. An interesting family of adders use non-binary arithmetic algorithms based on high-radix number systems or redundant number systems, such as the signed-digit (SD) adders (Avizienis, 1961) and the redundant-binary (RB) adders (Takagi, 1985). Because the carry propagations in these adders are restricted only to adjoining cells, it is possible to perform addition of two operands in constant time which is not dependent on n (Parhami, 1990; Parhami, 1993). Hereafter these non-binary adders are referred to as fast adders. Fast adders have promising characteristics, but their compact and efficient implementation still remains a big challenge. The conventional approaches use binary MOS logic gates to implement non-binary algorithms so that the adders are complex in circuit structure and are thus hard to design. Moreover, each type of fast adders requires specific consideration to optimize its performance. On the other hand, the multiple-valued current-mode logic (MVCL) approach can significantly reduce the number of devices in the circuit (Kawahito, 1988). However, MVCL suffers from relatively large power dissipation and it results in low overall area-time-power performances. Although novel approach using negative differential-resistance devices can greatly reduces the number of transistors (Gonzalez, 1998), it is only specific to one particular kind of fast adder.

In this chapter, we proposed circuit architecture and design methods to implement novel *fast adders and fast multipliers* by transferring & storing single electrons. We use the number of electrons to represent different logic values and we perform arithmetic operations by accurately manipulating electrons. We propose general fast single-electron adder architecture based on non-binary arithmetic and design methods to implement various fast adder circuits. We adopt the counter tree diagram (CTD) (Sakiyama, 2003) to represent and analyze our fast adders, and we use the MOSFET-based single-electron turnstile as the basic circuit element. We used the unique characteristic of MOSFET-based single-electron turnstile to finish complicated fast-addition arithmetic operations compactly. We propose two design styles to implement fast adder circuit blocks: the threshold approach and the periodic approach. The proposed adder circuits have several advantages: 1) The operation speeds are high; 2) The circuit structures are compact and the number of devices is small; 3) The power dissipations are much lower than conventional circuits; 4) The circuit design method based on the CTD is very simple and can be applied to a wide range of adders. In the following sections, first we introduce the background of single-electron devices and operation principle of MOSFET-based single-electron turnstile. Then we introduce fast addition algorithms and the circuit architecture to perform non-binary fast addition by transferring single-electrons. Then we introduce a family of SE transfer circuits based on MOSFET-based SE turnstile. Next we show the principles of the threshold approach and the periodic approach, and we show adder design examples for each approach. After that we study and compare the performances of the proposed adders. Finally, we summarize the results.

2. MOSFET-based Single Electron Turnstile

2.1 Working Principle

First we introduce the basic device of our work: the single-electron (SE) turnstile. MOSFET-based single-electron turnstile is a very promising SE transfer device, which could

accurately control the number of transferred electrons using the Coulomb blockade effect (Fujiwara, 2008). Room-temperature (RT) operation of a SE multilevel memory and RT operation of a digital-analog converter circuit (Nishiguchi, 2006) consisting of MOSFET-based SE turnstiles have been experimentally demonstrated. Fig. 1(a) shows the device structure of the SE turnstile. The turnstile has two MOSFETs, FET1 and FET2. The FET1 and FET2 are gate-all-around Si-nanowire MOSFETs on SOI wafer. By turning FET1 and FET2 on and off alternately, the single electrons are transferred from the source to the drain, like conventional charge-coupled devices (CCDs). Fig. 1 (b) shows a SEM picture of the SE turnstile (Fujiwara, 2004). Fig. 1(c) shows the equivalent circuit of the SE turnstile, which includes a source S, a drain D, a gate voltage terminal G and two clock voltage terminals $clk1$ and $clk2$. In the following circuits, the source of the SE turnstile is connected to a supply voltage, V_{ss} or $-V_{ss}$. The drain V_D is always connected to an electron storage node (SN), and it can be regarded as virtually grounded. The single electrons can be injected into the SN or ejected from the SN through the SE turnstile (Zhang, 2007a). The number of electrons in the SN can be detected by using the single-electron transistor as an electrometer. Experimentally, a SN with small capacitance C_{SN} can be realized by a silicon nanodot on SOI wafer.

Fig. 1(d) shows the pulse sequences for V_{clk1} and V_{clk2} applied to the gates of FET1 and FET2, respectively. The SE turnstile operation requires two repulsive voltage pulses with a duty cycle less than 50%. Fig. 1(e) shows how the electrons are transferred from the source to the SN, according to steps (i)-(iv) shown in Fig. 1(d). The source of the SE turnstile is biased by $-V_{ss}$ and V_G is negative. When both FET1 and FET2 are turned off, a single-electron-box (SEB) is electrically formed. Note that, the size of the SEB is much smaller than its lithography definition, due to the barriers of the two MOSFETs. The SEB is small enough to activate the Coulomb blockade effect. Since the SEB and source are separated by FET1, the potential of the SEB is only controlled by the gate voltage V_G via electrical coupling. Therefore, the number of captured electrons N_s is determined by the difference between V_G and $-V_{ss}$. Assuming an ideal case at working temperature $T=0$, N_s is given by (Zhang, 2008):

$$N_s = 0, \text{ if } V_G \leq -V_{ss}; \quad (1)$$

$$N_s = [(V_G + V_{ss}) / V_0 + 1/2], \text{ } V_0 = e / C_{ug}, \text{ if } V_G > -V_{ss}.$$

where V_0 is defined as constant logic value 1, C_{ug} is the capacitance between the gate and the SEB, and $[X]$ denotes the maximum integer which is smaller than X . When FET2 is turned on, the SEB is connected to the SN [step (iii)]. The capacitance of SN C_{SN} is much larger than the capacitance of the SEB, so when the electrons enter the SN, its potential change can not affect the behavior of the SE turnstile and thus can be neglected. Therefore we assume the potential of the SN is always 0V for simplicity. When $V_G < 0$, the potential of the SEB is higher than the SN so that all single electrons flow into the SN. In this case, the number $N=N_s$ of electrons transferred depends exclusively on V_G . On the other hand, when $V_G > 0$, not all electrons flow out of the SEB. In this case N only depends on the potential difference between the source and the SN. Finally FET2 is turned off [step (iv)], and a transfer cycle is finished. In summary, when the SE turnstile injects electrons into the SN, N is given by:

$$N = 0, \text{ if } V_G \leq -V_{ss};$$

$$N = [C_g(V_G + V_{ss}) / e + 1/2], \text{ if } -V_{ss} < V_G < 0;$$

$$N = [C_g V_{ss} / e + 1/2], \text{ if } V_G \geq 0. \quad (2)$$

Similarly, electrons can be ejected from the SN. In this case the source of the SE turnstile is connected to V_{ss} and V_G is positive. In this case, the number of captured electrons N_d in the SEB is determined by the potential difference between the SEB and SN. In step (iii) and step

(iv), electrons flow out of the SEB to the source. When $V_G < V_{ss}$, the potential of the SEB is higher than the source, and all electrons flow out of the SEB. So $N = N_d$ also depends exclusively on V_G . On the other hand, when $V_G > V_{ss}$, the potential of the SEB is lower than the source, and not all electrons flow out of the SEB. In this case N also only depends on V_{ss} . In summary, when the SE turnstile ejects electrons from the SN, N is given by:

$$\begin{aligned} N &= 0, \text{ if } V_G \leq 0; \\ N &= [C_g V_G / e + 1/2], \text{ if } 0 < V_G < V_{ss}; \\ N &= [C_g V_{ss} / e + 1/2], \text{ if } V_G \geq V_{ss}. \end{aligned} \quad (3)$$

The relationships between N and V_G , V_{ss} are summarized in Fig. 2(a). From equations (2) and (3) we see that, the gate voltage V_G directly controls N . Fig. 2(b) shows the relationship between N and V_G when V_{ss} is large enough. N is a periodical staircase function of V_G . This unique characteristic of SE turnstile makes the single-electron transfer highly flexible.

The parameters of the SE turnstile are determined as follows. Transfer error may occur in the transfer cycle. To reduce transfer errors, the capacitance of the SEB C_{SEB} must be small enough. Since a 0.76aF C_{SEB} was reported (Nishiguchi, 2006), we choose $C_{SEB} = 0.7\text{aF}$ and we choose $T = 60\text{K}$ to ensure low transfer error rate. We choose $C_{ug} = 0.53\text{aF}$ so that $V_0 = 0.3\text{V}$, and thus the circuit can have large noise margin.

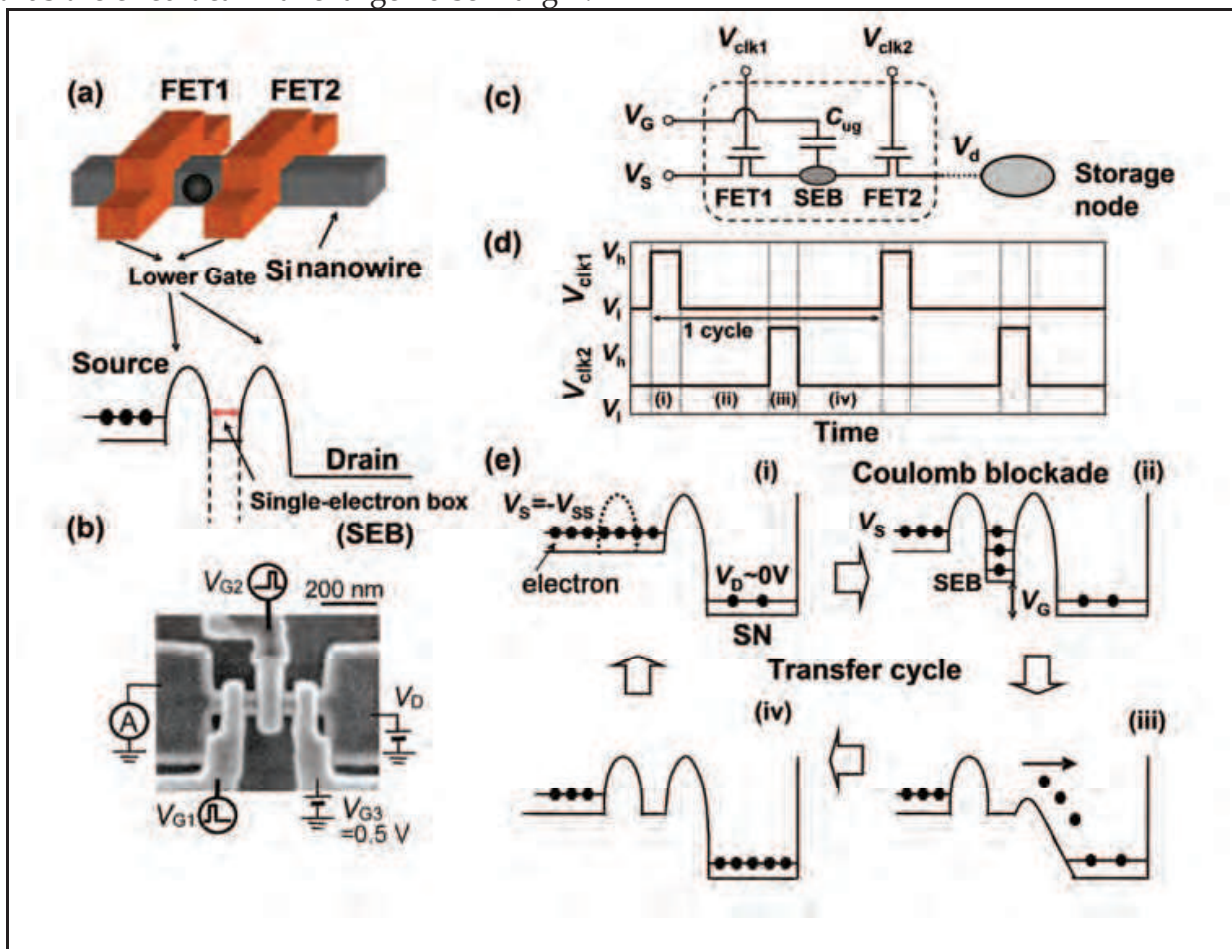


Fig. 1. (a) Device structure of the MOSFET-based SE turnstile. (b) SEM picture of the SE turnstile (Fujiwara, 2004). (c) Equivalent circuit of the SE turnstile. The drain connects to a storage node (SN). (d) Repulsive clock pulses for the SE turnstile operation. (e) Schematic diagram to accurately inject electrons into the SN. A transfer cycle has 4 steps.

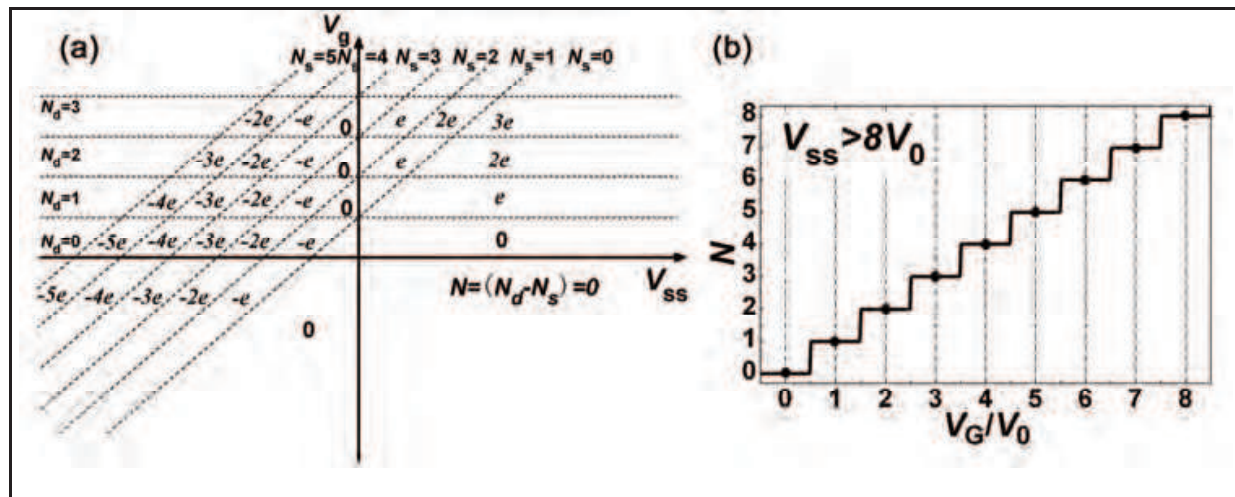


Fig. 2. (a) Relationship between the transfer electron number N with gate voltage and source voltage; (b) N as a function of gate voltage.

2.2 SPICE Simulation Model

Although the MOSFET-based turnstile is composed of MOSFETs, its behavior can not be directly simulated by SPICE because SPICE always assume that currents are continuous and thus can not handle the stochastic behavior of SE transfer. We proposed a behavioral SPICE model to simulate the MOSFET-based SE turnstile (Zhang, 2007c; Zhang 2008). The simplified model schematic is shown in Fig. 3. The most essential points of the model are: 1) to represent the discrete single-charge transfer event as a δ -type current $i_t = e\delta(t-t_0)$, where t_0 is the time of the transfer event; 2) to model the stochastic electron transfer by using random number generator. Although the transfer event is a complex random process, we assume that t_0 is the time when

$$ep = \int_0^{t_0} I_d(t) dt \quad (4)$$

where $I_d(t)$ is the current through the MOSFET and p is a random number distributed uniformly from 0 to 1, which represents the randomness of the transfer process.

In the model, the SEB is modeled as a pure capacitor with capacitance C_{SEB} . G1 is a voltage-controlled current mirror of I_1 , and it is controlled by the output of module P1. With the falling clock of $clk1$, C_{SEB} is charged and its voltage V_{SEB} is feed back to module P1. The number of electrons stored in the SEB N_{SEB} is controlled by V_g . When $V_{SEB} > N_{SEB}e/C_{SEB}$, the output of P1 shut off G1, so the equivalent charge stored in the SEB is exactly $N_{SEB}e$. A noise source generates a noise voltage to module P1, so N_{SEB} is randomly changed by the noise voltage with a possibility ε , and ε corresponds to the transfer error rate of the SE turnstile. With $clk1$, N_{SN} electrons are equivalently stored in C_{SEB} . With the rising clock of $clk2$, these electrons are transferred from C_{SEB} to drain one by one. G2 is a current mirror of I_2 . With the rising clock of $clk2$, G2 charges C_E . When the charge on C_E is larger than ep in (4), we assume that a SE transfer event will happen. Then the output of module P2 resets the charge on C_E to 0 and transiently enables G3 so that G3 outputs a delta-shape current pulse, as shown in Fig. 3. The area of the delta-shape current pulse is exactly e , and we use this current pulse to represent SE transfer. G3 is transiently opened for N times until all electron flow to the drain.

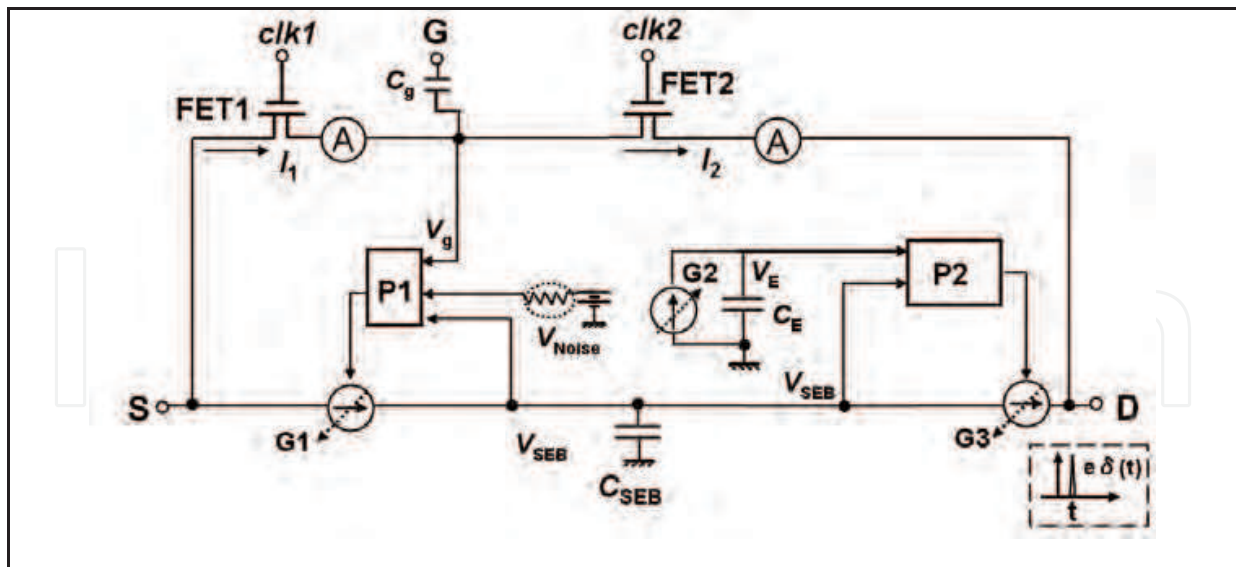


Fig. 3. SPICE circuit model of MOSFET-based single-electron turnstile

2.3 Electron Transfer Circuit Elements

Fig. 4 shows a family of SE transfer circuits using the MOSFET-based SE turnstile. These basic electron transfer circuits serve as the basic building blocks of single-electron arithmetic circuits. The circuit symbol of SE turnstile has terminals G, S and D. The linear ejector (LE) is simply a SE turnstile. It ejects N electrons from the SN per cycle and N depends on V_G according to (3). After one cycle, N_{SN} is decreased by N . In the linear injector (LI), V_G is summed with $-V_{ss}$ by a voltage adder and is then connected to the G terminal of the SE turnstile. The relationship between N and V_G is same as in the LE, according to (2). The fixed ejector (FE) has an E terminal. The $clk2$ terminal of the SE turnstile connects a PMOS transistor in series, and E connects the gate of the PMOS transistor. The G terminal of the SE turnstile connects a constant bias $V_G = NV_0$. When we apply high voltage (V_{ss}) to E, the PMOS transistor cuts off, and no electrons are transferred by the SE turnstile. When we apply low voltage ($-V_{ss}$) to E, the PMOS transistor turns on and N electrons are ejected per cycle. Similarly the fixed injector (FI) also has an E terminal and it injects N electrons into the SN per cycle if we apply $-V_{ss}$ to E.

Fig. 5 shows the schematics and functions of other useful circuit elements. The voltage adder is simply composed of capacitors with equal capacitances. The voltage divider consists of two capacitors C_1 and C_2 . The function of the voltage divider is $V_{out} = V_{in}/f$, where $f = (C_1 + C_2)/C_1$ is the division factor. The threshold inverter is a CMOS inverter and its logic threshold value is set to $(t-1/2)V_0$, where t is a designated integer. The reset circuit is a NMOS transistor with its drain connected to the ground. When a clock pulse is applied, all electrons flow out of the SN and the logic value of the SN is reset to 0.

The charge-voltage converter is a SET/MOS hybrid circuit and can readout the number of electrons stored in the SN. It consists of a dual gate SET, a PMOS transistor as a constant current source, and a NMOS transistor as a cascode device. The operation principle and implementation details of the SET/MOS hybrid circuit were investigated (Zhang, 2007b). The SET acts as a very sensitive electrometer. The output voltage of the SET/MOS hybrid circuit depends linearly on the input voltage and it can accurately represent N_{SN} , as shown in Fig. 5.

Name	Charge Reservoir	Linear Ejector (LE)	Linear Injector (LI)	Fixed Ejector (FE)	Fixed Injector (FI)
Symbol					
Schematic					
Function	$V_{CR} = -N_{CR}e/C_{CR}$ N_{CR} : number of electrons in the ER	$N_{CR}(t) = N_{CR}(t-1) - N$ $N = V_G/V_0 + 1/2 $	$N_{CR}(t) = N_{CR}(t-1) + N$ $N = V_G/V_0 + 1/2 $	If E is low $N_{CR}(t) = N_{CR}(t-1) - N$	If E is low $N_{CR}(t) = N_{CR}(t-1) + N$

Fig. 4. A family of SE transfer circuits based on MOSFET-based SE turnstiles. The schematic includes the symbol of the SE turnstile.

Name	Voltage adder	Voltage divider	Threshold inverter	Reset circuit	Charge-Voltage converter
Symbol					
Schematic					
Function	$V_{out} = (V_1 + V_2 + \dots + V_n)$	$V_{out} = V_{in}/f$ $f = (C_1 + C_2)/C_1$			

Fig. 5. Symbol, circuit schematic and function of other useful circuit elements.

3. Architecture of Single-electron Fast Adder

3.1 Fast addition algorithm and counter tree diagram (CTD)

The number system in the fast adder belongs to a generalized signed-digit (GSD) number system (Parhami, 1990). The operands belong to the digit set $\{-a, a+1, \dots, \beta\}$, where both a and β are positive integers or zero. The redundancy index ρ of the GSD number system is defined as $\rho = a + \beta + 1 - r$, where r is the number representation radix. For limited carry propagation, ρ must be larger than 0. The algorithms of the fast adders have been intensively studied. According to the number system used and its redundancy, the fast addition algorithms can be classified into many categories, such as carry-free, limited-carry, stored-carry, etc. Given a particular number system, there may be several valid choices for the range of carries and intermediate variables. Because these algorithms are quite complicated, it is difficult to image a circuit schematic only from definitions and equations.

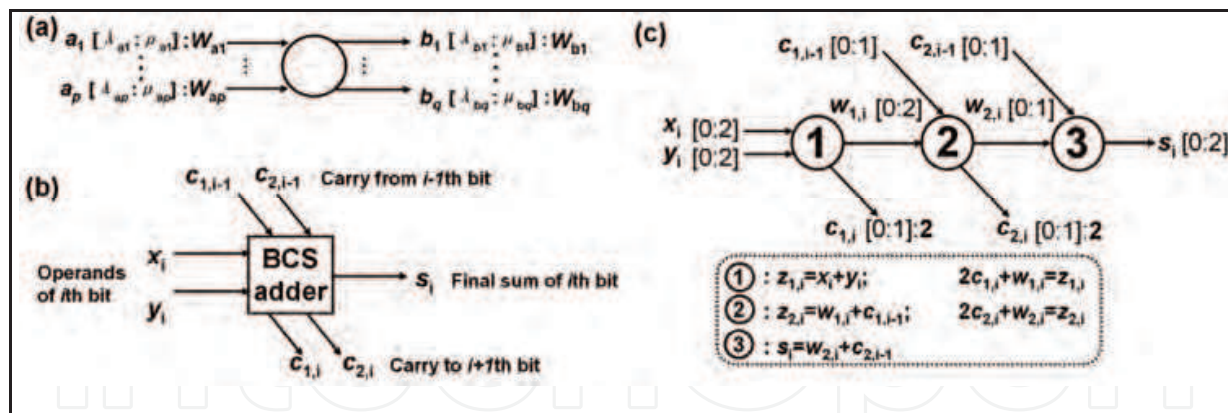


Fig. 6. (a) Symbol of a p -input & q -output counter node in the CTD. (b) Schematic of the i th bit BCS adder. (c) CTD representation of the BCS algorithm.

The counter tree diagram (CTD) is a graphic tool to represent fast addition algorithms and to design the adder circuits (Sakiyama, 2003; Homma, 2004). The CTD is a network that consists of counter nodes and directed edges. The directed edge is an abstraction of the flow of integer data between the counter nodes. Each directed edge is associated with a variable and a weighted interval $[\lambda_{a1}; \mu_{a1}] : w_{a1}$. Here a_1 is the variable name, $[\lambda_{a1}; \mu_{a1}]$ is the range of a_1 and w_{a1} is the weight. If the weight is 1, then it is not shown for simplicity. The counter node is an abstraction of a multi-operand addition function. Fig. 6(a) shows the symbol of a p -input & q -output counter node. The counter node receives p input variables a_1, a_2, \dots, a_p through the p directed edges and generates q output variables b_1, b_2, \dots, b_q through the q directed edges while keeping

$$\sum_{i=1}^p w_{ai} a_i = \sum_{j=1}^q w_{bj} b_j \quad (5)$$

Here p input variables a_1, a_2, \dots, a_p are associated with p ranges and weights $[\lambda_{a1}; \mu_{a1}] : w_{a1}, \dots, [\lambda_{ap}; \mu_{ap}] : w_{ap}$, respectively, and q outputs variables b_1, b_2, \dots, b_q are associated with q ranges and weights $[\lambda_{b1}; \mu_{b1}] : w_{b1}, \dots, [\lambda_{bq}; \mu_{bq}] : w_{bq}$, respectively. The weights denote the arithmetic relationships between the input variables and output variables. The variables and their ranges are clearly shown in Fig. 6(a).

The CTD provides a uniform graphic tool to depict the algorithms of different adders. We consider the addition of two n -bit operands $X=(x_{n-1} \dots x_1 \dots x_0)$ and $Y=(y_{n-1} \dots y_1 \dots y_0)$ using the radix-2 binary carry-save (BCS) algorithm. The addition requires $(n+1)$ identical BCS adders operating in parallel. The symbol of the i th BCS adder is shown in Fig. 6(b). The adder receives two carries $c_{1,i-1}, c_{2,i-1}$ from the $(i-1)$ th adder and the i th input operands x_i and y_i . The adder outputs the sum s_i and two carries $c_{1,i}, c_{2,i}$ to the $(i+1)$ th adder. Fig. 6(c) shows one type of the CTD representation of the i th BCS adder (Homma, 2004). The CTD shows that the adder consists of 3 stages and the carry propagation length is two, and it directly represents the algorithm of BCS addition. We can directly write the following steps to perform addition of X and Y :

$$\begin{aligned} 2c_{1,i} + w_{1,i} &= x_i + y_i; \\ 2c_{2,i} + w_{2,i} &= w_{1,i} + c_{1,i-1}; \\ s_i &= w_{2,i} + c_{2,i-1}; \end{aligned} \quad (6)$$

where x_i and y_i are the i th bits of the input operands, $s_i \in [0:2]$ is the final sum of the i th adder, $c_{1,i}, c_{1,i-1} \in [0:1]$ and $c_{2,i}, c_{2,i-1} \in [0:1]$ are carries (transfer digits), and $w_{1,i} \in [0:2]$ and $w_{2,i}$

$\in [0:2]$ are two intermediate variables. The equations and range of variables are clearly shown in Fig. 6(c). The weight 2 associated with $c_{1,i}$ and $c_{2,i}$ represents the arithmetic relationships in (5). We can further introduce two intermediate sums $z_{1,i}$ and $z_{2,i}$ to show the calculation process more clearly. Then the algorithm of the BCS addition is

$$\begin{aligned} z_{1,i} &= x_i + y_i; & 2c_{1,i} + w_{1,i} &= z_{1,i}; \\ z_{2,i} &= w_{1,i} + c_{1,i-1}; & 2c_{2,i} + w_{2,i} &= z_{2,i}; \\ s_i &= w_{2,i} + c_{2,i-1}; \end{aligned} \quad (7)$$

This algorithm is a representative fast addition algorithm. Generally an n -bit adder consists of $(n+1)$ full adders, and its CTD representation includes $(n+1)m$ counter nodes in all, where m is the CTD stages. In most cases, $m=2$ or $m=3$, according to carry-free algorithms and limited-carry algorithms, respectively (Parhami, 1990). The inputs of the k th counter node in the i th adder are $w_{k-1,i}$ and $c_{k-1,i-1}$, which are the output of the $(k-1)$ th counter node of the i th adder and the $(k-1)$ th carry output of the $(i-1)$ th adder, respectively (In some cases one counter node may receive more than one carries, as discussed later). The k th intermediate sum $z_{k,i}$ is defined as the sum of $w_{k-1,i}$ and $c_{k-1,i-1}$. The outputs of the k th counter node are $w_{k,i}$ and $c_{k,i}$, and $z_{k,i} = r c_{k,i} + w_{k,i}$, where r is the number radix.

3.2 General circuit architecture

We realize fast addition algorithms by manipulating SEs. Fig. 6 shows the general circuit structure of an n -bit fast adder. It consists of $(n+1)$ full adders with m -stage circuit blocks. The architecture has a similar structure to the MVCL-based adders. However, we use single electrons instead of currents to finish arithmetic operations. Given an addition algorithm, the first design step is to draw the CTD of the addition algorithm. The second step is to replace m counter nodes with m circuit blocks and replace the directed edges with the flow paths of the SEs, as shown in the bold lines in Fig. 6(a). The electron numbers are directly used to represent the variables. The arithmetic operations and the transfer of variables are finished by manipulating the SEs. The transfer of SEs in the i th adder is as follows. First, x_i and y_i electrons are transferred into the first circuit block. The first block performs the operation by following the addition algorithm, and then it outputs $w_{1,i}$ electrons and $c_{1,i}$ electrons to the 2nd block of the i th adder and to the 2nd block of the $(i+1)$ th adder, respectively. Similarly, the k th block receives $w_{k-1,i}$ and $c_{k-1,i-1}$ electrons from previous circuit blocks, and it outputs $w_{k,i}$ electrons to the $(k+1)$ th block of the i th adder and $c_{k,i}$ electrons to the $(k+1)$ th block of the $(i+1)$ th adder. Finally, the m th block outputs s_i electrons as the final sum.

Fig. 6(b) shows the circuit structure of the 1st, 2nd, ..., $(m-1)$ th circuit blocks in the i th adder. It consists of an electron storage node (SN), a charge-voltage converter, a reset circuit, and move electron blocks (MVEs) M_w , M_c . The SN connects to SE transfer devices, and SEs can be injected into the reservoir or ejected from the reservoir through the SE transfer devices. In the k th circuit block, first $w_{k-1,i}$ and $c_{k-1,i-1}$ electrons are transferred into the k th SN from previous blocks and are added to be $z_{k,i} = w_{k-1,i} + c_{k-1,i-1}$, as shown in Fig. 6(b). Then, $z_{k,i}$ electrons are stored there. The charge-voltage converter is a SET/MOS hybrid circuit. It readouts the number N_{SN} ($=z_{k,i}$) of the electrons stored in the SN and converts it to the output voltage signal $z_{k,i}V_0$, where V_0 is defined as the voltage of logic 1. Next, this output voltage is applied to the MVEs M_w and M_c . The proposed MVEs are mainly composed of the SE transfer devices. The number of electrons transferred through the MVEs can be accurately controlled by its input voltages. The M_w and the M_c blocks output $w_{k,i}$ and $c_{k,i}$

electrons, respectively. The combination of the SN, the charge-voltage converter, and the MVEs realizes the functions of the CTD counter nodes. The single electrons are transferred between the blocks stage by stage. After one circuit block has finished its function, the reset circuits release the electrons stored in the SN to the ground for the next operation cycle. Fig. 6(c) shows the structure of the last circuit block. It consists of a SN and a reset circuit. It receives $c_{m-1,i-1}$ and $w_{m-1,i}$ electrons so that $s_i = c_{m-1,i-1} + w_{m-1,i}$ electrons are stored in the SN as the adder's output. These electrons can be transferred to other circuits or converted to a voltage signal for further operations.

One merit of the above circuit structure is that the circuit implementation of an arbitrary addition algorithm can be directly obtained by mapping its CTD to the electrons flow paths and the MVEs. The arithmetic operations are achieved by accurately manipulating the single electrons, and the flexible SE transfer devices lead to simple and compact realization of MVEs. In the following sections, we will use the family of SE transfer circuits to build the MVEs.

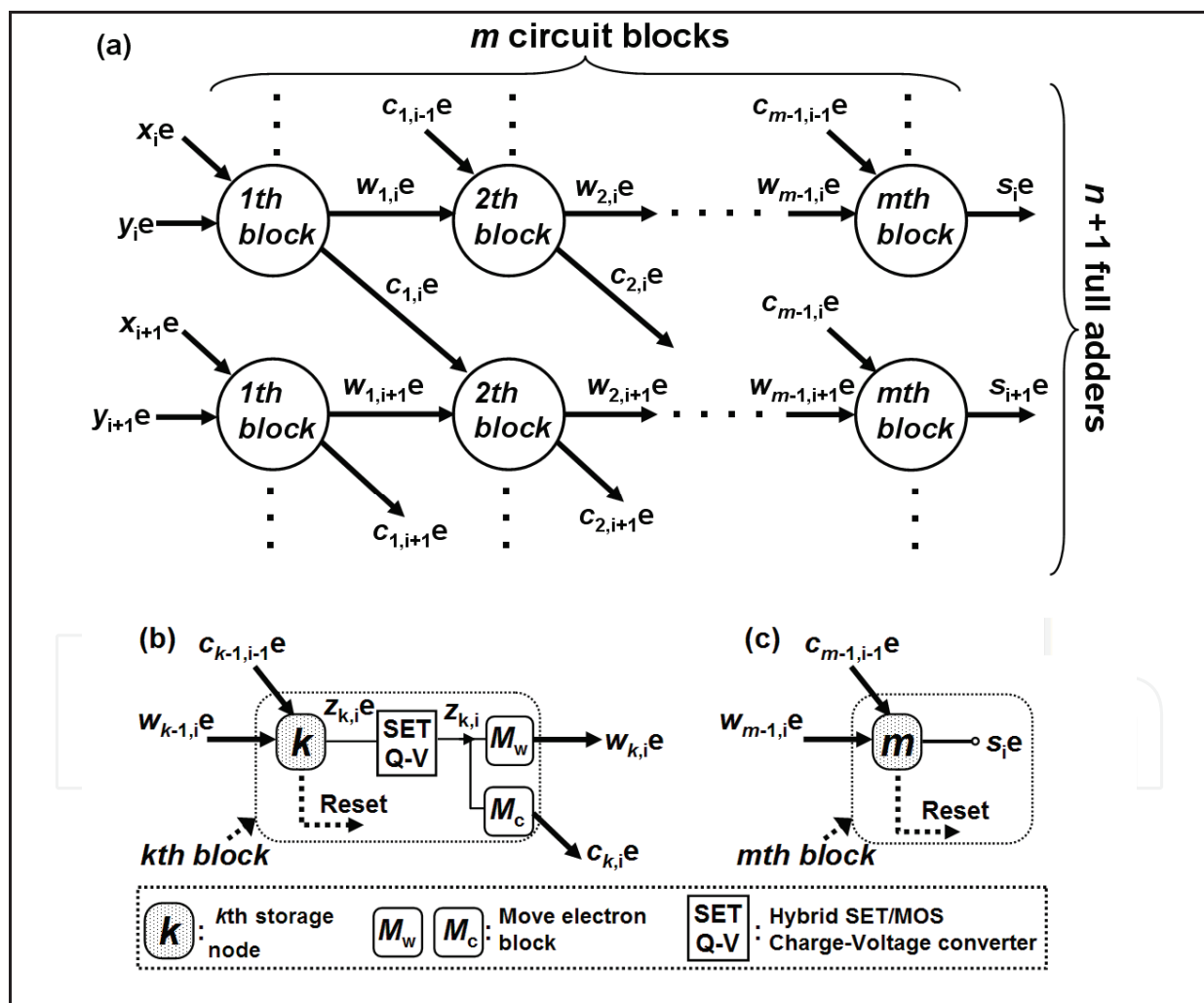


Fig. 6. (a) General circuit structure to implement fast adders by manipulating single-electrons. Each bit addition circuit has m circuit blocks. The bold arrows represent the flow paths of electrons. (b) Circuit schematic of the 1st, 2nd,...,($m-1$)th circuit blocks. (c) Circuit schematic of the m th circuit blocks.

4. Design of Single-electron Adder Circuits

In previous sections, we have shown the novel circuit architecture. The main task in circuit design is to implement the MVEs. In this section, we show two approaches to design the MVEs using the proposed family of SE transfer circuits.

4.1 Threshold Approach

The functions of the MVEs M_w and M_c are to output $w_{k,i}$ electrons and $c_{k,i}$ electrons, respectively, when a voltage signal $z_{k,i}$ is inputted. The values of $w_{k,i}$ and $c_{k,i}$ are obtained from the equation $z_{k,i} = r c_{k,i} + w_{k,i}$. Without loss of generality, we assume $c_{k,i}$ belongs to the interval $[0;\mu]$. The idea of the threshold approach is to compare $z_{k,i}$ with $\mu+1$ integer threshold constants $t_1, \dots, t_{\mu+1}$, and to obtain $c_{k,i}$ and $w_{k,i}$ from the comparison results. Here $t_\mu > t_{\mu-1} > \dots > t_1, t_{\mu+1} = \infty$. If $t_j \leq z_{k,i} < t_{j+1}$, then j comparison results are '1' and thus $c_{k,i} = j$. The comparison process is graphically shown in Fig. 7(a). We can obtain $c_{k,i}$ and $w_{k,i}$ from $z_{k,i}$ by performing all of the following conditional statements:

$$\begin{aligned}
 & \text{Initial } c_{k,i} = 0, w_{k,i} = z_{k,i} \\
 & \text{if } z_{k,i} \geq t_1, \text{ then } c_{k,i} \rightarrow c_{k,i} + 1, w_{k,i} \rightarrow w_{k,i} - r; \\
 & \text{if } z_{k,i} \geq t_2, \text{ then } c_{k,i} \rightarrow c_{k,i} + 1, w_{k,i} \rightarrow w_{k,i} - r; \\
 & \dots\dots\dots \\
 & \text{if } z_{k,i} \geq t_\mu, \text{ then } c_{k,i} \rightarrow \mu, w_{k,i} \rightarrow w_{k,i} - r.
 \end{aligned} \tag{8}$$

From this algorithm, the circuit implementation of the M_c block has μ conditional FIs and μ inverters, as shown in Fig. 7(b). We use the output results of the inverters to control the operations of the SE turnstiles. The logic threshold value of the j th threshold inverter is t_j , and its output terminal is connected to the E terminal of the j th FI. The j th threshold inverter and the j th FI correspond to the $(j+1)$ th statement in (8). If $t_j \leq z_{k,i} < t_{j+1}$, then j FIs are enabled and each FI ejects one electron into the SN. Therefore the overall M_c block injects $c_{k,i} = j$ electrons into the SN. Similarly, the M_w block has one LI, μ threshold inverters and μ FEs, as shown in Fig. 7(c). The LI's G terminal connects the input voltage, so LI injects $z_{k,i}$ electrons into the k th SN. If $t_j \leq z_{k,i} < t_{j+1}$, j FEs are enabled, and each FE ejects r electrons from the SN. Thus, the overall M_w block injects $w_{k,i} = z_{k,i} - jr$ electrons into the SN.

In summary, the threshold approach uses threshold inverters as comparators. The intermediate variables are obtained from the comparison results. To optimize the adder circuits, μ should be as small as possible.

Example1: Design of a BCS adder

The algorithm for the BCS adder was shown in (1). Fig. 8(a) shows one type of CTD of the BCS adder. Both $c_{1,i}$ and $c_{2,i}$ belong to $[0:1]$. Fig. 8(b) shows the characteristics of $w_{k,i}$ and $c_{k,i}$ as functions of $z_{k,i}$. We see that $c_{k,i} = 1$ is a simple threshold function of $z_{k,i}$, and $w_{k,i}$ and $c_{k,i}$ are:

$$\begin{aligned}
 & w_{1,i} = z_{k,i}, c_{k,i} = 0 \quad \text{if } z_{k,i} < 2, \\
 & w_{1,i} = z_{k,i} - 2, c_{k,i} = 1 \quad \text{if } z_{k,i} \geq 2. \quad (k=1 \text{ or } 2).
 \end{aligned} \tag{9}$$

Fig. 8(c) shows the schematic of the BCS adder using the threshold approach. The circuit consists of 3 blocks, since the CTD has 3 stages. The M_w block consists of a LI, an inverter, and a FE, since $\mu = 1$. The M_c block simply consists of a FI and it shares the inverter with the M_w block. The circuit has 29 transistors.

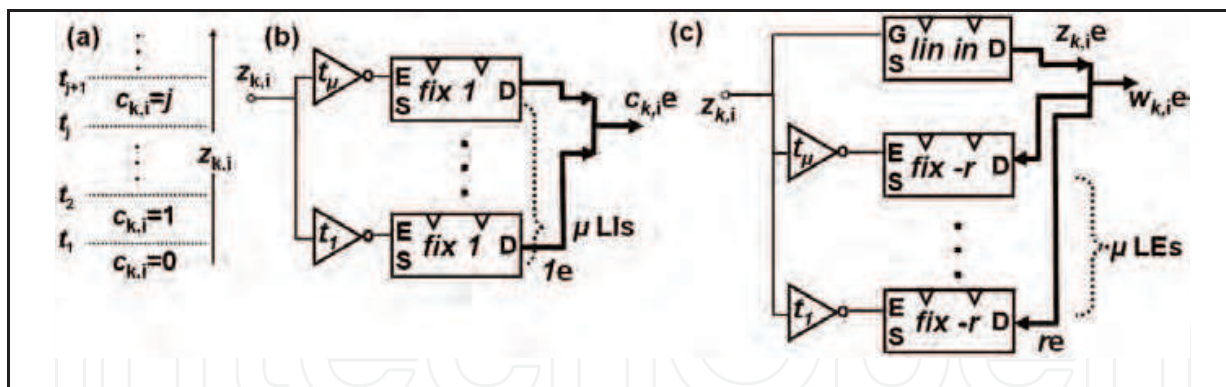


Fig. 7. (a) The threshold approach compares $z_{k,i}$ with comparison constants and obtains $c_{k,i}$ from comparison results. (b) Schematic of the M_c block and (c) Schematic of the M_w block.

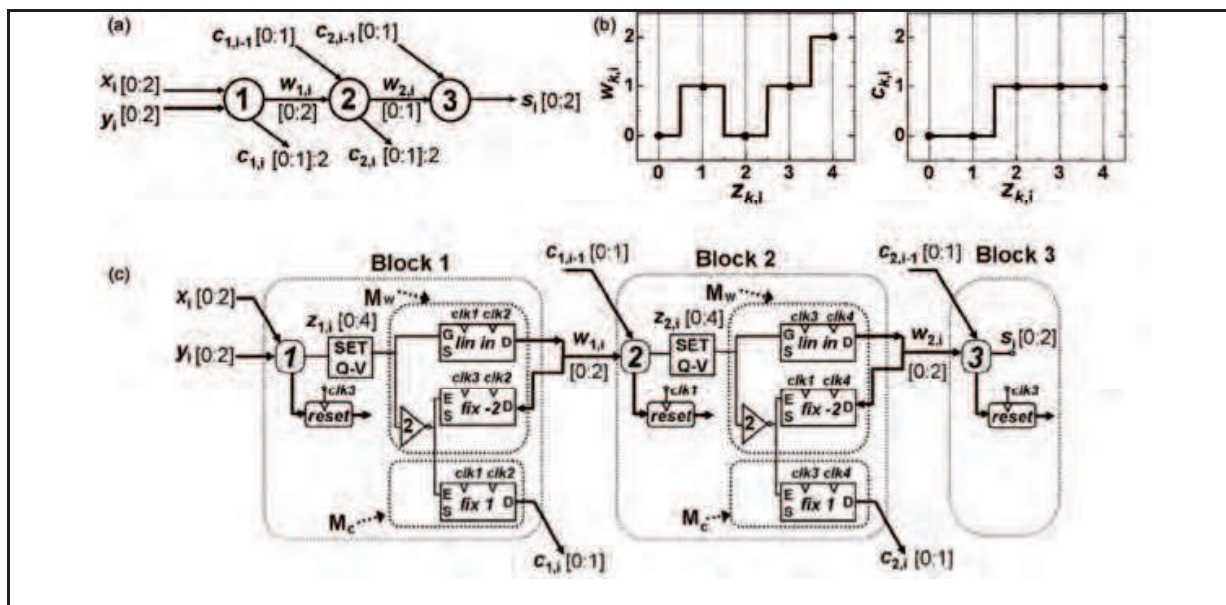


Fig. 8. (a) CTD representation of the BCS adder. The carries $c_{1,i}$ and $c_{2,i}$ belongs to interval $[0:1]$. (b) Characteristics of $w_{k,i}$ and $c_{k,i}$ as functions of $z_{k,i}$. (c) Schematic of the BCS adder circuit using threshold approach. The circuit consists of three circuit blocks.

The circuit requires 4 repulsive clock signals, $clk1$, $clk2$, $clk3$ and $clk4$, as shown in Fig. 9(a). Each SE turnstile is associated with two clock signals. Fig. 9(b) shows the change in the number of electrons in the 2nd SN and 3rd SN with time. With the rising edge of $clk2$, $z_{1,i}$ electrons enter into the 2nd SN from the LI, as shown in Fig. 9(b). Also $c_{1,i-1}$ electrons are injected to 2nd SN by the $(i-1)$ th adder. With the falling edge of $clk2$, electrons are ejected from the 2nd SN by the FE of the first block. Then $w_{1,i}=2$ electrons remain in the 2nd SN. After $clk2$ the first block finishes its function. Similarly, with the rising edge of $clk4$, $w_{1,i}$ electrons enter into the 3rd SN from the LI and $c_{1,i-1}$ electrons enter into the 3rd SN from the FI. With the falling edge of $clk4$, electrons are ejected from the 3rd SN by the FE. After the falling edge of $clk4$, exactly $s_i=1$ electron remains in the 3rd SN, and the second block finishes its function. Electrons retain in the 2nd SN until the second block finished its function, and the electron number is reset to 0 by $clk1$. The circuit performs the addition operation by repeating the clock sequences.

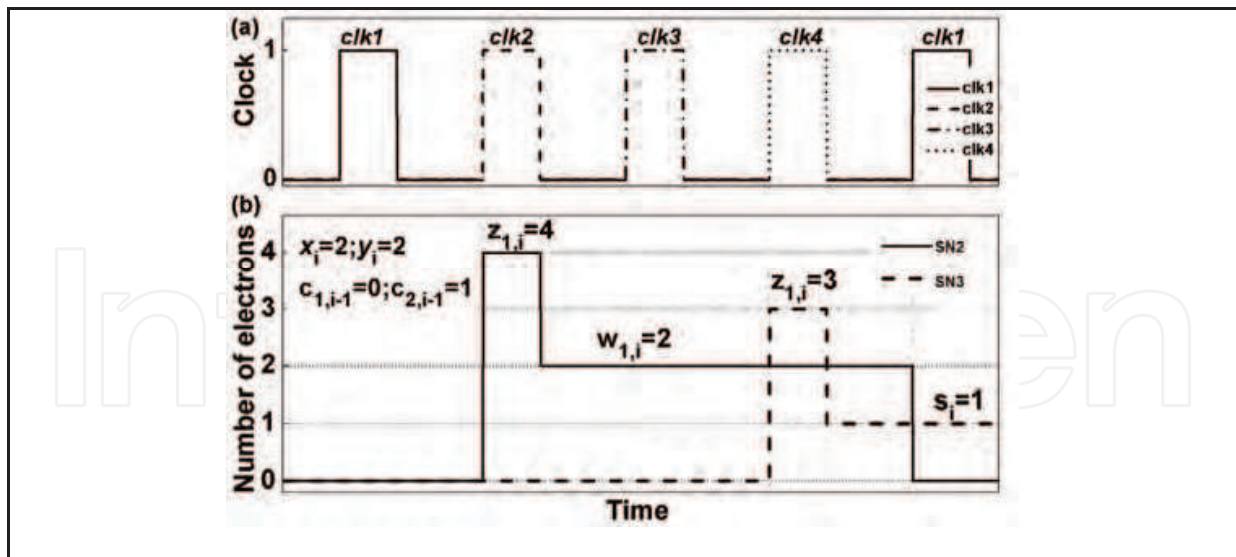


Fig. 9. (a) Clock sequences for the circuit. (b) Number of electrons in SN2 and SN3 as a function of time. After *clk4*, electrons number of SN3 corresponds to the final sum s_i .

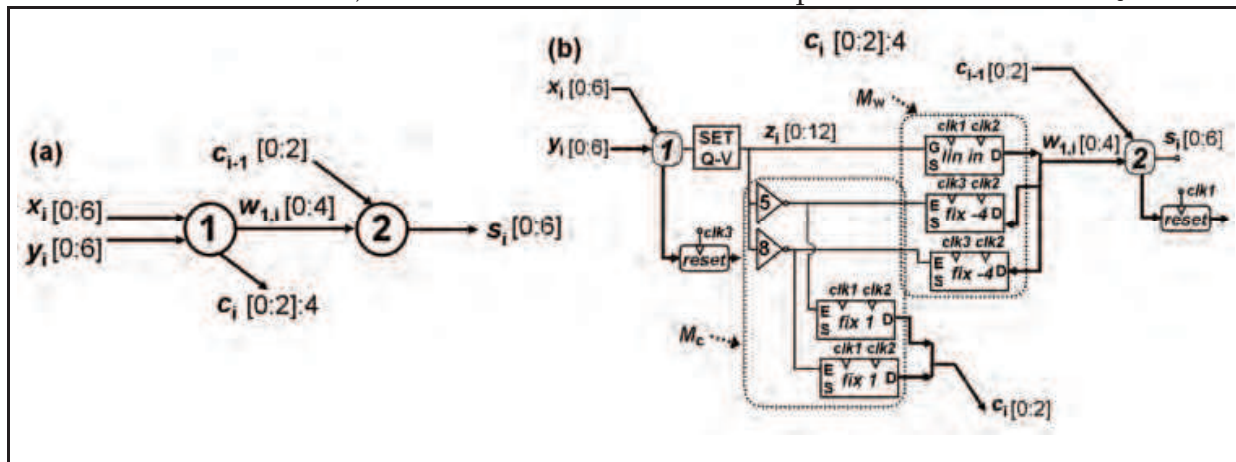


Fig. 10. (a) CTD of the SD4,3 adder. (b) Schematic of the SD4,3 adder circuit using threshold approach.

Example2: Design of a SD4,3 adder

The number system of the SD4,3 adder is the radix-4 signed-digit number system with a digit set [-3:3]. The SD4,3 adder has a redundancy index $\rho=3$ and it belongs to carry-free adders (Kawahito, 1988). However, in our circuit blocks the transfer of electrons is not bi-directional. To prevent complexity in circuit design, we use the digit set [0:6] to replace the former digit set [-3:3] of the SD4,3 algorithm. Fig. 10(a) shows the CTD of the SD4,3 algorithm:

$$\begin{aligned}
 z_i &= x_i + y_i; \\
 4c_{1,i} + w_{1,i} &= z_i; \\
 s_i &= w_i + c_{1,i-1}.
 \end{aligned}
 \tag{10}$$

$$\begin{aligned}
 w_{1,i} &= z_i, \quad c_{1,i} = 0, \quad \text{if } z_{1,i} \leq 4; \\
 w_{1,i} &= z_i - 4, \quad c_{1,i} = 1, \quad \text{if } 4 < z_{1,i} < 8; \\
 w_{1,i} &= z_i - 8, \quad c_{1,i} = 2, \quad \text{if } z_{1,i} \geq 8.
 \end{aligned}$$

Therefore $c_{1,i} \in [0:2]$ and $\mu=2$. Fig. 10(b) shows the adder schematic. The M_w block consists of a LI, two inverters, and two FEs. The M_c block has two FIs. The logic threshold values of the two inverters are 4.5 and 7.5, respectively, according to (10). Since the circuit has only two stages, it requires 3 repulsive clock signals. The circuit performs radix-4 addition using 23 transistors.

4.2 Periodic Approach

The periodic approach realizes the M_w block by circuit elements that have *periodic* transfer functions. In other words, the number of electrons outputted by the M_w block is a periodic symmetric function (PSF) of its input. Assume $z_{k,i}$ belongs to the interval $[0:Z]$ and $c_{k,i}$ belongs to the interval $[0:\mu]$. The periodic approach requires that: (1) $u=[Z/r]$; (2) $c_{k,i}=j$ if $t_j \leq z_{k,i} < t_{j+1}$, where $t_j=jr$, $0 < j \leq \mu$. In this case, $c_{k,i}$ and $w_{k,i}$ are given by:

$$\begin{aligned} c_{k,i} &= [(z_{k,i}+1/2)/r], \\ w_{k,i} &= z_{k,i}-rc_{k,i}. \end{aligned} \quad (11)$$

We propose to use the unique transfer characteristics of the SE turnstile to realize the PSF circuit and thus to finish the fast addition algorithm compactly. Fig. 11(a) shows the implementation of the M_c block. The circuit consists of SE turnstiles and voltage dividers. When $f=1$, the number of electrons transferred N_f equals $z_{k,i}$. Fig. 11(b) shows this case. The division factor f of the voltage divider is designed to be r ($r>1$). The input voltage is added with $V_1=-(f-1)V_0/2$, so according to (2) the number N_f of transferred electrons is $|(z_{k,i}V_0+V_1)/fV_0+1/2|$. This value corresponds to $c_{k,i}$ according to (7). Fig. 11(c) and Fig. 11(d) show the relationships between N_f and $z_{k,i}$ when $r=2$ and $r=4$, respectively.

Fig. 11(e) shows the implementation of the M_w block. Generally, the circuit consists of two voltage adders, two voltage dividers with division ratio f_1 and f_2 , respectively, one LI, and f_2/f_1 LEs. In the special case of $f_1=1$ and $f_2=r$, the circuit includes one voltage divider, one voltage adder, one LI, and r LEs. The LI injects N_{f_1} electrons and each LE ejects N_{f_2} electrons, and the overall M_w block injects $N=N_{f_1}-f_2N_{f_2}$ electrons per cycle. Since N_{f_2} corresponds to $c_{k,i}$, N directly corresponds to $w_{k,i}$ according to (8). Fig. 11(f) and Fig. 11(g) show the relationships between N and $z_{k,i}$ when $f_2=2$ and $f_2=4$, respectively. Both N_{f_1} and $f_2N_{f_2}$ increase monotonically with $z_{k,i}$ and thus their difference N is a PSF of $z_{k,i}$. Fig. 11(h) shows another case when $f_1=2$ and $f_2=4$. In this case, N also has a periodic relationship with $z_{k,i}$. Actually a 3-bit A/D converter can be realized by combining the circuits represented by Fig. 11(d), Fig. 11(h) and Fig. 11(f). It can convert an input voltage to 3-bit binary signal $D_0D_1D_2$.

In summary, the periodic approach specifies the range of intermediate variables so that $c_{k,i}$ is a staircase function of $z_{k,i}$, and $w_{k,i}$ is a PSF of $z_{k,i}$. Since N_f is always a staircase function of $z_{k,i}$, the PSF circuits can be realized using the difference of the number of electrons transferred by the LI and LEs. Compared with conventional PSF circuits, the SE turnstile-based PSF circuit has much fewer transistors.

Example1: Design of a BCS adder

In the BCS adder using periodic approach, $z_{1,i}$ and $c_{1,i}$ belong to $[0:4]$ and $[0:2]$, respectively. Fig. 12(a) shows the BCS adder CTD representation that is suitable for the circuit structure in the periodic approach. Note that the only difference between Fig. 12(a) and Fig. 8(a) is the range of $c_{1,i}$ and $w_{1,i}$. In Fig. 12(a), $c_{1,i}$ belongs to $[0:2]$ while in Fig. 8(a), $c_{1,i}$ belongs to $[0:1]$. Fig. 12(b) shows the relationship between $w_{k,i}$ and $z_{k,i}$. We see that $w_{k,i}$ is a periodic function of $z_{k,i}$. The circuit of the BCS adder using the periodic approach has the same structure as

Fig. 8(c), except for the realization of MVEs. Fig. 12(c) shows the circuit schematic of the first block. Since $r=2$, M_w consist of a voltage divider, a voltage adder, a LI and two LEs, while M_c consists of a LI. The circuit has 25 transistors.

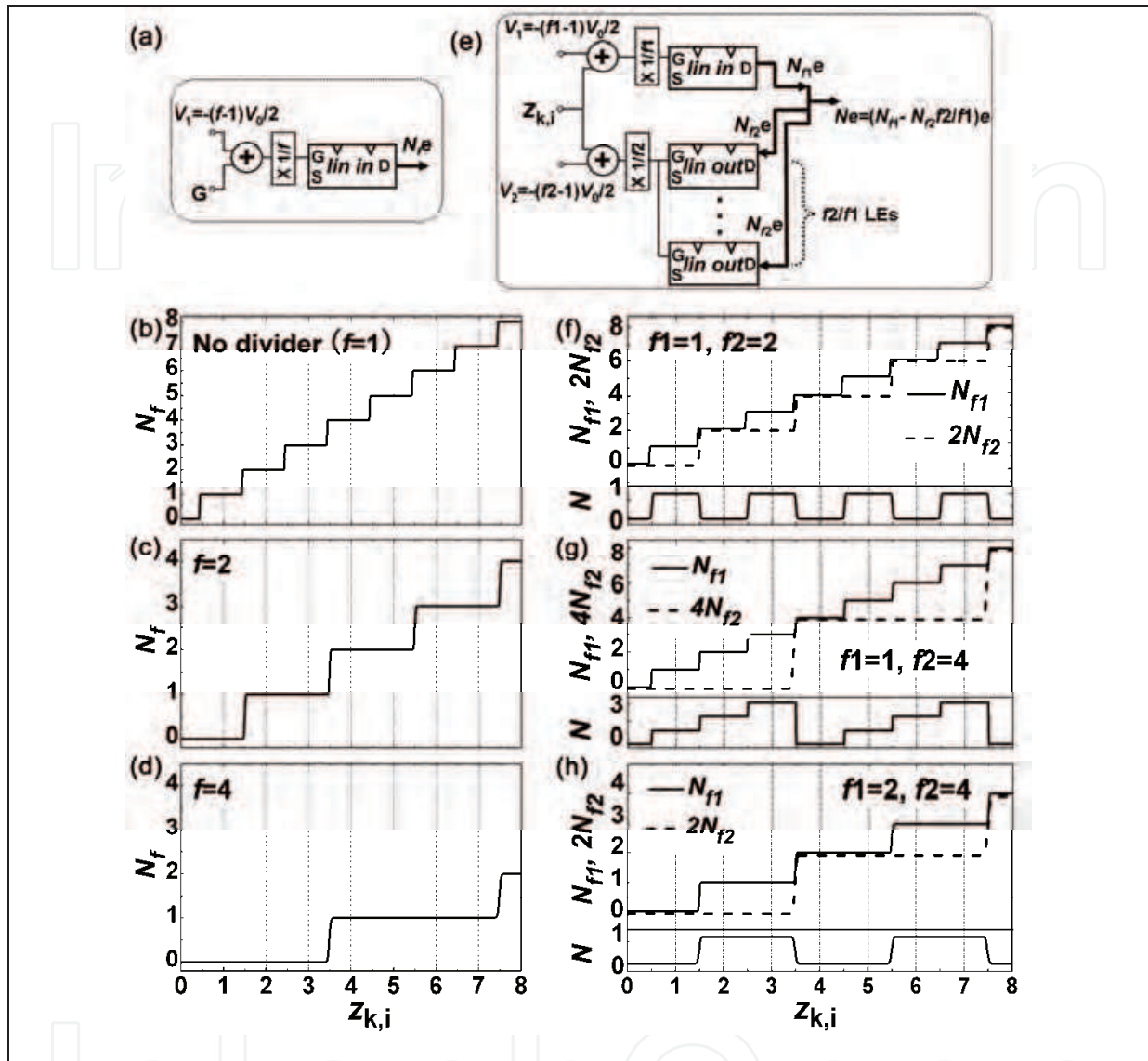


Fig. 11. (a) Schematic of the M_c block using the periodic approach. The circuit has a LI and a voltage divider. (b) Relationship between N_1 and $z_{k,i}$ when $f=1$ (no voltage dividers). (c) Relationship between N_2 and $z_{k,i}$ when $f=2$. (d) Relationship between N_4 and $z_{k,i}$ when $f=4$. (e) Schematic of the M_w block using the periodic approach. The circuit has a LI and f_2/f_1 linear ejectors. (f) Relationship between N and $z_{k,i}$ when $f_1=1, f_2=2$. (g) Relationship between N and $z_{k,i}$ when $f_1=1, f_2=4$. (d) Relationship between N and $z_{k,i}$ when $f_1=2, f_2=4$.

Fig. 8(a) and Fig. 12(a) represent the only two valid 3-stage BCS algorithms. The algorithm represented in Fig. 8(a) is suitable for the threshold approach, while the algorithm shown in Fig. 12(a) is suitable for the periodic approach. Traditional implementations of the BCS adder used the algorithm shown in Fig. 8(a). The algorithm shown in Fig. 12(a) leads to a more compact circuit by using the periodic approach.

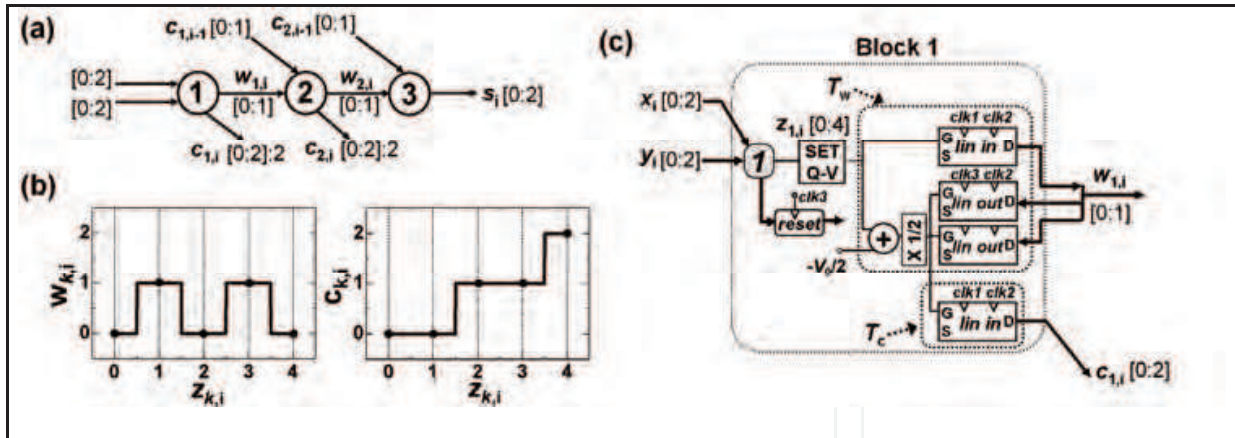


Fig. 12. (a) Another CTD representation of the BCS adder. The carries $c_{1,i}$ and $c_{2,i}$ belongs to interval $[0:2]$. (b) Characteristics of $w_{k,i}$ and $c_{k,i}$ as functions of $z_{k,i}$. (c) Schematic of the BCS adder circuit using periodic approach.

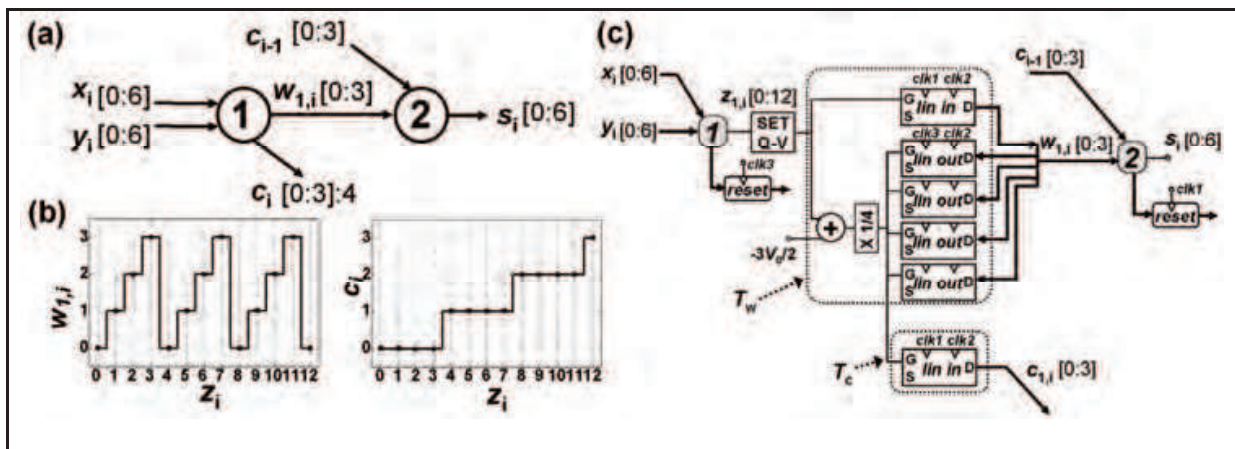


Fig. 13. (a) CTD representation of the SD4,3 adder using the periodic approach. (b) Characteristics of $w_{k,i}$ and $c_{k,i}$ as functions of $z_{k,i}$. (c) Schematic of the SD4,3 adder circuit using periodic approach.

Example2: Design of a SD4,3 adder

In the SD4,3 adder using the periodic approach, $z_{1,i}$ and $c_{1,i}$ belong to $[0:12]$ and $[0:3]$, respectively. Fig. 13(a) shows the other CTD of the SD4,3 adder. The only difference between Fig. 13(a) and Fig. 10(a) is the range of $c_{1,i}$ and $w_{1,i}$. In Fig. 13(a), $c_{1,i}$ belongs to $[0:3]$ while in Fig. 10(a), $c_{1,i}$ belongs to $[0:2]$. Fig. 13(b) shows $w_{1,i}$ and $c_{1,i}$ as functions of $z_{1,i}$. In fact, the characteristics of $w_{1,i}$ are same as in Fig. 11(g), and the characteristics of $c_{1,i}$ are same as in Fig. 11(d). Fig. 13(c) shows the circuit schematic. Since $r=4$, the M_w block has one LI and 4 LEs, and the M_c block consists of a LI. Multiple-valued periodic $w_{1,i}-z_{1,i}$ characteristics are compactly achieved using the SE turnstiles. The circuit has only 17 transistors in all. Actually, Fig. 10(a) and Fig. 13(a) represent the only two valid SD4,3 algorithms. Conventional SD4,3 adders use the algorithm shown in Fig. 10(a). As far as we know, the algorithm shown in Fig. 13(a) has not been implemented by conventional approaches yet.

Example3: Design of a PD2,3 adder

The number system of the PD2,3 adder is the radix-2 positive-digit number system with a digit set [0:3]. The PD2,3 adder is a special adder in which more than 1 carries are transferred between two stages (Parhami, 1989). The CTD of the PD2,3 algorithm is shown in Fig. 14(a). The algorithm for the PD2,3 adder is:

$$\begin{aligned} z_i &= x_i + y_i; \\ 4c_{1,i} + 2c_{2,i} + w_{1,i} &= z_i; \\ s_i &= w_i + c_{1,i-2} + c_{2,i-1}. \end{aligned} \tag{12}$$

Since one circuit block outputs two carries $c_{1,i}$ and $c_{2,i}$, now three blocks M_{c1} , M_{c2} , and M_w are required. Fig. 14(b) shows the characteristics of $w_{1,i}$, $c_{1,i}$ and $c_{2,i}$. If z_i is converted to a 3-bit binary signal $D_0D_1D_2$, then $w_{1,i}$, $c_{2,i}$ and $c_{1,i}$ correspond to D_0 , D_1 and D_2 , respectively. So we can directly use the circuits represented by Fig. 11(h), Fig. 11(d) and Fig. 11(f) to implement the M_w , M_{c1} and M_{c2} blocks, respectively. Fig. 14(c) shows the circuit schematic. The M_w block has one LI and two LEs. The M_{c2} block has one LI and two LEs. The M_{c1} block has one LI. The circuit has 19 transistors. This algorithm is particularly suitable for the periodic approach since all intermediate variables are PSFs of z_i .

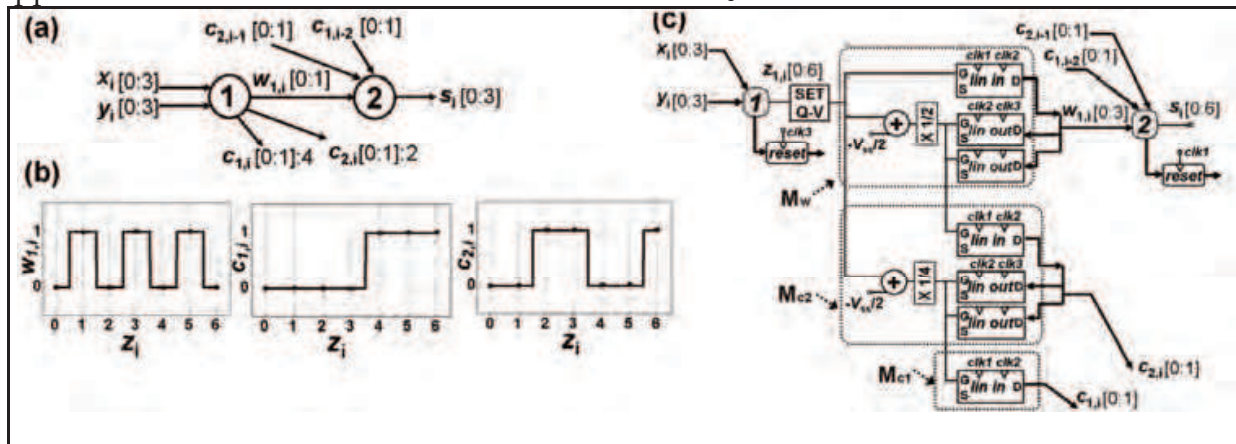


Fig. 14. (a) CTD representation of the PD2,3 adder. (b) Characteristics of $w_{1,i}$, $c_{1,i}$ and $c_{2,i}$ as functions of $z_{k,i}$. (c) Schematic of the PD2,3 adder using periodic approach.

4.3 Single-electron fast multiplier

We also used the above PD2,3 carry-free adders to construct a tree-structure single-electron fast multiplier. Fig. 15 shows the block diagram of an $X \times Y$ [0:11] multiplier. The circuit structure is same as the CMVL PD2,3 multiplier circuit (Kawahito et al., 1988). The multiplication algorithm has 4 steps. In the first step, 12×12 partial-product generator (PPG) generates 12×12 partial-products $p_{i,j}$ of multiplicand Y and multiplier X , $p_{i,j} \in \{0:1\}$. In our circuit the PPG is simply a SE turnstile. Only when both x_i and y_i is 1, a SE is injected to the SN. In step2, the output electrons of PPGs are grouped and transferred into SNs and are then are converted to voltage signals by the SET/MOS hybrid circuit. The SNs naturally finish the sum operation of partial-products. After this step, 4 operands with PD2,3 representation $P'_j = (p'_{12,j} \dots p'_{i,j} \dots p'_{1,j} p'_{0,j})$ ($j=0,1,2,3$) are generated, where $p'_{i,j} = p_{i,3j} + p_{i-1,3j+1} + p_{i-2,3j+2}$ corresponds to the number of electrons stored in the SN. In step3, these operands are added by two levels of parallel single-electron PD2,3 adders. Finally in step 4, the outputs of the second level PD2,3 adders are converted by conventional PD-binary converters.

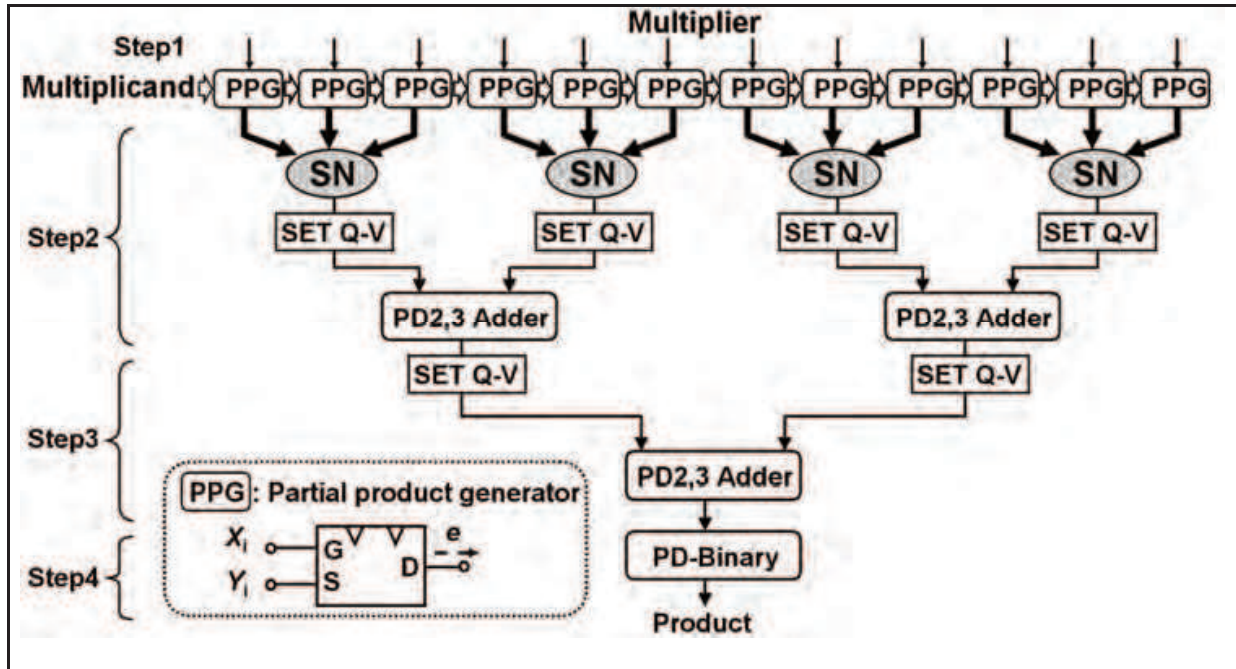


Fig. 15. Block diagram of the 12x12bit single-electron fast multiplier using two levels of single-electron PD2,3 fast adders. The bold lines show the flow paths of electrons.

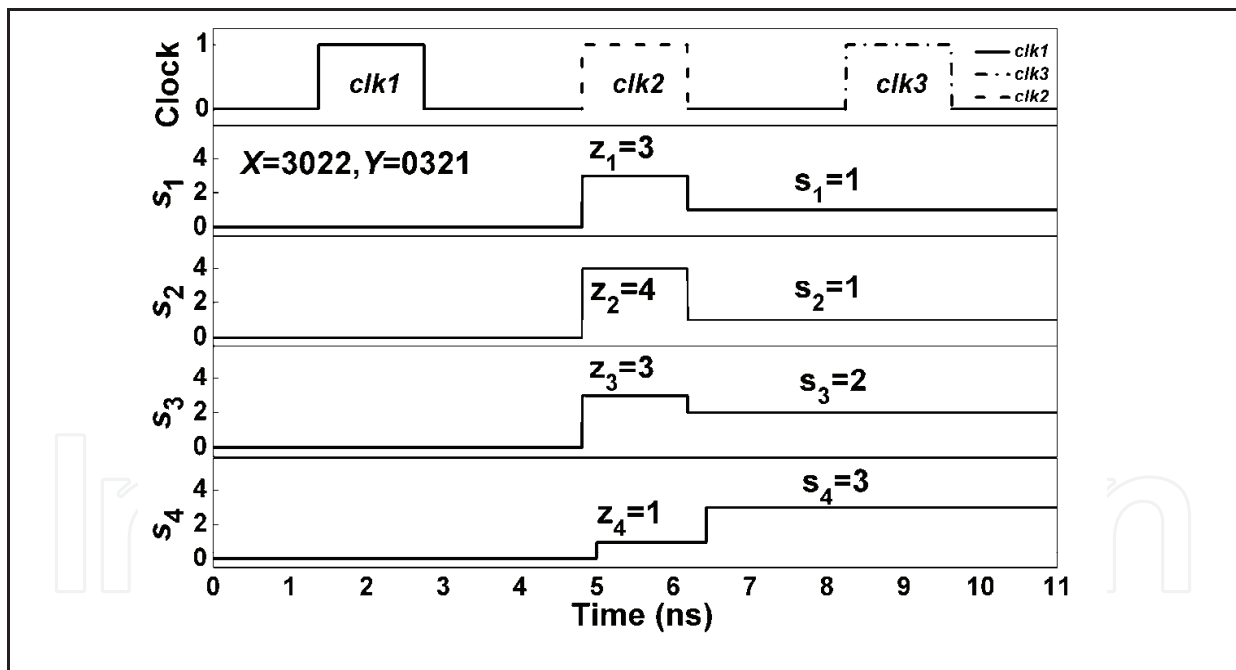


Fig. 16. Simulation results of the single-electron PD2,3 adder.

5. Circuit Performances

We use the HSPICE simulator and the proposed SPICE model of SE turnstile to investigate the performances of the adders. The SETs are described by the compact SPICE model of SET (Inokawa & Takahashi, 2003). The MOS transistors are described by 65nm technology node Predictive Technology SPICE models (Zhao & Cao, 2006).

5.1 Simulation Examples

Fig. 16 shows the simulated waveforms of the PD_{2,3} adder. The operation frequency f is 100MHz. The circuit finishes the addition function successfully. Correct operations of the other proposed adders were also verified.

5.2 Area

The adder circuits have compact structures and a small number of devices. This small device number is due to: 1) the use of electron counting paradigm to finish the sum operation and 2) the use of SE turnstiles to realize PSF circuits efficiently. Another advantage of the adders is that the transistors number does not depend on the radix of the number system. This can greatly reduce the number of transistors in large-size adders. For example, a 64-bit adder which is composed of 32 SD_{4,3} adders shown in Fig. 12(c) has only 608 transistors. On the other hand, one of the most area-efficient CMOS 64-bit adders has more than 1800 transistors (Ono, 2002), and the 64-bit SET adder has more than 1900 SETs (Lageweg et al., 2004) or 1136 SETs (Suliman & Beiu, 2004).

5.3 Speed

The speed of the adders is limited by two factors. The first factor is that the inherent arithmetic operation frequency is limited by the transfer error rate of the SE turnstile. The electron transfer speed of the SE turnstile is very high. Unlike SETs, the MOSFET-based SE turnstiles have a CCD-like structure and they do not have static tunneling barriers when transferring single electrons. Therefore, the equivalent RC delay of the SE turnstile is very small compared to SETs. However, transfer error is inevitable in SE circuits. Transfer error in SE turnstile has many different origins, such as thermal error and dynamic error (Zimmermana et al., 2004). The thermal error rate is around $5e-10$ with $C_{SEB}=0.7aF$ at $T=60K$. The dynamic error rate dominates when the falling times of the clock signals are too small. We calculate the dynamic error rate. Considering a total error rate $\epsilon=1e-8$ at $T=60K$, the falling time t_{fall} should be larger than 0.1ns (Zhang, 2008). Assuming the rising times of the clock signals are the same as t_{fall} , the transfer error rate limits the maximum frequency to $f_{max}=1/8t_{fall}$, which is higher than 1GHz. At lower temperature $T=10K$, f_{max} can be increased up to 5GHz.

The second factor is the delay of the charge-voltage converter. The delay of the SET/MOS hybrid circuit t_d is inverse proportion to the bias current I_0 . Simulation results show that $t_d \approx 0.5ns$ when $I_0 \approx 200nA$. In adders that require 4 repulsive clock signals, $f_{max}=1/4t_d$, which is around 500MHz.

The inherent speed of the fast adder is regardless of its length n . In practical applications, the fast adders may require extra conversion circuits to convert binary operands/results to non-binary operands/results. This will introduce an additional delay in the order of $O(\log n)$. In applications consisting of multiple stages of adders like fast multiplier, several stages of adders work in non-binary mode in series. Only one conversion circuits is required to convert the final outputs to binary. In this case, the speed merit of fast adders can be fully exploited.

5.4 Power dissipation

The power dissipation can be grouped into two parts. The first part is the power dissipated by performing the *arithmetic operations*. Since all arithmetic operations are achieved by moving single electrons, the power dissipation of the arithmetic part is $W_{\text{arth}} = N_{\text{arch}} e V_{\text{ss}} f$, where N_{arch} is the number of electrons transferred in one operation cycle. At $f = 100 \text{ MHz}$ and $V_{\text{ss}} = 2 \text{ V}$, W_{arth} of the periodic approach BCS adder is 0.67 nW , and W_{arth} of the periodic approach SD4,3 adder is 0.85 nW . The second part is the power dissipated by the conversion circuits W_{conv} , which is usually much larger than the W_{arth} . W_{conv} of the periodic approach BCS adder is 0.48 uW , while W_{conv} of the threshold approach BCS adder is around 2 uW due to the existence of threshold inverters.

5.5 Comparison with the state-of-the-art

Comparison of area

Table 1 shows comparison of the transistors numbers of several 1-bit *fast* adders implemented by the threshold approach, the periodic approach, the CMOS approach, and the CMVL approach. The SE fast adders have a small number of transistors. Table 2 shows comparison of circuit elements with other *binary* adders based on single-electron technology. One MOS transistor of the SE turnstile is treated as one tunneling junction of the SET. All coupling capacitors and load capacitors are also counted, since these capacitors may have larger area than the tunneling junctions. The results indicate that the proposed SE non-binary adder has similar number of circuit elements with other binary SE adders. Moreover, one SD4,3 adder can replace two binary adders due to its high radix.

Comparison of speed and power dissipation

Table 3 shows the comparison of several 32-bit PD2,3 fast adders using different approaches. Compared with CMOS, the proposed adder has a more than 98% reduction in power dissipation and more than 90% reduction in power-delay-product (PDP). The speed of the proposed adder is lower than its CMOS counterpart, due to the low speed of the charge-voltage converter. With the scaling down of the MOS transistors, the adder speed can be further increased.

Name	Threshold	Periodic	CMOS	CMVL
BCS	29	25	58	50
SD4,3	23	17	>80	52
PD2,3	29	19	>80	28

Table 1. Number of Transistors Comparison of Fast Adders

Adder Name	Junctions	Capacitors	Sum
TLG-SET (Suliaman and Beiu, 2005)	8	20	28
MAJ-SET (Suliaman and Beiu, 2005)	14	29	43
SE adder (Cotofana, 2005)	9	18	27
SD4,3 periodic	18	12	30
PD2,3 periodic	20	17	37

Table 2. Comparison of Number of Elements with Other Single-Electron Adders

Name	Delay	Power	PDP
CMOS	~0.4ns	~0.8mW	~0.3pJ
CMVL	~0.15ns	~3mW	~0.5pJ
This chapter	2ns	15uW	30fJ

Table 3. Number of Transistors Comparison of Fast Adders

Name	Delay	W_{arch} at $f=100\text{MHz}$		PDP	
	Typical value	Scale with	Typical value	Scale with	
TLG adder (Suliaman, 2004) $V_{\text{ss}}=6.5\text{mV}$, $T=4\text{K}$	~3ns	$>O(\log n)$	~20pW	$nC_L V_{\text{ss}}^2$	~0.4eV
SE adder (Cotofana, 2005) $V_{\text{ss}}=16\text{mV}$	~20ns	$O(n/r)^*$	~500pW	$n2^{r+1}e V_{\text{ss}}/r$	~65eV
PD2,3 this chapter $V_{\text{ss}}=2\text{V}$, $T=60\text{K}$	2ns	$O(1)^{**}$	20nW	$nN_{\text{arch}}e V_{\text{ss}}$	250eV

* n is the adder length and r is a technology dependent constant.

** Additional $O(\log n)$ delay when output is converted to binary

Table 4. Comparison of Delay & Power with Other 32-bit Single-Electron Adders

Table 4 shows the comparison of delay and power dissipation with other 32-bit SE binary adders. Although the proposed adder performs high-radix non-binary addition algorithm, it still has higher speed than other SE adders.

In Table 4 we did not consider the power dissipation W_{conv} of the converter circuits. This is reasonable because practically all SE circuits require converters or amplifiers to obtain large voltage gain and to drive output loads. Therefore we only compare W_{arch} of the adders. The power of the TLG-SET adder (Suliaman, 2004) is much lower than others. However, this value is obtained with a $V_{\text{ss}}=6.5\text{mV}$ and $T=4\text{K}$. To work at higher temperature, the junction capacitances of the SETs should be decreased, and thus V_{ss} has to be increased. Moreover, power of the CMOS-alike SET adder is proportional to the square of V_{ss} . It will be larger than the power of our PD2,3 adder when V_{ss} is larger than 160meV. On the other hand, W_{arch} of the SE adder by (Cotofana, 2005) and W_{arch} of our PD2,3 adder scale linearly with V_{ss} and they are proportional to the maximum total number of electrons N_{tot} involved in the arithmetic operation. The 32-bit SE adder by (Cotofana, 2005) has $N_{\text{tot}} \approx 2^{(r+1)}n/r \approx 2048$ when $r=8$. The 32-bit PD2,3 adder has $N_{\text{tot}}=nN_{\text{arch}}=672$. Therefore, the two adders have similar W_{arch} values with same V_{ss} . In this chapter, we use a 2V V_{ss} to obtain a large noise margin ($V_0=0.3\text{V}$) and we use experimental parameters of the SE turnstile in simulation. With lower $V_{\text{ss}}=0.1\text{V}$, lower temperature $T=5\text{K}$, and larger $C_{\text{seb}}=15\text{aF}$, the adder can also work well with a PDP=12eV. Therefore, with same temperature and V_{ss} , the PDPs of the proposed SE fast adders are not worse than previous SE binary adders.

In summary, the proposed SE fast adders have high overall time-area-power performances. The PDP of the fast adder is much lower than advanced CMOS adders (Zlatanovici, 2006). This point is rather critical in system-on-chip applications. Consider the 54x54 bit fast multiplier circuit based on radix-2 signed-digit arithmetic (Mochizuki, 2005). This CMVL circuit consumes more than 70mW with 500MHz operation frequency and it would be difficult to integrate hundreds of these multipliers in a single chip. However, using the SE fast adders to construct multipliers, the power dissipation will be largely reduced and thus thousands of multipliers can be integrated.

5.5 Comparison of two approaches

Each of the proposed approach has its merits and disadvantages. In some sense, the two approaches are complementary. Here we briefly compare the two approaches.

- 1) The threshold approach is more general. The periodic approach is better in adders in which more than 1 carry is transferred between two stages.
- 2) Number of transistors. The threshold approach has more transistors with small r , and the periodic approach has more transistors with large r .
- 3) Power dissipation. The threshold approach has much larger power dissipation due to existence of inverters.

6. Conclusion

In this chapter, we proposed novel fast adders based on single-electron devices. We proposed a family of SE transfer circuits based on the MOSFET-based SE turnstile. The adders can be designed by directly mapping the CTD representation of the addition algorithm to circuits using the threshold approach or the periodic approach. The two design approaches have their own advantages. The threshold approach can be viewed as a special kind of CMVL circuit with ultimate small current. The periodic approach uses the flexible staircase $N-V_g$ characteristics of the SE turnstile to compactly realize PSFs. We used SPICE to simulate the adders. The high time-area-power performances of the adders were demonstrated. Parameter dispersions should be considered for practical implementation of single-electron circuits. For the adder circuits, methods to reduce the calculation error rate and fabrication-related analysis are important, which will be our future work. In conclusion, the single-electron fast adder circuits have simple structure, fast operation speed and low power dissipation, and are promising in future nanoscale information-processors.

7. References

- Asahi, N.; Akazawa, M. & Amemiya, Y. (1997). Single-electron logic device based on the binary decision diagram. *IEEE Trans. Electron Devices*, Vol. 44, No. 7, pp. 1109.
- Avizienis, A. (1961). Signed-Digit Number Representations for Fast Parallel Arithmetic. *IRE Trans. Electronic Computers*, Vol. 10, Sept. 1961, pp. 389-400
- Cotofana, S.; Lageweg, C. & Vassiliadis, S. (2005). Addition Related Arithmetic Operations via Controlled Transport of Charge. *IEEE Trans. Comput.*, Vol. 54, No. 3, pp. 243-256.
- Fujiwara, A.; Zimmerman, N. M.; Ono, Y. & Takahashi, Y. (2004). Current quantization due to single-electron transfer in Si-wire charge-coupled devices. *Appl. Phys. Lett.* Vol. 84, pp. 1323.
- Fujiwara, A.; Nishiguchi, K.; & Ono, Y. (2008). Nanoampere charge pump by single-electron ratchet using silicon nanowire metal-oxide-semiconductor field-effect transistor. *Appl. Phys. Lett.* Vol. 92, pp. 042102.
- Gonzalez, F. A. & Mazumder, P. (1998). Multiple-valued Signed-digit Adder Using Negative Differential Resistance Devices. *IEEE Trans. Comput.*, Vol. 47, No. 9, pp. 947 - 959.
- Homma, N.; Sakiyama, J.; Wakamatsu, T.; Aoki, T. & Higuchi, T. (2004). Systematic Approach for Analyzing Fast Addition Algorithms Using Counter Tree Diagrams. *Proceedings of the 2004 International Symposium on Circuits and Systems*, vol. 5, pp. 197-200, May. 2004., IEEE, Vancouver

- Inokawa, H.; Fujiwara, A. & Takahashi, Y. (2003). A Multiple-valued Logic and Memory with Combined Single-electron and Metal-oxide-semiconductor Devices. *IEEE Trans. Electron Devices*, Vol. 50, No. 2, pp. 462-470.
- Inokawa, H. & Takahashi, Y. (2003). A Compact Analytical Model for Asymmetric Single-Electron Tunneling Transistors. *IEEE Trans. Electron Devices*, Vol. 50, pp. 455-461.
- Kawahito, S.; Kameyama, M.; Higuchi, T. & Yamada, H. (1988). A 32 x 32-bit Multiplier Using Multiple-valued MOS Current-mode Circuits. *IEEE J. Solid-State Circuits*, Vol. 23, No. 1, pp. 124 - 132.
- Kawahito, S.; Ishida, M.; Nakamura, T.; Kameyama, M.; & Higuchi, T. (1994) High-speed Area-efficient Multiplier Design Using Multiple-valued Current-mode Circuits. *IEEE Trans. Comput*, Vol. 43, pp. 34-42.
- Lageweg, C.; Cotofana, S. & Vassiliadis, S. (2004). Binary Addition Based on Single Electron Tunneling Devices. *Proceedings of 4th IEEE Conf. Nanotechnology*, pp. 327-330, Aug. 2004, IEEE, Munich.
- Likharev, K. K. (1999). Single-electron devices and their applications. *Proceeding of the IEEE.*, Vol. 87, No. 4, pp. 606-632.
- Mochizuki, A. & Hanyu, T. (2005) A 1.88ns 54×54-bit Multiplier in 0.18μm CMOS Based on Multiple-valued Differential-pair Circuitry. *Digest of Technical Papers, 2005 IEEE Symposium on VLSI Circuits*, vol. 17-3, pp. 264-267, June 2005.
- Nishiguchi, K.; Fujiwara, A.; Ono, Y.; Inokawa, H. & Takahashi, Y. (2006). Room-temperature-operating Data Processing Circuit Based on Single-electron Transfer and Detection with Metal-oxide-semiconductor Field-effect transistor Technology. *Appl. Phys. Lett.* Vol. 88, pp. 183101.
- Ono, Y.; Takahashi, Y.; Yamazaki, K.; Nagase, M.; Namatsu, H.; Kurihara, K. & Murase, K. (2000). Si complementary single-electron inverter with voltage gain. *IEEE Trans. Electron Devices*, Vol. 47, pp. 147.
- Ono, Y.; Inokawa, H. & Takahashi, Y. (2002). Binary Adders of Multi-gate Single-electron Transistor: Specific Design Using Pass-transistor Logic. *IEEE Trans. Nanotechnol.*, Vol. 1, No. 3, pp. 93-99.
- Ono, Y.; Fujiwara, A.; Nishiguchi, K.; Inokawa, H. & Takahashi, Y. (2006). Manipulation and detection of single electrons for future information processing. *J. Appl. Phys.*, Vol. 97, pp. 031101.
- Parhami, B. (1989) A New Method for Designing Highly Parallel Binary Multipliers," *Proceeding of the Third Ann. Parallel Processing Symp.*, pp. 176-185, Mar. 1989.
- Parhami, B. (1990). Generalized Signed-digit Number Systems: A Unifying Framework for Redundant Number Representations. *IEEE Trans. Comput.*, Vol. 39, No. 1, pp. 89 - 98.
- Parhami, B. (1993). On the Implementation of Arithmetic Support Functions for Generalized Signed-Digit Number Systems. *IEEE Trans. Comput.*, Vol. 42, No. 3, pp. 379 - 384.
- Sakiyama, J.; Aoki, T. & Higuchi, T. (2003). Counter Tree Diagrams for Design and Analysis of Fast Addition Algorithms. *Proceedings of the 33rd IEEE International Symposium on Multiple-Valued Logic*, pp. 91 - 98, May. 2003., IEEE.
- Suliaman, M.H. & Beiu, V. (2004). Characterization of a 16-bit Threshold Logic Single Electron Technology Adder. *Proceedings of the 2004 International Symposium on Circuits and Systems*, pp. III- 681-4, May. 2004, IEEE, Vancouver
- Suliaman, M.H. & Beiu, V. (2005) On Single-electron Technology Full Adders. *IEEE Trans. Nanotechnol.*, Vol. 4, No. 6, pp. 669-680.
- Takagi, N.; Yasuura, H.; & Yajima, S. (1985). High-speed VLSI Multiplication Algorithm with a Redundant Binary Addition Tree. *IEEE Trans. Comput.*, Vol. 34, No. 9, pp. 789 - 796.

- Yano, K.; Ishii, T.; Hashimoto, T.; Kobayashi, T.; Murai, F. & Seki, K. (1994). Room-temperature single-electron memory. *IEEE Trans. Electron Devices.*, Vol. 41, pp. 1628-1638.
- Zhang, W-C.; Nishiguchi, K.; Ono, Y.; Fujiwara, A.; Hiroshi, Y.; Inokawa, H.; Takahashi, Y. & Wu, N-J. (2007 a). Transfer and Detection of Single Electrons using Metal-Oxide-Semiconductor Field-Effect-Transistors. *IEICE Trans. Electron*, Vol. E90-C, pp. 943-948.
- Zhang, W-C. & Wu, N-J. (2007 b). Novel Hybrid Voltage Controlled Ring Oscillators Using Single Electron and MOS Transistors. *IEEE Trans. Nanotechnol.*, Vol. 6, pp. 146-157.
- Zhang, W-C. & Wu, N-J. (2007 c). A Novel Hybrid Phase-locked-loop Frequency Synthesizer Using Single Electron Devices and CMOS Transistors. *IEEE Trans. Circuits Syst. I*, Vol. 54, No. 11, pp. 2516-2527.
- Zhang, W-C.; Wu, N-J. & Yang, F-H. (2007 d). Compact Universal Logic Gates realized using Quantization of Current in Nanodevices. *Nanotechnology*. Vol. 18, pp. 495201.
- Zhang, W-C. & Wu, N-J. (2008). Smart Universal Multiple-Valued Logic Gates by Transferring Single Electrons. *IEEE Trans. Nanotechnol.* Vol. 7, No. 4, pp. 440-450.
- Zhao, W. & Cao, Y. (2006). New generation of Predictive Technology Model for sub-45nm design exploration. *IEEE International Symposium on Quality Electronic Design*, pp. 585-590, IEEE, San Jose.
- Zimmermana, N.M.; Hourdakakis, E.; Ono, Y.; Fujiwara, A. & Takahashi, Y. (2004) Error Mechanisms and Rates in Tunable-barrier Single-electron Turnstiles and Charge-coupled devices. *J. Appl. Phys.*, Vol. 96, pp. 5254.
- Zlatanovici Kao, S. & Nikolic, B.R. (2006) A 240ps 64b Carry-lookahead Adder in 90nm CMOS. 2006 *Digest of Technical Papers, IEEE International Solid-State Circuits Conference*, pp. 1735 - 1744, Feb. 2006.

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The main purpose of this book is to describe important issues in various types of devices ranging from conventional transistors (opening chapters of the book) to molecular electronic devices whose fabrication and operation is discussed in the last few chapters of the book. As such, this book can serve as a guide for identifications of important areas of research in micro, nano and molecular electronics. We deeply acknowledge valuable contributions that each of the authors made in writing these excellent chapters.

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