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# 52-GHz Millimetre-Wave PLL Synthesizer

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## 1. Introduction

Multiple 60-GHz WPAN (Wireless Personal Area Network) radio transceiver chips using CMOS or BiCMOS process have been developed as wireless communication service of several-gigabit rate [Reynolds, 2006] [Razavi, 2006]. In a 60GHz millimetre-wave transceiver, frequency synthesizer is a key building block. It is very difficult to design the PLL-based programmable synthesizer directly at 60GHz band without tripler or doubler. A 14.25-16-GHz programmable PLL synthesizer was presented as a frequency source for 60GHz direct-conversion receiver. Its output frequencies of 28.5-32GHz are generated using Wilkinson power combiner [Lee, 2008]. A 16-18.8GHz programmable PLL was developed as a local oscillator for 60GHz dual-conversion super-heterodyne transceiver [Floyd, 2008]. Its tripled output frequency becomes 46 to 54GHz. Also, various non-programmable PLLs have been developed as millimetre-wave frequency sources, but they are not suitable for 60GHz WPAN radio covering 57 to 64GHz range [Winkler, 2005] [Lee, 2007].

In this chapter, we present a 52-GHz PLL-based synthesizer for 60GHz dual-conversion super-heterodyne receiver. The synthesizer is composed of 26GHz programmable PLL and 52GHz frequency doubler. The 26GHz PLL consists of PFD, charge pump, loop filter, LC VCO, and four-modulus divider. The synthesizer shows a 50-53GHz locking range, and generates two channels of 50.304GHz and 52.4GHz when 262MHz reference is used. The PLL achieves phase noises of – 89dBc/Hz from 26.2GHz and – 81dBc/Hz from 52.4GHz, at 1MHz offset frequency, respectively. The synthesizer represents spurious noise level of – 42dBc/Hz, and consumes 160mA at 2.5V.

In section 2 of this chapter, a 60GHz dual-conversion super-heterodyne receiver is briefly introduced. In section 3, the 52GHz PLL synthesizer including frequency doubler is described in detail. The experimental results are presented in section 4, and finally, conclusion is drawn in section 5.

## 2. 60GHz Dual-Conversion Super-Heterodyne Receiver

Fig. 1 shows a dual-conversion super-heterodyne receiver for 60GHz WPAN radio including RF and IF PLL. The 60-GHz dual-conversion receiver consists of RF LNA, RF Mixer, RF PLL, VGA, IF Mixer, and IF PLL. In the 60GHz receiver, the LNA amplifies the RF signals between 57GHz and 64GHz, which are down converted to 10GHz IF signal by the RF mixer. Then, the amplitude of the 10-GHz IF signal is controlled by the variable-gain

amplifier (VGA). And it is fed to the double-balanced IF mixer which performs the IF-to-base-band signal conversion. The local oscillator (LO) module is configured with 52GHz RF PLL and 10GHz IF PLL. The RF PLL should provide three channels between 48.208GHz and 52.4GHz in step of 2.096GHz or between 48.576GHz and 52.8GHz by 2.112GHz step, with RF mixer down-converting the RF signals of 57-64GHz. The IF PLL provides only 10GHz or 10.032GHz fixed carrier, depending upon which reference clock of 262MHz and 264MHz is used.

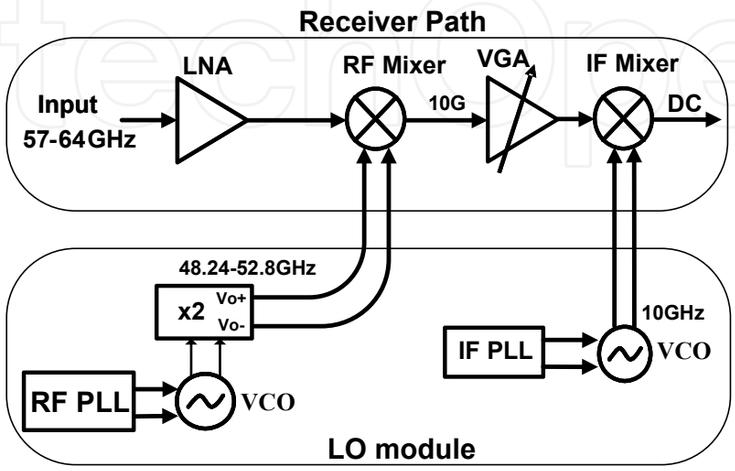



Fig. 1. 60GHz dual-conversion superheterodyne receiver with RF PLL

## 3. Design of 52GHz PLL Frequency Synthesizer

### 3.1 Frequency Synthesizer Architecture using PLL

Fig. 2 represents the 52-GHz frequency synthesizer block diagram using phase-locked loop. The frequency synthesizer consists of PFD, charge pump, loop filter, LC-tank VCO, and four-modulus divider. In the frequency synthesizer, all components including frequency doubler and loop filter are implemented by on chip. The 52-GHz PLL is designed for providing local signal to the 60-GHz receiver covering unlicensed WPAN band (57-63GHz). As shown in Fig. 2, the PLL generates 52GHz frequency through the frequency doubler making twice the output frequencies of the 26GHz VCO. The frequency doubler configured with a differential amplifier suppresses odd-mode harmonic carriers such as $f_o$, $3f_o$, $5f_o$, etc, but it combines the even-mode carriers ($2f_o$, $4f_o$, etc) of the differential VCO, additively. Therefore, only differential even-mode harmonic carriers are emerged from the output port of the frequency doubler whose circuit diagram is presented in 3.5.

The phase-frequency detector is designed to operate at high speed of 264MHz. The third order loop filter is implemented on chip. Since the on-chip passive loop filter occupies large chip area, each optimized values of loop-filter components should be chosen, considering its chip area, loop settling time, and spurious noise level. The LC-tank VCO is designed to generate high oscillation frequencies of 24.4-26.5GHz. In Fig.2, a four-modulus divider is designed to provide the divide number of 20 to 25 for snythesizing three-channel carriers. Also, the four-modulus divider must operate at high speed to divide the high output frequencies of the 26-GHz VCO. In a millimeter-wave PLL synthesizer, it is very difficult to design a high-speed programmable divider for synthesizing multiple channels because there are many digital logic circuits operating at low speed and some logic-signal delay in

the divider block. Also, a high-speed divider consisting of many digital latches requires much amount of current, and hence, contributes to most of power consumption in the whole PLL circuit. Therefore, the programmable divider should be designed, considering trade-off between power consumption and speed. In this chapter, the 52GHz PLL synthesizer provides two channels of 50.304GHz and 52.4GHz when the reference clock of 262MHz is input. Also, the PLL generates two channels of 50.688GHz and 52.8GHz when the reference clock of 264MHz is input to the PFD.

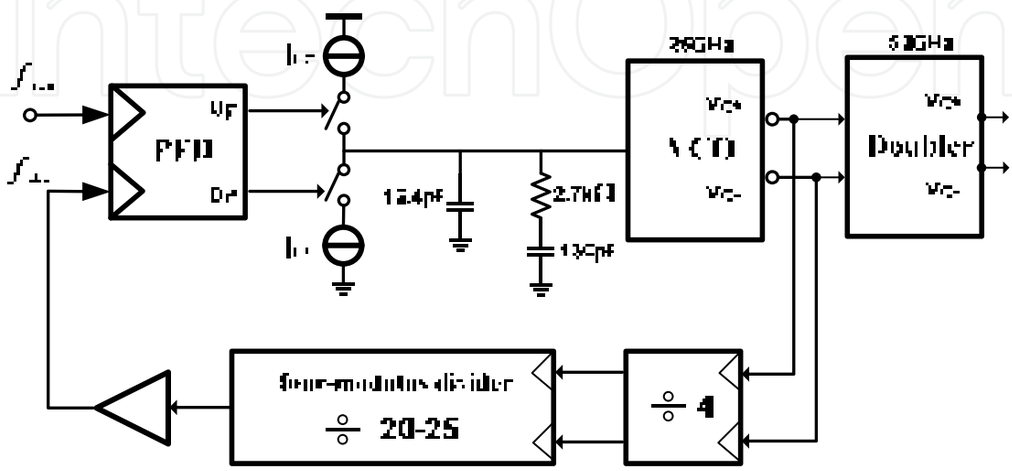


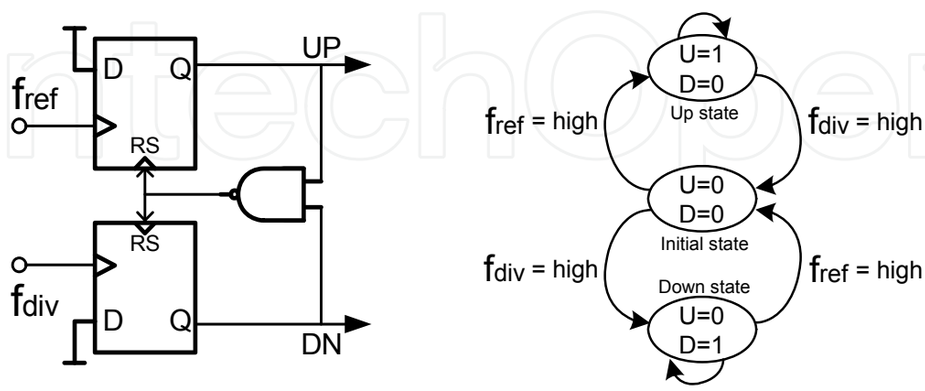

Fig. 2. 52GHz PLL frequency synthesizer

### 3.2 PFD and Charge Pump

Fig. 3 illustrates a common linear PFD block diagram, configured with two-edge triggered resettable DFFs and a NAND gate, and its state diagram. This PFD generates UP and Down signals that switch the current of charge pump and control its amount. The D inputs of the DFFs are fixed to logic high, and the two input signals ($f_{ref}$ and $f_{div}$) of PFD trigger each DFF. The pulsewidth of both UP and Down signals is proportional to the phase difference between $f_{ref}$ and $f_{div}$. As shown in Fig. 3(b), initially, both outputs are low. When one of the PFD inputs rises, the corresponding outputs becomes logic high. The state of the finite-state machine (FSM) moves from an initial state to an Up or a Down state, depending on the state of the input signal. According to the state diagram, therefore, the phase and frequency differences of the two input signals are detected by the PFD [Razavi, 2001].

Fig. 4 (a) shows the ideal graph of plotting the input-output characteristics of the tri-state PFD. Defining the output $V_{out}$ as the difference between the average values of Up and Down signals when $f_{ref} = f_{div}$ and neglecting the effect of the narrow reset pulses, we note that the output varies symmetrically as $|\Delta\phi|$ begins from zero as shown in Fig. 4 (a). That is, the PFD ideally shows the linear characteristics for the entire range of input phase differences from -2π to 2π. The PFD including charge pump senses the transitions at the inputs, detects phase or frequency differences, and activates the charge pump accordingly. When $f_{ref}$ is initially far from $f_{div}$, the PFD and the charge pump keep varying the control voltage of VCO until $f_{ref}$ approaches $f_{div}$ closely. When $f_{ref}$ and $f_{div}$ are sufficiently close, the PFD operates as a phase detector, performing phase lock. Once the phase difference is within the lock-in range and drops to zero, the cycle slipping stops and the PLL loop is locked. Here, the cycle

slipping means that the phase difference changes each cycle by $2\pi\times[(T_{fref} - T_{fdiv})/\max(T_{fref}, T_{fdiv})]$. At this view point, the phase defector behaves as a linear system as shown in Fig. 4(a). However, due to the delay of the reset path, the linear range is less than $4\pi$ as shown in Fig. 4(b). The reset pulses prevent the PFD/charge pump from undergoing a deadzone around $\Delta\phi = 0$ in which the PLL loop gain drops to zero and the phase of $f_{div}$ is locked.




(a) (b)

Fig. 3. (a) linear tri-state PFD, (b) tri-state PFD state diagram

Fig. 4(c) illustrates the nonideal behavior with the reference clock $CKf_{ref}$ leading the output clock $CKf_{div}$, causing an Up output. As the input phase difference nears $2\pi$, the next leading edge of $CKf_{ref}$ arrives before the DFFs are reset due to the finite reset delay. The reset pulse overrides the new $CKf_{ref}$ edge and then the Up signal is not activated. The subsequent $CKf_{div}$ edge causes a Down signal. The effect appears as a negative output for phase differences higher than $2\pi$-$\Delta$, where $\Delta = 2\pi\times(t_{reset}/ T_{fref})$, which depends on the reset path delay $t_{reset}$ and the reference clock period $T_{fref}$. Note that $t_{reset}$ is determined by the delay of logic gates in the reset path and is not a function of input frequency. During acquisition, the frequency will not monotonically approach lock-in range because the nonideal PFD gives the wrong information periodically. The acquisition slows by how often the wrong information occurs, which depends on $\Delta$. At an input frequency $T_{fref} = 2\times t_{reset}$ where $\Delta$ equals $\pi$, the PFD output generates the wrong information half the time and, thus, fails to acquire frequency lock unconditionally. The maximum operating frequency can be expressed as $f_{ref} \leq 1/(2\times t_{reset})$ [Mansuri, 2002].

A commonly used tri-state PFD is implemented by using NOR-based latch to build the edge-triggered resettable DFFs. The reset path includes one two-input NAND, one inverter, and three two-input NORs, which are counted twice in the reset path. Thus, the delay of the reset path is approximately equal to 10 gate delays [Razavi, 2001]. This reset pulse delay is required to remove a deadzone. However, the reset delay makes the settling time of PLL slow and disables the phase lock in the worst case of $\Delta \geq \pi$. In this PLL, the short pulse period is about 210 ps, the reference clock frequency 262MHz and $\Delta$ is about $0.11\pi$, which can slow the loop settling time to some extent.

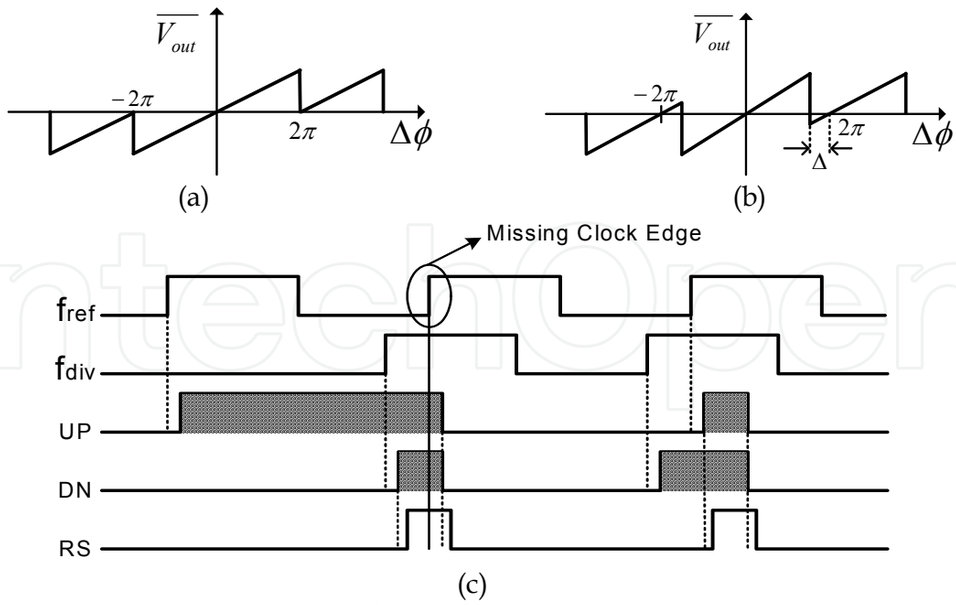



Fig. 4. (a) ideal linear characteristic of tri-state PFD (b) nonideal characteristic (c) nonideal behaviour due to nonzero reset delay

In the commonly improved PFD circuit of Fig. 5, two inverting delay stages are inserted between the clock input and the precharged PMOS (P2 and P5) [Tak, 2005]. The characteristics of the improved PFD are shown in Fig. 6. It can generate effective Up signals without missing the edge of $CKf_{ref}$ even when the phase difference between the two input clocks is significantly close to $2\pi$. The improved PFD represents lower power consumption and higher precision than the latch-based PFD presented by Razavi [2001] because the dynamic logic circuit has lower propagation delay and better matching, which are the advantages of the improved PFD. Therefore, the phase noise contribution of PFD can be relieved. Fig. 6(a) illustrates the operation of the improved PFD. Here, td1 is the inserted delay time between $CKf_{ref}$ and $D\_CKf_{ref}$ ($CKf_{div}$ and $D\_CKf_{div}$), td2 is the pulse width for preventing the dead zone, and td3 is the time period from a rising edge of a subsequent input clock between $CKf_{ref}$ and $CKf_{div}$ to the falling edge of the reset signal. At the second rising edge of $CKf_{ref}$, the phase difference $\Delta\Phi$ is in the range of $2\pi-\Delta < \Delta\Phi < 2\pi-\delta$. At the falling edge of the following Reset signal, $D\_CKf_{ref}$ is "Low", and node X is charged to "High". Because $CKf_{ref}$ is "High" at that moment, node Y is discharged to "Low" and Up signal becomes "High" earlier than the Down signal. Therefore, the improved PFD does not lose the edge that arrives during reset and generates the right information. At the third rising edge of $CKf_{ref}$, the phase difference is in the range of $\Delta\Phi \geq 2\pi - \delta$ and the Up signal remains "Low". The inserted delay td1 should be designed to be slightly smaller than td3, otherwise the PFD will fail to lock at zero input phase difference. If td1 > td3, then the delayed input clocks activate the output after the reset pulse ends. This design criterion results in a negative output voltage for $\Delta\Phi \geq 2\pi - \delta$, as illustrated in Fig. 6(b). The maximum operating frequency of the PFD is dependent on the duty ratio of each input clock. With a higher duty ratio, the PFD can operate at a higher clock frequency because the input clock should be "High" at the rising edge of the delayed input clock. Assuming half duty ratio,

the maximum operating frequency of the improved PFD is 1/(2×td3), approximately equal to $1/(2\times t_{reset})$, while that of the latch-based PFD is about $1/t_{reset}$ [Mansuri, 2002] [Tak, 2005].

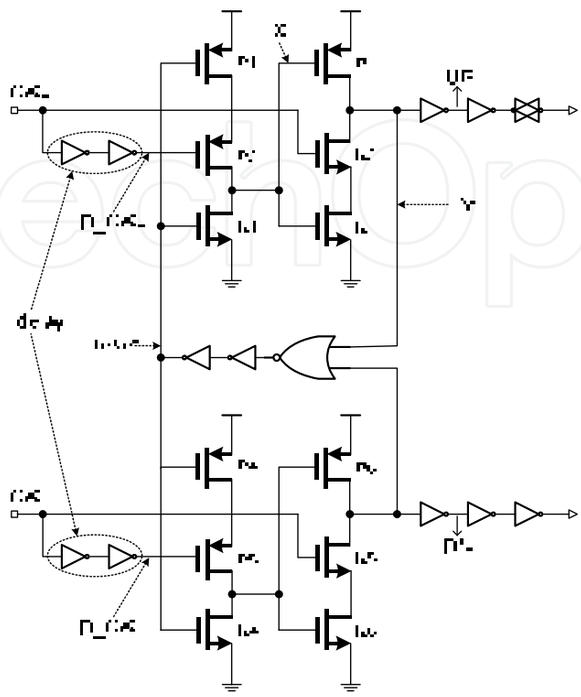


Fig. 5. PFD using edge-triggered resettable DFF

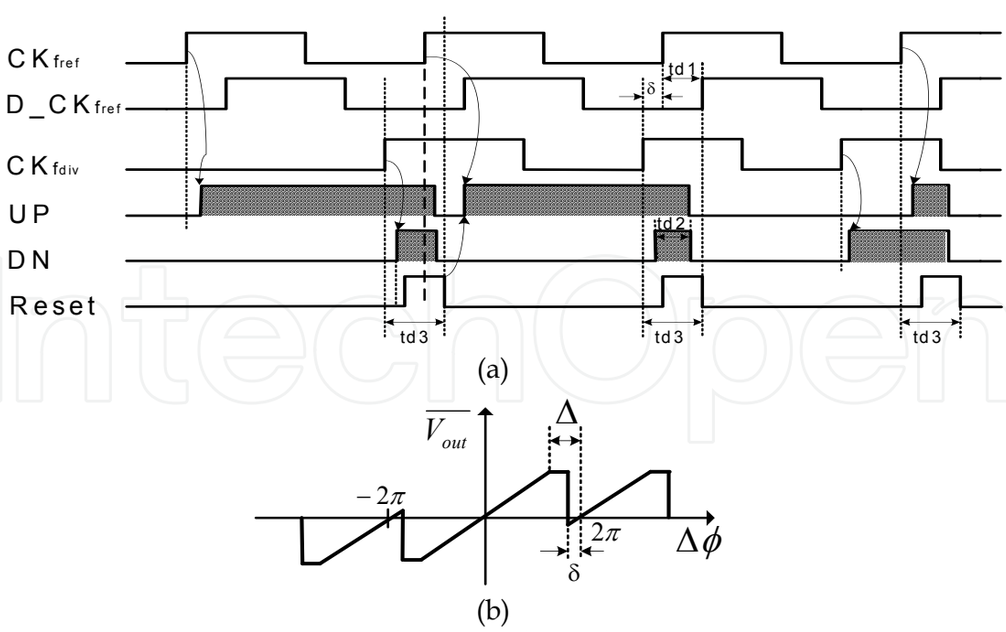



Fig. 6. (a) Operating timing diagram of the PFD (b) its characteristics

Charge pump is an important building block commonly used in PLLs for frequency synthesizers and clock generators. The dominant block causing reference spurs in a PLL is

the charge pump. The reference spurs are commonly generated because there are current mismatch, leakage current, and timing mismatch in charge pump circuit. The total phase offset in PLL loop due to the non-idealities of charge pump is approximately expressed in (1) [Rhee, 1999].

$$\Delta\phi_{tot} = 2\pi\left(\frac{I_{leak}}{I_{cp}} + \frac{\Delta i}{I_{cp}} \cdot \frac{t_{on}}{T_{ref}} + \frac{\Delta t_{delay} \cdot t_{on}}{T_{ref}^2}\right) \tag{1}$$

where $I_{cp}$ is the charge-pump current, $I_{leak}$ is the leakage current, $T_{ref}$ is the reference clock period, $t_{on}$ is the PFD turn-on time, $\Delta i$ and $\Delta t_{delay}$ are current and timing mismatch, repectively. The resulting reference spurs for a 3rd–order PLL can be approximately given by (2)

$$P_r = 20\log\left(\frac{N \cdot f_{bw} \cdot \Delta\phi_{tot}}{\sqrt{2} f_{ref}}\right) - 20\left(\frac{f_{ref}}{f_{p1}}\right) \tag{2}$$

where N is the division ratio of the divider, $f_{bw}$ is the loop bandwidth and $f_{p1}$ is the frequency of the pole in the loop-filter. Eq. (2) represents that the reference spurs can be reduced by lowering loop phase error and loop bandwidth, or increasing reference frequency. The phase offset due to leakage current can be significant in sub-micron CMOS circuits, but may be reduced with a large charge-pump current. This results in high power consumption and should be hence avoided in low power application.

The use of a differential charge-pump circuit is preferable since leakage current then appears as a common mode glitch at output. The influence of current mismatch can be reduced by minimizing the turn-on time of the PFD. A small turn-on time also helps to reduce the in-band noise of the PLL. A small turn-on time requires a fast switching charge pump with minimum current mismatch. For charge pump to operate with small turn-on time and high speed, current steering techniques have to be used instead of charge pumps with drain, gate or source switching. Charge pumps with drain switching are limited by high current spikes in the first moments of the pump UP/DN operations. This is due to triode region operation of the current source transistors. These current spikes are difficult to match since the current varies with output voltage. The gate-switched charge pump eliminates the problem of current spikes, since the transistors in the current mirrors are then either off or in saturation. The main drawback is increased gate capacitance, which limits the operating speed. A higher speed is achieved with a source-switching charge pump. However, the operating speed is still limited by the time of the current mirror because the switch is connected to a low impedance node, which results in the current mirrors of either ON or in saturation [Rhee, 1999].

Fig. 7 shows the high-speed single-ended charge pump circuit using current steering technique, which improves switching time and thus allows high-speed operation. The drawback of using the current-steering charge pump switch is the mismatch between the NMOS and the PMOS transistors. This inherent mismatch can be avoided by using only NMOS switches [Magnusson, 2003]. Also, if the rise/fall times of the input signals are very

small, there will not be enough time for the gate-drain capacitors to be charged or discharged by drain current. Hence, there will be very large spikes of current at the output of the charge pump and very high content of the higher harmonics in the filter output voltage [Bahreyni, 2002]. A PFD will produce logic level UP/DN signals, which are the inputs to the charge pump in Fig. 7. The large amplitude of UP and DN signals will cause the bias current of $I_{up}$ and $I_{down}$ to be completely switched from one branch of the corresponding differential pair to the other. For example, when both UP and DN singal are low, P2 and N1 will be ON while P1 and N2 will be OFF. Thus, the tail current, $I_{up}$, will be forced to flow into the loop filter. When both UP and DN signals are high, N2 and P1 will be ON while P2 and N1 will be OFF. Thus the tail current, $I_{down}$, will be forced to flow out from the loop filer. However, if one of the inputs is high and the other is low or vice versa, the output transistors, P2 and N2, will be on or off at the same time and no current flows into the loop filter.

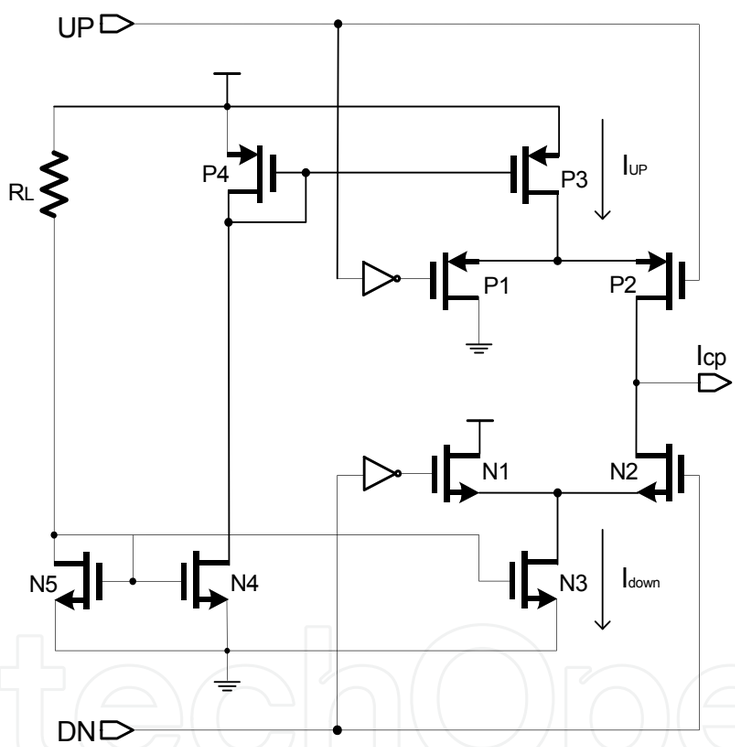



Fig. 7. High-speed current-steering single-ended charge pump

Fig. 8 shows the simulation result of the $I_{up}$ and $I_{down}$ current mismatch in the current-steering charge pump circuit. When the output voltage of the charge pump changes 0.2 V to 2.2 V by 0.1 V step, the $I_{up}$ and $I_{down}$ currents varies from 380μA to 426μA, and hence the charge pump represents about 10% current mismatch. Fig. 9 illustrates the simulation result of PFD deadzone when the input phase difference is varied across zero point. Since the curve of Fig. 9 increases linearly across zero value at Y-axis without plateau, there is no deadzone in the designed PFD circuit, which fills up the demand of td1 < td3. Here, td1 is 60ps and td3 is greater than 260 ps.

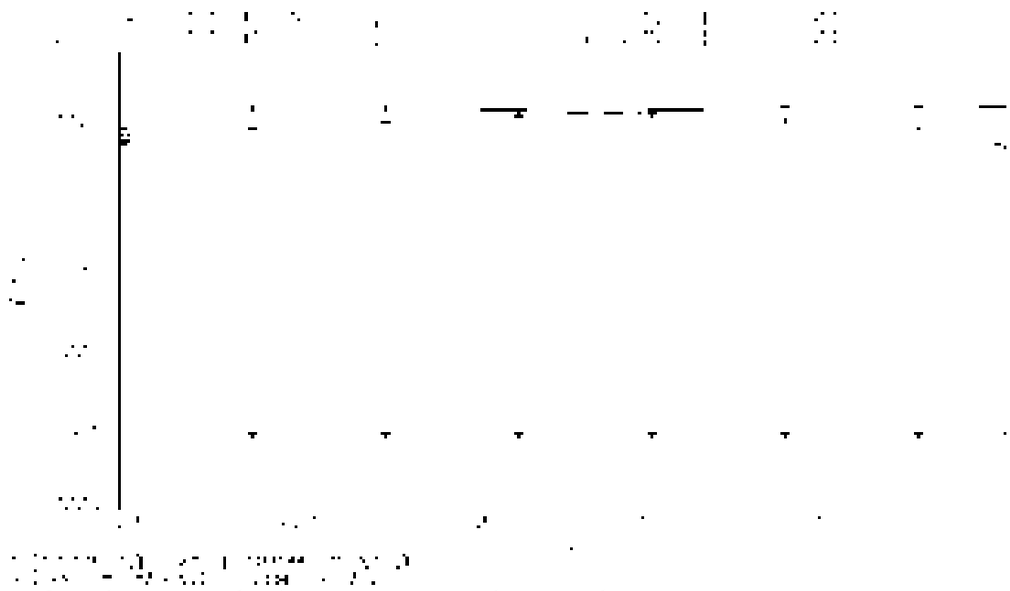


Fig. 8. Simulation result of current mismatching in charge pump

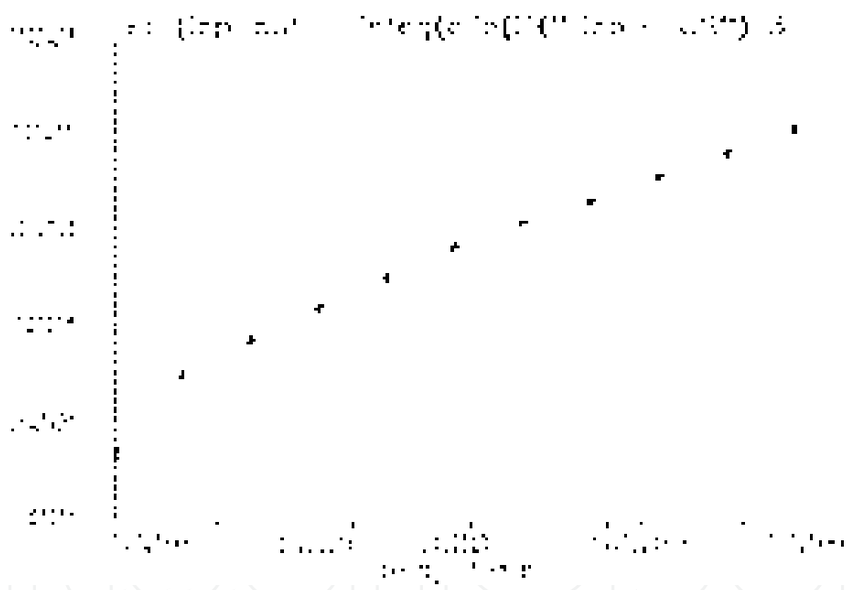
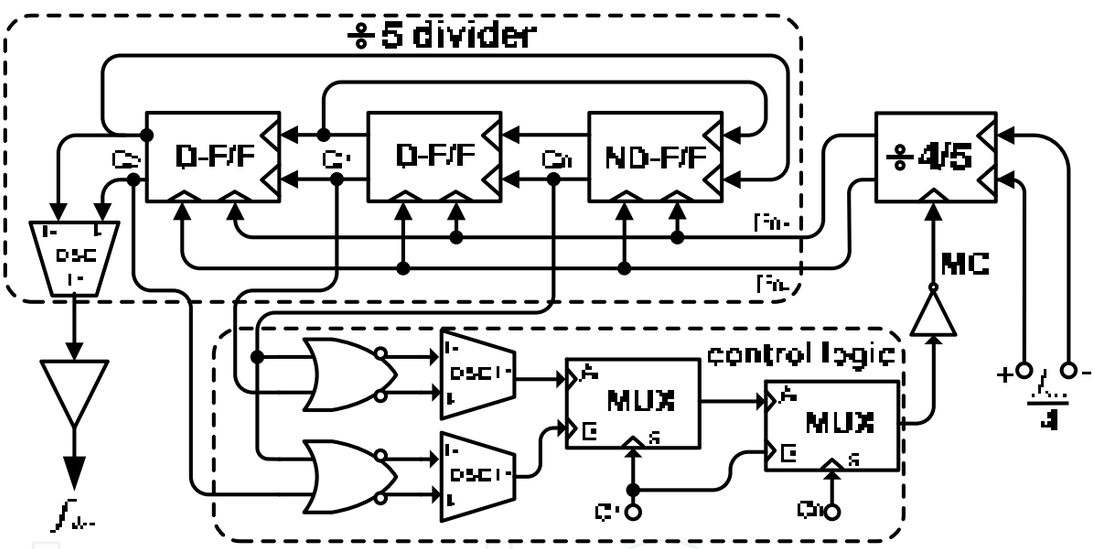


Fig. 9. Simulation result of dead zone in PFD

### 3.3 Programmable Divider

A multi-modulus prescaler that operates at very high frequency is one of the key building blocks for frequency synthesizers in wireless communications. The major issues for designing a multi-modulus prescaler are high operating frequency and low power consumption, while keeping low phase noise contribution to the synthesized output signal. Fig. 10 represents the block diagram of the four-modulus divider in the 52-GHz frequency synthesizer of Fig. 2. The four-modulus divider, which has four divide ratios controlled by mode control (MC) signal, is designed to simplify the hardware required for frequency

synthesis. It is composed of a divid-by-4/5 dual-modulus prescaler, a divide-by-5 divider, and a control logic unit. The control logic unit generates the MC signal modulating its divide rato, and the divide ratio of the four-modulus divider can be set to be ÷ 20, ÷ 23, ÷ 24, and ÷ 25 by varying the duty ratio of the MC signal. And its duty ratio is determined by the logic values of control bits $c_0$ and $c_1$, as shown in Table of Fig. 10. For example, if $c_1$ is low and $c_0$ is high, the total divide ratio becomes ÷ 23; if $c_1$ is high and $c_0$ is low, the total divide ratio becomes ÷ 25. Fig. 11 illustrates the timing diagrams of the four-modulus divider. If the MC signal is low, the divide-by 4/5 prescaler divides the input clock signal by 5. If the signal MC is high, its divide ratio becomes ÷ 4. Therefore, if $c_0$ is low and $c_1$ is high, the dual-modulus prescaler divides the input signal of $f$vco/4 by ÷ 4 for two $P_{o+}$ cycles and by ÷ 5 for three $P_{o+}$ cycles, while the followed divide-by-5 divider swallows five Po+ cycles. Thus, a total divide ratio (TDR) is calculated as TDR= (÷ 4) × 2 cycles + (÷ 5) × 3 cycles = ÷ 23. The operating timing waveform of the four-modulus divider is illustrated in Fig. 11. Using the same technique as explained above, the modulus number of the four-modulus divider could be extended to more numbers of divide ratios.




Divide ratio table

| $c_1$ $c_0$ | 0 0 | 0 1 | 1 0 | 1 1 |
|---|---|---|---|---|
| divide ratio | ÷ 24 | ÷ 23 | ÷ 25 | ÷ 20 |

Fig. 10. Four-modulus divider and its divide ratio

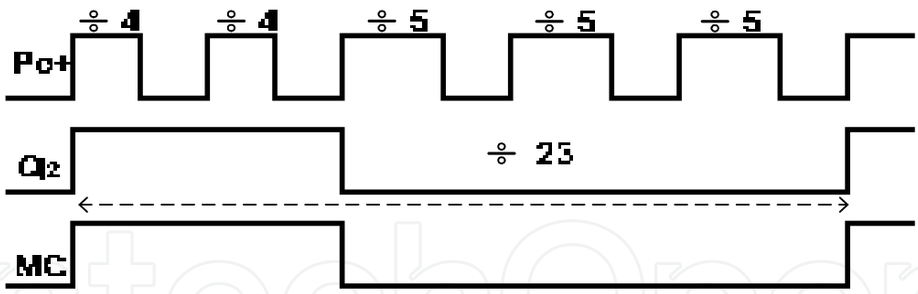



Fig. 11. Operating timing waveform of the four-modulus divider

The implementation of a high-speed prescaler in mixed-signal environment requires careful attention to certain aspects of the circuit design to contribute low noise to such sensitive analog circuit as VCO, which shares the same substrate with noisy circuits, and to the synthesized output signal. Here, both current-mode logic (CML) and ECL-like D-flipflops instead of a static CMOS logic are used to implement the four-modulus divider. The CML logic uses constant current source, which generates lower digital noise, and differential signals at both input and output, which reduce common-mode noise coupled from the power supply line and substrate because the differential circuit topology does inherently suppress the common-mode power supply and substrate noise [Park, 1998]. Another issue of the programmable divider design is reduction in power consumption at a given frequency range. Most power consumption in divider occurs in the front-end synchronous 4/5 dual-modulus prescaler because it is a part of the circuit operating at the maximum frequency of the input signal. The 4/5 synchronous dual-modulus prescaler shown in Fig. 12 contains two high-frequency fully functional ECL-like D-flipflops and one ECL-like D-flipflop with NOR logic. In the dual-modulus prescaler, the outputs of both the second D-flipflop and the third D-flipflop are feedback into the NOR D-F/F as the control inputs for generating proper division ratio. The MC signal is given to the third NOR D-F/F for modulating division ratio. The delay requirement in a critical path of the prescaler loop is severe because the 4/5 dual-modulus prescaler must operate up to a maximum of 10 GHz. The operating speed of the prescaler is limited by the delay time of each D-flipflops, and the prescaler layout. Therefore, the prescaler should be designed and laid out to achieve a delay time as small as possible and to obtain an operating frequency as high as possible.

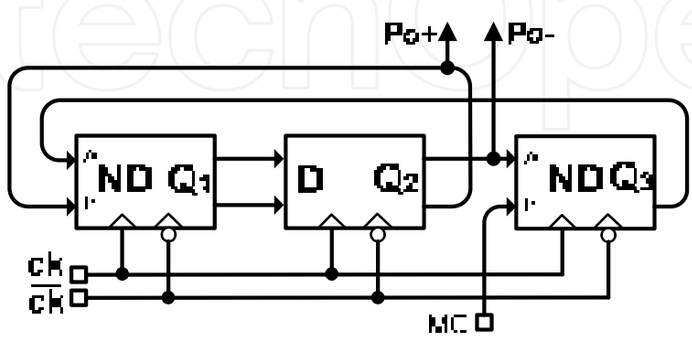


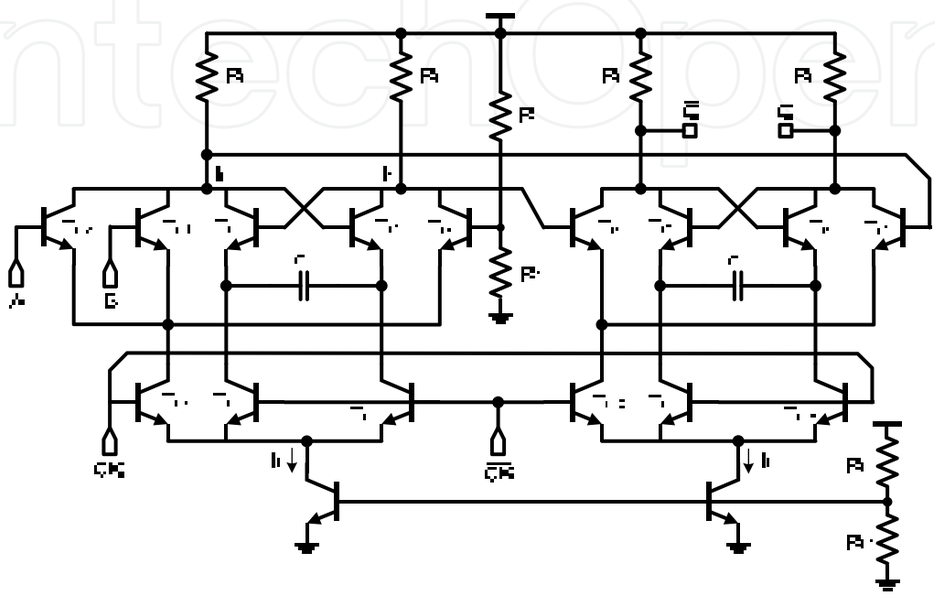

Fig. 12. 4/5 dual-modulus prescaler

Fig. 13 represents the divider circuit consisting of master-slave D-type latches. They are a rising edge-triggered E²CL D-flipflop with embedded NOR gate and a E²CL D-type flipflop, which are used in the front-end design to achieve a maximum speed and a minimum power. The master-slave D flipflop is driven by an applied clock signal (CK), and the Q of D-flipflop changes on each rising edge of the clock. Each latch consists of a differential stage ($T_{r3}/T_{r4}$, $T_{r7}/T_{r8}$) for the read-data operation and a cross-coupled stage ($T_{r1}/T_{r2}$, $T_{r5}/T_{r6}$) for the hold operation. Both load resistance $R_L$ and bias current $I_L$ determine logical swing. There are four distinct states that the D latch may occupy, representing state transition between latched and transparent, and on every edge of the clock the D flipflop changes state. To complete a cycle, all four-state transitions in which both master and slave latches alternate between transparent and latched states should be carried out in the divider. The maximum speed of operation of the divider circuit shown in Fig.13 can be determined by the sum of the delays of each transition. The D latches have two basic operations. The first is a current steering operation in the $T_{r9}$, $T_{r10}/T_{r11}$ and $T_{r12}$, $T_{r13}/T_{r14}$ differential pairs, moving between latched and transparent settings. The second is a voltage operation that can only occur after the current steering, changing the output voltage at I and Q nodes. Both of these operations introduce delay into the divider circuit and limit the maximum operating speed of the divider. Here, the delay contribution of the master's transition should be commonly improved because the master latch shows more slow cycle transition than the slave [Collins, 2005]. Also, in each latch, high-speed operation could be impaired whenever the cross-coupled stage of each latch failed to accomplish the hold-data phase. Therefore, in the master-slave D-type flip-flop, the cross-coupled pair with capacitive degeneration ($C_d$) is used for enhancing operation speed. In this case, it can be shown that the input conductance $G(\omega)$ of the cross-coupled pair is negative up to the frequency given by (3).

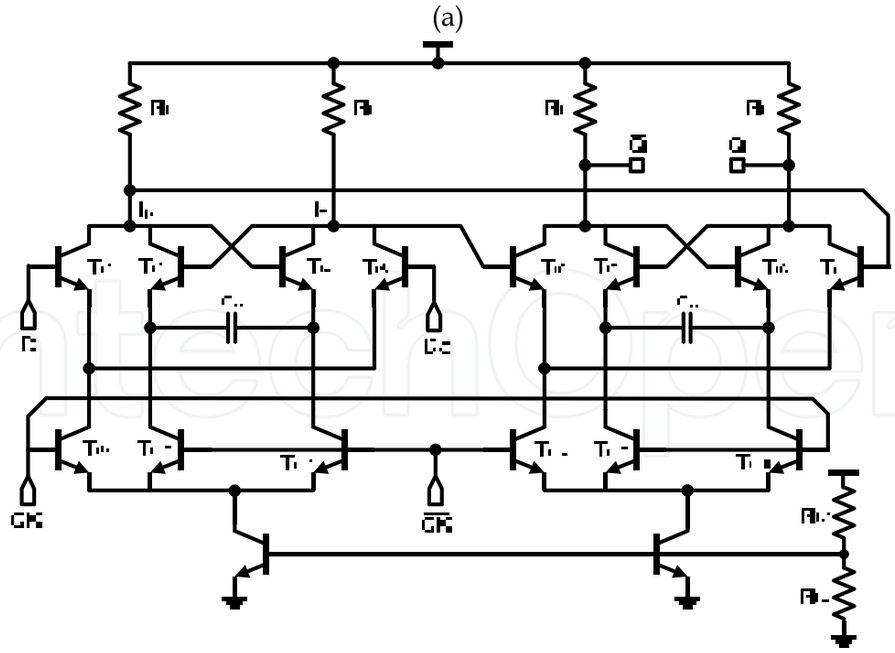
$$f_{G=0} = \frac{1}{2\pi}\sqrt{\frac{2\pi f_T\left(\frac{1}{C_d}+\frac{1}{C_\pi}\right)}{r_B}} \tag{3}$$

Here, $C_\pi$ is base-emitter capacitance of transistor, $r_B$ is base resistance, and $f_T$ is cut-off frequency. From (3), the capacitive-degeneration cross-coupled pair has higher conductance-zero frequency point than the common cross-coupled pair, and hence there is less possibility to miss the hold-data phase at higher operating frequency. In the capacitive-degeneration divider, drawbacks such as local instabilities and unwanted oscillations could be expected. Nevertheless, a careful choice of $C_d$ and tail current $I_L$ results in a high free-running switching time so that oscillations do not start due to the current steering of the bottom differential pair operating at the input clock frequency [Girlando, 2005]. The method finding the optimum values of $C_d$ and $I_L$ is illustrated in the simulation curves of Fig. 14 through which their values are set to guarantee both operating speed as high as possible and no oscillation in the divider. First, the proper value of $I_L$ should be set within the range of no oscillation. The Nyquist diagram of Fig. 14(a) shows the divider oscillates above 2.5mA of $I_L$, and then, the tail current is set by 1.5mA in this design considering power and speed. The clockwise encirclement of "1" at the horizontal axis of the Nyquist polar chart means that the transfer function of the divider circuit has poles in the right half plane i.e, it oscillates [Paul,

2001][Lee, 2002]. Second, after fixing $I_L$, we must check whether the divider oscillates by sweeping the value of $C_d$. As shown in the Nyquist diagram of Fig.14(b), the divider oscillates over 900f, and the optimum value of $C_d$ is set to 100fF, considering process variation and speed. The value of $C_d$ is the smaller, the higher increases the $f_G$ of Eq. (3). When $C_d$ is fixed to 100fF, the conductance zero frequency point of the divider is simulated by 84GHz, as shown in Fig.14(c)

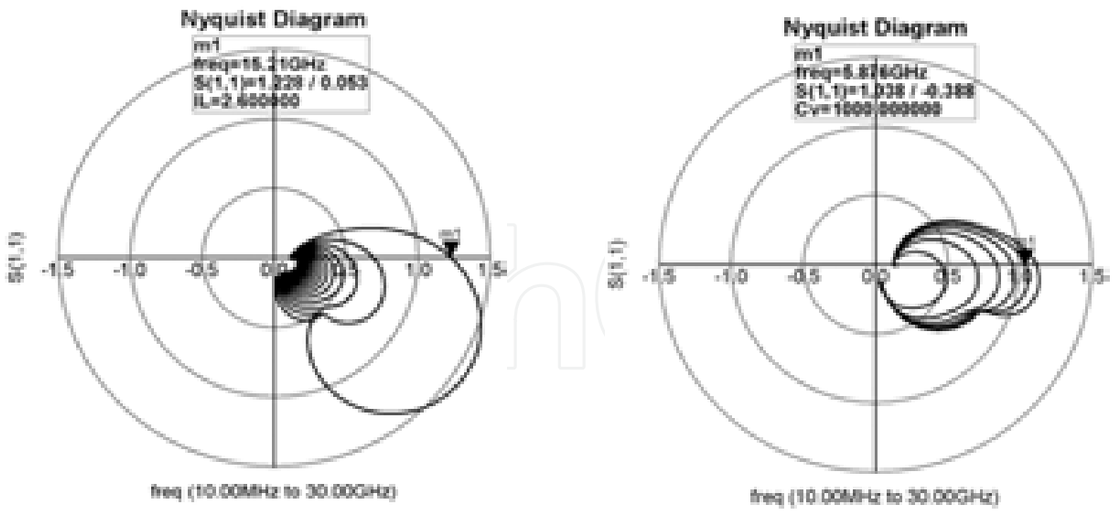


(a)

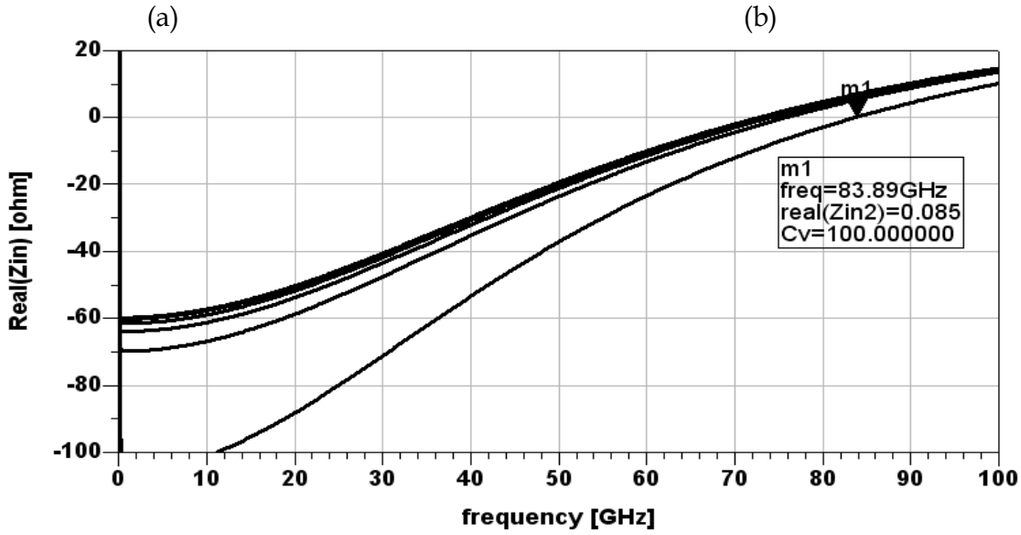


(b)

Fig. 13. (a) E²CL D-type flipflop with embedded NOR gate (b) E²CL D-type flipflop




(a) (b)




(c)

Fig. 14. (a) Nyquist test diagram for oscillation vs $I_L$, (b) Nyquist test diagram for oscillation vs $C_d$, (c) $f_G$ simulation vs $C_d$, here $C_d = C_v$

The CML DFF used in the divide-by-5 circuit is made up of a cascade of a master D-latch and a slave latch with the clocks reversed in the second ones as shown in Fig. 15. The differential clocks steer the current of the current source from one side to the other side, and from the tracking mode to the hold mode. The values of load resistors are set to be as large as possible to confirm high speed at low current consumption. Transistors such as M1, M2, M3, and M4 are sized just large enough to be able to completely steer the current at worst case. Transistors M5 and M6 must be just large enough to quickly regenerate the current state during the hold mode. Finally, the current magnitude of Is must be high enough to allow a large swing at the output node and not limit switching bandwidth [Lam, 2000].

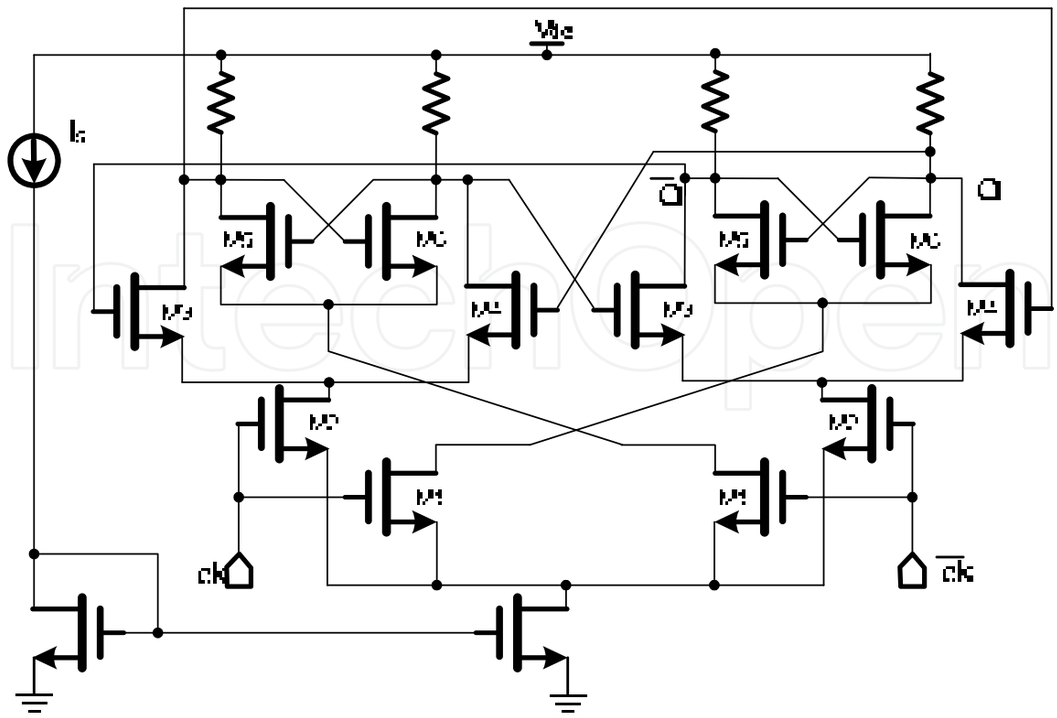



Fig. 15. CML D-type flipflop

As static logics require single-ended rail-to-rail swing, the non-rail-to-rail differential swing of the prescaler must be converted appropriately. A differential-to-single-ended signal level converter (DSC) must be inserted at the output $Q_2$ of the CML DFF in figure 10. The simplest circuit for this task is the four-transistor circuit shown in Fig. 16. The differential outputs of the CML DFF drive the input PMOS transistors (P1, P2), and then the single-ended output is at the drains of P2 and N2. P2 charges the output, and N2 discharges it.

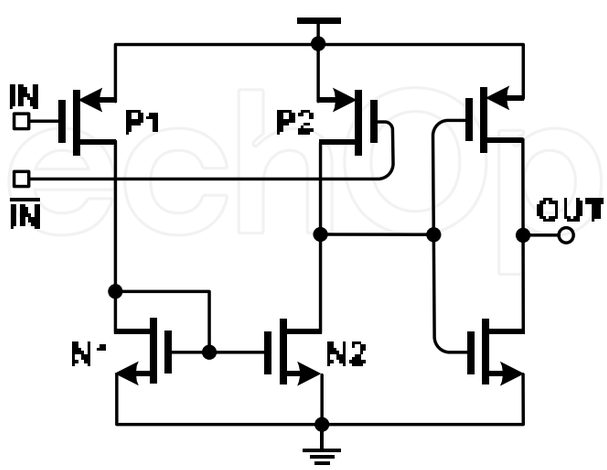



Fig. 16. Differential-to-single-ended converter

In designing this circuit, there are two factors to keep in mind. The first is the load capacitance at the input and output. The second is the power consumption since the current

is not fixed and it must still be operated at a relatively high frequency. A current source cannot be used to bias this circuit because a rail-to-rail swing at the output is required. The size of input PMOS pairs must be as small as possible while providing the necessary current to charge the output node. The amount of current N2 gets to discharge the output node is determined by the current mirror configuration of N1 and N2. Thus, those transistors can almost be minimum size and still provide enough current to discharge the output node if N1 is smaller than N2. This results in a multiplication of the current through N1 to N2. In this design, N2 is 1.5 times larger than N1. For sharper rise and fall edges, one inverter is added at its output.

Fig. 17 represents a single-phase CML OR/NOR logic, which receives two single-phase inputs and then outputs complementary differential logic signals. In the CML logic, both road resistor and current-mirror transistor should be optimally sized to achieve high speed and low current at the same time. The gate voltage of inverted MOS transistor outputting Q is fixed by the voltage divider configured with $R_1$ and $R_2$, which determins the output logic level.

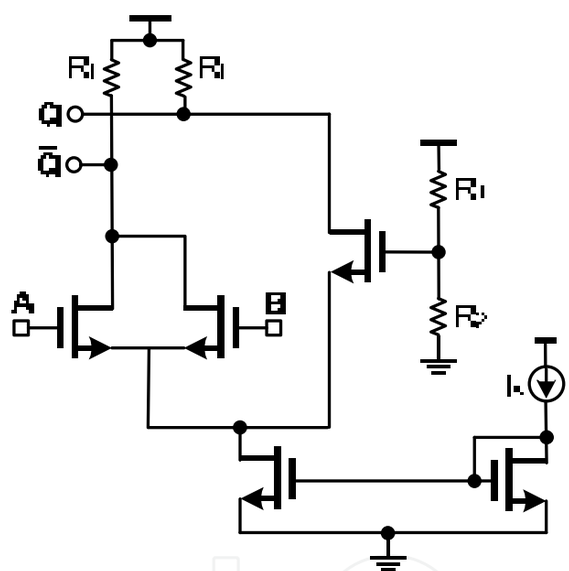
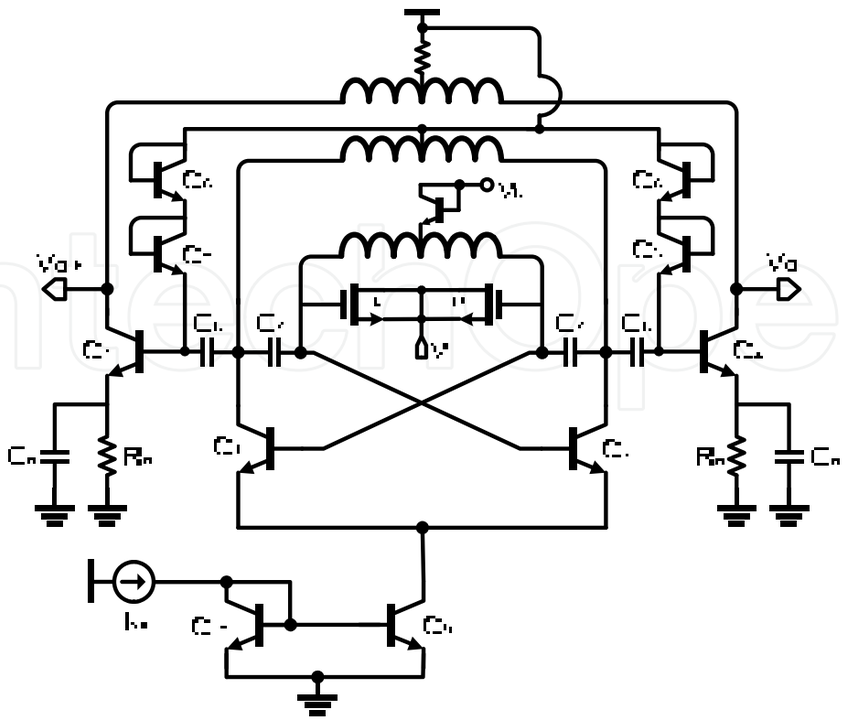


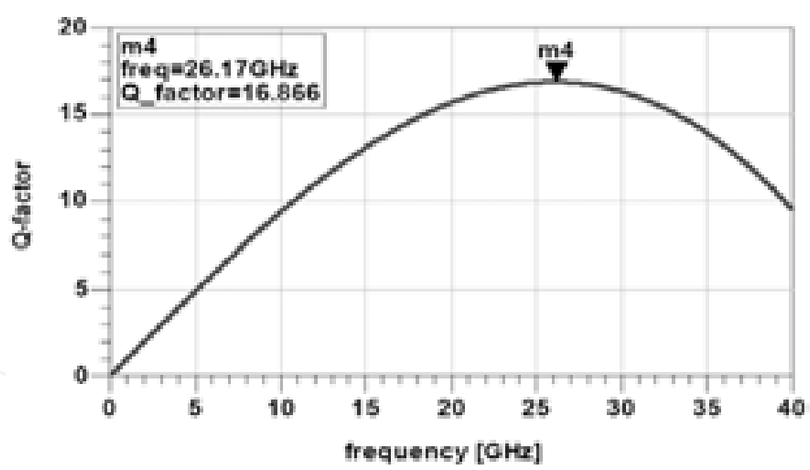

Fig. 17. Single phase complementary OR/NOR logic

### 3.4 Design of LC-tank VCO

In this section, a 26-GHz LC-tank VCO with 6 % tuning range is described. Here, we should design only a 26-GHz VCO because a 52-GHz frequency doubler follows it. Fig. 18(a) illustrates the circuit diagram of the 26-GHz LC-tank VCO used in the 52-GHz frequency synthesizer. It is a basic balanced differential oscillator that uses a cross-coupled differential pair. In the VCO circuit, the cross-coupled pair consisting of Q1 and Q2 generates negative conductance to compensate the LC-tank loss. In Fig. 18(a), one of three 700-pH inductors is used in the LC-tank resonator, another is connected to the collector node of oscillation transistors($Q_1$ and $Q_2$), the remaining inductor is used as the load impedance of the common- emitter amplifier.



(a)




(b)

Fig. 18. (a) LC-tank VCO circuit (b) Differential Q-factor of center-tapped inductor

As shown in Fig. 18(b), the center-tapped inductor represents a quality factor of 16.8 around 26GHz. For compensating loss due to the resistance component of inductor and guaranteeing enough oscillation, a cross-coupled pair having much larger negative conductance around 26 GHz should be used. That is, since only the cross-coupled pair does not replenish enough energy causing oscillation around 26GHz due to the large loss of inductor, in Fig.18(a), the feedback capacitor $C_f$ is inserted into the positive feedback path of the cross-coupled pair, and thus negative conductance is increased. The feedback capacitor

has a role to block DC flow and couple the RF signal power. Also, $C_f$ prevents the forward bias of the base-collector junction of the oscillation transistor, which results in high negative conductance as well as high oscillation signal amplitude. The high signal swing lowers phase noise of VCO. That is, the negative conductance is pulled up to higher frequency and increased. Both input negative resistance and effective input capacitance of the cross-coupled pair with feedback capacitor can be estimated as (4) and (5) [Veenstra, 2004][Jung, 2004].

$$R_{in} = \frac{2(r_b + r_e)^2 + 2\left[\frac{1}{\omega C_f} + \left(\frac{\omega_T}{\omega}\right)(\frac{1}{g_m} + r_e)\right]^2}{(r_b + r_e) - (\frac{\omega_T}{\omega})^2(\frac{1}{\omega_T C_f} + \frac{1}{g_m} + r_e)} \tag{4}$$

Here, $g_m$ is transconductance, $C_f$ is feedback capacitance, $r_e$ is intrinsic emitter resistance, and $r_b$ is intrinsic base resistance. In (4), negative resistance decreases with frequency, and then the zero-point frequency negative resistance becomes zero is finally reached. Therefore, the addition of the feedback capacitor in the cross-coupled path raises the zero-point frequency upward higher frequency band. This is proved by the factor of $(1/\omega C_f)^2$ in the nominator of (4).

$$C_{in} = \frac{\left(\frac{\omega_T}{\omega^2}\right)(\frac{1}{\omega_T C_f} + \frac{1}{g_m} + r_b + 2r_e)}{2(r_b + r_e)^2 + 2\left[\frac{1}{\omega C_f} + (\frac{\omega_T}{\omega})(\frac{1}{g_m} + r_e)\right]^2} \tag{5}$$

As shown in (5), the effective input capacitance is a function of the feedback capacitance $C_f$. It is noted that the effective input capacitance decreases in proportional to the factor of $(1/\omega C_f)^2$ in the denominator. As a result, the oscillation frequency can be increased due to the reduced $C_{in}$.

Commonly, the quality factor of LC-tank resonator in VCO is degraded by the load connected to it, and therefore, the LC-tank resonator consisting of a center-tappled inductor and two NMOS varactors is wired on the base node of the cross-couled pair. As shown in Fig.19(a), the collector and base nodes of the cross-coupled pair is separated by $C_f$, which has a role to protect the LC-tank resonator against the load. Additionally, it is worth noting that the negative conductance of the cross-coupled pair is different, depending upon the position looking into it from the LC-tank resonator, as illustrated in Fig.19. The curve of $G_{cin}$ represents the input negative conductance looking into the collector node of the cross-coupled pair, and the bold line serves as the curve of $G_{bin}$ looking into the base node of the cross-coupled pair. In Fig. 19, it is clearly apparent that $G_{bin}$ is greater than $G_{cin}$ about 25GHz frequency. That is, $G_{bin}$ could be made greater than $G_{cin}$ in some target frequency range by

tuning $C_f$ and tail current, which results in larger oscillation amplitude and lower phase noise. In summary, the feedback capacitor $C_f$ does not only improve the loaded quality factor of the VCO, but also enlarge negative conductance at target frequency.

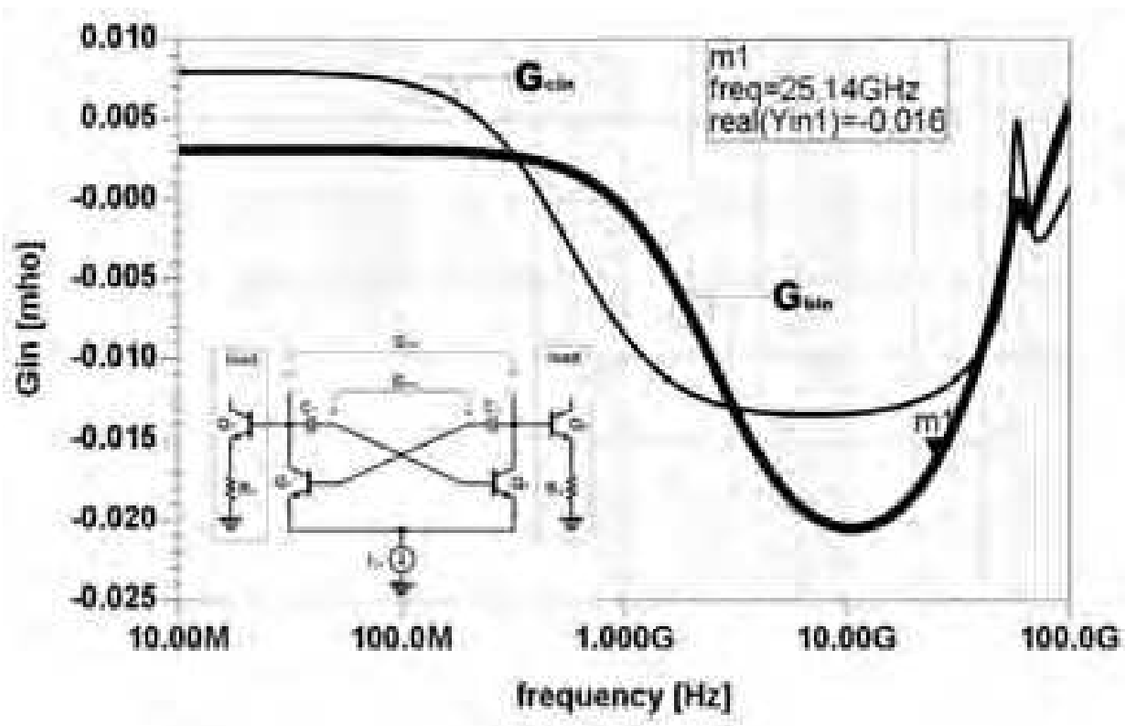



Fig. 19. Simulated input negative conductance of the cross-coupled pair

### 3.5 Design of 52GHz Frequency Doubler

A 52-GHz frequency doubler is presented as shown in Fig. 20. In the doubler circuit, the collector nodes of the differential amplifier configured with Q1 and Q2 are put together for extracting the even-mode signal. Also, another even-mode signal with different phase is extracted from the combined emitter node of the differential amplifier. The common-base amplifier Q3 is used for amplifying the even-mode signal extracted from the emitter node. Both Cm and Rm are used to tune the amplitude and phase difference between the signal extracted from the emitter node and the signal extracted from the collector node [Gruson, 2004]. The common-emitter amplifiers of Q4 and Q5 are used to amplify the extracted even-mode differential signals. Fig. 21 shows the simulated output spectrum of the frequency doubler, which suppresses the fundamental frequency component of 26GHz by 75dB, the third harmonic frequency component of 78GHz by 90dB, and the fourth harmonic component of 104GHz by 25dB. Since other harmonic components have been suppressed above 20dB, therefore, the second harmonic frequency component of 52GHz will show a linear sine waveform without distortion.

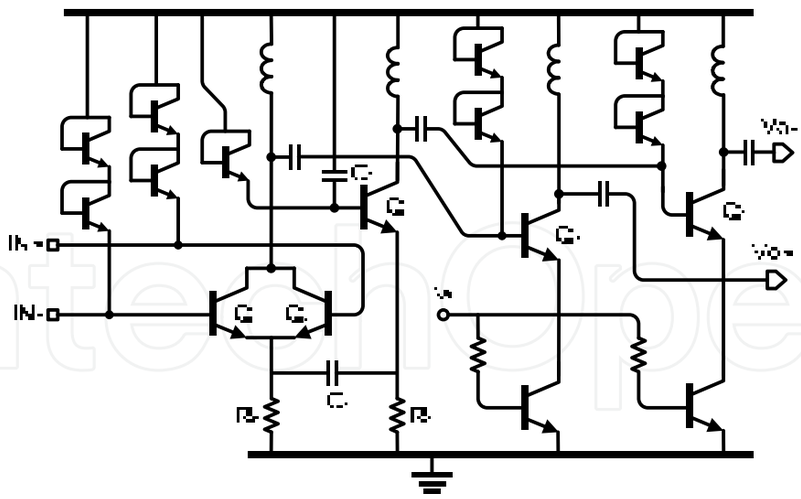



Fig. 20. 52GHz frequency doubler

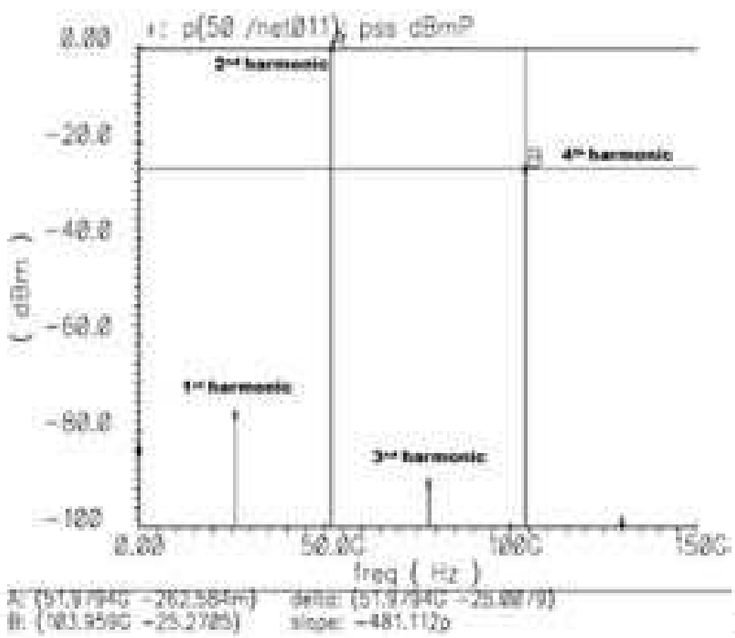



Fig. 21. Simulated output spectrum of the frequency doubler

In designing the 52GHz frequency synthesizer of Fig. 2, its full circuit is simulated using Cadence Spectre RF simulator. In the frequency synthesizer, the 3rd order loop filter is used, and is implemented by using poly resistor and MIM capacitor. In the test circuit, 262MHz reference frequency is used for close-loop simulation. Fig. 22 shows the simulated close-loop settling time of the frequency synthesizer, which is about 0.8μs.

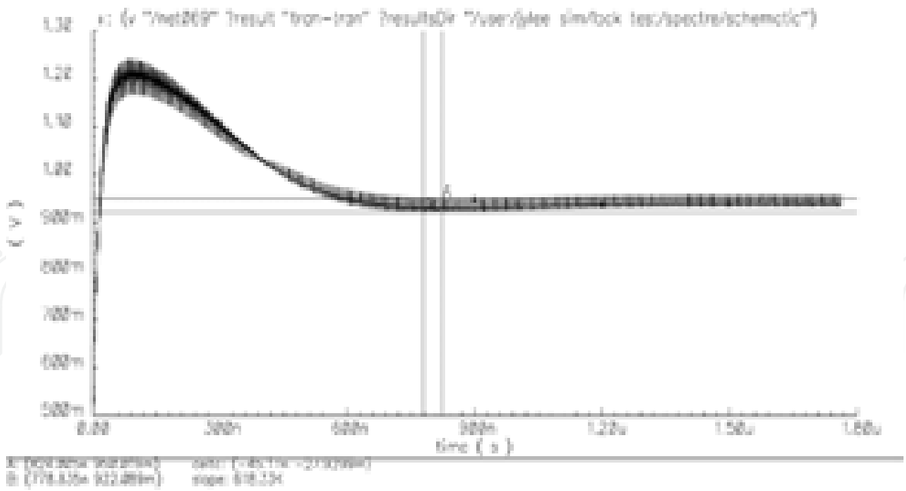


Fig. 22. Simulated close-loop settling time of the frequency synthesizer

## 4. Measured results

Fig.23 represents the chip microphotograph of the 52-GHz PLL synthesizer whose die area is 1.2mm² area including bonding pads. The PLL chip was designed and fabricated using 0.25-µm SiGe:C BiCMOS process technology. Both $f_T$ and $f_{max}$ of a HBT (hetero-junction bipolar transistor) used in this design are 180GHz and 200GHz, respectively. The PLL chip was measured using Agilent E4440A 26.5-GHz spectrum analyzer and 11970V harmonic mixer after it was mounted on probe station.

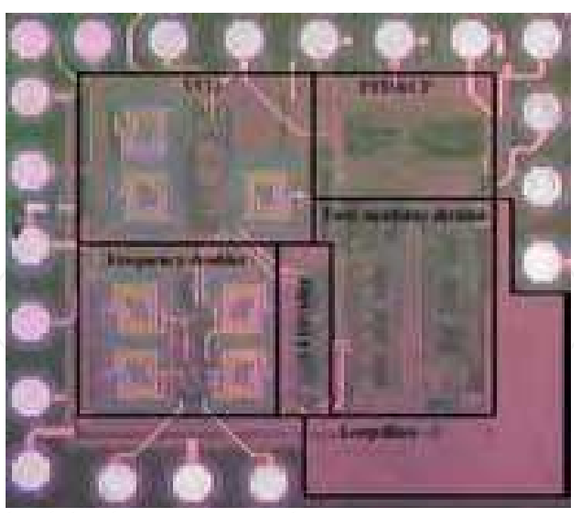


Fig. 23. Chip photograph of the frequency synthesizer

Fig. 24 shows the measured frequency tuning range of the cross-coupled differential LC VCO. Its tuning range is measured from 24.72GHz to 26.44GHz, consuming a current of 38 mA at 2.5 V. Fig. 25 shows the locked signal of 52.4GHz when 262 MHz is input to PFD and a divide ratio of ÷ 100 is selected. The PLL synthesizes two channels of 50.304GHz and

52.4GHz by 2.096GHz step. The spurious noise level is measured as – 42dBc, and this poor suppression about spurious noise is due to the small value of capacitors used in the loop filter. In this PLL chip, the size of the loop capacitors has been reduced as small as possible due to the limited chip area. The output power of the PLL is measured as – 17.6 dBm, and the decreased output power is due to both cable loss and unexpected low quality factor of the load inductor used in the amplifiers of $Q_4$ and $Q_5$. Fig. 26 represents the output power spectrum in span of 8MHz.

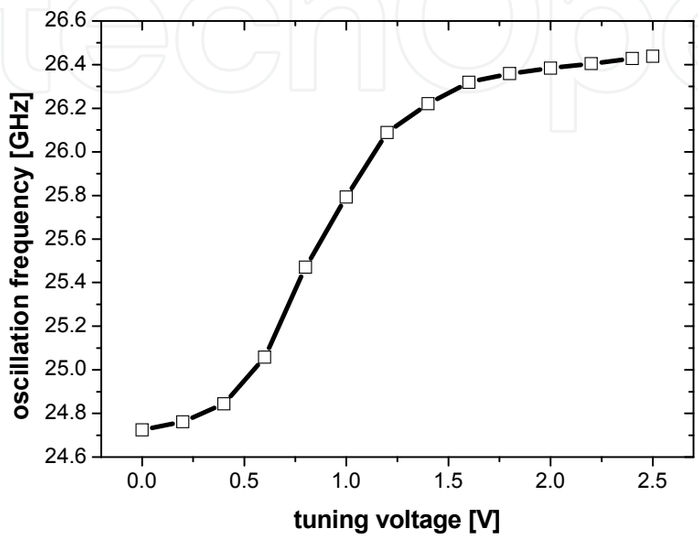



Fig. 24. Measured frequency tuning range of VCO

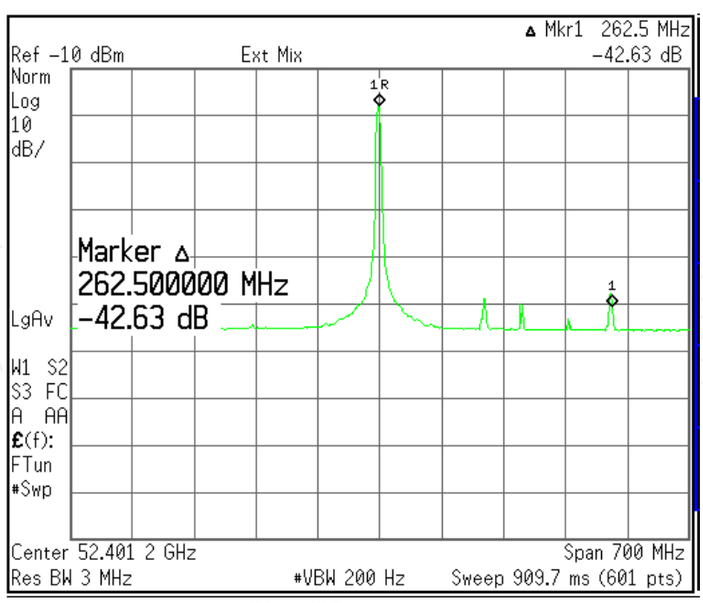



Fig. 25. Measured output spectrum of 52.4GHz locked carrier

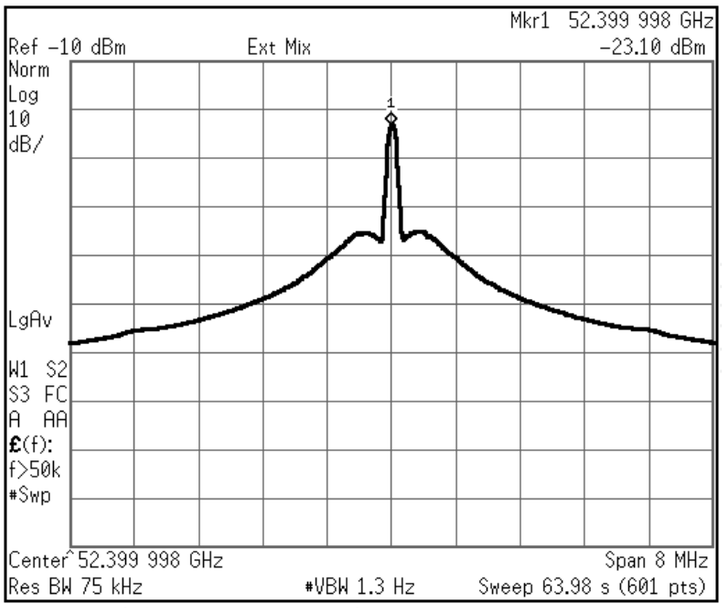



Fig. 26. Output spectrum of the PLL in span of 8MHz

Fig. 27 represents its measured phase noises, which are – 89dBc/Hz from 26.2GHz and – 81dBc/Hz from 52.4GHz, respectively, at 1MHz offset frequency. Its integrated RMS phase noise from 1MHz to 100MHz is estimated as 7.42°. The phase noise of the 52.4GHz second harmonic carrier is approximately estimated from formula (6) using the measured phase noise data of 26.2GHz first harmonic carrier in Fig. 27. Since the 26.2GHz carrier having a phase noise of – 109dBc/Hz at 10MHz offset doubles to 52.4 GHz due to the doubling operation of the frequency doubler, the phase noise of 52.4GHz carrier increases by 6 dB and becomes approximately – 102dBc/Hz due to the $(f_o)^2$ term of formula (6), which does almost fit to the measured phase noise curve of Fig. 27. That is, the phase noise of the 52.4-GHz carrier is degraded by about 7dB at offset frequency under 10MHz, compared with that of 26.2GHz fundamental carrier. This is close to the expected degradation of 6dB caused by the operation doubling frequency. Above 10MHz offset, the phase noise degradation of the doubled 52.4GHz carrier increases more and more due to the noise floor of the measurement system.

$$L(f_{off}) = 10\log\left\{\left(1+\frac{f_o}{2Qf_{off}}\right)^2\left(\frac{FkT}{2P_o}\left(1+\frac{f_{1/f^3}}{f_{off}}\right)\right)\right\} \tag{6}$$

Here, $f_o$ is carrier frequency, Q is loaded factor, F is noise floor of active oscillator, k is Boltzman constant, $P_o$ is signal power, $f_{off}$ is offset frequency, and $f_{1/f^3}$ is $1/f^3$ corner frequency [Lee, 2000][Leeson, 1966].

In Table 1, the measured results of the 52GHz PLL synthesizer are summarized. Here, the settling time of the PLL is simulated as 800ns in Fig. 22. The PLL chip consumes a total current of 160mA of which 45% is drawn by the programmable divider.

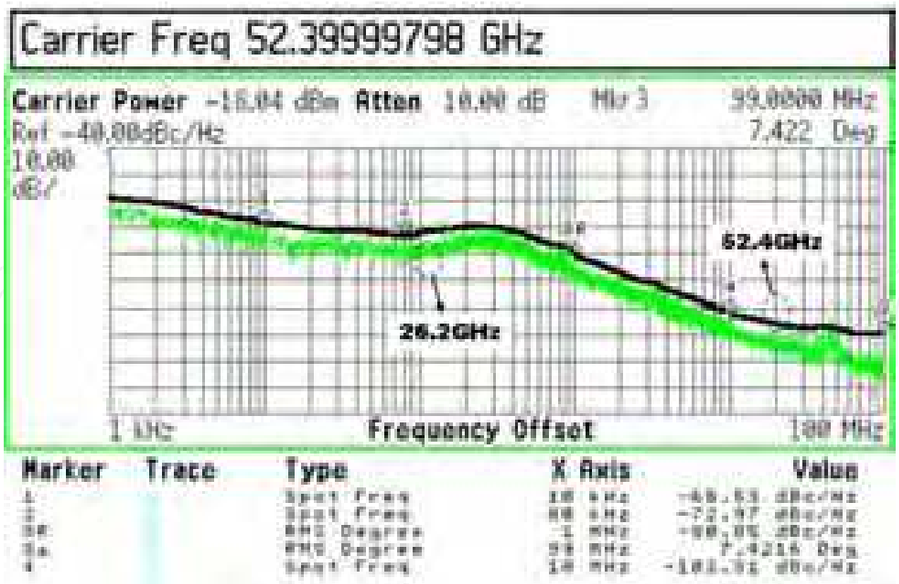



Fig. 27. Measured phase noise of the PLL

| | |
|---|---|
| Technology | 0.25μm SiGe:C BiCMOS |
| Supply voltage | 2.5V |
| Reference frequency | 262-264MHz |
| VCO tuning range | 24.723 – 26.439GHz (6%) |
| PLL output frequency | 24.9–26.50GHz |
| (PLL + doubler) output frequency | 50.1 –52.8GHz |
| Loop bandwidth | 600kHz-1 MHz |
| In-band phase noise @100kHz offset | -80 dBc/Hz from 26.2 GHz<br>-73 dBc/Hz from 52.4 GHz |
| Out-band phase noise @1MHz offset | -89 dBc/Hz from 26.2 GHz<br>-81 dBc/Hz from 52.4 GHz |
| Out-band phase noise @10MHz offset | -109 dBc/Hz from 26.2 GHz<br>-102 dBc/Hz from 52.4 GHz |
| RMS Jitter | 7.42° (from 1MHz to 100MHz) |
| Spurious noise level | < - 42 dBc |
| Settling time | < 800 ns |
| Current consumption | 160mA at 2.5V |
| Chip size | 1.0 mm × 1.2 mm |

Table 1. Measured results of the 52GHz frequency synthesizer

## 5. Conclusion

In this chapter, we design and fabricate a 52GHz frequency synthesizer for 60GHz dual-conversion receiver using SiGe BiCMOS process technology. The designed PLL-based frequency synthesizer consists of a 26-GHz PLL and a 52-GHz frequency doubler. In the

programmable divider, a capacitive-degeneration D-F/F is used to achieve high-speed operation. The method finding the optimum values of both degeneration capacitance and tail current is presented in order to attain high speed and guarantee no self-oscillation in the degeneration D-F/F circuit. A cross-coupled differential LC VCO with feedback capacitor is designed to generate 26GHz oscillation frequency. By tuning feedback capacitance and tail current properly, the input negative conductance at the base node of the cross-coupled pair could be enlarged at target frequency, and also, the feedback capacitance stops the loaded quality factor of VCO from being degraded by the load.

The 52GHz PLL synthesizer provides two channels of 50.304GHz and 52.4GHz by 2.096GHz step through the frequency doubler. The phase noises of the PLL are measured as – 89dBc/Hz at 1MHz offset from 26.2GHz first harmonic carrier, and – 81dBc/Hz at the same offset frequency from 52.4GHz second harmonic carrier. The PLL consumes 160mA at 2.5V and takes silicon-die area of 1.2mm$^2$.

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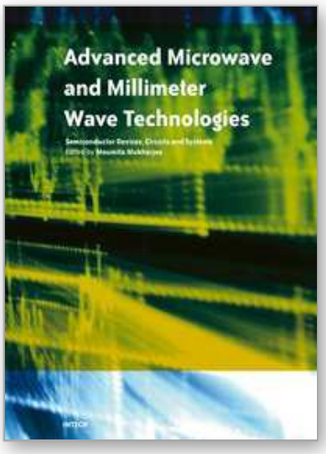


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