View metadata, citation and similar papers at core.ac.uk

brought to you by CORE

provided by IntechOpen

We are IntechOpen, the world's leading publisher of Open Access books Built by scientists, for scientists

4,800
Open access books available

122,000
International authors and editors

135M
Downloads

Our authors are among the

154
Countries delivered to

TOP 1%
most cited scientists

12.2%
Contributors from top 500 universities

WEB OF SCIENCE™

Selection of our books indexed in the Book Citation Index in Web of Science™ Core Collection (BKCI)

Interested in publishing with us?
Contact book.department@intechopen.com

Numbers displayed above are based on latest data collected.
For more information visit www.intechopen.com

18

The Switched Mode Power Amplifiers

Elisa Cipriani, Paolo Colantonio, Franco Giannini and Rocco Giofrè
University of Roma Tor Vergata
Italy

1. Introduction

The power amplifier (PA) is a key element in transmitter systems, aimed to increase the power level of the signal at its input up to a predefined level required for the transmission purposes. The PA's features are mainly related to the absolute output power levels achievable, together with highest efficiency and linearity behaviour.
From the energetic point of view a PA acts as a device converting supplied dc power (P_{dc}) into microwave power (P_{out}). Therefore, it is obvious that highest efficiency levels become mandatory to reduce such dc power consumption. On the other hand, a linear behaviour is clearly necessary to avoid the corruption of the transmitted signal information. Unfortunately, efficiency and linearity are contrasting requirements, forcing the designer to a suitable trade-off.
In general, the design of a PA is related to the operating frequency and application requirements, as well as to the available device technology, often resulting in an exciting challenge for PA designers, since not an unique approach is available.
In fact, PAs are employed in a broad range of systems, whose differences are typically reflected back into the technologies adopted for PAs active modules realisation. Moreover, from the designer perspective, to improve PAs efficiency the active devices employed are usually driven into saturation. It implies that a PA has to be considered a non-linear system component, thus requiring dedicated non linear design methodologies to attain the highest available performance.
Nevertheless, for high frequency applications it is possible to identify two main classes of PA design methodologies: the trans-conductance based amplifiers with Harmonic Tuning terminations (HT) (Colantonio et al., 2009) or the Switching-Mode (SM) amplifiers (Grebennikov & Sokal, 2007; Krauss et al., 1980). In the former, the active device acts as a nonlinear current source controlled by the input signal (voltage or current for FET or BJT devices respectively). A simplest schematic view of such an amplifier for FET is reported in Fig. 1a. Under this assumption, the high efficiency condition is achieved exploiting the device nonlinear behaviour through a suitable selection of both input and output harmonic terminations. More in general, the trans-conductance based amplifiers are identified also as Class A, AB, B to C considering the quiescent active device bias points, resulting in different output current conduction angles from 2π to 0 respectively.
The most famous solution of HT PA is the Class F approach (Gao, 2006; Colantonio et al, 2009), while for high frequency applications and taking into account practical limitations on

the control of harmonic impedances, several solutions have been successfully proposed (Colantonio et al., 2003).

Conversely, in the SM PA, the active device is driven by a very large input signal to act as a ON/OFF switch with the aim to maximise the conversion efficiency reducing the power dissipated in the active devices also. A schematic representation of a SM amplifier is depicted in Fig. 1b. When the active device is turned on, the voltage across its terminals is close to zero and high current is flowing through it. Therefore, in this part of the period the transistor acts as a very low resistance, ideally short circuit (switch closed) minimising the overlap between the current and voltage waveforms. In the other part of the period, the active device is turned off acting as an open circuit. Therefore, the current is theoretically zero while high voltage is present at the device terminals, once again minimising the overlap between voltage and current waveforms. If the active device shows a zero on resistance and an infinite off resistance, a 100% efficiency is theoretically achieved. The latter is of course an advantage over Class A or B, where the maximum theoretical efficiencies are 50 % and 78 % respectively. On the other hand, Class C could achieve high efficiency levels, despite a significant reduction in the maximum output power level achievable (theoretically 100% of efficiency for zero output power). Nevertheless, the HT PAs are intrinsically able to amplify the input signal with higher fidelity, since the active device is basically represented by a controlled current source (FET case) whose output current is directly related to the input voltage. Instead, in SM PAs the active device is assumed to be ideally driven in the ON and OFF states, thus exhibiting a higher nonlinear behaviour. However, this characteristic does not represent a trouble when signals with constant-envelope modulation are adopted.

On the basis of their operating principle, SM amplifiers are often considered as DC to RF converter rather than RF amplifiers.

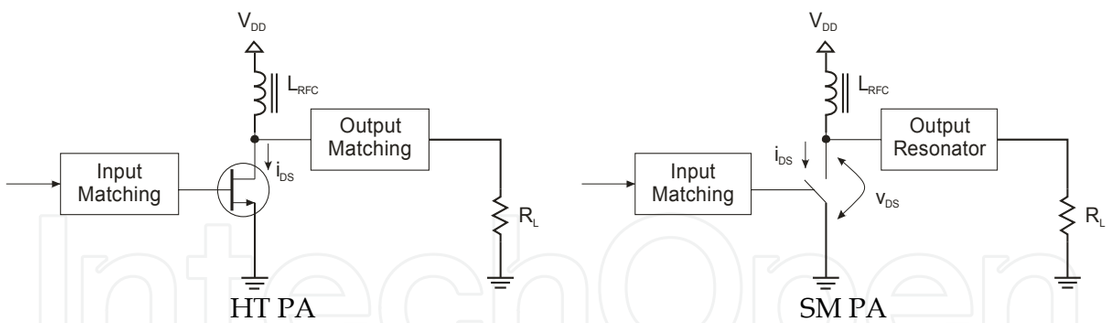


Fig. 1. Simplified view of a simple single ended HT (left) and SM (right) PA.

Different SM PA classes of operation have been proposed over the years, namely Class D, S, J, F-1 (Cripps, 2002; Kazimierczuk, 2008), while the most famous and adopted is the Class E PA (Sokal & Sokal, 1975; Sokal, 2001) that will be described in deep detail in the following. As will be shown, these classes are based on the same operating principle while their main differences are related to their circuit implementation and current-voltage wave shaping only.

The applications of SM PAs principles have initially been limited to amplifiers at lower frequencies in the megahertz range, due to the active device and package parasitics practically limiting the operating frequencies (Kazimierczuk, 2008). They have also been

applied to DC/DC power converters that also operate at lower switch frequencies (Jozwik & Kazimierczuk, 1990; Kazimierczuk & Jozwik, 1990). Recently, their principles of operation have been extended and applied to RF and microwave amplifier design, made possible by the high-performance active devices nowadays available based on silicon (Si), gallium arsenide (GaAs), silicon germanium (SiGe), silicon carbide (SiC), and gallium nitride (GaN) technologies (Lai, 2009).

2. Switching mode generic operating principle

The operating principle of every SM PA is based on the idea that the active device operates in saturation, thus it can be represented as a switch and either voltage or current waveforms across it are alternatively minimized to reduce overlap, so minimizing power dissipation in the device itself. If the transistor is an ideal switch, a 100% of efficiency can be achieved by the proper design of the output matching network. As reported in Fig. 1b, the output resonator can be assumed, in the simplest way, as an ideal *L*-*C* series resonator at fundamental frequency, terminated on a series load resistance (R_L). The role of the resonator is to shape the voltage and current waveforms across the switch in order to avoid power dissipation at higher harmonics. In fact, an ideal *L*-*C* series resonator shows zero impedance at resonating frequency ($\omega_0=(LC)^{-1/2}$) and infinite impedance for every $\omega\neq\omega_0$. It follows that fundamental current only is flowing into the output load and fundamental voltage only is generated at its terminals. Consequently, 100% of efficiency is obtained (being zeroed the overlap between voltage and current waveforms over the transistor, thus being nulled the power dissipated in it) and no power is delivered at harmonic frequencies in the load, being the latter not allowed to flow into the load R_L.

In actual cases, several losses mechanisms, such as ohmic and capacitive discharge or leakage, cause an unavoidable overlapping between the voltage and current waveforms, together with power dissipation at higher harmonics, thus limiting the maximum achievable efficiency levels.

The most relevant losses in SM PA are represented by:

- parasitic capacitors, such as the device drain to source capacitance C_{ds}. The presence of such capacitance causes a low pass filter behaviour at the output of the active device, affecting the voltage wave shaping with a consequent degradation in the attainable power and efficiency levels. In fact, considering the active device as the parallel connection of a perfect switch and the parasitic capacitance C_{ds}, the higher voltage harmonics are practically shorted by C_{ds} and only few harmonics can be reasonably controlled by the loading network.
- parasitic resistance, such as the drain-to-source resistance when the transistor is conducting R_{ON} (ON state). In fact, due to the non zero resistance when the switch is closed, a relevant amount of active power will be dissipated in the transistor causing a lowering in the achievable efficiency.
- non-zero transition time, due to the presence of parasitic effects, which increase the voltage and current overlap.
- implementation losses due to the components (distributed or lumped elements) employed to realise the required input and output matching networks.

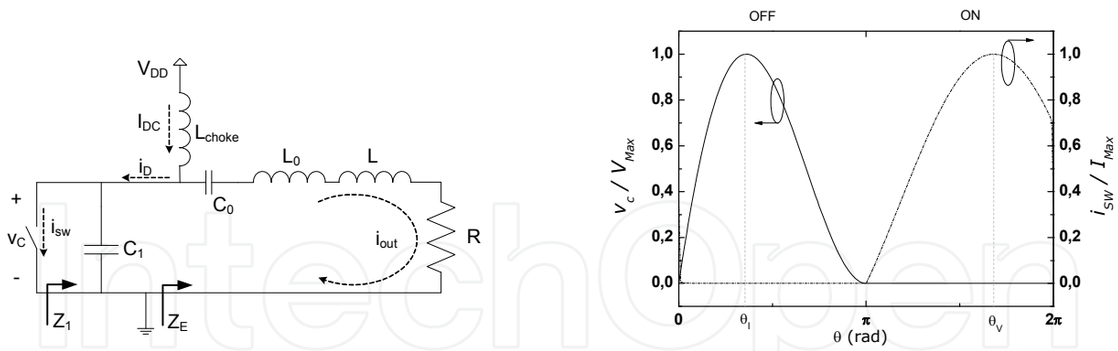
The entity of the parasitic components as well as the associated losses are strictly related to the characteristics of the active device used, especially when designing RF PA (Kazimierczuk, 2008; Lai, 2008).

3. The Class E Amplifier

Firstly presented in the early 70's in (Sokal & Sokal, 1975), the Class E power amplifier recently received more attention by microwave engineers with the growing demand of high efficient transmitters in wireless communication systems.
It has been widely adopted in constant envelope based communication systems, but represents a valid alternative if combined with envelope varying technique also, like envelope elimination and restoration or Chireix's outphasing technique (Cripps, 2002).
A complete analysis of the Class E amplifier is herein presented, making the assumption of a very idealized active device switching action. The topology considered is the most common one, firstly presented in (Sokal & Sokal, 1975), although different Class E topologies have been conceived and studied during the past (Mader et al., 1998; Grebennikov, 2003; Suetsugu & Kazimierczuk, 2005). In order to clarify Class E operation, a real device-based design is also briefly presented.

3.1 Analysis with a generic duty cycle

The basic topology of a single ended Class E power amplifier is depicted in Fig. 2. The active device is schematically represented as an ideal switch and it is shunted by the capacitance C_1, which include the output equivalent capacitance of the active device also. The output network is composed by an ideal filter C_0-L_0 with a series R-L impedance.



(a) (b)

Fig. 2. Basic topology of a Class E amplifier (a) corresponding ideal waveforms (b).

Such a circuit is usually analyzed in time domain, which is a straightforward but tedious process, requiring the solution of non linear differential equations. Anyway, some hypotheses can be adopted to carry out a simplified analysis useful to understand the underling operating principle.
Considering the series resonator C_0-L_0 to behave as an ideal filter, i.e. with an infinite (or high enough) Q factor, harmonics and all frequency components different from the fundamental frequency can be considered as filtered out and do not play any role in the

solution of the system. As a consequence, the current flowing into the output branch of the circuit can be assumed as a pure sinusoidal, with its own amplitude I_M and its phase ϕ (Raab, 2001):

$$i_{out} = I_M \cdot \sin(\theta + \phi) \tag{1}$$

Where $\theta = \omega \cdot t$.
Consequently, from Kirchhoff laws the current i_D (see Fig. 2), which flows entirely through the switch during the ON period (i_{SW}) or entirely through the capacitance C_1 during the OFF period, can be written as:

$$i_D = I_{DC} - I_M \cdot \sin(\theta + \phi) \tag{2}$$

Assuming for simplicity a 50% of duty cycle (the analysis for a generic duty cycle is available in (Suetsugu & Kazimierczuk, 2007)), the current flowing into the switch i_{SW} can be expressed as:

$$i_{sw}(\theta) = \begin{cases} 0, & 0 \le \theta \le \pi \\ I_{DC} - I_M \cdot \sin(\theta + \phi), & \pi \le \theta \le 2\pi \end{cases} \tag{3}$$

And analogously the current in the capacitor C_1 becomes:

$$i_C(\theta) = \begin{cases} I_{DC} - I_M \cdot \sin(\theta + \phi), & 0 \le \theta \le \pi \\ 0, & \pi \le \theta \le 2\pi \end{cases} \tag{4}$$

While the voltage across the capacitance v_C can be easily inferred by integration of (4), resulting in the following expression:

$$v_C(\theta) = \begin{cases} \frac{1}{\omega \cdot C_1} \cdot \left(I_{DC}\theta + I_M \cdot \cos(\theta + \phi) - I_M \cdot \cos(\phi) \right), & 0 \le \theta \le \pi \\ 0, & \pi \le \theta \le 2\pi \end{cases} \tag{5}$$

The resulting theoretical current and voltage waveforms are depicted in Fig. 2b.
It can be noted that current and voltage across the switch do not overlap, thus no power dissipation exists on the active device. The unique dissipative element in the circuit is the loading resistance R, which is active at fundamental frequency only. Then, from these assumption it follows that the DC to RF power conversion happens without losses and the theoretical efficiency is 100%.
The quantities I_{DC}, I_M and ϕ have still to be determined as functions of maximum current and voltage allowed by the adopted active device, I_{Max} and V_{Max} respectively, and of operating angular frequency ω.
For this purpose, it has to note that the capacitance C_1 should be completely discharged at the switching turn on, which implies that the voltage v_C has to be null in correspondence of the instant π (see Fig. 2b):

$$v_C(\theta)\big|_{\theta=\pi} = 0 \tag{6}$$

Such condition is usually referred as Zero Voltage Switching (ZVS) condition, which implies that the capacitance C_1 should not be short circuited by the switch turn on when its voltage is still high (Sokal & Sokal, 1975).
The second condition, namely Zero Voltage Derivative Switching (ZVDS) condition, or soft-switching condition, implies that the current starts to flow from zero after the switch turn on and then increases gradually, in order to prevent worsening in circuit performance due to mistuning of the waveforms (Sokal & Sokal, 1975). This condition is written as:

$$i_C(\theta)\big|_{\theta=\pi} = \frac{d}{d\theta} v_C(\theta)\bigg|_{\theta=\pi} = 0 \tag{7}$$

Substituting (4) in the previous equations, from (6) it follows:

$$I_{DC} \cdot \pi - 2 \cdot I_M \cos(\phi) = 0 \tag{8}$$

While from (7) it follows:

$$I_{DC} + I_M \cdot \sin(\phi) = 0 \tag{9}$$

Thus the following relationships can be inferred:

$$\tan(\phi) = -\frac{2}{\pi} \tag{10}$$

$$\frac{I_{DC}}{I_M} = -\sin(\phi) = \frac{2}{\pi} \cdot \cos(\phi) \tag{11}$$

The maximum current flowing into the switch is given by:

$$I_{Max} = I_{DC} + I_M \tag{12}$$

And it occurs in correspondence of the angle

$$\theta_I = \frac{3}{2} \cdot \pi - \phi \tag{13}$$

Similarly, for the voltage across the switch its maximum value occurs in correspondence of the angle θ_V (see Fig. 2b), which can be inferred nulling the derivate of v_c given by (5).
Thus, accounting for (11), it follows:

$$\theta_V = -2 \cdot \phi \tag{14}$$

and

$$V_{Max} = -2 \cdot \phi \cdot \frac{I_{DC}}{\omega C_1} \tag{15}$$

However, the value of the capacitance C_1 is still an unknown variable. It appears in the definition of the voltage waveform, and it is convenient to use voltage constraints in order to obtain its expression. In fact, its average value must be equal to the supplied DC voltage V_{DD}; thus it follows:

$$V_{DD} = \frac{1}{2\pi} \int_0^{\pi} v_C(\theta) d\theta \tag{16}$$

Which solved lead to:

$$V_{DD} = \frac{1}{2\pi} \cdot \frac{1}{\omega \cdot C_1} \cdot \left(I_{DC} \cdot \frac{\pi^2}{2} + 2 \cdot I_M \sin(\phi) - I_M \cdot \pi \cdot \cos(\phi) \right) \tag{17}$$

from which the value of C_1 can be finally determined remembering (11)

$$C_1 = \frac{I_{DC}}{\pi \cdot \omega \cdot V_{DD}} \tag{18}$$

This also suggests a simple relationship between DC current and bias voltage.
At this point, waveforms in Fig. 2b have been completely determined in the time domain, without recurring to the frequency domain. However, the remaining elements of the circuit, DC power, output power and output impedance have still to be determined.
As stated before, all the DC power is converted to RF power and dissipated into the load resistance at fundamental frequency:

$$P_{DC} = I_{DC} \cdot V_{DD} = \frac{1}{2} \cdot I_M \cdot V_M = P_{RF} \tag{19}$$

where V_M is the amplitude of fundamental component of the voltage across R which can be obtained by (19) and replacing (11):

$$V_M = 2 \cdot \frac{V_{DD} \cdot I_{DC}}{I_M} = -2 \cdot V_{DD} \cdot \sin(\phi) \tag{20}$$

The value of the resistance R is simply obtained as the ratio between V_M and I_M:

$$R = \frac{V_M}{I_M} = 2 \cdot \frac{V_{DD}}{I_{DC}} \cdot \sin(\phi)^2 \tag{21}$$

Clearly, if a standard 50 Ohm termination is required, an impedance transformer is necessary to adapt such load to the required R value.
Finally, the inductance L is computed taking into account that its reactive energy is exchanged, at every cycle, with the capacitance C_1. Thus it follows:

$$\frac{1}{2\cdot\pi}\cdot\frac{1}{\omega C_1}\int_0^{\pi}\left[I_{DC}-I_M\cdot\sin\left(\theta+\phi\right)\right]^2 d\theta=\frac{1}{2}\cdot\omega\cdot L\cdot {I_M}^2 \tag{22}$$

where the expression in the integral represents the voltage across the capacitance C_1 during the OFF period. The value for the inductance L is therefore given by:

$$L=\frac{1}{\omega\cdot C_1}\cdot\left(\frac{\pi}{2}-\frac{4}{\pi}\cdot\cos\left(\phi\right)^2\right) \tag{23}$$

Alternatively, R and L can be found by calculation off in-phase and quadrature voltage components, as elsewhere reported (Mader et al., 1998; Cripps, 1999).
The series impedance R-L can be put together in order to obtain a more compact and useful expression for the output branch impedance (Mader et al., 1998) normalized to the shunt capacitance C_1:

$$Z_E=\frac{0.28}{\omega C_1}\cdot e^{j49^\circ} \tag{24}$$

With reference to Fig. 2, the impedance Z_1 seen by the ideal switch is obtained by the shunt connection of the capacitance C_1 and Z_E and is herein given in its simplified formulation (Colantonio et al., 2005):

$$Z_1=\frac{0.35}{\omega C_1}\cdot e^{j36^\circ} \tag{25}$$

Remaining reactive components, L_0 and C_0, are easily calculated by means of:

$$\omega^2=\frac{1}{L_0\cdot C_0} \tag{26}$$

Provided a high enough Q factor, the values of L_0 and C_0 are non uniquely defined and any pair of resonant element can be used.
The analysis performed here was intended for the most common case of 50% duty cycle (i.e. π conduction angle). In this case the relations are greatly simplified thanks to the properties of trigonometric functions. However, Class E approach is possible for any value of duty cycle: a detailed analysis can be found in (Suetsugu & Kazimierczuk, 2007; Colantonio et al., 2009) where all electrical properties and component values are evaluated as a function of duty cycle. It can be demonstrated that under ideal assumption the maximum output power does not occur in correspondence of a 0.5 duty cycle, but for a slightly higher value (0.511). Anyway, in terms of output power capability, this increment is extremely low (about 1‰) and a standard 0.5 duty cycle could be assumed in the design, unless differently required.

3.2 A Class E design example

In order to illustrate the application of the relations obtained in the analysis, a simple Class E design example is described, based on an actual active device, specifically a GaAs pHEMT.

The device exhibits a breakdown voltage of about 25 V and a maximum output current of 400 mA. From S-parameter simulation, an output capacitance of 0.35pF results at 2.5 GHz, the selected operating frequency. Considering this capacitance as the minimum value for the shunt capacitance C_1, the network elements can be easily calculated through the previous relationships.
From (20) and taking into account the maximum voltage, the bias voltage is set to V_{DD}=6V. Hence, from the inversion of (18), the DC component of drain current is determined, resulting in I_{DC}=105 mA.
At this point, using (21) and (23) or, alternatively, equation (24), the values of output matching network are R=33Ω and L=1.67 nH. If considering a standard output impedance of 50Ω, a transforming stage is necessary.

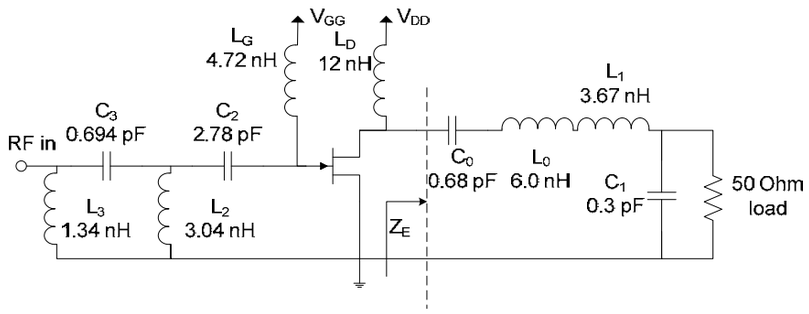


Fig. 3. Schematic of a 2.5GHz GaAs HEMT Class E amplifier.

Standing the value of optimum load, the impedance matching can be easily accomplished by a single *L-C* cell. A series inductance - parallel capacitance configuration has been chosen.
Lumped elements for the filtering output network have then determined, selecting an inductance L_0=6nH and a resulting capacitance C_0=0.68pF. The complete amplifier schematic is depicted in Fig. 3, while the simulated output power, gain and efficiency versus input power are shown in Fig. 4.

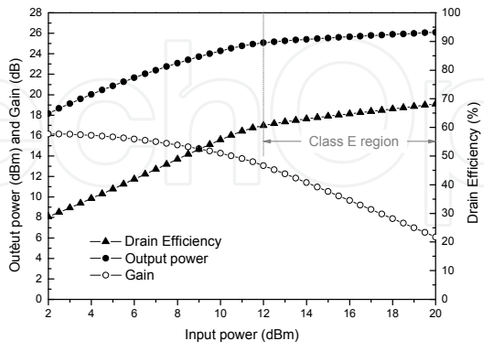
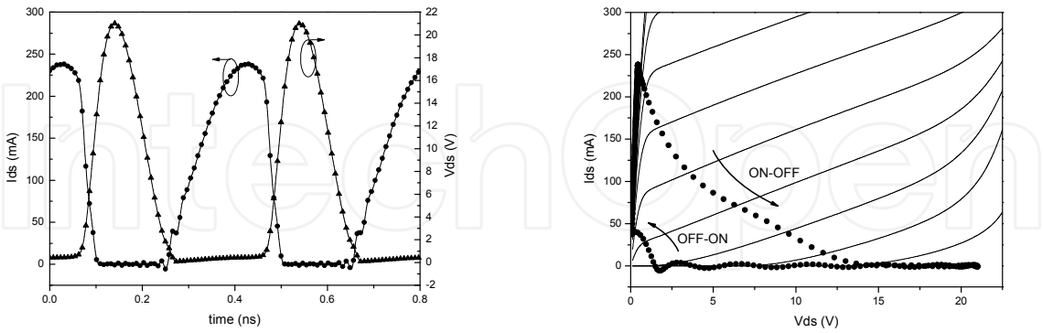


Fig. 4. Simulated performance of the 2.5GHz Class E amplifier.

It is worth to notice that, under a continuous wave excitation, Class E behavior is achieved only at a certain level of compression, i.e. when the large input sinusoidal waveform implies a "square-shaping" effect on the output current, due to active device physical limits, thus

approaching a switching behavior. The output current and voltage waveforms and load line are reported in Fig. 5, showing a good agreement with the theoretical expected behavior (compare with ideal waveforms depicted in Fig. 2b).



(a) (b)

Fig. 5. Output current and voltage waveforms (a) and load line (b) of the 2.5GHz Class E amplifier.

3.3 Drawbacks

As already outlined, Class E power amplifiers have some practical limitations, mainly due to their maximum operating frequency. Such limitations are partially related to the cut-off frequency of the active device, while are mainly due to the circuit topology and switching operation. In fact, as reported in (Mader et al., 1998), a Class E maximum frequency can be approximated by:

$$f_{Max} = \frac{I_{DS}}{2\pi^2 \cdot C_1 \cdot V_{DD}} \simeq \frac{I_{Max}}{56.5 \cdot C_1 \cdot V_{DD}} \tag{27}$$

Practically the lower limit of C_1 is given by the active device output capacitance C_{ds}. Consequently, the value of maximum operating frequency strongly depends on the device adopted for the design, on its size and then on the maximum current it can handle. For RF and microwave devices, the maximum frequency in Class E operation is generally included between hundred of megahertz (for MOS devices) and few gigahertz (for small MESFET or pHEMT transistors).

Additionally, at microwave frequencies higher order voltage harmonic components can be considered as practically shorted by the shunt capacitance, and the Class E behavior has to be clearly approximated. In particular, the voltage wave shaping can be performed recurring to the first harmonic components only (Raab, 2001; Mader et al., 1998), while the ZVS and ZVDS conditions cannot be longer satisfied.

Truncating the ideal voltage Fourier series at the third component, the resulting waveform is reported in Fig. 6, from which it can be noted the existence of negative values. Thus it becomes mandatory to prevent such negative values of drain voltage to respect active device physical constraint and safely operations.

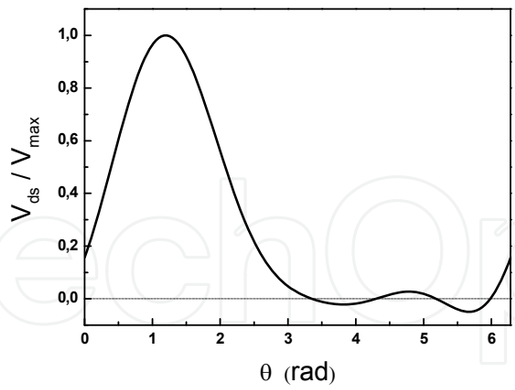
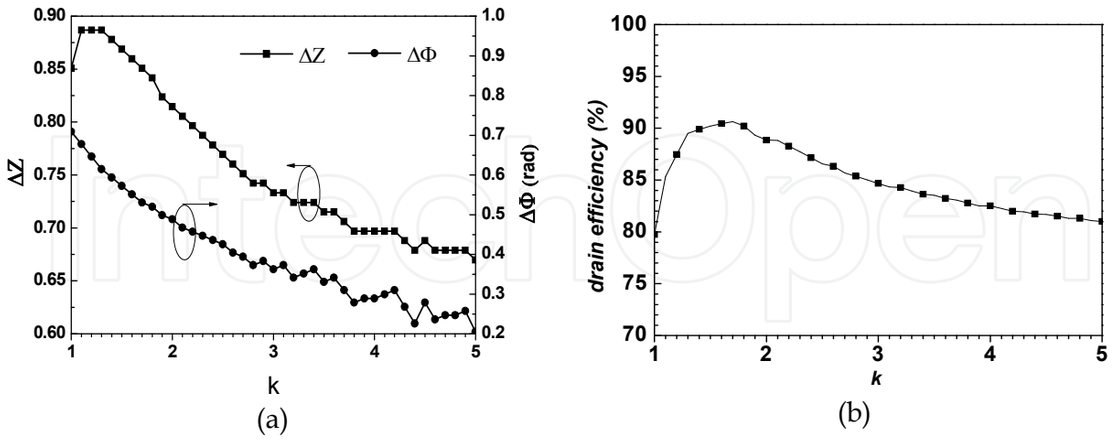


Fig. 6. Three harmonics reconstructed voltage waveform

As pointed out in (Colantonio et al., 2005), two solutions can be adopted. Obviously it is possible to increase drain bias voltage, but it would mean a non negligible increase in the DC dissipated power that in turn causes a decrease in drain efficiency levels. In addition, an increasing on peak voltage value could exceed breakdown limitations of the transistor. The other solution is based on the assumption of unaffected current harmonic components, thus optimizing the voltage fundamental component, while keeping fixed the other harmonics imposed by the network topology (i.e. the filter L_0-C_0 behavior and the device capacitance C_{ds}) (Cipriani et al., 2008). The optimization process must be implemented in a numerical form in order to reduce complexity and computing effort. The main goal is to avoid negative voltage values on drain voltage and, at the same time, maximize output power, hence efficiency. Then, for every value of frequency exceeding the maximum one, the optimum high frequency fundamental impedance, $Z_{1,HF}$, is optimized in magnitude and phase.



(a) (b)

Fig. 7. Class E optimum load impedance (a) and ideal efficiency (b) as a function of k

Obtained results are expressed as normalized to ideal load impedance at maximum frequency given by (27) and depicted in Fig. 7a as a function of normalized frequency $k=f/f_{Max}$, defined as the ratio between the assumed operating frequency f and the maximum

allowed one f_{Max}, defined in (27). The plot shown in Fig. 7a can be considered as a "design chart" for high frequency Class E development, once the maximum frequency is known.
A quasi monotonic decrease of magnitude of fundamental impedance is observed, leading to a reduced voltage fundamental component and a reduced output power. At the same time, the phase decreases tending to almost purely resistive values. The related drain efficiency is reported in Fig. 7b, showing an increasing reduction with respect the ideal 100% value due to non ideal operating conditions.
A high frequency Class E PA example is shown in Fig. 8.

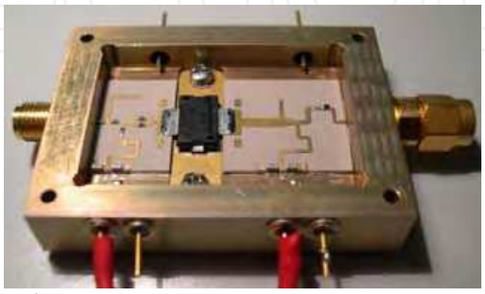


Fig. 8. A 2.14 GHz LDMOS Class E PA

The amplifier is designed using a medium power LDMOS transistor for base station application at 2.14 GHz. Once the bias point, maximum current and output capacitance of the transistor are fixed, the maximum frequency in Class E mode is directly derived. Considering a maximum current of 2.5 A, a bias voltage of 20 V and an output capacitance of 4.2 pF (estimated by S- parameters simulation), the maximum frequency in Class E results in 520 MHz, far below the frequency chosen for the design. If operating at 520 MHz, the load impedance would be $Z_1=25.1e^{j36°}$. At 2.14 GHz (4.1 times above f_{Max}), the load impedance is directly obtained by the design chart of Fig. 7a resulting in $Z_{1,HF}=17.5e^{j17°}$. Since a very simple equivalent model of the device is used, as Fig. 2 shows, this impedance is seen at the nonlinear current source terminals, so that eventual parasitic and package effects should be considered as belonging to the output load.

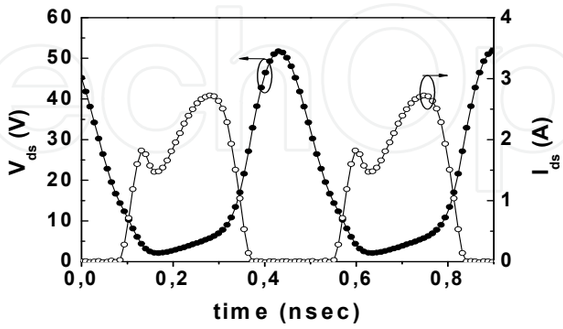


Fig. 9. Simulated voltage and current drain waveform of the designed PA

Simulated drain current and voltage waveform are depicted in Fig. 9, with reference to the internal nodes of the model. A good agreement with typical Class E waveform is

remarkable, above the maximum frequency, although the perfect switching behavior cannot be satisfied.

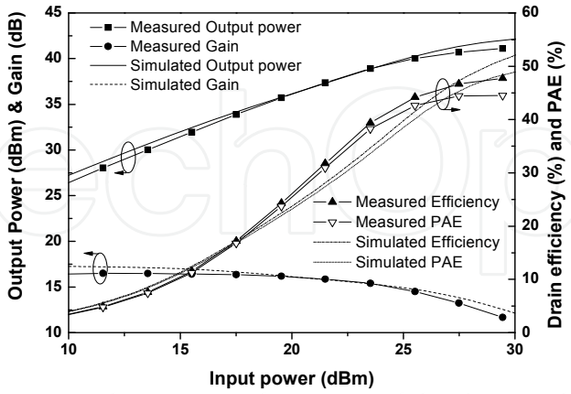


Fig. 10. Simulated and measured output performance of the designed PA

3.4 Class E matching network implementation and other topologies

Although Class E approach has basically a fixed circuit topology, different solution can be adopted for the synthesis of output matching network. Depending on the design frequency, distributed approaches are possible: proper load conditions at fundamental have to be satisfied, according to (24), and an open circuit condition must be provided at harmonics of the fundamental frequency, usually second and third harmonics (Negra et al., 2007; Wilkinson & Everard, 2001; Xu et al., 2006).

In Fig. 11a, no lumped elements are used unless block capacitors, while the 50Ω matching is synthesized through a very compact and simple structure reported in Fig. 11b (Mader et al., 1998). In order to provide harmonic suppression on the load, different quarter-wave open stubs can be used at different harmonics (Negra et al., 2007), while series transmission lines and wave impedances are properly chosen to provide the correct fundamental load.

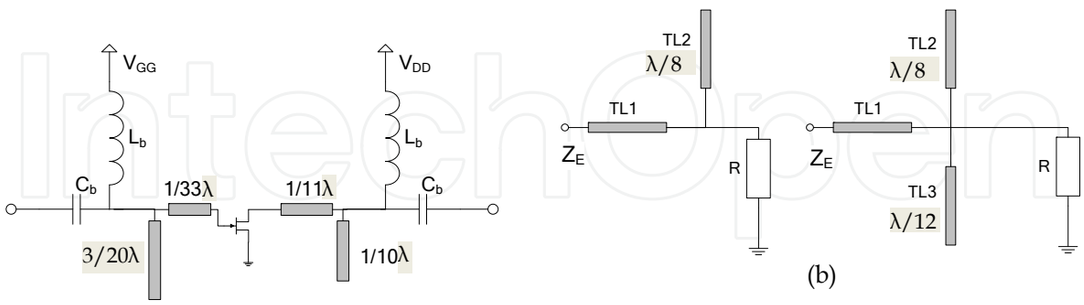


Fig. 11. Some practical examples of Class E transmission lines amplifiers.

Additionally, different circuit topologies exist that can provide the same results as the classical formulation: they have been widely investigated in (Grebennikov, 2003) and are commonly referred as parallel circuit Class E and their main characteristic is the presence of

a finite parallel inductor in the output network, required for the output device biasing supply, as reported in Fig. 12. As before assumed, the shunt capacitance *C* includes the transistor output capacitance C_{ds}.
The first circuit, in Fig. 12a, employs a very simple output matching network, which consist of a parallel inductor and a series blocking capacitance. Applying ZVS and ZVDS conditions on this circuit, and considering the transistor to behave as a perfect switch, the solution of the circuit is given by a second order non homogeneous differential equation, given by (28), which has to be solved in order to determine the value of all circuit parameters.

$$\omega^2 LC\frac{d^2 v_s(\omega t)}{d(\omega t)^2}+\frac{\omega L}{R}\frac{dv_s(\omega t)}{d(\omega t)}+v_s(\omega t)=V_{DD} \tag{28}$$

The values of reactive components, *L* and *C*, are:

$$C=\frac{1.025}{\omega R} \qquad L=0.41\frac{R}{\omega} \tag{29}$$

and the load resistance R is determined using the desired output power at fundamental frequency, P_1:

$$R=1.394\frac{{V_{DD}}^2}{P_1} \tag{30}$$

Due to the lack of any filtering action at the output, this circuit becomes not practical in applications - like telecommunications - which require harmonic suppression (Grebennikov, 2003). Moreover, a higher peak current value is obtained ($4.0I_{DC}$ instead of $2.862\ I_{DC}$ for the classical topology) that has to be taken into account in the choice of the active device.
The circuit in Fig. 12b adds a series LC filter in the output branch and it is very similar to a canonic Class E amplifier using a finite DC feed inductance, unless for the absence of the "tuning" series inductance. Providing a high Q factor for the LC series filter, the current i_R flowing into the output branch can be assumed as sinusoidal: this hypothesis is used as starting point for a complete time domain analysis which is similar to what reported in paragraph 4.1. Optimum parallel capacitance *C* and optimum load resistance *R* are obtained after inferring the phase angle between in-phase and quadrature components of fundamental current:

$$\psi=\arctan\left(\frac{R}{\omega L}-\omega RC\right)=34.244° \tag{31}$$

From which:

$$C=\frac{0.685}{\omega R} \qquad L=0.732\frac{R}{\omega} \tag{32}$$

Output resistance *R* is derived from desired fundamental output power, P_1:

$$R = 1.365 \frac{V_{DD}{}^2}{P_1} \tag{33}$$

Slightly different voltage and current peak values (Grebennikov, 2003) are obtained with respect to the traditional Class E approach:

$$V_{Max} = 3.647 \cdot V_{DD} \qquad I_{Max} = 2.647 \cdot I_{DC} \tag{34}$$

In Fig. 12c the parallel inductance is replaced by a short-circuited short length transmission line: this solution is quite popular at microwave frequencies. In order to approximate the Class E optimum impedance at fundamental frequency, the electrical length and the characteristic impedance of the transmission line are determined starting from the optimum fundamental impedance and according to the relation (Grebennikov, 2003):

$$Z_0 \cdot \tan(\theta) = \omega L. \tag{35}$$

The load impedance Z_E seen at device terminals should satisfy the optimum impedance at fundamental frequency, and remembering relation (31) it is rewritten as:

$$Z_E = \frac{R}{1 - j \tan\psi} \tag{36}$$

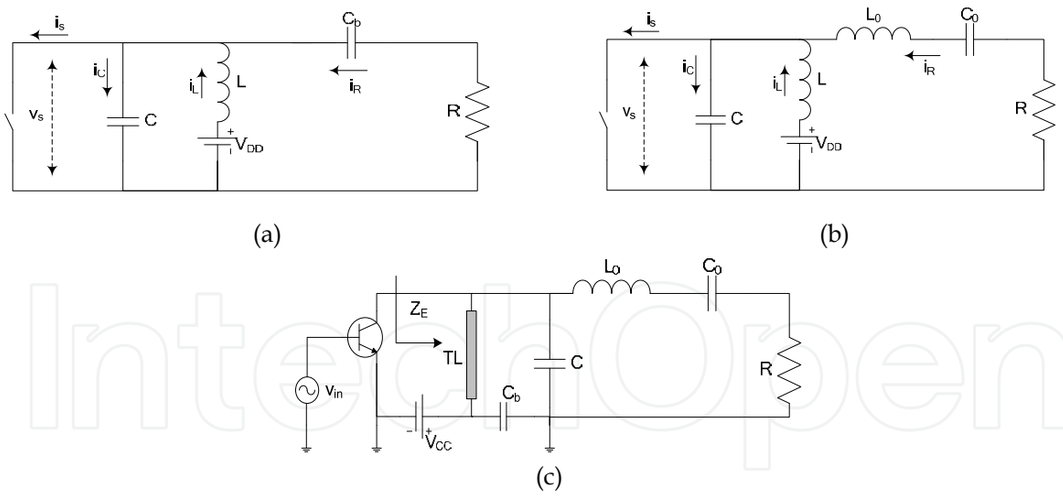


Fig. 12. Parallel circuit Class E topology (a), parallel circuit Class E with output filter (b) and transmission line parallel Class E (c).

Finally, using equation (32) to determine the optimum required parallel inductance, the electrical length of the parallel transmission line can be obtained:

$$\tan\theta = 0.732 \frac{R}{Z_0} \tag{37}.$$

4. The inverse Class E amplifier

The Inverse Class E amplifier, or voltage drive Class E amplifier, is commonly considered as the dual version of the Class E amplifier, in which current and voltage waveforms are interchanged, as shown in Fig. 13. It is also referred as "series-L/parallel tuned Class E", being the traditional topology defined as "parallel-C/series-tuned Class E" (Mury & Fusco, 2005; Mury & Fusco, 2007).

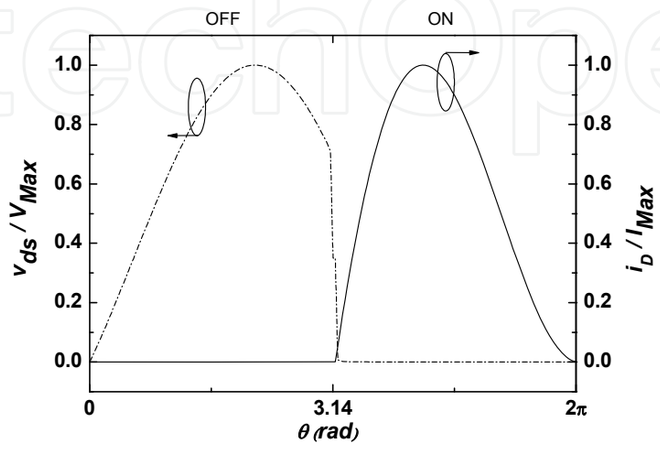


Fig. 13. Ideal inverse Class E waveforms.

A former version of the Inverse Class E amplifier was reported in (Kazimierczuk, 1981): the circuit does not have shunt capacitor, while a series tuned filter and a finite DC feed inductance is considered in the output network, as depicted in Fig. 14. Although this circuit seems to be similar to those reported in Fig. 12, it implies a different behavior, due to the different characteristic of the shunting element (an inductor instead of a capacitor). When the switch is open, and provided a high enough Q factor of the series filter, the only current flowing in the circuit is the sinusoidal output current i_R, that is the inductor current i_L. The latter causes a voltage drop across the inductor, v_L, which has a cosinusoidal form. When the switch is closed, the voltage across the inductor is instantaneously constant and equal to V_{DD}. This causes a linear increase in the current i_L. The current across the switch is calculated as the difference between i_L and i_R and assumes the typical asymmetrical shape.

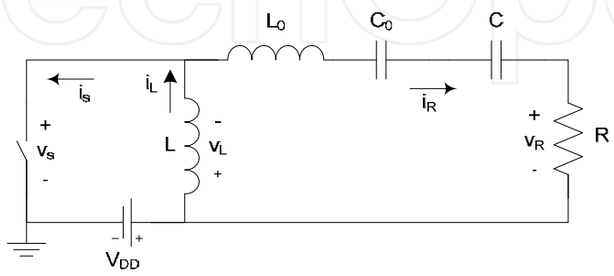


Fig. 14. Inverse Class E amplifier: no-shunt-capacitor/series-tuned topology with finite inductance.

A complete analysis of the inverse Class E amplifier is reported for the first time in (Mury & Fusco, 2005; Mury & Fusco, 2007), together with a defined topology which is shown in Fig. 15 and which is substantially different from the previous version given in (Kazimierczuk, 1981). As can be seen by a comparison of Fig. 15 and the circuit depicted in Fig. 2, each component of the traditional Class E amplifier has been replaced by its dual element in a dual configuration. A DC blocking capacitance C_b is inserted in order to prevent inductance L_0 from shorting the bias voltage.

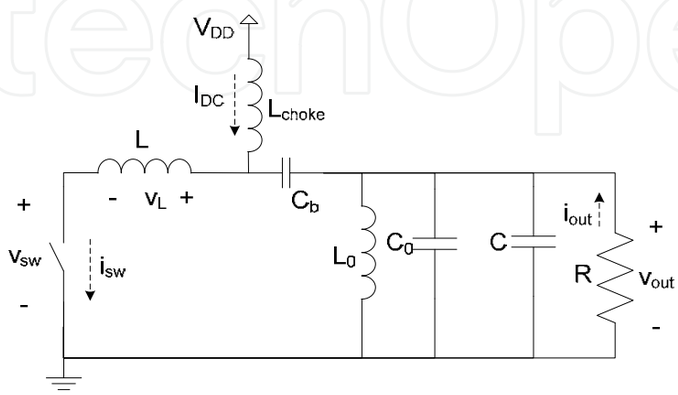


Fig. 15. Inverse Class E amplifier.

Hence, the analysis of the inverse Class E amplifier can be carried out starting from the assumption of a purely sinusoidal output voltage across the output resistance R, which produces a voltage across the inductor L given by:

$$v_L(\theta) = V_{DD} - v_o(\theta) = V_{DD} \cdot \left(1 - a \cdot \sin\left(\theta + \phi\right)\right) \tag{38}$$

This is the voltage present across the switch during the OFF time, while during the ON time the switch has no voltage across it and its current is given by integration of (38):

$$i_{SW} = \frac{1}{\omega L} \cdot \int_0^{\theta} v_L(\theta) d\theta \tag{39}$$

These expressions have the same form of those reported in paragraph 4.1, unless current and voltage are interchanged: the same kind of analysis as Class E can be performed on the Inverse Class E circuit. As a consequence, the same numerical results are obtained for the dual configuration, and are summarized in Table 1, referred to a 50% duty cycle operation. As can be seen, the maximum allowable voltage for the Inverse Class E operation is much smaller than for Class E: this is an unquestionable advantage of such a circuit, because the requirement on device breakdown can be drastically relaxed.
However, it is worth to notice that in Inverse Class E amplifier the output capacitance of the active device is not taken into account and set to zero in the ideal analysis: in real world circuit, this is clearly not true. Hence, some actions have to be taken in order to compensate its presence (e.g. a shunt inductance).

Circuit component or electrical value	Class E	Inverse Class E
V_{Max}	$3.562 \cdot V_{DD}$	$2.862 \cdot V_{DD}$
I_{Max}	$2.862 \cdot I_{DC}$	$3.562 \cdot I_{DC}$
C	$\frac{I_{DC}}{\pi \cdot \omega \cdot V_{DD}}$	$\frac{0.2116}{\omega^2 \cdot L}$
R	$\frac{0.1836}{\omega \cdot C}$	$\frac{1}{0.1836 \cdot \omega \cdot L}$
L	$\frac{0.2116}{\omega^2 \cdot C}$	$\frac{V_{DD}}{\pi \cdot \omega \cdot I_{DC}}$
C_0	$\frac{1}{\omega \cdot Q \cdot R}$	$\frac{Q}{\omega \cdot R}$
L_0	$\frac{1}{\omega^2 \cdot C_0}$	$\frac{1}{\omega^2 \cdot C_0}$

Table 1 - Class E and Inverse Class E comparison.

5. Class F and Class F-1 amplifier

Among the different switched mode amplifier design strategies, several authors include the Class F and inverse F (or Class F-1) schemes also.

5.1 Class F theoretical analysis

Such design strategy was introduced by Tyler at the end of fifties (Tyler, 1958) and further investigated several years later (Snider, 1967; Raab, 1996), as a simple and feasible way to improve power amplifier large-signal performances.

Following the widely accepted definition, Class-F design consists in terminating the device output with open-circuit terminations at odd harmonic frequencies of the fundamental component and short-circuiting it at even harmonics. Regarding the input network, it is typically synthesized in order to guarantee maximum power transfer at the operating frequency, neglecting or at least circumventing the device input non linear generation by using short-circuit terminations.

The theoretical output voltage and current waveforms of an ideal Class F PA are depicted in Fig. 16.

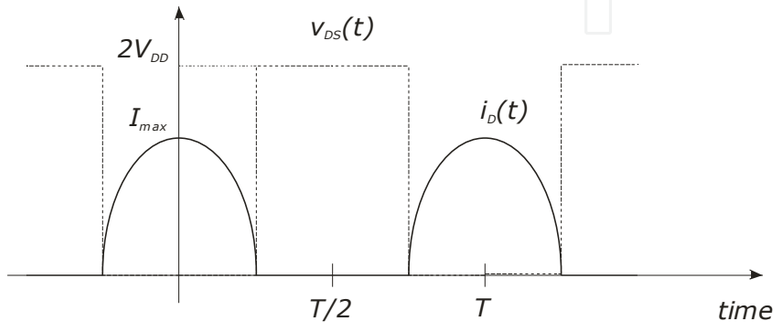


Fig. 16. Ideal output voltage (v_{DS}) and current (i_D) waveforms of a Class F PA.

The current is assumed as a truncated sinusoid waves (assuming a Class B bias condition), while the voltage is squared by the proper harmonic loading conditions. The two ideal waveforms do not overlap: no output current flows for high drain/collector voltages and maximum current occurs when drain/collector voltage waveform is at its minimum. Therefore the power dissipated in the active device is nulled ($P_{diss}=0$).
Such an ideal waveforms can be easily described by their Fourier components:

$$i_D(\theta)=\sum_{n=0}^{\infty} I_n\cdot\cos(n\theta) \qquad I_n=\begin{cases}\dfrac{I_{Max}}{\pi} & n=0\\ \dfrac{I_{Max}}{2} & n=1\\ \dfrac{2\cdot I_{Max}}{\pi}\dfrac{(-1)^{\frac{n}{2}+1}}{n^2-1} & n \text{ even}\\ 0 & n \text{ odd}\end{cases} \tag{40}$$

$$v_{DS}(\theta)=\sum_{n=0}^{\infty} V_n\cdot\cos(n\theta) \qquad V_n=\begin{cases}V_{DD} & n=0\\ -\dfrac{4\cdot V_{DD}}{\pi} & n=1\\ 0 & n \text{ even}\\ \dfrac{4\cdot V_{DD}}{\pi}\dfrac{(-1)^{\frac{n+1}{2}}}{n} & n \text{ odd}\end{cases} \tag{41}$$

where I_{Max} and V_{DD} the maximum output current and bias voltage, respectively.
From the previous equations it can be noted that the current and voltage Fourier components with the same order n are alternatively zeroed, thus nulling the power delivered at harmonic frequencies also ($P_{out,nf}=0$, $n>1$).
The values of the ideal terminations are inferred as the ratio between the respective Fourier components V_n and I_n, i.e.:

$$Z_n=\frac{V_n}{I_n}=\begin{cases}\dfrac{8}{\pi}\cdot\dfrac{V_{DD}}{I_{Max}} & n=1\\ 0 & n \text{ even}\\ \infty & n \text{ odd}\end{cases} \tag{42}$$

Therefore resulting in a purely resistive terminating impedance at fundamental frequency given by $4/\pi\cdot R_{TL}$, being R_{TL} the optimum impedance of a Tuned Load scheme (i.e. short circuiting all the harmonic terminations). Conversely, short circuit condition for even harmonics and open circuit for odd ones have to be synthesized, as schematically depicted in Fig. 17.

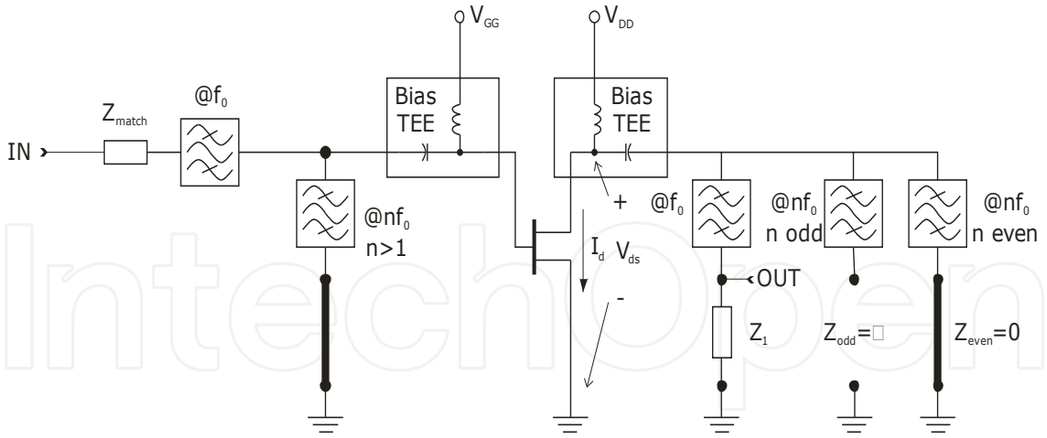


Fig. 17. Ideal structure of a Class F amplifier.

The results obtained following the Class F strategy were so interesting that, before the advent of fast switching devices, such approach was widely adopted to design PAs for amplitude modulated (AM) broadcast radio transmitters (operating at LF 30-300 KHz, MF 0.3-3 MHz and HF 3-30 MHz) or for frequency modulated (FM) broadcast radio transmitters (at VHF 30-300 MHz and UHF 0.3-3 GHz) (Wood, 1992; Lu, 1992).
Nowadays, the Class F technique is generally adopted for high frequency applications in the microwave range (i.e. up to tens of Gigahertz). Examples of Class F based on GaAs devices are available at X (9.6GHz) (Colantonio et al., 2007), Ku (14.5GHz) (Ozalas, 2005) and Ka (29.5GHz) (Reece et al., 2003) bands. For high frequency applications the active devices operate in current-mode rather than in switched-mode, and the harmonic loading conditions are implemented through lumped resonating circuits.

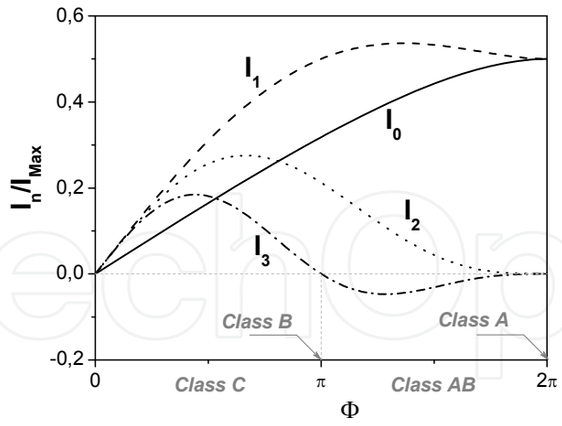


Fig. 18. Fourier components I_0, I_1, I_2, I_3 normalised to the device maximum current I_{Max}, as functions of the drain CCA Φ.

Several research efforts were focused to clarify and to implement the harmonic terminating scheme leading to the Class F optimum behavior and its experimental validation, inferring practical design guidelines also (Duvanaud et al., 1993; Blache, 1995; Colantonio et al., 1999).

The analytical results can be easily extended to bias conditions different from Class B, still assuming for the current waveform a truncated sinusoidal wave shaping, with a conduction angle (CCA) Φ larger than π (Class AB), while maintaining a square voltage waveform. In this case the corresponding current harmonic components as function of the CCA depicted in Fig. 18 result, while the estimated Class F performances are depicted in Fig. 19, compared with the corresponding theoretical one for a Tuned Load condition.

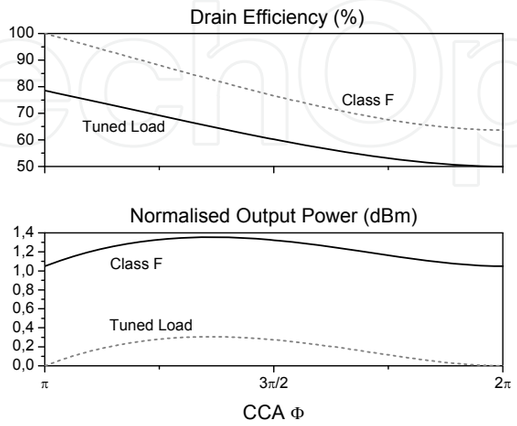


Fig. 19. Ideal performance for a Class F and reference TL amplifiers as functions of the CCA Φ. Output power normalized to the Class A output at full swing.

5.2 Class F practical limitations

Referring to the ideal solution proposed to implement the Class F loading scheme, depicted in Fig. 17, it is based on the use of resonating elements ensuring low impedance values (theoretically short-circuit conditions) for even harmonic frequencies or high values for the odd harmonics (theoretically open-circuit conditions).

Clearly, for a simple and manageable mathematical formulation, the active device model has to be strongly simplified, neglecting all parasitic and reactive elements. It implies that when dealing with an actual device, the loading condition expressed by (42) has to be fulfilled across the device intrinsic output current source, as already proposed in other similar simplified approaches (Cripps, 1983). From a practical point of view, the required ideal terminations pose significant restrictions when implementing the Class technique. In fact, while it is relatively simple to realize a short-circuit termination, compensating for the device reactive elements, the realization of an open-circuit condition becomes much more cumbersome. For example, in high frequency applications the dominant capacitive behavior shown by the active device (e.g. C_{ds}) tends to short-circuit the device output itself, thus practically not allowing the open-circuit loading condition for the higher-order odd harmonics.

At the same time, even if the internal C_{ds} capacitance can be effectively resonated by an external inductive element, the device output resistance (R_{ds}) cannot be removed, thus representing an upper limit for the impedance effectively synthesizable across the intrinsic current source. Therefore the realization of a true open termination is basically unfeasible. However, it has been demonstrated that lower-order harmonics are more effective in improving amplifier performance as compared to higher order ones (Raab, 2001). Therefore, accounting for the reduced number of harmonics can be effectively controlled, new

terminating impedance values have been inferred not only at fundamental but also at harmonics, resulting in a different voltage harmonic ratio also (Raab, 1997; Colantonio et al., 2009). In fact, the new optimum voltage ratio becomes $|V_3/V_1|=1/6$ rather than *1/3* as in the ideal case. Simultaneously, the fundamental loading impedance becomes

$$R_F = \frac{4}{\sqrt{3}} \cdot \frac{V_{DD}}{I_{Max}} \tag{43}$$

resulting in an efficiency improvement of 15% only with respect to the Tuned Load theoretical case (Colantonio et al., 2009).

A further critical point is represented by the physical mechanisms generating the harmonic components of both voltage and current waveforms. If the device output only is considered, it can be described by an independent and forcing current source, whose waveform results both from the input drive level and the device physical limitations (clipping effects), being independent on the device terminating impedances. Under this assumption, the output voltage waveform is dependent on the current one, being generated by loading each harmonic current component through the respective terminations ($V_n=Zn \cdot In$). Consequently a proper phase relationships between the output current harmonic components must be fulfilled, and in particular I_1 and I_3 must be opposite in sign. Such a condition, referring to Fig. 18 practically implies the selection of a suitable bias level close to the Class B condition, i.e. assuming a non-zero quiescent current level (deep AB bias), while leaving for instance the same harmonic terminations as derived in the ideal case. The theoretical load curve behaves as depicted in Fig. 20.

Conversely, the adoption of a Class C bias condition implies a wrong relationships among the current harmonics phase (see Fig. 18).

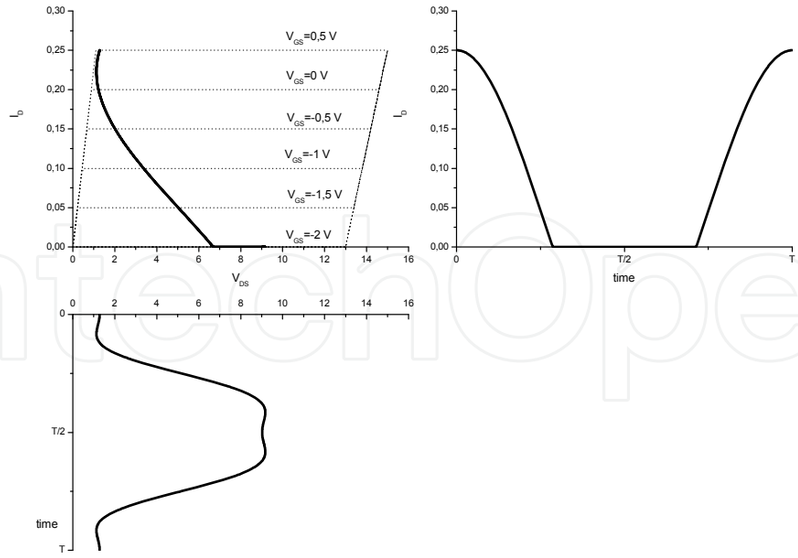


Fig. 20. Theoretical load line for a Class F amplifier.

5.3 Class F matching networks implementation

To design the Class F output section, resonating circuits are typically used as traps for the harmonic frequencies. Such resonators, sometimes referred as idlers, are limited to low-order harmonics, to reduce both circuit complexity and associated losses. Moreover, depending on the frequency range, their implementation can be performed either in lumped or distributed form, while accounting for also the DC bias.

For example, in Fig. 21 is depicted a possible implementation based on the use of a quarter-wavelength transmission line ($\lambda/4$-TL) and a parallel resonating L_0-C_0 tank to control the harmonic impedances. The optimum matching at fundamental frequency f_0 is achieved by the remaining passive components L_m and C_m (Gao, 2006).

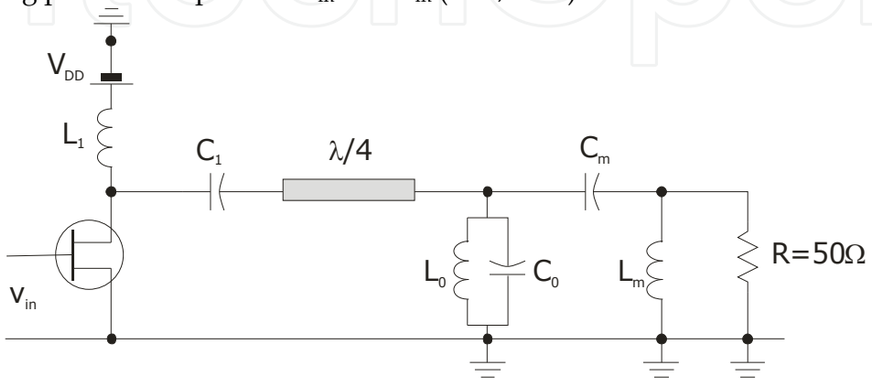


Fig. 21. Example of Class F output network design.

In practical situations, to account the biasing elements and the active device output capacitance C_{ds}, other proposed solutions are schematically depicted in Fig. 22, where the design relationships to calculate the element values can be derived evaluating the impedance loading the device output current source and then imposing the short circuit condition at $2f_0$ and the open circuit one at $3f_0$. (Trask, 1999).

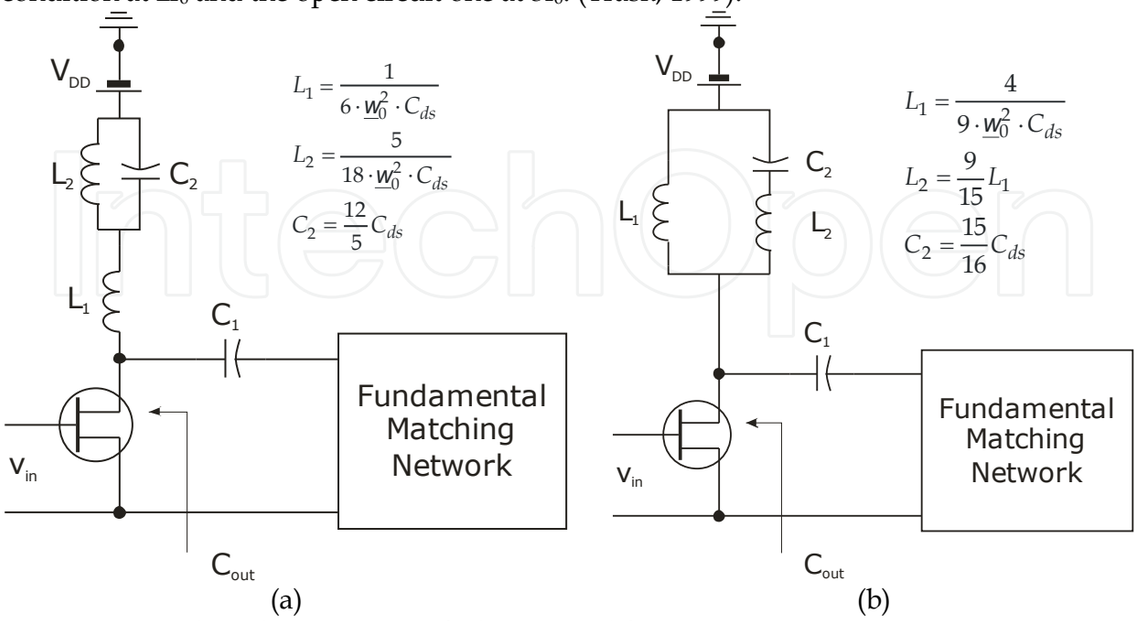
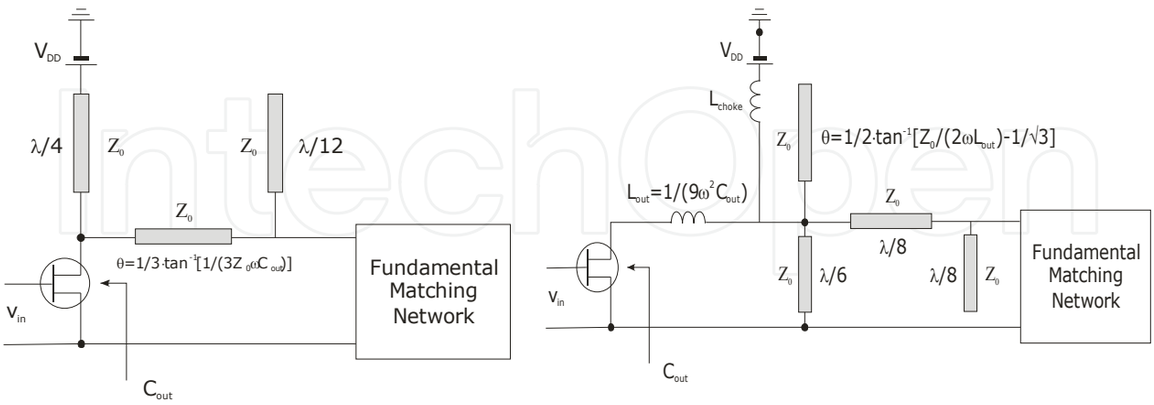


Fig. 22. Practical implementations of Class F amplifier.

In a similar way, a distributed solution can be designed and implemented by using transmission lines, as for instance reported in Fig. 23 (Grebennikov, 2000; Woo et al., 2006; Negra et al., 2007).



(a) (b)

Fig. 23. Distributed solutions implementing the Class F schemes.

Clearly the characteristic impedances of the TLs have to be properly selected when designing the matching network at fundamental frequency.

5.4 Class F example

An example of hybrid (MIC) Class F PA operating at 5GHz and based on GaAs device (1mm gate periphery) is reported in Fig. 24, where both the input and output matching networks were designed on Alumina substrate by using a dixtributed approach.

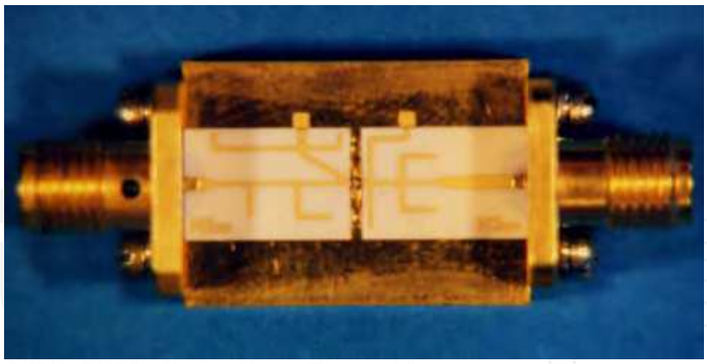


Fig. 24. Photo of a MIC 5GHz GaAs Class F amplifier.

The corresponding load curve and the performance as compared to a Tuned Load amplifier based on the same active device and bias point (Class B), are reported in Fig. 25 and Fig. 26, respectively.

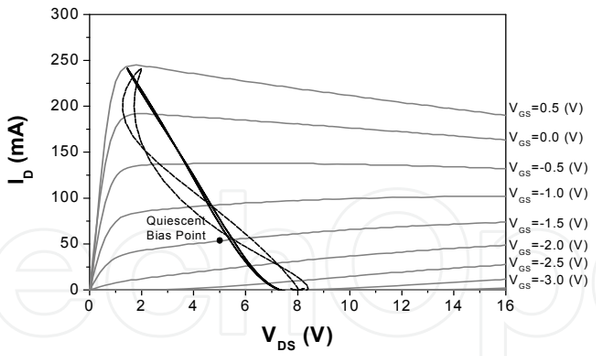
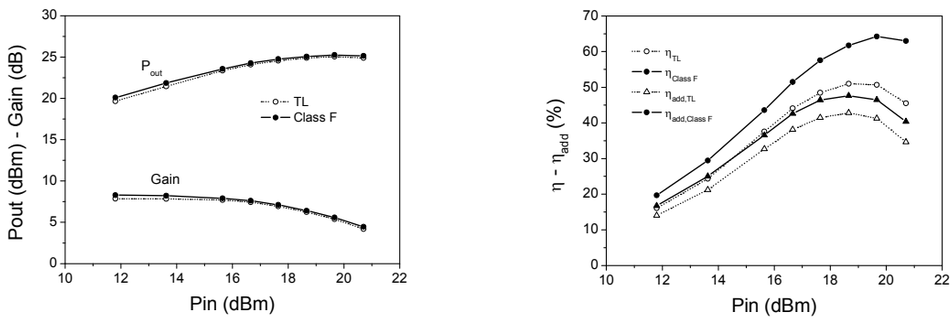


Fig. 25. Load curve of 5GHz MIC Class F amplifier (dashed curve) compared with Tuned Load case (continuous curve).



(a) (b)

Fig. 26. Output Power & Gain (a) and efficiency & power added efficiency (b) for the 5GHz MIC Class F amplifier as compared to Tuned Load amplifier.

Among the other features, it is to note that the Class F amplifier output power is higher as compared to the Tuned Load approach in the entire range of input drive. A 7-8% measured improvement (against a maximum theoretical 15% expected) is usually obtained.
It is to note that at low input power levels, a higher power gain with respect to a Tuned Load is obviously expected due to the larger output load that has been assured at fundamental frequency, as given by (43). Increasing the input drive level, the use of a Class F strategy force the output voltage (and current) to approach their maximum swings value, resulting in a proper bending of the load curve (see Fig. 25), thus improving the output power at saturation level also.

5.5 The inverse Class F amplifier

The term "inverse" in this kind of amplifier suggests somewhat inverted in the behavior: in fact, current and voltage drain waveforms are interchanged if compared to a traditional Class F amplifier (Ingruber et al., 1998; Lepine et al., 2007; Woo et al., 2006).
Inverse Class F power amplifier was introduced as a "rectangular driven Class A harmonic-controlled amplifier", in order to combine the advantage of high efficiency of a switched mode amplifier with the high gain of Class A operation (Ingruber et al., 1998).

It employs a rectangular driving voltage, which forces the active device to operate in the ohmic region or in the interdiction region, thus justifying - more than for a Class F - the classification as a switched mode amplifier. Assuming a piecewise linear simplified model for the active device, the drain current waveform can be directly inferred, resulting in a rectangular waveform. Thus, open terminations for even harmonics and short circuit terminations for odd harmonics - except for the fundamental one - give a truncated sinusoid voltage waveform. Current and voltage waveform do not overlap, thus preventing DC power consumption on the active device; additionally, thanks to the proper harmonic terminations, no power is delivered at harmonics of fundamental frequency and 100% drain efficiency is ideally achievable.

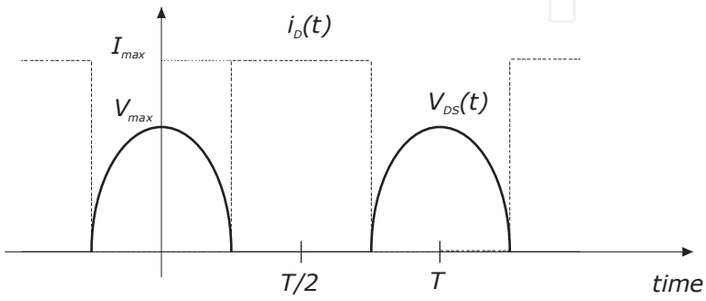


Fig. 27. Ideal output voltage (v_{DS}) and current (i_D) waveforms of an inverse Class F PA.

Referring to the ideal output current and voltage waveforms of Fig. 27, DC and fundamental frequency components can be obtained using a Fourier analysis:

$$I_0 = \frac{I_{Max}}{2} \tag{44}$$

$$I_1 = \frac{1}{\pi}\int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} I_{Max}\cdot\cos(\vartheta)\,d\vartheta = \frac{2\cdot I_{Max}}{\pi} \tag{45}$$

$$V_0 = V_{DD} = \frac{1}{2\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} V_{Max}\cos(\vartheta)\,d\vartheta = \frac{V_{Max}}{\pi} \tag{46}$$

$$V_1 = \frac{1}{\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} V_{Max}\sin(\vartheta)^2\,d\vartheta = \frac{V_{Max}}{2} \tag{47}$$

Then, the expression of harmonic load impedance is given by:

$$Z_n = \frac{V_n}{I_n} = \begin{cases} \frac{\pi^2}{4}\cdot\frac{V_{DD}}{I_{Max}} & n = 1 \\ \infty & n \text{ even} \\ 0 & n \text{ odd} \end{cases} \tag{48}$$

An inverse Class F amplifier requires an infinite number of resonator in order to maintain the square-shaped output current. Fig. 28 shows an immediate ideal implementation of an

inverse Class F amplifier using multiple even-harmonic resonators to control the voltage and current waveforms (Grebennikov & Sokal, 2008).

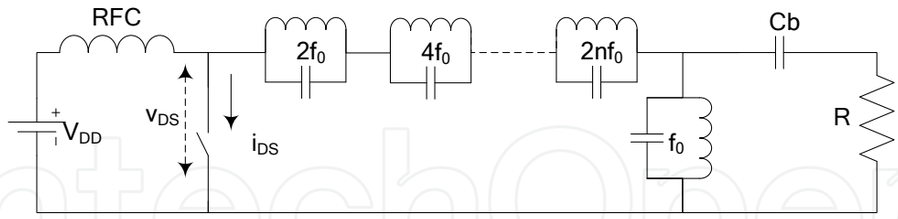


Fig. 28. Inverse Class F amplifier with multiharmonic resonator circuit.

In real world design, however, a limited number of harmonics has to be taken into account. Practical output networks implementations are often based on multiharmonic quarterwave-lenght stubs (Lepine et al., 2007; Woo et al., 2006). Input network design is the most critical aspect in inverse Class F design. In fact, if a continuous wave excitation is put on the gate, the required square wave driving voltage occurs only in deep saturation regime, thus affecting the gain. Ideal conditions would require a square wave driving voltage throughout the whole dynamic range of the amplifier. This can be obtained providing fundamental frequency and its second harmonic as a driving signal (Goto et al., 2001; Grebennikov & Sokal, 2008), so that an out of phase condition exist at their maximum amplitude. A network example which satisfied this condition is reported in Fig. 29.
Referring to switched mode finite harmonic operation, it is interesting to find a qualitative relation between the different classes of amplifier, as reported in (Raab, 2001). The transition from inverse Class F and Class F amplifiers is achieved by moving the second harmonic impedance (reactance) from zero to ∞, while decreasing the third harmonic impedance (reactance) from ∞ to zero, while in the intermediate condition, in which both second and third harmonic reactances have finite values, current and voltage waveforms assumes a resemblance to Class E amplifier.

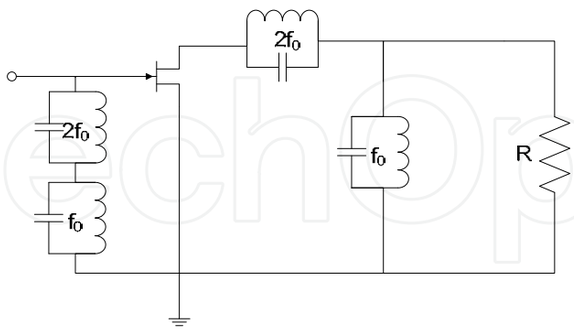


Fig. 29. Bi-harmonic inverse Class F amplifier.

6. References

Blache, F. (1995). A Novel Computerised Multiharmonic Active Load-Pull System for the Optimisation of High Efficiency Operating Classes in Power Transistors, *IEEE MTT-S Int. Microwave Symp. Dig.*, Orlando, FL, June 1995, pp.1037-1040.

Cipriani, E.; Colantonio, P.; Giannini, F. & Giofré, R. (2008). *Optimization of Class E Power Amplifier Design above Theoretical Maximum Frequency*, Proceedings of 38th European Microwave Conference, EuMC 2008, pp. 1541 - 1544, Amsterdam, October 2008.

Colantonio, P.; Giannini, F.; Leuzzi, G. & Limiti, E. (1999). On the Class-F Power Amplifier Design, *Intern. Journal of RF and Microwave Computer-Aided Engineering*, Vol. 9, No. 2, March 1999, pp.129-149.

Colantonio, P.; Giannini, F.; Leuzzi, G. & Limiti, E. (2003). Theoretical Facet and Experimental Results of Harmonic Tuned PAs, *Intern. Journal of RF and Microwave Computer-Aided Engineering*, Vol.13, No. 6, November 2003, pp. 459-472.

Colantonio, P.; Giannini, F.; Giofrè, R.; Medina, M. A. Y.; Schreurs, D. & Nauwelaers, B. (2005). High frequency class E design methodologies, *Proceedings of European Gallium Arsenide and Other Semiconductor Application Symposium*, GAAS 2005, pp. 329 - 332, Paris, October 2005.

Colantonio, P.; Giannini, F.; Giofrè R. & Limiti, E. (2007). Combined Class F Monolithic PA Design, *Microwave and Optical Technology Letters*, Vol. 49, No. 2, February 2007, pp. 360-362.

Colantonio, P.; Giannini, F. & E. Limiti (2009). *High Efficiency RF and Microwave Solid State Power Amplifiers*, John Wiley & Sons (ISBN: 978-0-470-51300-2).

Cripps, S.C. (1983). A theory for the prediction of GaAs FET Load-Pull power contours, *IEEE MTT-S Int. Microwave Symp. Dig.*, Boston, MA, May 1983, pp. 221-223.

Cripps, S.C. (1999). *RF Power Amplifiers for Wireless Communications*. Artech House, Norwood, MA (ISBN 0-89226-989-1).

Cripps, S. C. (2002). *Advanced Techniques in RF Power Amplifier Design*, Artech House, London.

Duvanaud, C.; Dietsche, S.; Pataut, G. & Obregon, J. (1993). High-Efficient Class F GaAs FET Amplifiers Operating with Very Low Bias Voltages for Use in Mobile Telephones at 1.75 GHz, *IEEE Microwave and Guided Wave Letters*, Vol.3, No. 8 , August 1993, pp.268-270.

Gao, S. (2006). High efficiency class-F RF/microwave power amplifiers, *IEEE Microwave Magazine*, Vol. 7, No. 1, February 2006, pp. 40 – 48.

Goto, S.; Kunii, T.; Ohta, A.; Inoue, A.; Hosokawa, Y.; Hattori, R. & Mitsui, Y. (2001). Effect of Bias Condition and Input Harmonic Termination on High Efficiency Inverse Class-F Amplifiers, *31st European Microwave Conference*, 2001. Oct. 2001, pp. 1 - 4.

Grebennikov, A.V. (2000). Circuit design technique for high efficiency Class F amplifiers, *IEEE MTT-S Int. Microwave Symp. Dig.*, Boston, MA, June 2000, Vol. 2, pp. 771–774.

Grebennikov, A. (2003). Switched-mode RF and microwave parallel-circuit Class E power amplifiers, *Intern. Journal of RF and Microwave Computer-Aided Engineering*, Vol. 14, No. 1, December 2003, pp. 21-35.

Grebennikov, A. & Sokal, N.O. (2007). *Switchmode RF power amplifiers*, Newnes, Elsevier, Burlington, MA, USA.

Ingruber, B.; Baumgartner, J.; Smely, D.; Wachutka, M.; Magerl, G. & Petz, F.A. (1998). Rectangularly driven class-A harmonic-control amplifier, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 46, No. 11, Part 1, November 1998, pp. 1667 - 1672.

Jozwik, J. J. & Kazimierczuk, M. K. (1990). Analysis and design of class-E² dc/dc converter, *IEEE Trans. Ind. Electron.*, Vol. 37, No. 2, April 1990, pp. 173-183.

Kazimierczuk M.K. (1981). Class E tuned power amplifier with shunt inductor, *IEEE Journal of Solid-State Circuits*, Vol. 16, No. 1, February 1981, pp. 2 – 7.

Kazimierczuk, M.K. (2008). *RF Power Amplifiers*, Wiley, New York.

Kazimierczuk M. K. & Jozwik, J. (1990). Analysis and design of class E zero-current-switching rectifier, *IEEE Trans. Circuits Syst.*, Vol. 37, No. 8, August 1990, pp. 1000-1009.

Krauss, H. L.; Bostian, C.W. & Raab, F. H. (1980). *Solid State Radio Engineering*, Wiley, New York.

Lai, J. B. (2008). Investigation into the use of high-efficiency, switched mode Class E power amplifier for high-dynamic range, pulse-mode application, *PhD dissertation*, University of New Mexico Albuquerque, New Mexico, December, 2008.

Lepine, F.; Adahl, A. & Zirath, H. (2007). L-band LDMOS power amplifiers based on an inverse class-F architecture, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 53, No. 6, Part 2, June 2005, pp. 2007 - 2012.

Lu, X. (1992). An alternative approach to improving the efficiency of high power radio frequency amplifiers, *IEEE Transaction on Broadcasting*, Vol. 38, No. 2, June 1992, pp. 85–89.

Mader, T.B.; Bryerton, E.W.; Markovic, M.; Forman, M. & Popović, Z. (1998). Switched-mode high-efficiency microwave power amplifiers in a free-space power-combiner array, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 46, No. 10, Part 1, October 1998, pp. 1391 – 1398.

Mury, T. & Fusco, V.F. (2005). Series-L/parallel-tuned comparison with shunt-C/series-tuned class-E power amplifier, *IEE Proceedings Circuits, Devices and Systems*, December 2005, pp. 709 - 717.

Mury, T. & Fusco, V.F. (2007). Inverse Class-E Amplifier With Transmission-Line Harmonic Suppression, *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 54, No. 7, July 2007, pp. 1555 - 1561.

Negra, R.; Ghannouchi, F. M. & Bächtold, W. (2007). Study and Design Optimization of Multiharmonic Transmission-Line Load Networks for Class-E and Class-F K-Band MMIC Power Amplifiers, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 55, No. 6, Part 2, June 2007, pp. 1390 - 1397.

Ozalas, M.T. (2005). High efficiency class-F MIMIC power amplifiers at ku-band, *2005 IEEE Wireless and Microwave Technology Conference*, WAMICON 2005, pp. 137 – 140.

Raab, F.H. (1996). Introduction to Class-F Power Amplifiers, *RF Design*, Vol.19, No. 5, May 1996, pp.79-84.

Raab, F.H. (1997). Class-F Power Amplifiers with Maximally Flat Waveforms, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 45, No. 11, November 1997, pp. 2007-2012.

Raab, F.H. (2001). Class-E, Class-C, and Class-F power amplifiers based upon a finite number of harmonics, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 49, No. 8, August 2001, pp. 1462 – 1468.

Reece, M.A.; White, C.; Penn, J.; Davis, B.; Bayne, M.Jr; Richardson, N.; Thompson, W.I.I. & Walker, L. (2003). A Ka-band class F MMIC amplifier design utilizing adaptable knowledge-based neural network modeling techniques, *IEEE International Microwave Symposium Digest*, June 2003, Vol. 1, pp. 615 – 618.

Snider, D.M. (1967). A Theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdriven RF Power Amplifiers, *IEEE Transaction on Electron Devices*, Vol. 14, No. 6, June 1967, pp.851-857.

Sokal N. O. (2001). Class-E RF power amplifiers, *QEX* (published by American Radio Relay League, 225 Main St., Newington, CT 06111-1494, USA), January - February 2001, pp 9–20.

Sokal, N.O. & Sokal, A.D. (1975). Class E - A new class of high efficiency tuned single-ended switching power amplifiers, *IEEE Journal of Solid State Circuits*, Vol. SC-10, No. 3, June 1975, pp. 168-176.

Suetsugu, T & Kazimierczuk M.K. (2005). Voltage-clamped class E amplifier with transmission-line transformer, *IEEE International Symposium on Circuits and Systems*, ISCAS 2005, May 2005, Vol. 1, pp. 712 - 715.

Suetsugu, T. & Kazimierczuk M.K. (2007). Off-Nominal Operation of Class-E Amplifier at Any Duty Ratio, *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 54, No. 6, June 2007, pp. 1389 - 1397.

Trask, C. (1999). Class-F Amplifier Loading Network: A Unified Design Approach, *IEEE International Microwave Symposium Digest*, Vol. 1, June 1999, pp. 351 – 354.

Tyler, V.J. (1958). A new high efficiency high power amplifier, *Marconi Rev.* Vol. 21, No. 130, Fall 1958, pp. 96-109.

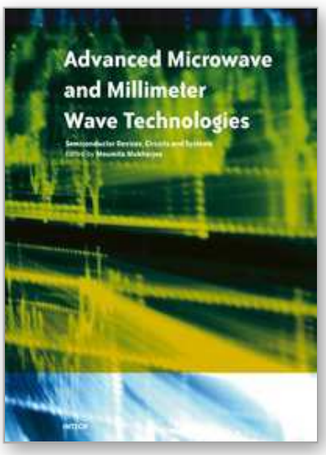
Wilkinson A. J. & Everard J. K. A. (2001). Transmission-Line Load-Network Topology for Class-E Power Amplifiers, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 49, No. 6, June 2001, pp. 1202 - 1210.

Woo, Y.Y.; Yang, Y. & Kim, B. (2006). Analysis and Experiments for High-Efficiency Class-F and Inverse Class-F Power Amplifiers, *IEEE Transaction on Microwave Theory and Techniques*, Vol. 54, No. 5, May 2006, pp. 1969 - 1974.

Wood, J. (1992). The history of International broadcasting, *IET History of Technology Series 19*, 1992 (ISBN 0863413021)

Xu H.; Gao, S.; Heikman, S.; Long S. I.; Mishra, U. K. & York, R. A. (2006). A High-Efficiency Class-E GaN HEMT Power Amplifier at 1.9 GHz, *IEEE Microwave And Wireless Components Letters*, Vol. 16, No. 1, January 2006, pp. 22 - 24.

IntechOpen



Advanced Microwave and Millimeter Wave Technologies
Semiconductor Devices Circuits and Systems
Edited by Moumita Mukherjee

ISBN 978-953-307-031-5
Hard cover, 642 pages
Publisher InTech
Published online 01, March, 2010
Published in print edition March, 2010

This book is planned to publish with an objective to provide a state-of-the-art reference book in the areas of advanced microwave, MM-Wave and THz devices, antennas and systemtechnologies for microwave communication engineers, Scientists and post-graduate students of electrical and electronics engineering, applied physicists. This reference book is a collection of 30 Chapters characterized in 3 parts: Advanced Microwave and MM-wave devices, integrated microwave and MM-wave circuits and Antennas and advanced microwave computer techniques, focusing on simulation, theories and applications. This book provides a comprehensive overview of the components and devices used in microwave and MM-Wave circuits, including microwave transmission lines, resonators, filters, ferrite devices, solid state devices, transistor oscillators and amplifiers, directional couplers, microstripeline components, microwave detectors, mixers, converters and harmonic generators, and microwave solid-state switches, phase shifters and attenuators. Several applications area also discusses here, like consumer, industrial, biomedical, and chemical applications of microwave technology. It also covers microwave instrumentation and measurement, thermodynamics, and applications in navigation and radio communication.

How to reference
In order to correctly reference this scholarly work, feel free to copy and paste the following:

Elisa Cipriani, Paolo Colantonio, Franco Giannini and Rocco Giofre (2010). The Switched Mode Power Amplifiers, Advanced Microwave and Millimeter Wave Technologies Semiconductor Devices Circuits and Systems, Moumita Mukherjee (Ed.), ISBN: 978-953-307-031-5, InTech, Available from: http://www.intechopen.com/books/advanced-microwave-and-millimeter-wave-technologies-semiconductor-devices-circuits-and-systems/the-switched-mode-power-amplifiers

INTECH
open science | open minds

InTech Europe
University Campus STeP Ri
Slavka Krautzeka 83/A
51000 Rijeka, Croatia
Phone: +385 (51) 770 447
Fax: +385 (51) 686 166
www.intechopen.com

InTech China
Unit 405, Office Block, Hotel Equatorial Shanghai
No.65, Yan An Road (West), Shanghai, 200040, China
中国上海市延安西路65号上海国际贵都大饭店办公楼405单元
Phone: +86-21-62489820
Fax: +86-21-62489821

© 2010 The Author(s). Licensee IntechOpen. This chapter is distributed under the terms of the Creative Commons Attribution-NonCommercial-ShareAlike-3.0 License, which permits use, distribution and reproduction for non-commercial purposes, provided the original is properly cited and derivative works building on this content are distributed under the same license.

IntechOpen

IntechOpen