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Analog to Digital Conversion Methods for Smart Sensing Systems

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Abstract

The new capabilities of smart sensing systems namely, adaptability, reconfiguration, low-energy consumption and cost, between others, require a wisely selection of the methods that are use to perform analog to digital conversion. It is very important to optimize the trade-offs between, resolution, accuracy, conversion rate, and energy consumption, between others, and above all to adapt dynamically the conversion parameters for different signals characteristics and applications' purposes. Establishing the best trade-offs are even more important when signals to be digitized have different signal-to-noise ratios (S/N) ratios, different requirements of measuring accuracy and acquisition rate, their characteristics are time-variant and above all if they are sharing the same digitalization device.

Very low resolution or conversion rate of data acquisition (DAQs) systems are generally not compliant with measurement systems' requirements since signal information is lost without any possible recovery procedure. Otherwise, if resolution or data acquisition rate are excessively high that means the sampling rate is much higher than its minimum value (Nyquist rate), the excessive amplitude and time resolutions provided by A/D conversion or frequency-to-digital conversion (FDC) does not improve measurements system's performance. Moreover, the excessive resolution or data acquisition rate implies an increase of hardware and software complexity, data processing load and a higher implementation cost, without any benefits. So, for any A/D or FDC conversion method the best trade-off between different conversion characteristics must be established considering applications' purposes. For example, in wireless sensing and actuating networks (WSAN) energy wastes are particularly important because a wrong choice of conversion method can affect deeply measurement system autonomy.

Whenever possible, classical A/D conversion methods are being replaced by discrete A/D conversion methods that are supported by low cost microcontroller (μC) (Microchip, 2010) connected to a few external resistive or capacitive components. This solution takes full advantage of μCs benefits, namely specific hardware and software capabilities and it provides a conversion rate that can be higher that several hundreds of kHz that is sufficient

for a large number of applications. These conversion also enables an easy implementation of trade-offs between resolution, conversion rate, and energy consumption (EC), errors' compensation, namely offset and gain errors, and linearization capabilities without need of any additional circuitry, look-tables or linearization algorithms. However, the main drawbacks of these conversion methods include a large sensitivity to noise and the need of frequent self-calibration routines.
Alternative digitalization methods that can be implemented without need of classical A/D converters are based on FDC methods.
Referring to the contents of the present chapter, the first session includes an introduction, state of the art and the main requirements of smart sensing systems (SSS) that must be considered in terms of signals' conditioning and digitalization.
The second session summarizes the main characteristics of two A/D digitalization methods that seem to be particularly suitable for smart sensing applications, namely, discrete A/D and FDC methods. Some implementation details, particularly those ones that take full advantage of low-cost microcontrollers and specific integrated circuits will be underlined. This section also includes the description of the working principle and main advantages of each conversions FDC method together with some simulation and experimental results. The last session is dedicated to conclusions.

Keywords: digitalization methods, smart sensing, error compensation, resolution, signal-to-noise ratio.

1. Introduction

Analogue to digital (A/D) and digital to analogue (D/A) conversions are subjects of paramount importance in every digital data acquisition system. In the last years, especial demands appear in a large number of applications namely the ones that are supported by smart sensing devices. These demands were mainly related with A/D conversion resolution, data sampling rate and energy consumption. Improving the performance is each parameter is obviously possible but in more than one conversion parameter needs to be improved simultaneously it is not an easy task because those are correlated. A clear correlation exists always between two main conversion parameters; if resolution is increased, the maximum A/D conversion's rate always decreases. Other compromise, particularly important for wireless measuring systems, exists between sampling and energy consumption. If low energy consumption is a main requirement for a given measuring system, its maximum A/D conversion rate must be reduced as much as possible taking account to the Nyquist[1] frequency required for the input signal's bandwidth.
Even when an A/D converter is used to convert a single signal with time variable characteristics, for example harmonic contents or voltage range, there is also the need do adapt its conversion parameters according to the dynamic characteristics of the signal.
Using multiple A/D converters in the same data acquisition unit and processing their outputs is a possible solution to surpass previous drawbacks. However, this is not a cost

[1] Nyquist rate is two times the bandwidth of a band-limited signal or a band-limited channel.

effective solution and it is not acceptable solution for smart [2]sensing systems, especially when many sensing unit are remote nodes of a wireless sensing network. In these applications, a single A/D with a flexible configuration must be used to optimize A/D conversion performance according signals' characteristics. These A/D converters, denominated as flexible analogue-to-digital converters (Pereira J. et al, 2001; Pereira J. et al, 2007), throughout this chapter, are aimed to establish the best trade off between the main A/D conversion's parameters in order to improve measuring system's performance. It is also important to underline previous trade-off must also A/D conversion errors[3], namely, linearity errors, offset and gain errors, signal to noise and distortion rate, jitter and latency time, to name a few, that must be minimized.
Additional advantages that are associated with a flexible A/D converter include an easy implantation on non-uniform sampling, particularly important in which concerns minimization of measuring system's energy consumption, generation of non-linear digital transfer characteristics and capability to implement different conversion methods. Since conversion rate is not a crucial requirement for the applications that are focused in the present chapter, the hardware and software parts of the A/D converter are mainly implemented by low cost microcontrollers (μCs), digital signal processors (DSPs) or field programmable gate arrays (FPGAs), between others processing devices.

2. Suitable digitalization methods for smart sensing applications

There are a large number of non-traditional and low-cost A/D conversion methods very suitable for SSS applications. Between these methods it is possible to underline pulse-width modulation methods, potentiometric methods, voltage to frequency methods, RC charge time constant methods, single, dual and multislope methods, sigma-delta methods and frequency to digital (F/D) conversion methods. It is important to underline that any of these methods can provide low energy power consumption, measurements error's compensation, namely, offset, gain and non-linearity errors compensations, easy implementation of the trade-offs between A/D or D/A conversion parameters, namely accuracy and conversion rate, and capability to implement multiple variable measurements with a single virtual sensor[4]. Moreover, it is also important to remember that in SSS applications accuracy is not the main goal of several applications and usually a number of bits lower than ten can fulfill applications' requirements. Data processing techniques that are exploited in SSS enhance conversion accuracy using different signal processing techniques after digitalization (e.g. data averaging, correlation and prediction techniques, errors' compensation, between others) and can compensate errors caused by influence variables[5] such as temperature, humidity and mechanical vibrations.

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[2] A smart sensors or smart transducer is a device with built-in intelligence, whether apparent to the user or not.

[3] Institute of Electrical and Electronics Enginneers, Inc., IEEE Std 1241 DRAFT: Standard for Terminology and Test Methods for Analog-to-Digital Converters.

[4] A virtual sensor is a sensor that can provide indirect measurement of several variables by using data processing algorithms that are applied to direct measurement's results provided by a single sensor.

[5] Influence variables are variables that are cross-correlated with measuring variables affecting measurement's accuracy.

It is beyond the scope of this chapter to describe a huge number of alternative conversion methods that can be used for SSS applications. Instead, two A/D conversion methods already utilized by the authors will be presented. One of these methods is based on an improved PWM A/D conversion method and the other one is based on a FDC converters. Some implementation details, particularly those ones that take full advantage of low-cost microcontrollers and specific integrated circuits are underlined together with some limitations of each method.

2.1 PWM based A/D conversion

Traditional PWM based A/D converters require a very high resistive-capacitive (RC) time constants and their sampling rate is very low. Typically, lower than a few tens of samples per second (S/s) for an eight bits' converter. This conversion method uses a PWM signal use mean value, obtained from the output of a low-pass-filter (LPF) is sequentially incremented by the quantization step amplitude and then compared with the input voltage. However, this A/D conversion method contains several disadvantages, namely, as previously referred, this method only supports very sampling rates, and it is very sensitive to noise and to components' deviations from their nominal values, usually resistors and capacitors tolerances.

A variant much more interesting of the traditional PWM based conversion method can be obtained if the input voltage conversion is performed using a single a square signal that contains a number (n) of high levels pulses and a number of low level pulses that depends on input voltage's amplitude to be converted. The resolution of this method is easily controlled by software. Each time the number of pulses contained in the conversion cycle is doubled an additional resolution bit is obtained. For each positive or negative conversion pulse, the voltage variation of LPF output is incremented or decremented by the quantization step amplitude of the converter, respectively. This A/D conversion method is especially suitable for SSS with a sampling rate requirements lower than a few hundreds of samples per second. It enables analogue-to-digital conversion without need of dedicated A/D integrated circuits, takes full advantage of microcontrollers' compare, capture and PWM (CCP) capabilities and supports an easily implementation of self-calibration routines to compensate gain, offset and nonlinearity errors without any requirements of additional circuitry, look-tables or linearization algorithms.

2.1.1 Improved PWM based A/D converter: working principle

Figure 1 represents the hardware block diagram of the converter. Its hardware part includes two digital ports of the μC, an analog comparator (Comp.) that can be inside the μC, a low-pass (RC) filter and an analogue switch (S).

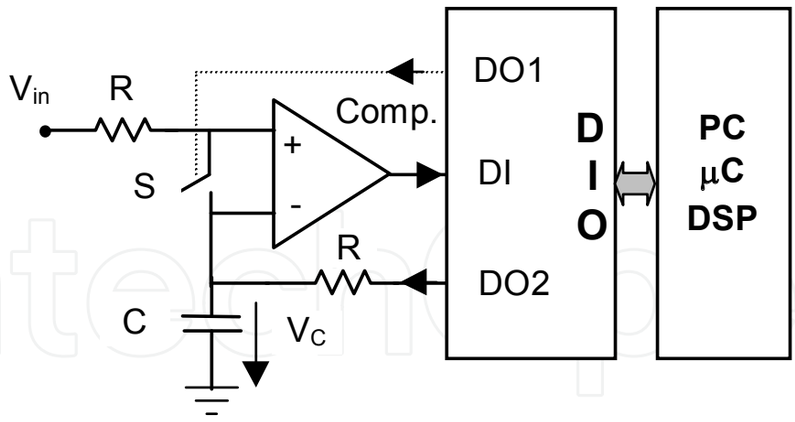

Fig. 1. Hardware block diagram (Comp.- comparator; DI- digital input; DO- digital output; DIO- digital input-output interface; PC- personal computer; µC- microcontroller; DSP- digital signal processor)

Before each A/D conversion, the analogue switch (S) is closed, and, the capacitor is charged with an initial voltage (V_{C0}) equal to the input voltage (V_{in}). It is assumed that the signal amplitude variation during acquisition time is lower than one LSB (Least Significant Bit). After this initialization cycle, the analogue switch (S) is opened, and the measurement cycle takes place. During this phase, the voltage delivered by the digital output (DO2) tends to maintain the capacitor charge by monitoring the output voltage of the comparator (Comp.). If the digital input (DI) is high, meaning that capacitor voltage is lower than V_{in}, digital output (DO2) is settled to the high level voltage (V_H), otherwise digital output (DO2) is settled to the low level voltage (V_L). Different values can be assigned for V_H and V_L and it is this way possible to reduce the voltage range of the A/D converter and to increase its resolution. Assuming that the R·C time constant is much higher than the pulse period (T_P) and lower than the capacitor's voltage variation in the order of few LSB's during T_P, it is possible to obtain the relationship between the input voltage amplitude (V_{in}) and the A/D converter's output code (n) (Pereira J. et al, 2001),

$$V_C(T_C) = V_{in} + n \cdot (V_H - V_{C0}) \cdot \left(1 - e^{-\frac{T_{P1}}{RC}}\right) + m \cdot (V_L - V_{C0}) \cdot \left(1 - e^{-\frac{T0}{RC}}\right) \quad (1)$$

where n and m represent the number of positive and negative pulses delivered by the µC during the conversion period (T_C), V_H represents the voltage amplitude of the positive pulses that have a time duration equal to (T_{P1}) and V_L represents the voltage amplitude of the negative pulse that have.

For a binary A/D converter coding $n+m=2^B$, where B represents the number of A/D converter's bits, from the previous relationship it is possible to obtain,

$$V_{in} = \frac{nk}{(2^b - n) + nk} V_H + \frac{2^B - n}{(2^B - n) + nk} V_L \quad (2)$$

where $k = \frac{1 - e^{-T_{P1}/RC}}{1 - e^{-T_{P2}/RC}}$ is a non-linear factor modulated by the relation between positive (T_{P1}) and negative (T_{P0}) pulse duration of the PWM signal, B is the number of bits of the ADC and V_H/V_L are the high and low digital voltage levels delivered by digital output (DO2), respectively.

Figure 2 represents the A/D converter's characteristic for five different values of k parameter. An eight's bits A/D converter with a ratio between pulse duration and time (τ=RC) is equal to 1/18. As expected for k=1, T_H=T_L, a linear characteristic is obtained.

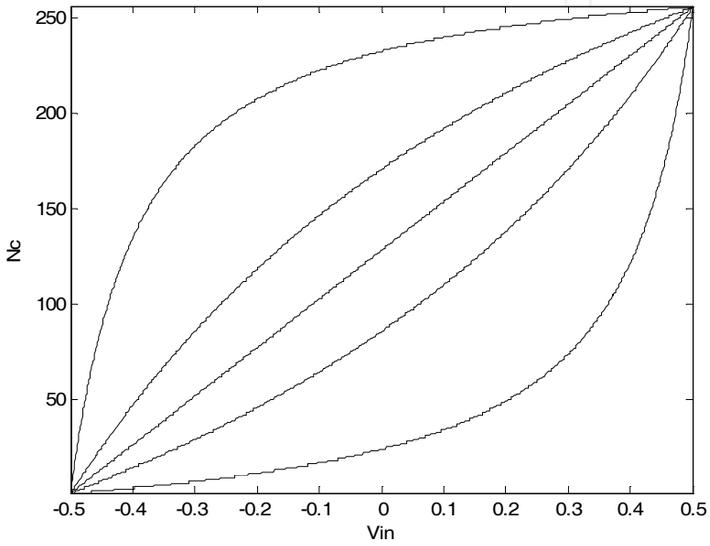

Fig. 2. A/D conversion characteristics for normalized input voltages and for an amplitude of positive pulse (VH) and amplitude negative pulses (VL) equal to -0.5 V and to 0.5 V, respectively (B=8 bits, TP/τ=1/28, TH=K·TL and k={1/10; 1/2; 1; 2; 10})

In which concerns sampling rate (S_R), for traditional PWM based converters, its value maximum value is given by,

$$(S_R)_{max} = \frac{(f_{\mu C})_{clk}}{4^B \cdot N} \tag{3}$$

where B represents the converter's number, $(f_{\mu C})_{clk}$ represents the converter's clock rate and N represents the number conversions that are performed during one period of the sinusoidal input signal (oversampling factor). Figure 3 represents the maximum frequency of a sinusoidal signal that can be converted by a traditional PWM based A/D converter as a function of the number of samples per second. As represented the maximum sampling rate is almost equal to 10 Hz S/s for the Nyquist rate (N=2).

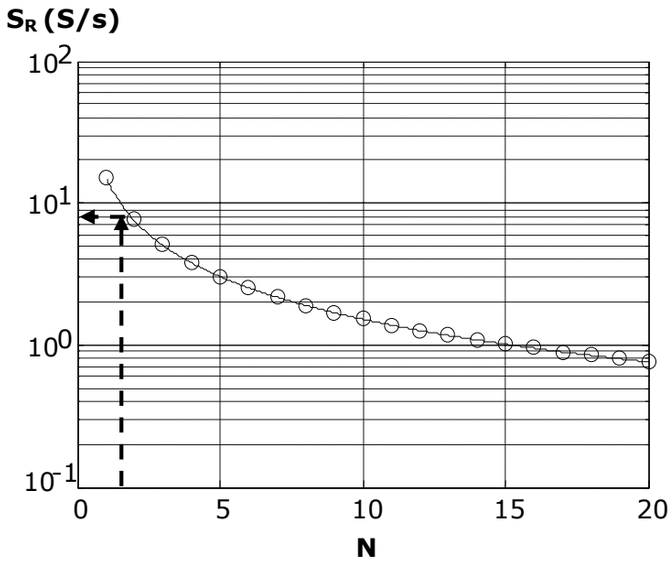

Fig. 3. A/D conversion rate for a converter with 8 bits resolution and running under a μC frequency clock equal to 1 MHz (traditional PWM based A/D converter)

If similar conditions are considered for the improved PWM based A/D converter the maximum sampling rate value is given by,

$$(S_R)_{max} = \frac{(f_{\mu C})_{clk}}{2^B \cdot N} \tag{4}$$

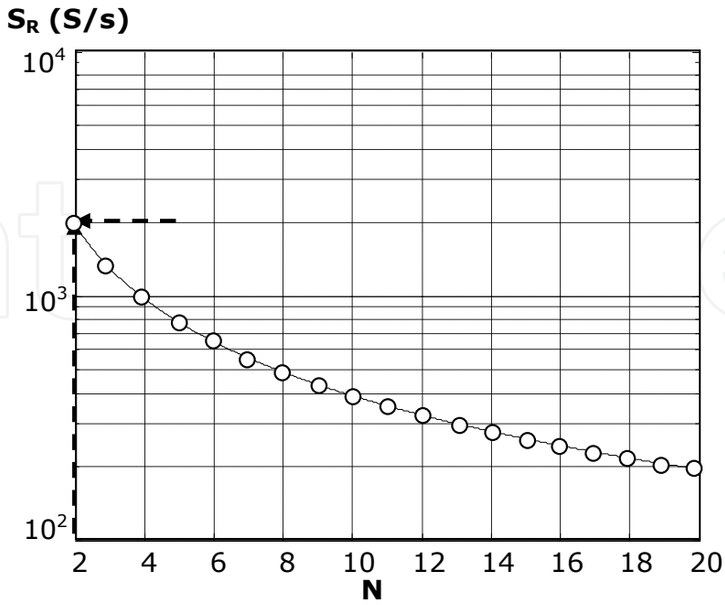

Fig. 4. A/D conversion rate for a converter with 8 bits resolution and running under a μC frequency clock equal to 1 MHz

Figure 4 represents the maximum frequency of a sinusoidal signal that can be converted by an improved version of the traditional PWM based A/D converter as a function of the oversampling factor. As represented in the figure signal's bandwidth is almost equal to 2 kS/s for the Nyquist rate (N=2).

2.1.2 Self-calibration capability

In order to improve the accuracy of the A/D converter, the measurement cycle can include an auto-calibration procedure (Goes F. & Gerard M., 1997; Goes F. & Gerard M., 1997), multiplexing three input signals: V_{in}, V_{REF} and V_{OFF}. The hardware block diagram of the PWM-A/D converter with continuous auto-calibration capability is represented in Figure 5.

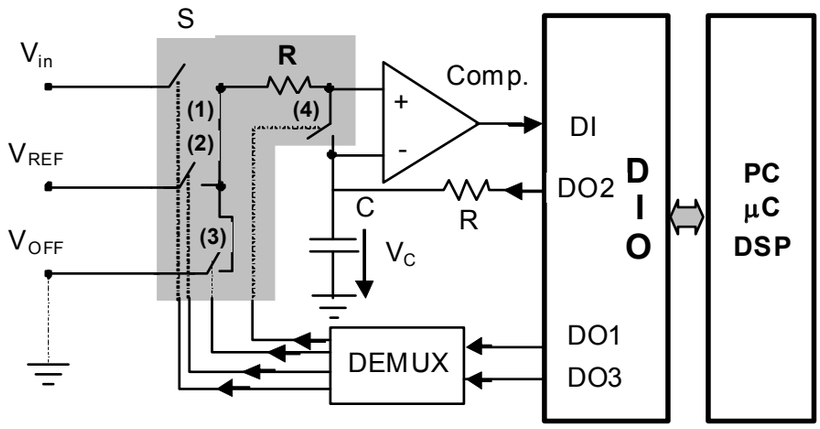

Fig. 5. Hardware block diagram of the PWM-A/D converter with continuous auto-calibration capability (Comp.- comparator; DI- µC's digital input port; DO- µC's digital output port; DIO- µC's digital input-output communication's interface; DEMUX- demultiplexer; PC- personal computer; µC- microcontroller; DSP- digital signal processor)

The reference voltage (V_{REF}) is usually equal to the ADC full-scale voltage (FS) and is used to correct the gain error. This reference voltage must have, at least, accuracy higher than ½ LSB of the A/D converter. For example, for an 8-bit converter, the reference voltage error must be lower than 0.195% of FS. The offset voltage (V_{OFF}) is usually equal to ground voltage level and is used to correct the offset error.
If the measurement results for V_{in}, V_{REF} and V_{OFF}, are equal to n, n_{REF} and n_{OFF}, respectively, the offset and gain errors can be continuously cancelled by using the following relation:

$$n_C = \frac{n - n_{OFF}}{n_{REF} - n_{OFF}} \cdot 2^B \tag{5}$$

where n_C represents the offset and gain compensated A/D converted code.
Another advantage of this measurement technique is that low-frequency noise (1/f) and temperature drift errors are almost cancelled because their bandwidth is generally much lower than the conversion period (T_C).

2.1.3 Experimental results

In this section we will considered the linearization characteristic of a circuit that includes a nonlinear thermistor (ON-400) (Omega, 1995) whose characteristic is represented in Figure 6. Linearity errors are represented for three different cases: without any correction of linearization errors for the temperature range [0, 50] (figure 7); with a first order least mean square (LMS) curve fitting (figure 8) and with the proposed PWM based A/D converter (figure 9). The advantage of the proposed solution for linearization purposes is clearly shown in Figure 9. It enables a non-linearity error reduction of an almost equal to 10 and 5 when compared with the terminal based linearity error and the first order LMS curve fitting, respectively, without the need of look-up tables or mathematical routines for linearization.

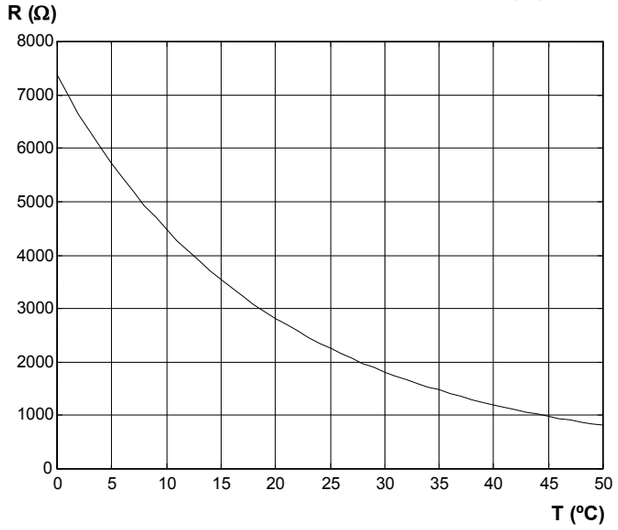

Fig. 6. Resistance-temperature characteristic of an ON-400 thermistor probe with standard 10'' leads

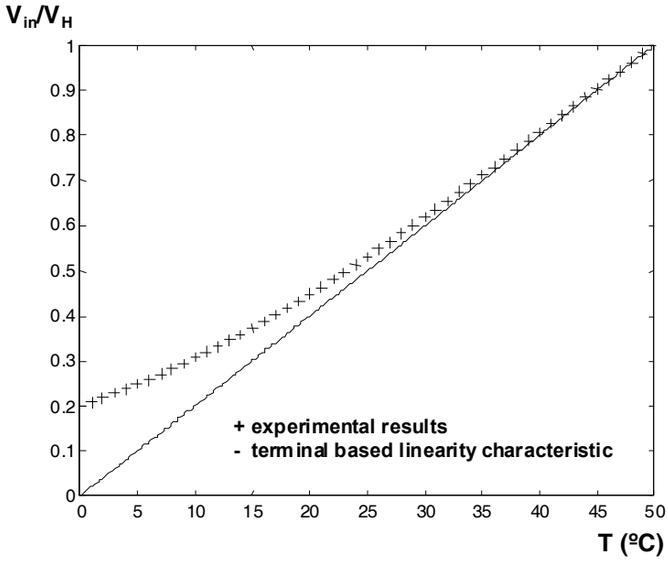

Fig. 7. Experimental results and linear characteristic without any correction of linearization errors for the temperature range [0, 50] ºC (maximum relative error=19.9 % of FS)

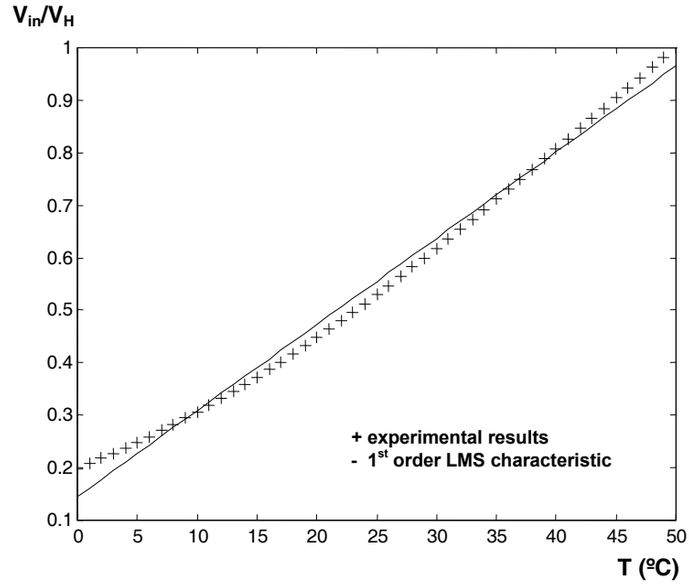

Fig. 8. Experimental results and 1st order LMS for the temperature range [0, 50] ºC (maximum relative error=5.4 % of FS)

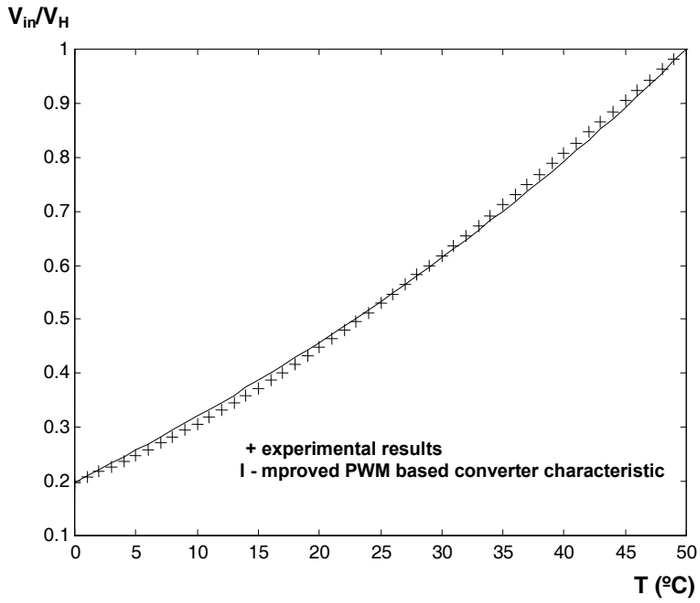

Fig. 9. Experimental results and curve fitting characteristic obtained with the improved PWM based A/D converter for the temperature range [0, 50] ºC (maximum relative error=1.4 % of FS, $k=k_{OPT}=0.72$)

2.2 Frequency to digital conversion methods

Nowadays the number of transducers that use frequency-time domain parameters modulated by a physical, chemical or biological quantity is increasing and they are a promising alternative that must be considered in the design and implementation of any measurement system. Several advantages are associated with FDC methods. Based on

calibration data or on-line historical measurement data, an appropriate accuracy of the FDC device can be settled avoiding excessive conversion duration (T_C) that restricts, without any benefit, the maximum sampling rate of the measurement system. An intrinsic advantage of FDC conversion methods is that they eliminate the need of traditional A/D and D/A converters and they can compensate a large number of, internal and external, error sources that are associated with any measurement system. Additional advantages include higher accuracy, resolution, dynamic range, noise immunity, simplicity of implementation and interfacing, and a lower cost compared with equivalent digitalization methods with identical performances. Moreover, the advantages, previously referred, the high accuracy of this conversion method is related with accuracy. It can achieve a relative errors (δ) lower than 0.001 % FS (full-scale), being this error negligible for almost any measuring system.
The next paragraphs will underline main characteristics of FDC conversion methods presenting their working principle and their self-adaptive characteristics that make them a suitable for SSS applications.
In which concerns implementation, any microcontroller or a set of commercial off-the-shelf (COTS) integrated circuits, without any complex circuitry, can support the hardware that is required for the implementation of a FDC.

2.2.1 Frequency to digital conversion methods: working principle

The working principle of FDC methods is based on different techniques that can perform time and frequency measurements (IFSA, 2004, Kirianaki et al, 1998; Kirianaki et al, 2002). Between these techniques, we can underline the method of dependent count (MDC) due to its advantages and easy implementation.
Using this method a fixed number of pulses is counted according to the required measurement accuracy. Figure 10 represents the timing diagram of the MDC during a single measurement cycle for accuracy better than δ.

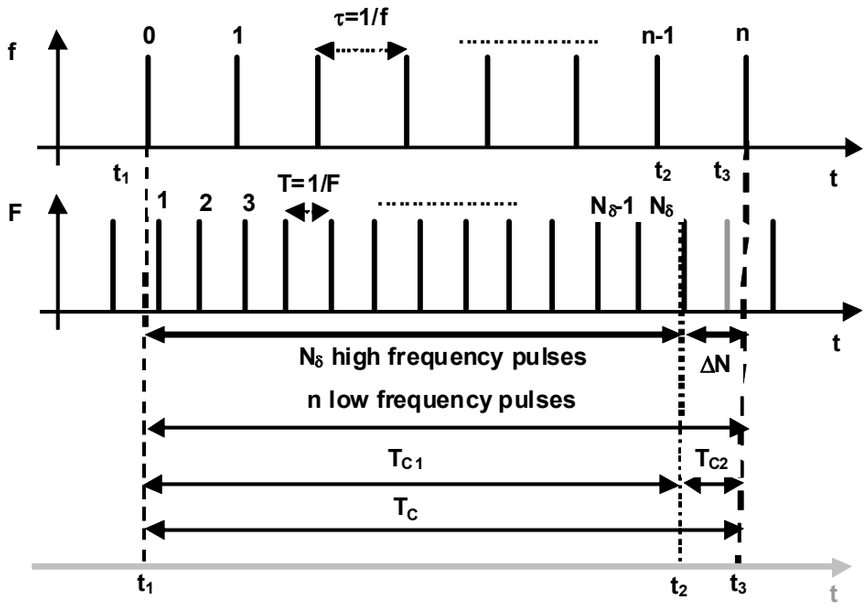

Fig. 10. Timing diagram of the MDC during a single measurement cycle (accuracy better than δ)

To obtain a relative measurement error lower than δ we must count at least $N_\delta=1/\delta$ pulses of the signal with higher frequency (F). If F is higher frequency signal's value and f the lower frequency signal's value and the unknown frequency (f_x) is given by,

$$\begin{cases} f_x = f_0 \cdot \dfrac{n}{N_\delta} \text{ if } f_x \le f_0 \\ f_x = f_0 \cdot \dfrac{N_\delta}{n} \text{ if } f_x > f_0 \end{cases} \tag{6}$$

where f_x represents the unknown frequency, f0 represents the reference frequency, N_δ and n represents the number of high frequency and low frequency pulses counted during conversion period (T_C), respectively. As represented in figure 10, T_C is an integer number (n) of the low frequency signal period (τ).

The conversion period contains a number of high frequency pulses equal to N_δ plus a remaining number of pulses ΔN contained in time interval T_{C2}. Minimum and maximum values of quantization error are associated with the minimum and maximum number remaining pulses counted during time interval [t_2, t_3], respectively. These values are given by,

$$\begin{cases} \Delta N_{min} = 0 \\ \Delta N_{max} = \dfrac{\tau}{T} = \dfrac{F}{f} \end{cases} \tag{7}$$

From the previous expression, taking account the real number of high frequency pulses that are counted, the minimum and maximum values of quantization errors are given by,

$$\begin{cases} \delta_{max} = \dfrac{1}{N_\delta + \Delta N_{min}} = \dfrac{1}{N_\delta} \\ \delta_{min} = \dfrac{1}{N_\delta + \Delta N_{max}} = \dfrac{1}{N_\delta + F/f} \end{cases} \tag{8}$$

We can conclude that MDC is particularly suitable for time and frequency measurements. This method enables an easy adjustment of measurement's accuracy by selecting an appropriate value of N_δ for the requirements of each application. It is important to underline that it does not make any sense to define a quantization error much lower than the required accuracy since sampling rate and processing load are unnecessary affected. If the reference frequency (f_0) is selected to minimize the ratio F/f from expression (8) we can conclude that the measurement error is almost constant an equal to $1/N_\delta$. In which concerns conversion time (T_C) its minimum and maximum values are given by,

$$\begin{cases} (T_C)_{min} = N_\delta \cdot T \\ (T_C)_{max} = (N_\delta + F/f) \cdot T \end{cases} \tag{9}$$

From the previous relationships, we can conclude that as long as N_δ is much higher that F/f ratio the conversion time is almost constant without any waste overtime.

As expected MDC is not an exception, in which concerns accuracy and conversion rate, the conversion rate is inversely proportional to the requested accuracy.

2.2.2 Experimental results

In this section, we will consider a relative humidity measurement system with temperature compensation.

A smart sensing temperature kit (Smartec, 2010) containing four temperature sensors (SMT 160-30) was used to perform temperature measurements. The electrical schematic diagram and view are represented in figures 11 and 12, respectively. Each temperature sensor delivers a duty-cycle modulated signal.

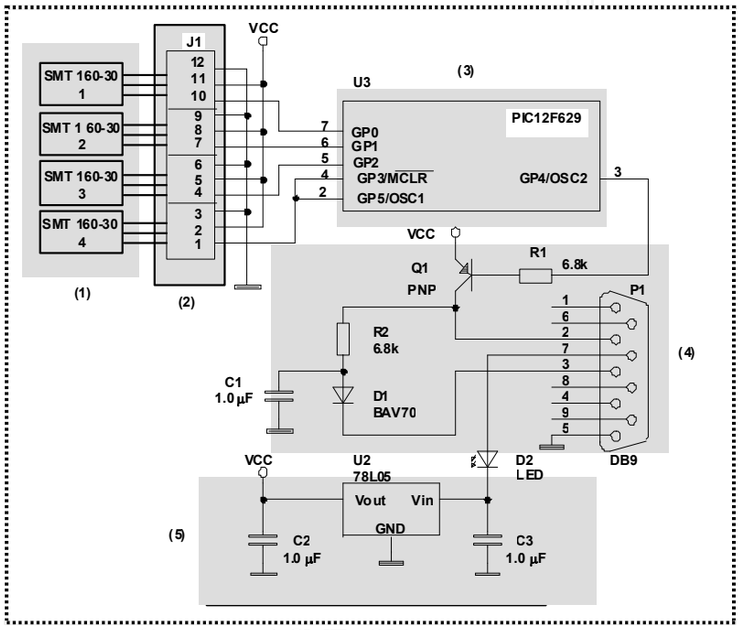

Fig. 11. Hardware block diagram of SMTAS04: (1) temperature sensors; (2) connecting terminals; (3) µC- PIC12F629; (4) DB9- RS232 interface plug; (5) voltage regulator

Fig. 12. View of the Evaluation Board SMTAS04 (with permission from SMARTEC Inc.)

The output signal for each sensor is a square wave with a well-defined temperature-dependent duty cycle. The temperature is linearly related with the DC according to the following relationship,

$$T = \frac{DC - 0.320}{0.00470} \tag{10}$$

where DC represents the duty-cycle and T the temperature in ºC.
Since the DC modulated signal delivered by SMT 160-30 is TTL/CMOS compatible it can be directly connected to the digital input of a microcontroller device, for example, without need of any interface circuits. Measurement's accuracy can be increased by sampling the DC signal over a larger number of periods, however this cause a lower conversion rate and a higher value of power consumption. According to applications' requirements it is possible to optimize the trade-offs between accuracy, conversion rate and power consumption that can eventually change during real time operation. Statistical parameters of measurement or self-calibration data can be used to improve measurement's system performance (Pereira J. et al, 2009).
The relative humidity transducer (HF3223) (Humirel Inc., 2001) delivers a square wave signal whose frequency is given by,

$$F_{out} = 9740\text{-}18 \cdot RH \quad (Hz) \tag{11}$$

where RH represents relative humidity in percentage and F_{out} is the frequency in kHz. The frequency varies between 9560 Hz and 8030 Hz when RH varies between its minimum and maximum values, 10 % and 95 %, respectively.
Time and frequency measurements were performed using the universal frequency to digital converter integrated circuit UFDC (IFSA, 2010) whose block diagram and view are represented in figures 13 and 14, respectively.

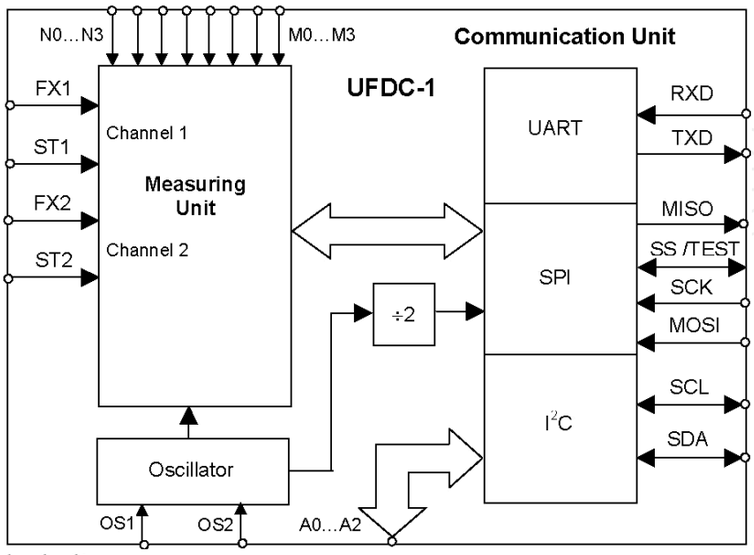

Fig. 13. UFDC block diagram

Fig. 14. View of the Evaluation Board SMTAS04 (with permission of Sergey Yurish)

The experimental tests of the temperature compensated humidity measurement system were performed using the UFDC that performs frequency, period, its ratio, duty-cycle and phase-shift measurements using a set of programmable accuracies levels. In the following, we propose a method that can be used to configure the FDC. The FDC parameters were configured to improve measurement's system performance, namely, to prevent FDC waste overtime and superfluous processing load (Pereira J. et al, 2005).
The method that was used to reach those objectives is based on the statistical parameters of measurement and self calibration data in order to configure properly the FDC device. The main tasks of the software programs that were include the uncertainty evaluation of the measurement data, the accuracy selection of the UFDC device, the detection of abnormal and faulty working conditions and the compensation of RH measurements caused by temperature variations.
The criteria used for UFDC accuracy selection is based on a Gaussian curve fitting histogram of the calibration data. Being the standard deviation (σ_c) and the mean value of the calibration (X_c) data defined by:

$$\sigma_c = \sqrt{\frac{\sum_{i=1}^{N}\left(X_c(i)-\overline{X}_c\right)^2}{N-1}} \qquad \overline{X}_c = \frac{\sum_{i=1}^{N} X_c(i)}{N} \tag{12}$$

where $X_c(i)$ represents the calibration measurements of a set of N points. The standard deviation, or a multiple of its value, is generally used to quantify measurement uncertainty. An uncertainty value equal to $\pm 3 \cdot \sigma_c$ of the calibration data set assures, for a statistical

Gaussian distribution, that 99.7% of the measurements, of a given quantity (Xm), are within the interval $[X_m\text{-}3\cdot\sigma_c;\ X_m+3\cdot\sigma_c]$.
Based on these premises, the UFDC selected accuracy (δ_{max}) is the higher one that verifies the following condition:

$$\delta \le 100 \cdot \min\left(\frac{3\cdot\sigma_C}{\overline{X}_C}\right) \quad (\%) \tag{13}$$

where σ_c represents the standard deviation obtained from Gaussian curve fitting histogram, $\overline{X}_C$ represents the average value of measurement results, obtained during calibration phase, and min() represents the minimum value of the argument evaluated for the set of N calibration points.
The above criteria assures that selected UFDC accuracy is adjusted to 99.7 % of the calibration data being the major part of measurement noises' automatically cancelled without need of superfluous computing procedures (e.g. averaging). This result optimizes measurement's system performance especially when the UFDC device converter multiple signals with different accuracies and sampling rates requirements. Figures 15 and 16 represent the Gaussian curve fitting for a set calibration points (N=1024) and the front panel of the virtual instruments (VI) (NI, 2010) used to display temperature and humidity measurement results, respectively.

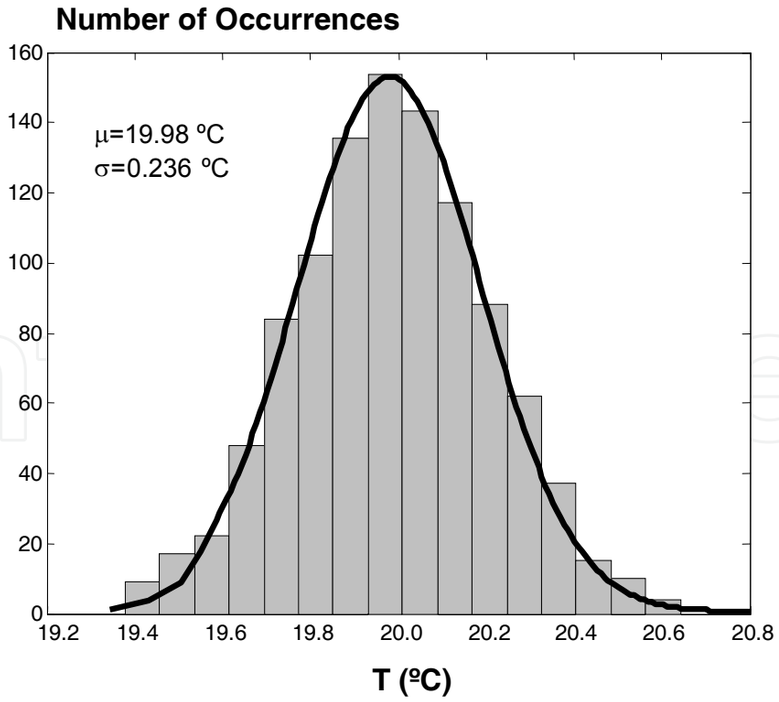

Fig. 15. Gaussian curve fitting of measurement data distribution

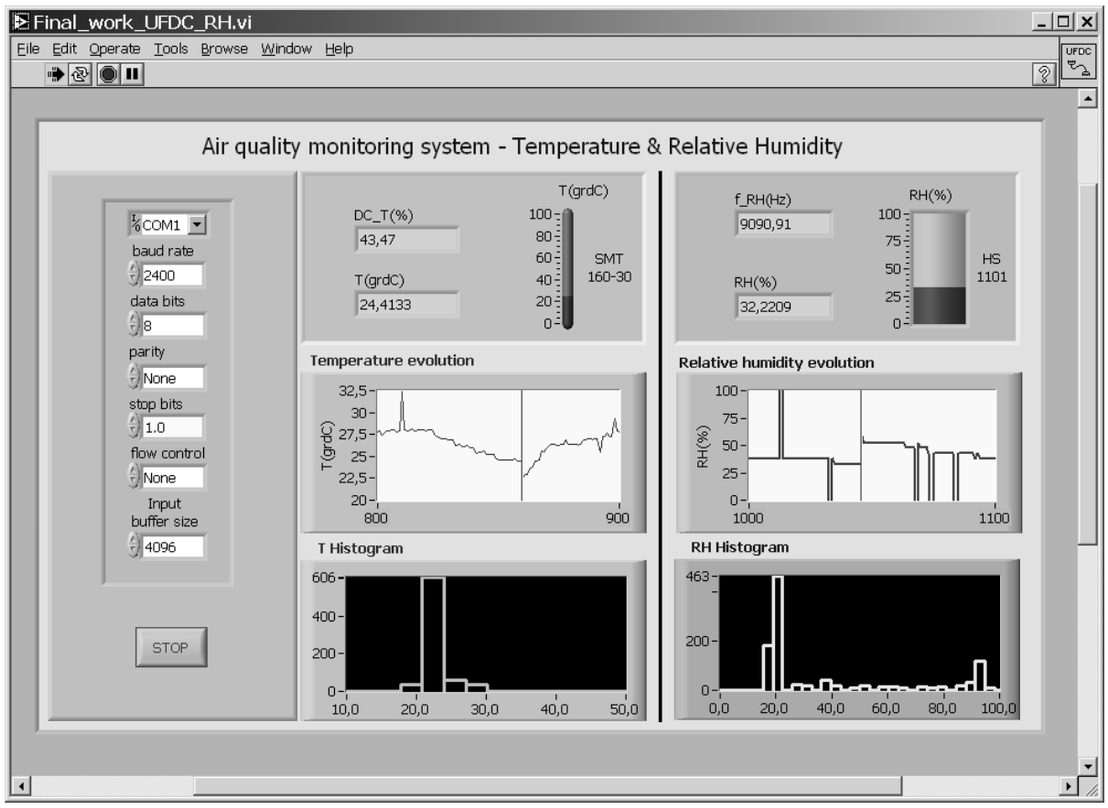

Fig. 16. VI front panel of the VI used to display temperature and relative humidity measurement results

In this example, the normalized standard deviation of measurement data is approximately equal to 3.5 %. Therefore, since the UFDC integrated circuit is used to perform FDC is implanted by the UFDC, accuracy equal to 0.5% is enough to fulfill application's requirements. If the maximum measurement accuracy of the UFDC was selected (δ=0.001%) the conversion time would be 500 times higher without any performance gain.

3. Conclusions

This chapter presents two A/D conversion methods that are particularly suitable for SSS applications. Both methods exhibit a set of characteristics that ensures an easy establishment of trade-offs between, resolution, accuracy, conversion rate, dynamic range and energy consumption. Moreover, both methods enable the establishment of flexible choice of conversion parameters that can be dynamically adjusted to optimize measurement's systems performance for different input signals characteristics and applications' purposes.
Finally, it is important to underline that exists many others A/D conversion solutions, not based on conventional A/D, that are also suitable for SSS A/D conversion. However, as previously referred, it is beyond the scope of this chapter to describe a huge number of alternative conversion methods that can be used for SSS applications.

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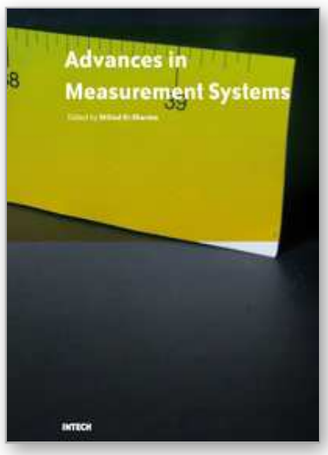

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