We are IntechOpen, the world's leading publisher of Open Access books Built by scientists, for scientists

4,800
Open access books available

122,000
International authors and editors

135M
Downloads

Our authors are among the

154
Countries delivered to

TOP 1%
most cited scientists

12.2%
Contributors from top 500 universities

CLARIVATE ANALYTICS BOOK CITATION INDEX INDEXED

WEB OF SCIENCE™

Selection of our books indexed in the Book Citation Index in Web of Science™ Core Collection (BKCI)

Interested in publishing with us?
Contact book.department@intechopen.com

Numbers displayed above are based on latest data collected.
For more information visit www.intechopen.com

10

Advanced Simulation for ESD Protection Elements

Yan Han and Koubao Ding
ZJU-UCF Joint ESD Lab, Zhejiang University, Hangzhou 310027, P.R.China

1. Introduction

Electrostatic discharge (ESD) failure is one of the most important causes of reliability problems, therefore the design and optimization of ESD devices have to be done. To achieve very short time to market and reduce the development effort, one tries to make use of the benefit of simulation tools. However, due to the complex physical mechanism of ESD events and the hard mathematic calculation in the snapback region, simulation of the I-V characteristic of ESD protection devices has been proved to be difficult.

This chapter aims at providing a systematic way to ESD simulation, including the process simulation, device simulation and circuit level simulation. Process/device simulation offers an effective way to evaluate the performance of ESD protection structures. However, to prevent the injury of ESD, protection circuits are used sometimes. Therefore circuit level simulation is needed.

There are several process/device simulation tools in the world, the most widely used of which include Tsuprem4/Medici, Athena/Atlas and Dios/Mdraw/Dessis. Tsuprem4, Athena and Dios are process simulators, while Medici, Atlas and Dessis are device simulators. Mdraw is an independent mesh optimization tool, and the similar functions are integrated in device simulation tools, such as Medici and Atlas. The process and device simulation methods introduced in the following will be based on Dios/Mdraw/Dessis, except for the mixed-mode simulation, which is based on Tsuprem4/Medici. And the circuit level simulation will be carried out on the Candence platform.

2. Process simulation

The starting point of ESD simulation is to construct an electronic pattern of the device which can be generated by manual device set-up or process simulation. And obviously, process simulation provides more realistic description of the device. The principle of process simulation is to minimize the errors that might be brought into the following device simulation. Therefore, the physical models used should be carefully chosen. The most important process steps are implantation and diffusion which will be discussed in the following.

Taking Dios for example, this section will introduce physical models used for implantation and diffusion. The implantation models used in Dios consists of analytic implantation models and Monte Carlo implantation model. Monte Carlo implantation model simulates at

Source: Advances in Solid State Circuits Technologies, Book edited by: Paul K. Chu,
ISBN 978-953-307-086-5, pp. 446, April 2010, INTECH, Croatia, downloaded from SCIYO.COM

the atomic level, and it consumes too much time, therefore, in most cases, it is not suitable for ESD simulation. Analytic implantation models are analyzed by series of distribution functions, including Gauss distribution function, Pearson distribution function, Pearson-IV distribution function (P4), Pearson- IV distribution with linear exponential tail function (P4S), Pearson- IV distribution with general exponential tail function (P4K), Gauss distribution with general exponential tail function (GK), Jointed half-Gauss distribution function (JHG), Jointed half-Gauss distribution with general exponential tail function (JHGK). The eight distribution functions are called single primary distribution functions. The complicated expressions of the functions will not be discussed here, and all of them can be found in the DIOS USER'S MANUAL.

The single primary distribution functions describe the relationship between impurity distribution and seven key parameters, which are determined by implantation process step. The seven key parameters are RP (Rp), STDV (σp), STDVSec (σp2), GAMma (γ), BETA (β), LEXP (lexp), LEXPOW (α). The range of parameters that must be specified for each of the single primary distribution functions are shown in Table1. In Table1, x means the parameter must be a real number, x0 means the parameter must be nonnegative, > 0 means the parameter must be positive, and ∅ means the parameter is not allowed for the particular function. Once the implanted element, energy, dose, tilt and rotation of an implantation process step are defined by users, the relevant parameter set will be looked up in implant tables. With proper parameter set, the impurity distribution will be calculated subsequently. If users have data fitted to experiments, the parameter set can be defined in implantation command.

Symbol:	R_p	σ_p	σ_{p2}	γ	β	l_{exp}	α
Keyword:	RP	STDV	STDVSec	GAMma	BETA	LEXP	LEXPOW
Gauss	x	> 0	∅	∅	∅	∅	∅
Pearson	x	> 0	∅ T	x	x	∅	∅
P4	x	> 0	∅	x	x	∅	∅
P4S	x	> 0	∅	x	x	x0	∅
JHG	x	> 0	> 0	∅	∅	∅	∅
GK	x	> 0	∅	∅	∅	> 0	> 0
P4K	x	> 0	∅	x	x	> 0	> 0
JHGK	x	> 0	> 0	∅	∅	> 0	> 0

Table 1. Range of parameter specification for the distribution functions

According to the simulation results, the single primary distribution functions can be divided into 3 groups. Group1 contains Pearson distribution function; group2 contains P4, P4S, P4K distribution functions; group3 contains Gauss, GK, JHG, JHGK distribution functions. Fig.1 (a) shows the 2D impurity distribution with different implantation models; Fig.1 (b) shows the impurity distribution along Y direction. From Fig.1 (a) and Fig.1 (b), we can see that functions in the same group have similar simulation results. Actually, the distribution functions in group3 are usually used in deep implantations, such as WELL implantation in CMOS process; and the distribution functions in group1 and group2 are usually used in shallow implantations, such as drain/source implantation in CMOS process.

In order to obtain more accurate simulation result, we should take ion channeling into consideration. Then the dual primary distribution functions should be used. That is, the profile

is divided into two components, the first components representing the profile of ions, which don't channel, and the second one representing the channel ions. A dual primary distribution function is obtained by specifying two single primary functions for the two components mentioned above. It can be defined in the implantation command following the format:

Implantation (…, Function=(function1,function2))

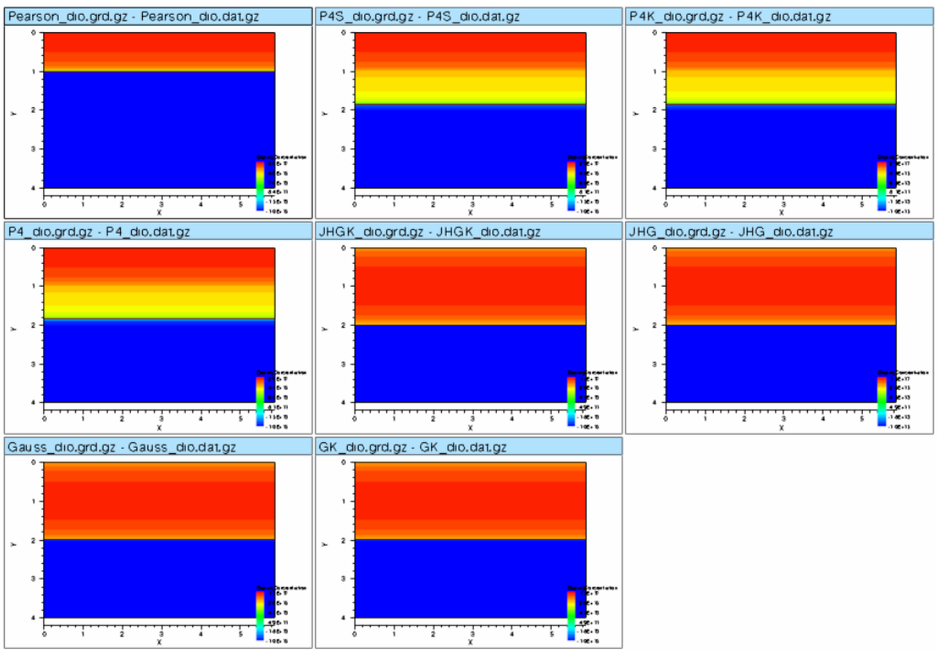


Fig. 1. (a) 2D impurity distribution

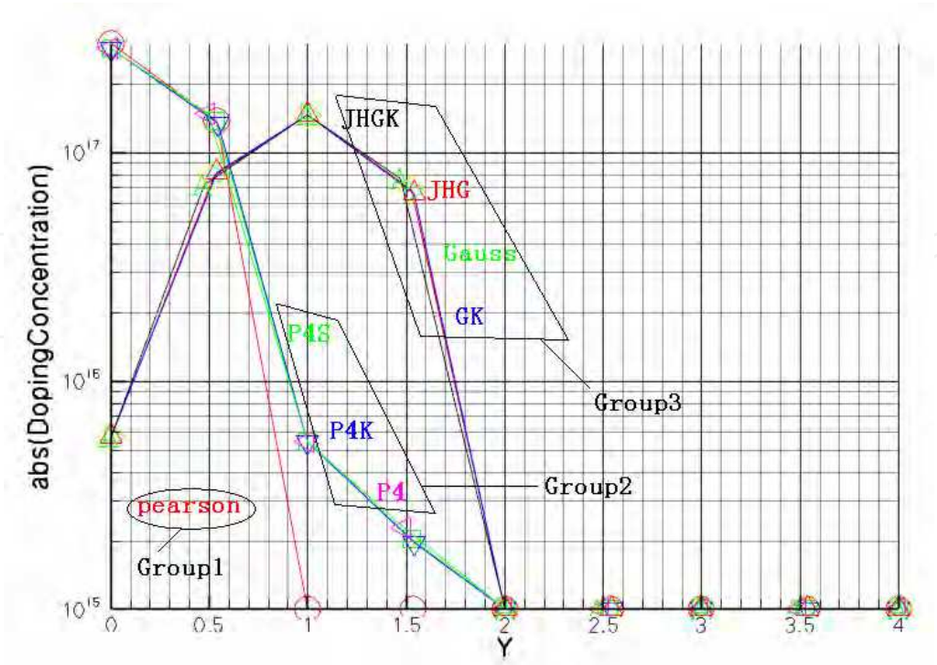


Fig. 1. (b) impurity distribution along Y direction

DIOS provides 5 models for the diffusion process step: Conventional, Equilibrium, Loosely coupled, Semicoupled, and Pairdiffusion. Conventional model is the simplest model but consumes the least time, while Pairdiffusion model is the most accurate model but consumes the most time. In ESD simulation, we'd better select Pairdiffusion model, because it always provides the best boundary shape, which will benefit in convergence problems in the following device simulation.
After selecting proper physical model, the process simulation can be carried out, and the produced electronic pattern of device is then imported into the mesh optimization tool-Mdraw. After the mesh optimization, device simulation is ready.

3. Device simulation

Device simulation is based on solving a set of mathematic and physical equations. And the physical parameters used in these equations are described by different physical models, parts of which are from papers and others are fitted by software engineers. The parameter sets of the physical models are based on the data from several process technologies, and can not cover every process technology. Therefore, to a detailed process technology, some parameters of physical models should be modified. To simulate an ESD event correctly, accurate physical models and proper parameter sets are the most important, no matter which simulation method is chosen.
To account for high electrical field and high temperature effects during an ESD event, the physical models below in ISE TCAD must be included: 1)Fermi-Dirac statistics. When the carrier density exceed 1×10^{19} cm-3, the default Boltzmann statistics becomes not suitable for simulation. 2) Accurate effective intrinsic carrier density model with band gap narrowing and Fermi correction included. 3) A comprehensive mobility model with doping dependence, carrier-carrier scattering, and high field saturation taken into consideration (In MOS devices, surface mobility degradation due to acoustic surface phonons and surface roughness should be also taken into consideration). 4) Recombination model should contain both Shockley-Read-Hall (SRH) model and Auger model, and SRH model should take doping dependence, temperature dependence and field-enhanced recombination into consideration. 5) Avalanche generation. 6) Thermodynamic model considering the self-heating effect. 7) Thermoelectric power model.
Simulating ESD events, three physical parameters are the most important: mobility of carriers (μ), lifetime of free-carrier (τ), and the generation rate (G) dominated by ionization impact.
Mobility is described in ISE TCAD with several degradation models, just as illustrated above. Taking all of these issues into consideration, the mobility is finally formulated as:

$$\mu = \mathrm{f}(\mu_{low}, F) \tag{1}$$

The function is determined by which model is chosen for high field saturation. And μlow in Eq.(1) is formulated as:

$$\mu_{low}^{-1} = \mu_{dop}^{-1} + \mu_{eh}^{-1} + D\mu_{ac}^{-1} + D\mu_{sr}^{-1} \tag{2}$$

In Eq.(2), μ_{dop} represent the doping-dependent mobility degradation mechanism, μ_{eh} is the mobility due to carrier-carrier scattering, μ_{ac} illustrates the surface contribution due to acoustic surface phonons, μ_{sr} is the surface contribution attributed to surface roughness, and D is given by:

$$D = \exp(-x / l_{crit}) \tag{3}$$

where x is the distance from the interface and l_{crit} is a fit parameter. μ_{ac} and μ_{sr} can be ignored in non-surface devices.

We have run simulations using different models, and it is found that Masetti model for doping dependence mobility degradation, Conwell-Weisskopf model for carrier-carrier scattering, and Canali model for high field saturation provide the best result. In Masetti model, μ_{dop} is expressed as:

$$\mu_{dop} = \mu_{\min 1} \exp\left(-\frac{P_c}{N_i}\right) + \frac{\mu_{const} - \mu_{\min 2}}{1 + \left(\frac{N_i}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1 + \left(\frac{C_s}{N_i}\right)^{\beta}} \tag{4}$$

In Eq.(4), Ni is the total doping concentration, μ_{const} is the mobility in low doping level condition, and other parameters are fit parameters. In Conwell-Weisskopf model, μ_{eh} is expressed as:

$$\mu_{eh} = \frac{D\left(\frac{T}{T_0}\right)^{3/2}}{\sqrt{np}} \left[\ln\left(1 + F\left(\frac{T}{T_0}\right)^2 (pn)^{-1/3}\right)\right]^{-1} \tag{5}$$

In Eq.(5), n, p are the electron and hole densities, T_0=300 K, and T denotes the lattice temperature. In Canali model, high field mobility degradation is expressed as:

$$\mu(F) = \frac{\mu_{low}}{\left(1 + \left(\frac{\mu_{low} F}{v_{sat}}\right)^{\beta}\right)^{1/\beta}} \tag{6}$$

In Eq.(6), μ_{low} is the low field mobility, v_{sat} and β are temperature dependent parameters, and are expressed as:

$$v_{sat} = v_{sat,0}\left(\frac{T_0}{T}\right)^{v_{sat},\exp}, \quad \beta = \beta_0\left(\frac{T}{T_0}\right)^{\beta_{\exp}} \tag{7}$$

In Eq.(7), except of T_0 and T, all of the parameters are fit parameters.

Lifetimes of free-carriers are governed by recombination models. SRH recombination rate and Auger recombination rate are given in Eq.(8) and Eq.(9) separately.

$$R_{net}^{SRH} = \frac{np - \gamma_n \gamma_p n_{i,eff}^2}{\tau_p(n + \gamma_n n_1) + \tau_n(p + \gamma_p p_1)} \tag{8}$$

$$R^A = \left(C_n n + C_p p\right)\left(np - n_{i,eff}^2\right) \tag{9}$$

In Eq.(8), $n_{i,eff}$ is the effective intrinsic carrier density, γ_n and γ_p are correction parameters for Fermi statistics, n_1 and p_1 are expressed as:

$$n_1 = n_{i,eff} e^{\frac{E_{trap}}{kT}},\ p_1 = n_{i,eff} e^{\frac{-E_{trap}}{kT}} \tag{10}$$

where E_{trap} is the difference between defect level and intrinsic level. The silicon default value is E_{trap} =0. In Eq.(8), τ_n and τ_p are temperature and field dependent parameters, expressed as:

$$\tau_c = \tau_{dop} \frac{\mathrm{f}(T)}{1+\mathrm{g}_c(F)},\quad \mathrm{c} = \mathrm{n,p} \tag{11}$$

The component $[1+\mathrm{g}_c(F)]^{-1}$ in Eq.(11) is a field enhancement factor. τ_{dop} and $\mathrm{f}(T)$ are expressed as:

$$\tau_{\mathrm{dop}}(N_i) = \tau_{\min} + \frac{\tau_{\max} - \tau_{\min}}{1+\left(\frac{N_i}{N_{ref}}\right)^{\gamma}},\ \mathrm{f}(T) = \left(\frac{T}{300}\right)^{T_\alpha} \tag{12}$$

Except for N_i and T, other parameters in Eq.(12) are all fit parameters.
Auger recombination rate is formulated in Eq.(9), in which the temperature-dependent coefficients C_n and C_p are expressed as:

$$C_i(T) = \left(A_{A,i} + B_{A,i}\left(\frac{T}{T_0}\right) + C_{A,i}\left(\frac{T}{T_0}\right)^2\right)\left(1 + H_i e^{-\frac{i}{N_{0,i}}}\right), i = n, p \tag{13}$$

Except for T, all other parameters in Eq.(13) are fit parameters.
Another important physical parameter is the ionization impact generation rate G, and it is formulated as $G=a_n n v_n + a_p p v_p$, where $v_{n,p}$ denotes the drift velocity. And $a_{n,p}$ is described by many models, in which vanOverstraeten-deMan model is proved to be the best. In this model, $a_{n,p}$ is formulated as:

$$\alpha(F) = \gamma a e^{-\frac{\gamma b}{F}},\ \text{with}\ \gamma = \frac{\tanh\left(\frac{h\omega_{op}}{2kT_0}\right)}{\tanh\left(\frac{h\omega_{op}}{2kT}\right)} \tag{14}$$

Two coefficients a and b are used for high and low ranges of electric field. And low electric field and high electric field are distinguished by a parameter E_0 whose default value is 4×10^5 V/cm. In low range of electric field below E_0, the values a(low) and b(low) are applied, while in high range of electric field above E_0, the values of a(high) and b(high) are used. The parameter $h\omega_{op}$ represents the optical phonon energy.
As the physical model has been chosen, the fit parameters mentioned above should be modified. And then the simulation can be carried out. In the simulation, the most difficult problem we may face is the convergence problem. Next, convergence problems and solutions will be proposed.
In our simulation practice, it is found out that convergence problems are mostly caused by five factors: 1) Not enough iteration times. 2) Bad initial guess. 3) Bad mathematic calculation method. 4) Coarse mesh or bad boundary shape. 5) Bad parameter set of physical models.

Fig.2 shows the simulation flow of the device simulator. The parameters, "Notdamped" and "Iterations", dominate when the simulation will be terminated. Therefore, too small values for these two parameters will induce abnormal termination. However, this case rarely happens because the default values for these two parameters are big enough in most times.

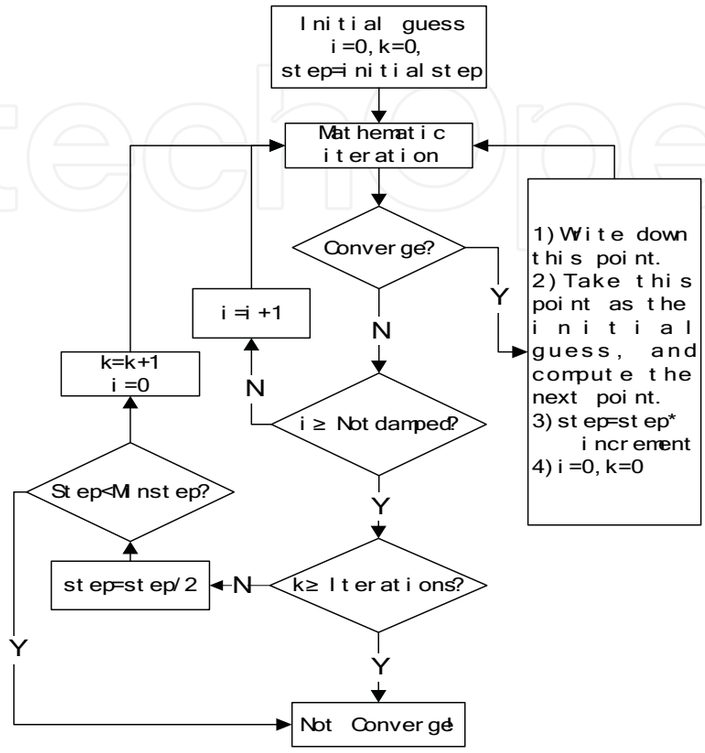


Fig. 2. Device simulation flow

From Fig.2, it is easy to find that all calculations are based on an initial guess. And a bad initial guess will surely induce convergence problem. This case often happens on two occasions. Sometimes, the simulation should be divided into subsections, and in some regions small value for "initialstep" should be used to obtain a good initial guess while in other regions large value for "initialstep" should be used to save time. And a mistaken use of large value for "initialstep" may induce the first point failing to converge. To prevent this convergence problem, the simulation should be divided into subsections in a reasonable way. Meanwhile, large initial voltage imposed on electrodes will also bring on convergence problems. Therefore, another simulation method is necessary. We can set the initial voltage at the electrode to 0 V, and then ramp the voltage to the value we need. In this way, a good convergence will meet. The commands in Fig.3a will cause convergence problems in a great probability while commands in Fig.3b always provide good convergence.

In the snapback region of ESD protection structure, the current increase rapidly. Thus, in the simulation, a small ΔV will induce a large ΔI which induces the simulation failing to converge. Aiming at soling this problem, a particular simulation method is provided in the simulator as shown in Fig.4. A series resistor is put together with the ESD protection structure. Therefore, the current can be written as: $I= (V_{out} - V_{internal})/R$, and in this way, a small ΔI can be gained, which will improve the convergence. In the simulation of ESD events, this method must be included, and generally the value for R is set to be larger than $1\times10^7\ \Omega$.

```
Electrode {
        { Name="drain" Voltage=0.0}
        { Name="source" Voltage=0.0 }
      { Name="gate" Voltage=5.0 }
        { Name="sub" Voltage=0.0 }
}
```

(a)

```
Electrode {
        { Name="drain" Voltage=0.0}
        { Name="source" Voltage=0.0 }
    { Name="gate" Voltage=0.0 }
        { Name="sub" Voltage=0.0 }
}
.....
Solve{.....}
Goal {name="gate" voltage=5.0V}
```

(b)

Fig. 3. (a) Commands hard to converge, (b) Commands with good convergence

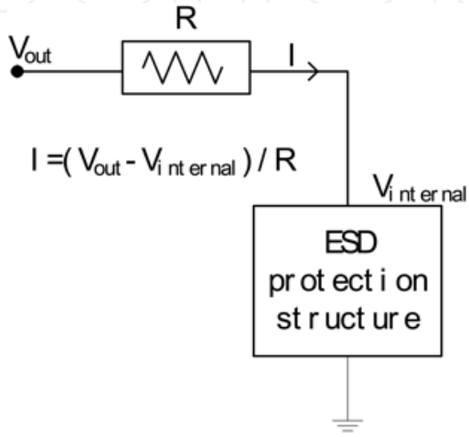
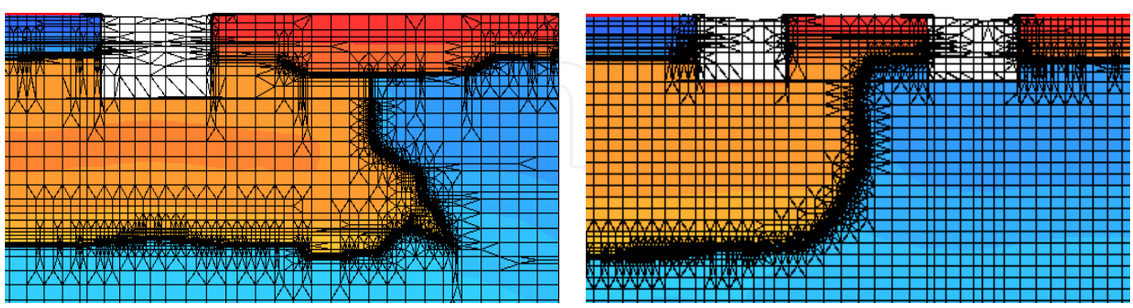


Fig. 4. ESD simulation method

Coarse mesh or bad boundary shape will also cause converge problems. Fig.5 shows the comparison of a bad boundary shape and a good boundary shape. A sharp-angled region can be found in Fig.5a which will cause convergence problem in the later device simulation. It is mainly caused by bad diffusion model and implantation model used in process simulation. It is found that pairdiffusion model used for diffusion and implantation tables based on Crystal-TRIM used for implantation always provide good boundary shape.



(a) (b)

Fig. 5. (a) Bad boundary shape, (b) Good boundary shape

Another reason for convergence problems is the bad parameter set for device simulation. A small value for the parameter "α" in Eq.(14) and a large value for the parameter "τ_{max}" in Eq.(12) may result in convergence problem, the current failed to increase near the breakdown region. In addition, a great difference between the values of "α" in low field

region and high field region may result the simulation failed to converge after it snapbacks, just as shown in Fig.6. When the curve snapbacks, the simulation will change from the high field condition to low field condition, and the sudden change of the value for "α" finally result in the convergence problem. Therefore, when modifying the parameters, great difference between *a*(low) and *a*(high), *b*(low) and *b*(high) is forbidden.

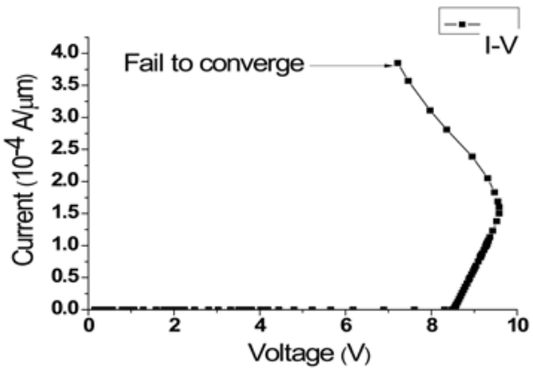


Fig. 6. Simulation fails to converge after the snapback happens

4. ESD simulation methods

There are three main methods to simulate the I-V characteristic of the ESD protection device: DC simulation, TLP simulation and mixed mode simulation. DC simulation provides the fastest simulation speed while it is confronted with the most serious convergence problem. TLP simulation method and mixed mode simulation method can both reflect transient characteristic of devices. In this section, DC simulation and traditional TLP simulation and their limitations will be illustrated. Then a new simulation method based on the traditional TLP simulation method is proposed, which can predict key parameters of ESD protection devices precisely. Mixed mode simulation will be illustrated separately, which is carried out in TSUPREM4/MEDICI environment, and the method to evaluate the effectiveness, the robustness, the speed, the transparency of ESD protection devices is proposed.

To illustrate DC simulation and TLP simulation method, a traditional LSCR (Lateral Silicon-controlled rectifier) shown in Fig.7 is considered, in which D1 is 1.5 μm, D2 is 0.5 μm, D3 is 0.6 μm, and D4 is 1 μm. Fig.8 is the doping profile which is simulated by DIOS, and the total concentration of different layers is shown in Table 2.

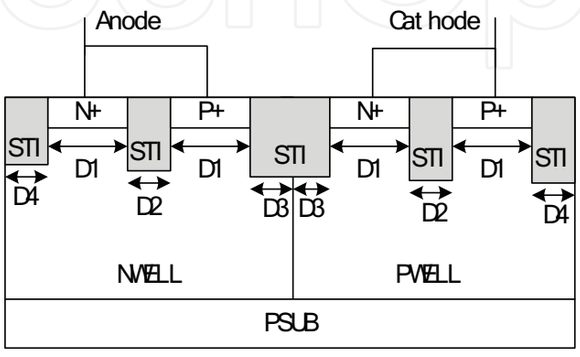


Fig. 7. A cross section of LSCR

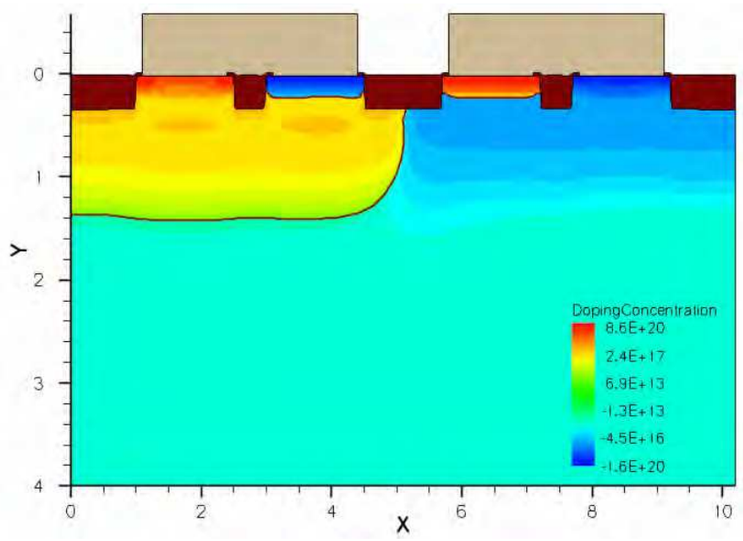


Fig. 8. Doping profile of LSCR

	PSUB	NWELL	PWELL	N+	P+
Total Concentration	1×10^{15}	3.7×10^{17}	2.6×10^{17}	5.1×10^{20}	2.4×10^{20}

Table 2. Total concentration of varies layers

Then, the structure obtained from the process simulation is imported into the device simulator. And the device simulation can be carried out in two ways. To evaluate the trigger voltage (V_{t1}), the holding voltage (V_h), and the second breakdown current (I_{t2}) precisely, selecting proper physical models and parameters is the key point. Table 3 lists the parameters modified in the simulation, and the parameters not mentioned in the table remain default. The value for parameter α mentioned in Eq.(14) determines V_{t1}, while the values for μ mentioned in Eq.(1) and τ mentioned in Eq.(11) are crucial for V_h.

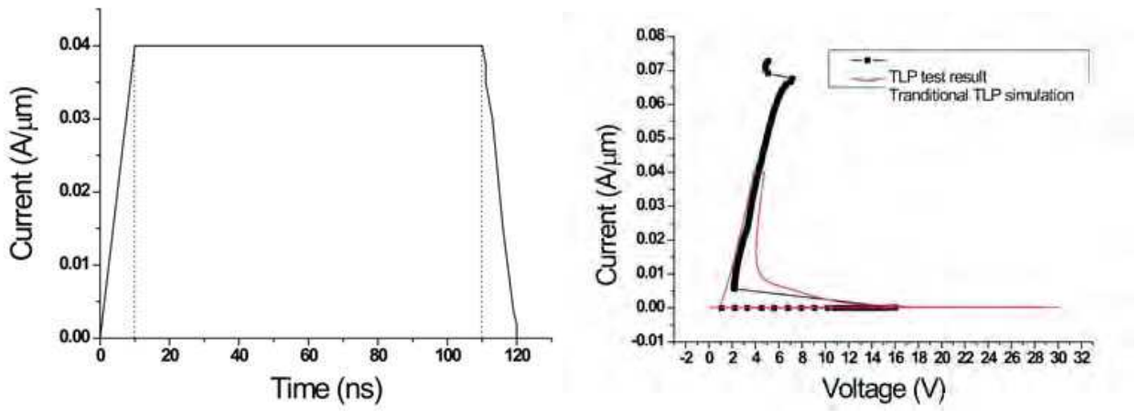
Parameter	Value	Value for electron	Value for hole	Mentioned in Eq.
b(low)	-	9.85×10^{5}	1.629×10^{6}	Eq.(13)
b(high)	-	9.85×10^{5}	1.354×10^{6}	Eq.(13)
F	1×10^{13}	-	-	Eq.(5)
Cr	-	9×10^{16}	1.5×10^{17}	Eq.(4)

Table 3. Parameter set in the simulation

Actually, traditional TLP simulation can not evaluate DC characteristic of ESD protection devices, due to the voltage overshoot. Fig.9 (a) shows the current pulse imposed on the devices simulated, and Fig.9 (b) shows the corresponding I-V curve, comparing with the TLP test result. From Fig.9 (b), we can see that the simulation result deviates from the test result a lot.

DC simulation can evaluate V_{t1} and V_h, but it can not evaluate I_{t2} precisely. DC simulation is based on the solving of thermal equilibrium equations, but in fact, there is no thermal equilibrium established in the structure when the ESD event happens. Therefore, DC simulation can no longer evaluate the characteristic of ESD events when the temperature

becomes much more than 300K. The non-equilibrium can only be described by a transient simulation. Fig.10 shows the result of DC simulation, together with the TLP test result.



(a) (b)

Fig. 9. (a) Current pulse imposed on the simulated structure (b) I-V characteristic obtained from TLP test and traditional TLP simulation method

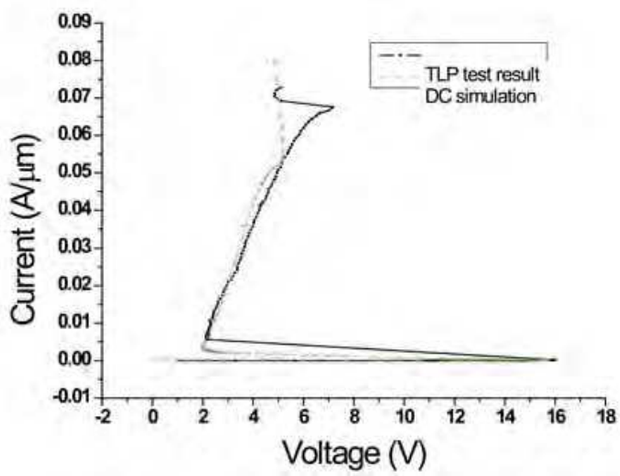
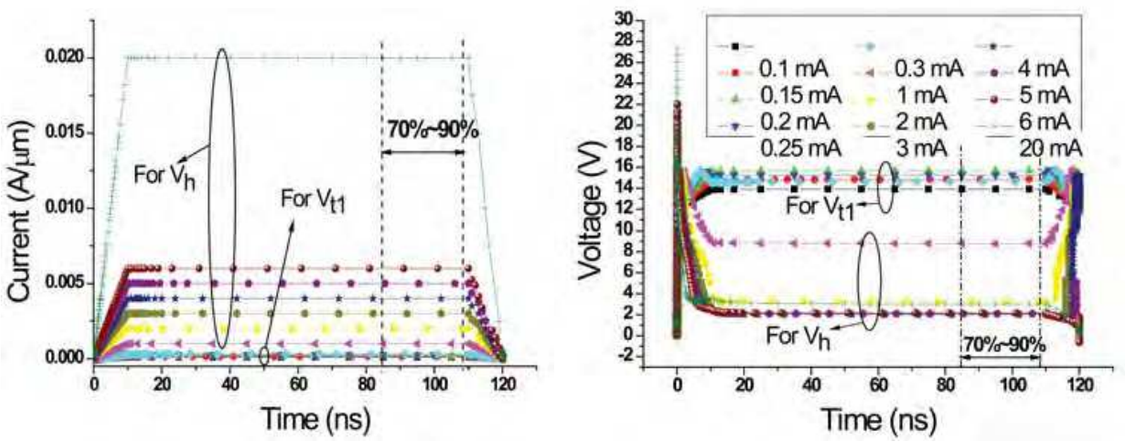


Fig. 10. Comparison of DC simulation and TLP test result

To evaluate the performance of ESD protection devices, Vt1, Vh, and It2 are all indispensable. Based on traditional TLP simulation, we propose a novel TLP simulation method, which can simulate all of the three parameters precisely. Firstly, we should make sure that this method can evaluate V_{t1} and V_h. As the novel TLP simulation begins, series of current pulses are imposed on the structure as shown in Fig.11 (a). The obtained voltage vs. time curves are shown in Fig.11 (b). Then average current value in the range of 70%~90% time for each I-t curve is calculated, and so is the average voltage value, the same as the TLP measurement works. Then each pair of voltage and current is plotted as a point in Fig.12. After connect these points together, comparing it with the tested results, it is found that they meet very well.

Table 4 lists the TLP test results and simulation results with DC simulation method and the novel TLP simulation method. We can see that DC simulation method and the novel simulation method provide almost the same result in terms of evaluating V_{t1} and V_h.



(a) (b)

Fig. 11. (a) Series of current pulses are imposed on the structure simulated, and average currents of the 70%~90% section of each curve are calculated, (b) Voltage vs. time curves are obtained from the simulation. And the average voltage of the 70%~90% section of each curve is calculated.

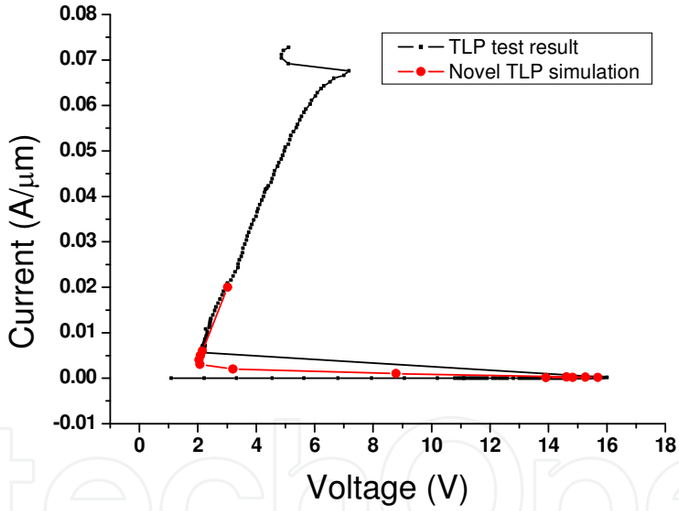


Fig. 12. Comparison of TLP test result and the novel TLP simulation result

	V_{t1}(V)	Absolute error (V)	Relative error	V_h(V)	Absolute error (V)	Relative error
TLP test	16	-	-	2.16	-	-
Novel TLP simulation	15.69	0.31	1.94%	2.03	0.13	6.02%
DC simulation	15.69	0.31	1.94%	2.02	0.14	6.48%

Table 4. Test result and simulation results

To evaluate I_{t2}, current pulses whose peak values are 0.04A, 0.05A, 0.06A, 0.066A, 0.068A, 0.07A, 0.08A, 0.09A are imposed on the structure, and several points obtained from

simulation, together with the points obtained before, the whole curve is shown in Fig.13, from which we can see that that as the current arrive 0.066A, the voltage comes back. And this current is treated as I_{t2}.

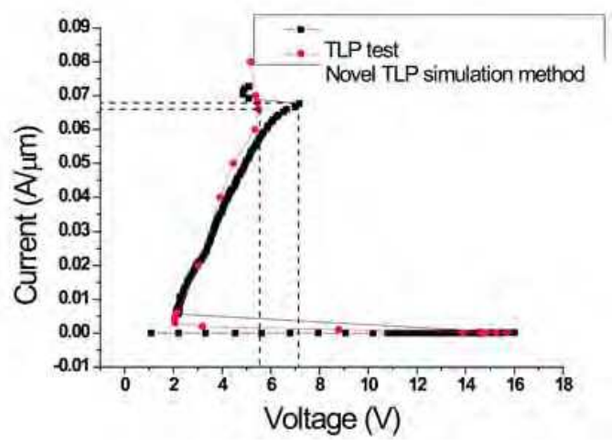


Fig. 13. I_{t2} obtained from novel TLP simulation and that from TLP test

We can also evaluate I_{t2} by the maximum temperature in the structure, as thermal breakdown is caused by high temperature ultimately. After the simulation, we can obtain T_{max} vs. time curves, as shown in Fig.14. When the maximum value of T_{max} exceeds the melting point of Si (1687 K), it can be judged that thermal breakdown happens. From Fig.14, we can see that I_{t2} is about 0.064 A.

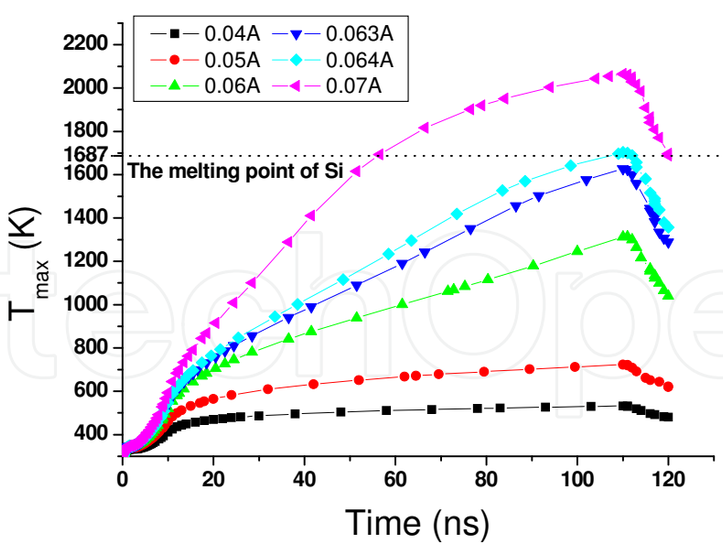


Fig. 14. Maximum temperature in the structure vs. time curves when series of current pulses are imposed on the structure.

Table 5 lists the test result, the result simulated with the novel TLP simulation method and judged by the voltage's snapback, and the result simulated with the novel TLP simulation method and judged by the maximum temperature in the structure.

	I_{t2}(A/μm)	Absolute error(A/μm)	Relative error
TLP test	0.068	-	-
Judged by voltage's snapback	0.066	0.002	2.94%
Judged by maximum temperature	0.064	0.004	5.88%

Table 5. Test and simulation results

From the discussion above, we can conclude that the most effective and fastest way to evaluate the performance of ESD protection devices is to evaluate V_{t1} and V_h with DC simulation method, and evaluate I_{t2} with the novel TLP simulation method introduced above.

Next, the mixed mode simulation method is introduced, taking the CDM model for example. The equivalent circuit of CDM model is shown in Fig.15. The device to be evaluated is a MLSCR, as shown in Fig.16, and the doping profile gained by simulation with TSUPREM4 is shown in Fig.17.

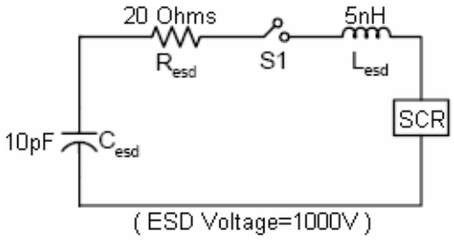


Fig. 15. Equivalent circuit of CDM Model

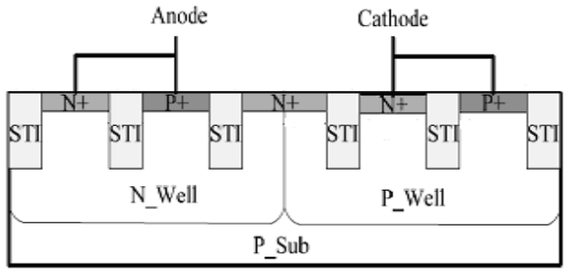


Fig. 16. A cross section of MLSCR

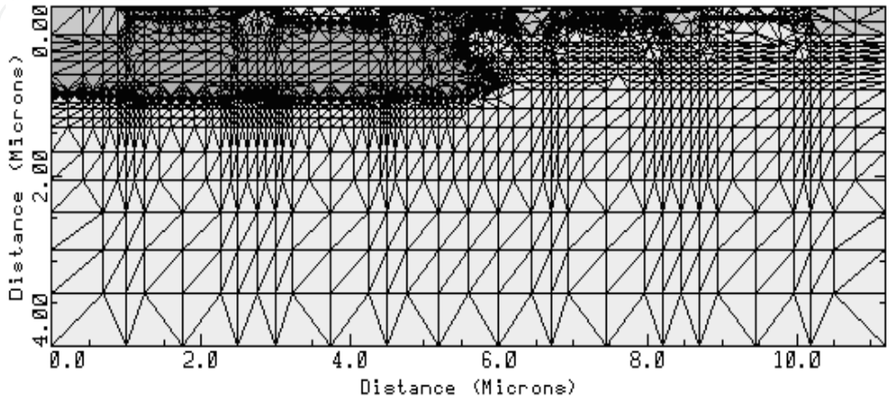


Fig. 17. Doping profile of MLSCR

4.1 Effectiveness evaluation

From the current vs. time curve gained from the mixed mode simulation, as shown in Fig.18, we can see that the ESD current is completely released through the device in 2.5 ns. This time and the peak current at the T_{imax} point reflect the effectiveness of the device. Smaller value of the time and larger peak current mean that the device can release larger current in smaller time, in other words, the device is more effective.

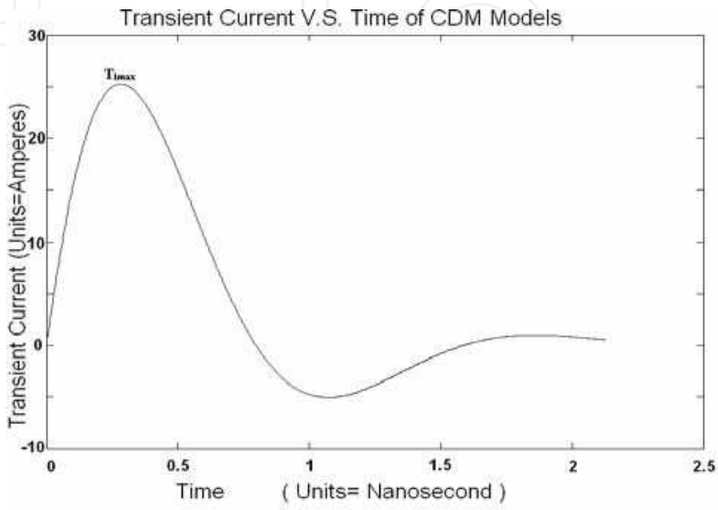


Fig. 18. Current vs. time curve

4.2 Speed evaluation

From the voltage vs. time curve shown in Fig.19, we evaluate the speed using the recover time. The recover time is defined as the time that the device voltage quickly rises and then returns to the normal working voltage, which is described as the $T_{recover}$ in Fig.19. The smaller value of $T_{recover}$ shows that the ESD protection device can make faster reaction to the electrostatic signal.

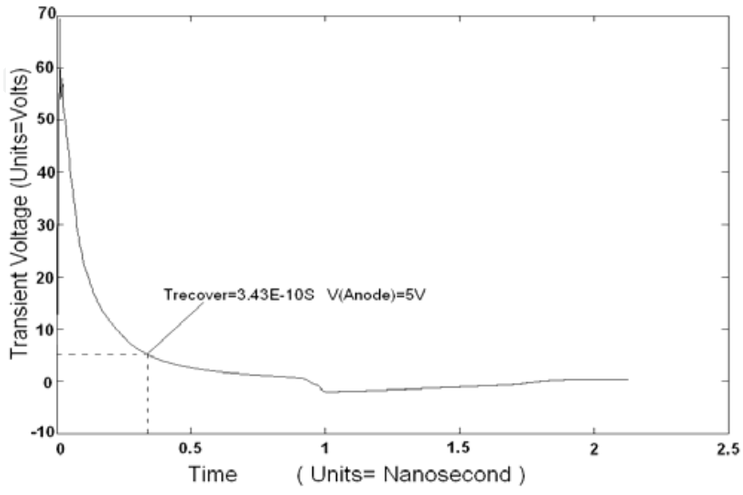


Fig. 19. Voltage vs. time curve

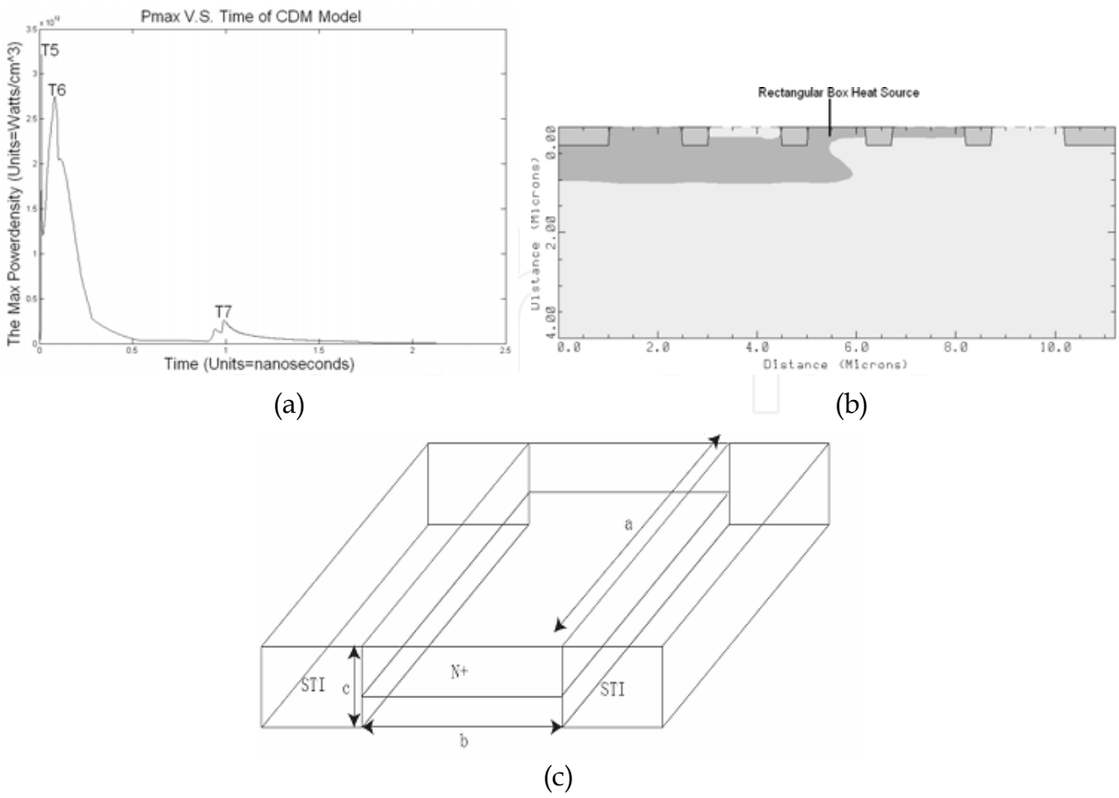


Fig. 20. (a) Pmax-t, (b) Rectangular box heat source model (Zoom out), (c) Rectangular box heat source model (Zoom in)

4.3 Robustness evaluation

There are mainly two aspects should be considered when evaluating the robustness: the first one is to inspect whether the electro thermal characteristics become uncontrollable, when the instantaneous power of ESD comes to the maximum (P_{max}); the second one is to inspect the power distribution in the ESD protection device when the ESD event happens. Taking advantage of the P_{max}-t curve in Fig.20 (a) and the rectangular box heat source model of Ajith Amerasekera, a modified rectangular box heat source model is proposed to evaluate the robustness of the SCR protection device. In the modified model, the power is supposed to be concentrated in a cuboid whose three side lengths are a, b and c respectively, as shown in Fig.20 (b) and Fig.20 (c). Define $P_{normalized}(t)$ as $(\int_{t=0}^{\tau=t} P_{max}(t)\partial t)/t$, the power instilled into the SCR device is $P(t)=abcR(t)P_{normalized}(t)$, where R(t) is a fitting parameter ($0<R(t)<1$), and $R(t)P_{normalized}(t)$ is the average power density of the rectangular source heat source. The relationship between the temperature difference $\Delta T(t)$ (at this time, the highest temperature $T_{max}=T0+\Delta T$, T0 is the initial temperature, T_{max} is the highest temperature) and P(t) is a subsection function depicted in equations (15) to (18):

$$P = \frac{\rho abc C_p \Delta T}{t} \quad (0 \le t < t_c) \tag{15}$$

$$P = \frac{ab\sqrt{\pi K \rho C_p}\Delta T}{\sqrt{t} - \sqrt{t_c}/2} \quad (t_c \le t < t_b) \tag{16}$$

$$P = \frac{4\pi K a \Delta T}{\log_e(t/t_b) + 2 - c/b} \quad (t_b \le t < t_a) \tag{17}$$

$$P = \frac{2\pi K a \Delta T}{\log_e(a/b) + 2 - c/2b - \sqrt{t_a/t}} \quad (t \ge t_a) \tag{18}$$

In these equations, K is the thermal conductivity, C_p is the specific heat capacity, $D = K/\rho C_p$, ρ is the density of silicon, $t_c = c^2/4\pi D$, $t_b = b^2/4\pi D$, $t_a = a^2/4\pi D$, and K, C_p, and $\rho$is dependent on the process. Therefore we can calculate the highest temperature at every time point, and then calculate the heat produced carriers n_d caused by highest temperature. If n_d extends the background impurity concentration, the robustness of this device cannot meet the need. The transform equation is depicted in Eq.(19):

$$n_d = 1.69 \times 10^{19} \exp\left(\frac{-6.377 \times 10^3}{T\max}\right) \cdot \left(\frac{T\max}{300}\right)^{3/2} \tag{19}$$

The method to estimate whether the device enters electro thermal uncontrollable condition through the curve of P_{max}-t, as mentioned above can also be quickly implemented by mathematic project software such as Matlab.

The inside power distribution profiles of the ESD protection device when ESD event happens can reflect the robustness of the device. An ESD protection device with strong robustness should spread the inner power as dispersive as possible, especially when the power extremum is very large. Fig.21 shows the power distribution when the power comes to its peak.

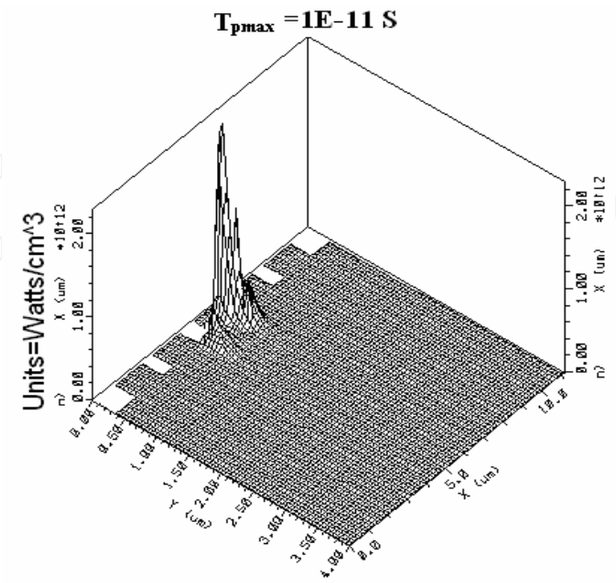


Fig. 21. The power distribution when the power comes to its peak

4.4 Transparency evaluation

We can inspect the leak currents on 0 to 1.2 VDD bias voltages when evaluating DC transparency (depicted in Fig.22 (a)). We need to inspect the leak current under I/O signal frequency when evaluating the transparence of AC signal. (Take 100K rectangular wave as example, see Fig.22 (b)). The leak current under frequency signal is larger than that under DC voltage, which is mainly caused by high frequency couple effect.

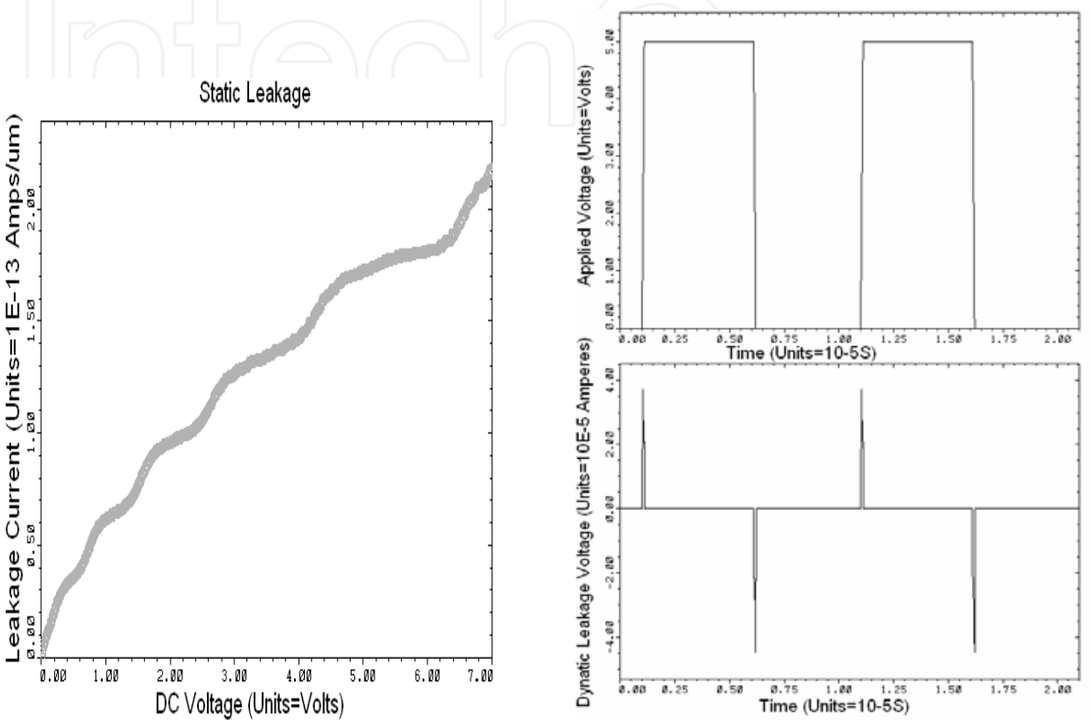


Fig. 22. (a) DC leakage current of the SCR-based ESD protection device, (b) Leakage current of the SCR-based ESD protection device under 100K frequency signal

4.5 Overall evaluation

At the last, we can obtain the transient curve [I(t),V(t)] which describes the entire ESD event as shown in Fig.23, from which we can make a comprehensive evaluation on the effectiveness, speed, robustness and transparency of the ESD protection device. T0 < T3 = T5 < T6 < T7 < T1 < $T_{recover}$ < T4 < T2. The current value at T1 reflects the effectiveness of the ESD protection device. $T_{recover}$ reflects the trigger speed of the ESD protection device. The hyperbola family in this figure represents the power of the ESD protection device, and the distance from the hyperbola family to the origin reflects the robustness of the ESD protection device. Besides, the power density extremum also reflects the robustness of the ESD protection device. When time is 1E-11 S, the max power density of the device comes to the peak. The current when the device first comes to 5V in an ESD event reflects the transparency of the ESD protection device. An ideal transient curve of an ESD protection device should be close to the vertical axis with most of the points staying on the left of the line V=VDD.

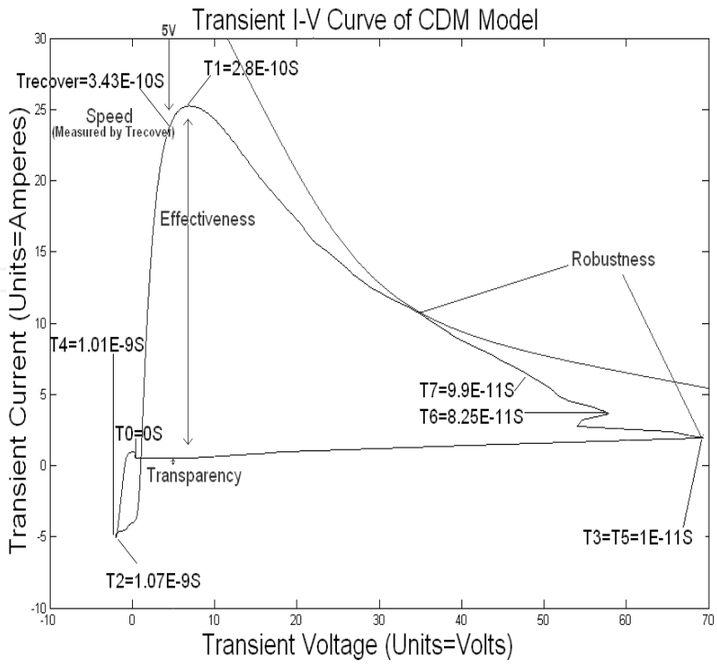


Fig. 23. Ransient I(t) versus transient V(t) of SCR-based ESD protection device

5. ESD protection element characteristic evaluation based on SPICE simulation

5.1 SPICE Simulation based design-transient power clamp

As technology is scaling down, the gate oxide is shrinking and becoming more vulnerable to ESD. The resistance of the routing rail metal increases apparently with the technology advances. Traditional rail-based static ESD power clamp protection (Fig.24) is more challenge. Transient power clamp, which consists of a RC network based detection circuit and the main ESD device NMOS (Fig.25), is becoming more and more attracting for their fast turn-on speed and low turn-on voltage. The key advantage of the transient power clamp is the capability with the SPICE simulation, which enables the optimization in the pre-silicon phase. A major drawback of the transient power clamp is the large RC network, needed to trigger the main protection device, will response any fast event on the power rails.

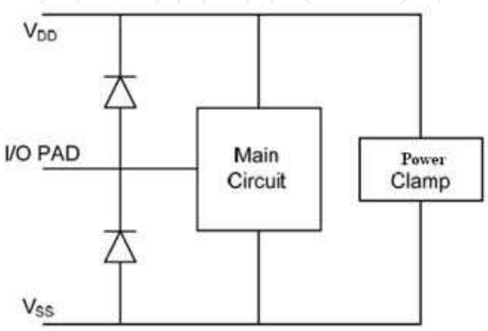


Fig. 24. Rail-based ESD protection scheme with power clamp

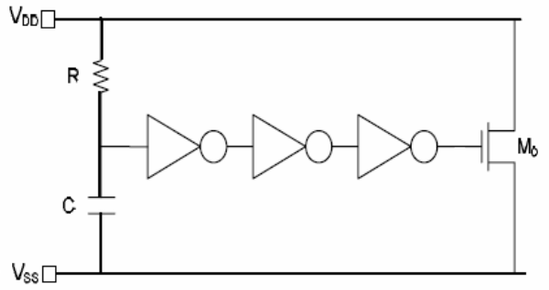


Fig. 25. Three-stage inverter based transient ESD power clamp

The transient power clamp uses the RC network to detect the ESD event and turns on the main ESD protection device NMOS (Fig.25), to shunt the ESD event on the supply pin. The main NMOS conducts the ESD current through the channel and this can be simulated in the SPICE. As the peak current of the HBM is around the orders of amperes, the main NMOS needs to be large enough to shunt the ESD current safely. It is always about millimeter. In normal condition, the gate of the NMOS is low and the main protection device is off. The rise time of ESD event is between 100ps and 60ns.However, the rise time of power up is about millisecond range. In order to keep the main protection device on, the RC constant is set to larger than the duration of the ESD event, which is about 1μs for HBM ESD stress, and shorter than the rise time of power on. The typical value of RC time constant is 1μs. The large RC time constant not only consumes large silicon area but also leads susceptibility to the power bus noise.

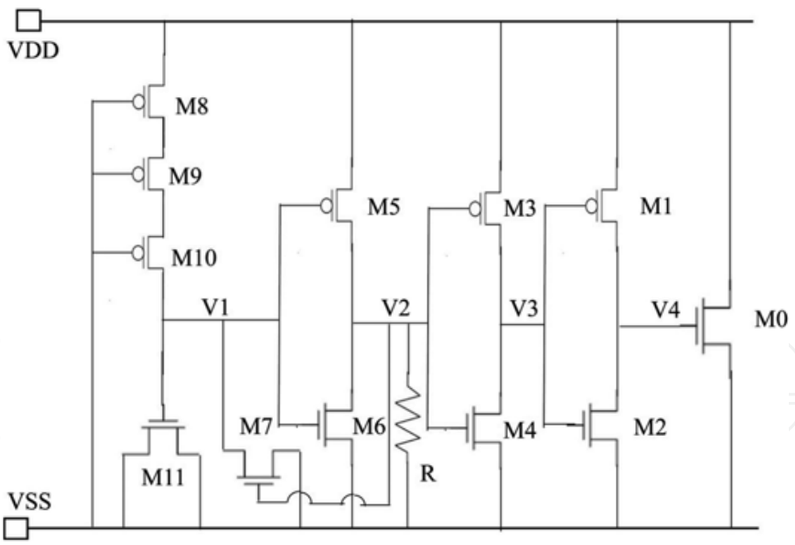


Fig. 26. Proposed three-stage inverter based ESD power clamp with feedback

The M0 is the main protection NMOS to shunt the ESD current.M1~M6 consist of the three stage inverter. The signal at the node V1 transfers through the three stage inverter to control the gate of main device M0. M8~M10 consist of the resistor M11 is the NMOS capacitor. M7 is the feedback NMOS and R is the pull-down resistor. In normal conditions, the node V1 charge up to VDD and V2 is low. The pull-down resistor R confirms the node to couple to VSS. This ensures the feedback NMOS is in its off state. And the voltage at node V2 transfers

through two stage inverter to ensure the node V4 is Low. And the M0 is in off. The low voltage at the node V4 enables the reduction in the leakage of M0.In ESD conditions, because of the RC delay, the voltage at the node V1 is low. The M5 is on and the node V2 is charge to VDD. The high voltage in V2 enables the feedback NMOS M7.The M7 pulls the node of V1 to VSS. And the low voltage at the node V1 enhances the pull-up of the POMS M5.The high voltage at node V2 transfers through two stage inverter and enables the M0.The main protection device M0 shunts the ESD current. The feedback significantly increases the time to keep V4 in high voltage. So the RC time constant can be reduced significantly which translates into reduction in the silicon area. The most advantage is the smaller RC time constant reduces the susceptive to the fast transient event on the power lines. In the design, the specific dimension of the RC network is list in Table 6.

Device	Dimension
M8	W/L=7.12um/0.4um
M9	W/L=7.12um/0.4um
M10	W/L=7.12um/0.4um
M11	W/L=1.4um/3.5um

Table 6. RC network device dimension

The power clamp is simulated in the Cadence Specture environment. A simplified RC network (Fig.27) is to simulated the HBM ESD event. The switch SW1 and SW2 are voltage controlled switch. When SW2 is on and SW1 is off, the C1 is charge through the voltage source V2 before 1ns.After 1ns, the switch SW1 is on and SW2 is off, the capacitor discharge through the 1.5k resistor R2 to the power clamp.

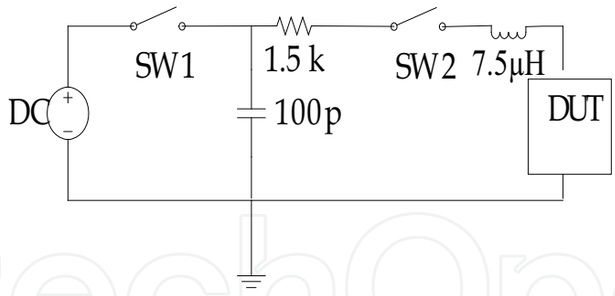


Fig. 27. The simplified RC network to simulated HBM ESD event.

The simulated result of the transient power clamp under a 5kV HBM ESD event in 90nm process is shown in Fig.28.The width of the main protection device M0 is 3000μm. The breakdown voltage of gate oxide for 1.0V core device is about 5V in DC condition. The transistor in the power clamp is 1.8V devices to reduce the leakage. The breakdown voltage of gate oxide for 1.8V device is about 9.5V in DC condition. From the simulated results, the voltage at the gate of the M0 is smaller than the breakdown voltage 9.5V. And the NMOS keeps on state at almost 1μs.The voltage at the VDD rail is also smaller than 9.5V.The NMOS can safely shunt the 5KV HBM ESD current.

To evaluate the immunity to the fast transient, a fast power on 100μs pulse with a rise time of 10μs and a fall time of 10μs is applied at the power clamp. The pulse voltage is 1.8V. The voltage response is shown is Fig.29.The peak voltage at node 4 is 0.05V and it keep almost

0V at most time. So the main NMOS in is off state. And the power clamp is immunity to the fast transient power on.

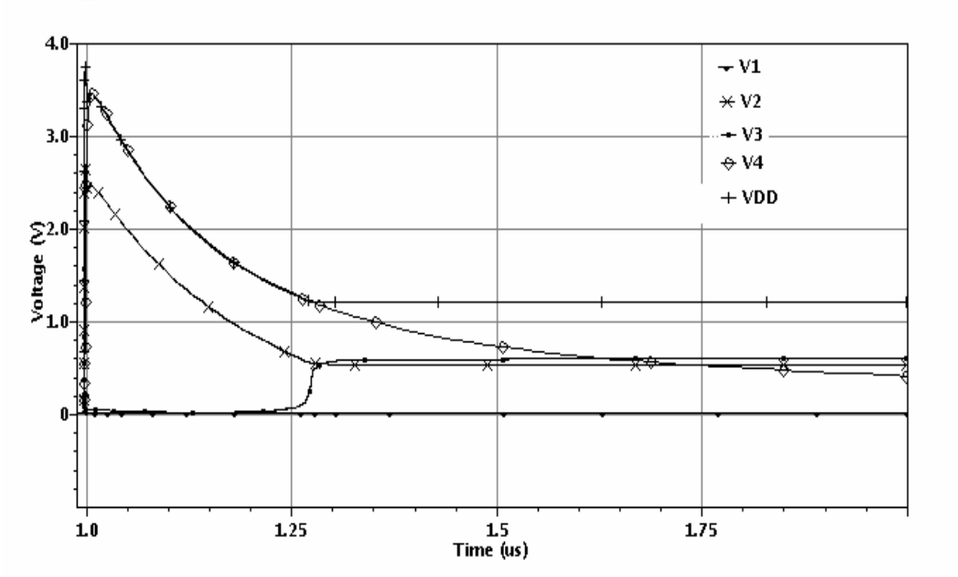


Fig. 28. Simulated voltage at the different node under 5KV HBM ESD event

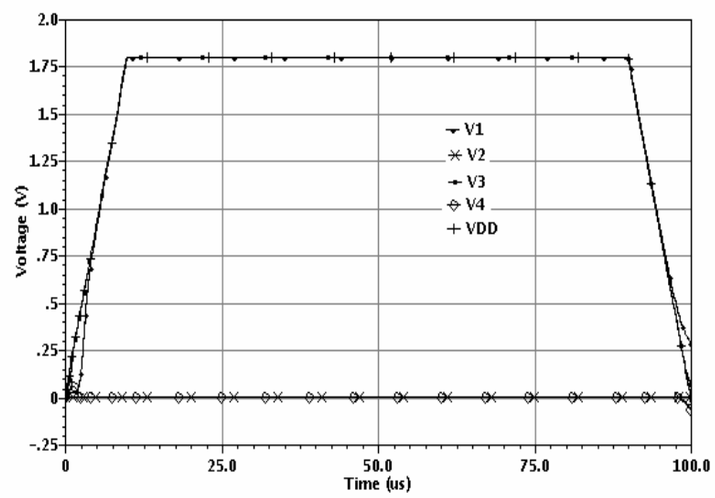


Fig. 29. Simulated voltage at the different node at fast power on state

TLP like pulse with rise time of 10ns and fall time of 10ns and pulse with 100ns is stressed at the power clamp. The pulse voltage is 1.8V. The results are shown in Fig.30. The voltage at node V4, which transfers after three-stage inverter, is a square like pulse. This ensures the main NMOS is on in the pulse width and can shunt the ESD current safely.

The SPICE simulation based transient power clamp is compatibility with the normal SPICE simulation. This enables an early optimization phase in a pre-silicon state. The transient power clamp responds to any fast transient event. An example of the transient power clamp is introduced in the 90nm CMOS process to show the design flow. The susceptibility to fast power on issue is addressed in the example. From the simulation result, the power clamp can achieve a level of 5KV HBM ESD without suffering mistriggering from fast power on.

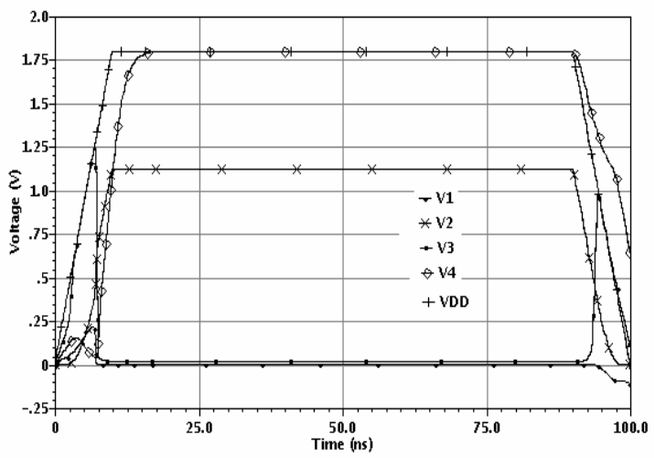


Fig. 30. Simulated voltage at the different node at TLP like pulse

5.2 Triggering characteristic evaluation

SCR is an efficient ESD protection device in integrated circuit area. In order to estimate the ESD device performance, including trigger voltage (Vt1), holding voltage (Vh), failure current (It2), a lot of research are spent base in TCAD simulation. However, a precise evaluation method does not exist as the high ESD current model is not support in spice model. Therefore, a desirable technique is in need to evaluating the ESD device performance in ESD protection device design process. In this section, a new technique is proposed to evaluate the trigger voltage of SCR base in spice simulation.

5.2.1 SCR triggering characteristic evaluation

The equivalent schematic of SCR is showed in Fig.31, which consists of Bipolar junction transistor PNP and NPN. The left part of Fig.31 is an ESD voltage pulse generation circuit. There are different ways to trigger a SCR, including voltage-triggering by slowly stepping up Vac(voltage of anode to cathode) or using a dV/dt transient, and current-triggering by injecting seeding currents from the base of PNP or NPN. A current source is employed to regard as the base current of NPN when the SCR occurring avalanche breakdown. The SCR will turn to latch up state once the base current reaches a value which induces the inside feed back of SCR occurring. The simulation results are showed in Fig.32. As Fig.2 shows, the SCR reaches latch up state when the base current of NPN is 1.3mA.

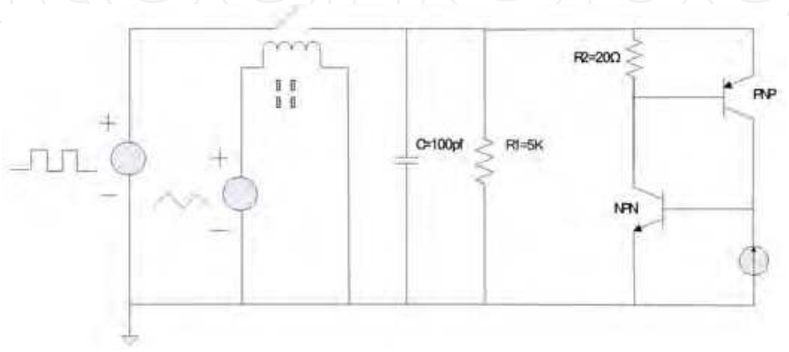


Fig. 31. ESD voltage pulse generation circuit and equivalent schematic of SCR

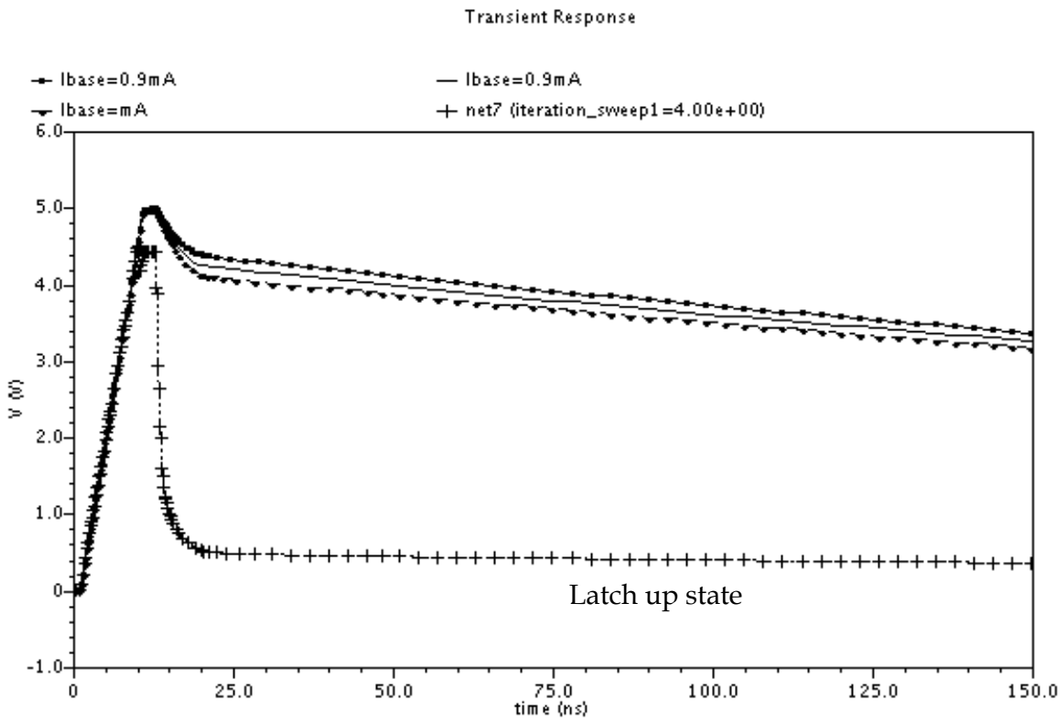


Fig. 32. Simulation results of normal SCR triggering characteristic

5.2.2 Darlington SCR triggering characteristic evaluation

Increasinig the common-base current gains βof PNP and NPN can make for reducing the trigger voltage of SCR. A Darlington SCR configure is showed in Fig.33. The Q2 and Q3 form to a Darlington transistor, which equates to a NPN transistor here. A current source is also employed to emulate base current as above SCR simulation. The simulation results are showed in Fig.34. SCR turns to latch up state when the base current achieves 0.37mA which is almost one third of normal SCR. In other words, the Darlington configured SCR needs less base current to trigger the SCR into latch up and, therefore, low breakdown voltage to keep the NPN operation. The triggering characteristics of normal SCR and Darlington SCR are showed in Fig.35 when the base current of NPN is 0.37mA.

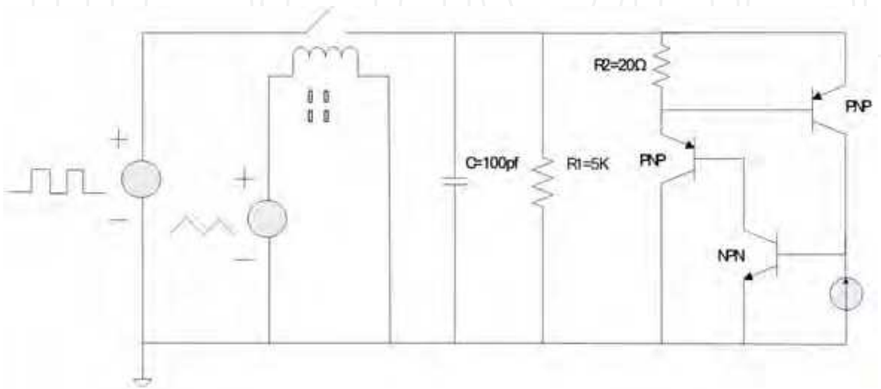


Fig. 33. ESD voltage pulse generation circuit and equivalent schematic of Darlington SCR

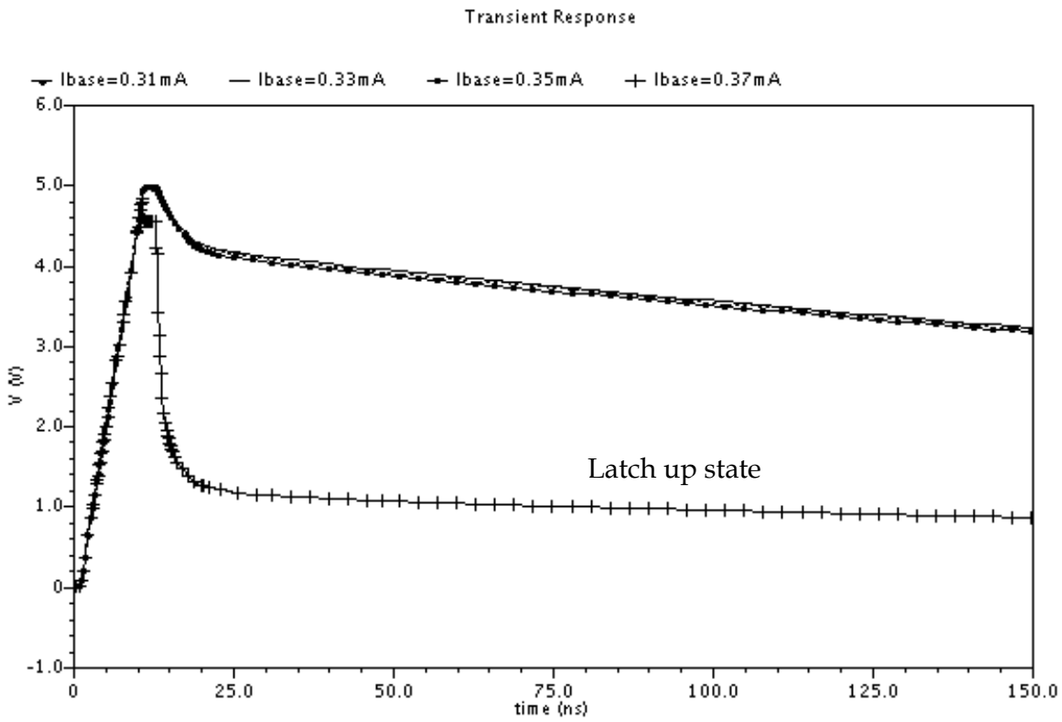


Fig. 34. Simulation results of Darlington SCR triggering characteristic

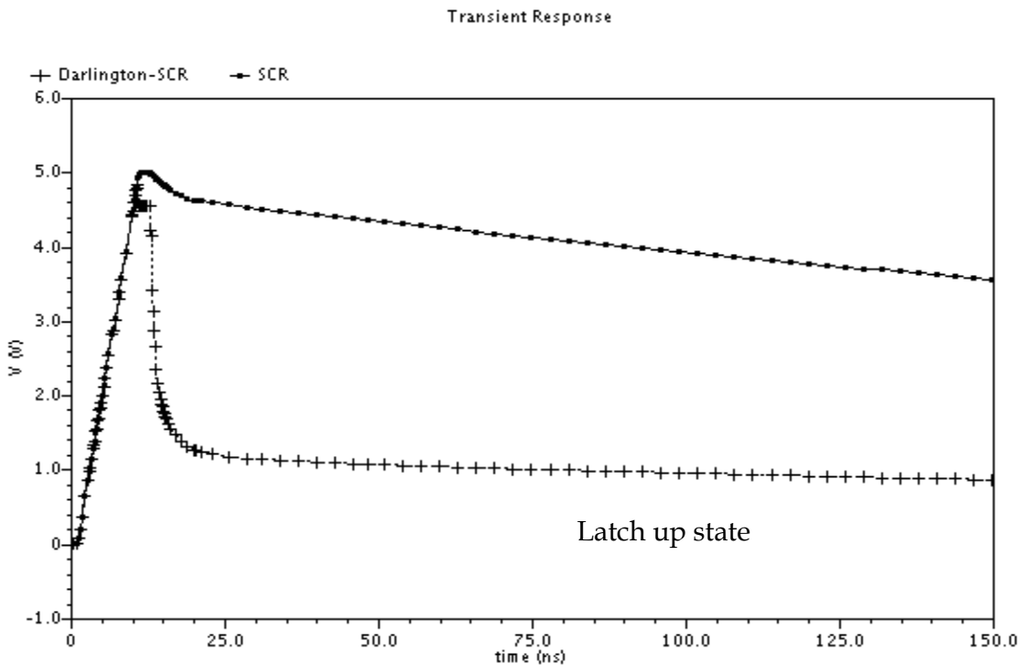


Fig. 35. Trigger characteristic comparison of normal SCR and Darlington SCR when the base current is 0.37mA

6. Acknowledgements

The authors would like express thanks to our students: M.S.E candidates Dahai Huang, Mingliang Li and D.E. candidate Bo Song, Qiang Cui for their help in writing the first draft.

7. References

[1] Ajith Amerasekera (2002). *ESD in Silicon Integrated Circuits.* JOHN WILEY & SONS

[2] Bin Li (2006). An ESD Protection Device Simulation Design Methodology based on MEDICI. *ICSICT 2006*, 2:1358-1360.

[3] Amerasekera A. (1991) .Characterization and modeling of second breakdown in NMOST's for the extraction of ESD-related process and design parameters. *ElectronDevices, IEEE Transactions*,38: 2161-2168

[4] Javier A. Salcedo (2007). TCAD Methodology for Design of SCR Devices for Electrostatic Discharge (ESD) Applications. *Electron Devices, IEEE Transactions* .54:822-832

[5] Salamero C (2006) . TCAD Methodology for ESD Robustness Prediction of Smart Power ESD Devices. *Device and Materials Reliability, IEEE Transactions*. 6:399-407

[6] Salamero, C (2005). Efficient TCAD methodology for ESD failure current prediction of smart power ESD protection. *Power Semiconductor Devices and ICs, 2005*. 115–118

[7] Amerasekera. A (1993). Prediction of ESD robustness in a process using 2D device simulations. *Reliability Physics Symposium*, 161-167

[8] Hillkirk (2003). Investigation of thermal breakdown mechanism in 0. 13um technology ggNMOS under ESD conditions. *Simulation of Semiconductor Processes and Devices*,125-128

[9] Tremouilles D. (2002). TCAD and SPICE modeling help solve ESD protection issues in analog CMOS technology, *Microelectronics, 2002. MIEL 2002. 23rd International Conference* 2: 749 – 752

[10] Amerasekera A (1994). Electrothermal behavior of deep submicron nMOS transistors under high current snapback (ESD/EOS) conditions. *Electron Devices Meeting, 1994. Technical Digest.*, 455 – 458

[11] Cui, Q., Dong, S.R., Liou, J.J., Han, Y., 2008. Robustness Evaluation of ESD Protection Devices in NEMS Using a Novel TCAD Methodology. Proceedings of the 3rd IEEE Int. Conf. on Nano/Micro Engineered and Molecular Systems., Sanya, China.

[12] DESSIS User's Manual, Integrated Systems Engineering AG, Switzerland, 2004.

[13] DIOS User's Manual, Integrated Systems Engineering AG, Switzerland, 2004.

[14] Esmark, K., 2001. Device Simulation of ESD Protection Elements. PhD Thesis, University of Hamburg, Germany.

[15] Fankhauser, B. and B. Deutschmann (2004). Using device simulations to optimize ESD protection circuits. Electromagnetic Compatibility, 2004. EMC 2004. 2004 International Symposium on.

[16] Feng, H.G., Chen, G., Zhang, R.Y., Wu, Q., Guan, X.K., Xie, H.L., Wang, A.Z., Gafiteanu, R., 2003. "A mixed-mode ESD protection circuit simulation-design methodology." Solid-State Circuits, IEEE Journal of 38(6): 995-1006. [doi: 10.1109/JSSC.2003.811978]

[17] Fichtner, W., Esmark, K., Stadler, W., 2001. TCAD Software for ESD On-Chip Protection Design. Electron Devices Meeting, 2001. IEDM Technical Digest. International. Washington, DC, USA. [doi: 10.1109/IEDM.2001.979493]

[18] Huang, C. Y., 2005. "Simulation prediction of electrothermal behaviors of ESD N/PMOS devices." Solid State Electronics 49(12):1925-1932.[doi:10.1016/j.sse.2005.08.016]

[19] Jiang, L.,Yang, X., Wang, J.J., 2001. Simulation models of ESD event in ICs. Solid-State and Integrated-Circuit Technology, 2001. Proceedings. 6th International Conference on.

[20] Li, B., Li, R.Y., Luo, H.W., 2006. An ESD Protection Device Simulation-Design Methodology based on MEDICI. Solid-State and Integrated Circuit Technology, 2006. ICSICT '06. 8th International Conference on.

[21] Salcedo, J.A., Liou, J.J., Liu, Z.W., Vinson, J.E., 2007. TCAD Methodology for Design of SCR Devices for Electrostatic Discharge (ESD) Applications. IEEE Transactions on Electron Devices. [doi: 10.1109/TED.2007.891251]

[22] Salaméro, C., Nolhier, N., Gendron, A., Bafleur, M., Besse, P., Zécri, M., 2006. TCAD Methodology for ESD Robustness Prediction of Smart Power ESD Devices. IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY. [doi: 10.1109/TDMR.2006.881483]

[23] Stricker, A.D., Mettler, S., Wolf, H., Mergens, M., Wilkening, W., Gieser, H., Fichtner, W., 1999. Characterization and optimization of a bipolar ESD-device by measurements and simulations. Microelectronics Reliability. [doi: 10.1109/EOSESD.1998.737049]

[24] Voldman, S., W. Anderson, et al., 2001. "A strategy for characterization and evaluation of ESD robustness of CMOS semiconductor technologies." Microelectronics Reliability 41(3): 335-348. [doi:10.1109/EOSESD.1999.819064]

[25] Wang, A. Z., Tsay, C., Lele, A., Deane, P., 1998. "A study of NMOS behavior under ESD stress: simulation and characterization." Microelectronics Reliability 38(6-8): 1183-1186. [doi: 10.1016/S0026-2714(98)00117-6]

[26] K. Esmark, H. Gossner, and W. Stadler, Advanced simulation methods for ESD protection development: Elsevier Science, 2003.

[27] R. Merrill and E. Issaq, "ESD design methodology," in *Proc EOS/ESD Symp*, 1993, pp. 233-237.

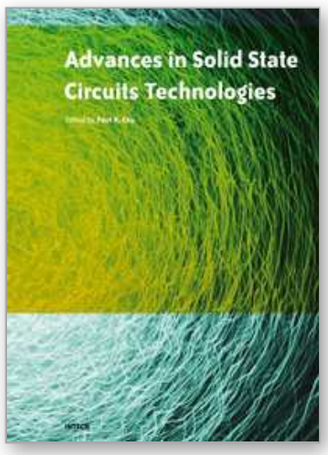
[28] S. Dabral, R. Aslett, and T. Maloney, "Core clamps for low voltage technologies," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium*, 1994, pp. 141-149.

[29] C. A. Torres, J. W. Miller, M. Stockinger, M. D. Akers, M. G. Khazhinsky, and J. C. Weldon, "Modular, portable, and easily simulated ESD protection networks for advanced CMOS technologies," *Microelectronics Reliability,* vol. 42, pp. 873-885, 2002.

[30] J. C. Smith and G. Boselli, "A MOSFET power supply clamp with feedback enhanced triggering for ESD protection in advanced CMOS technologies," *Microelectronics and Reliability,* vol. 45, pp. 201-210, 2005.

[31] M. D. Ker and C. C. Yen, "Investigation and Design of On-Chip Power-Rail ESD Clamp Circuits Without Suffering Latchup-Like Failure During System-Level ESD Test," *IEEE Journal of Solid-State Circuits,* vol. 43, p. 2533, 2008.

[32] H. Sarbishaei, O. Semenov, and M. Sachdev, "A transient power supply ESD clamp with CMOS thyristor delay element," in *29th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), 2007. EOS/ESD*, 2007, pp. 7A.3-1-7A.3-8.
[33] Ajith Amerasekera, ESD in silicon integrated circuits, John wiley & Sons, LTD, 1992.
[34] Albert Z.H.Wang, On-chip ESD protection for integrated circuits, Springer, 2002.



Advances in Solid State Circuit Technologies

Edited by Paul K Chu

ISBN 978-953-307-086-5
Hard cover, 446 pages
Publisher InTech
Published online 01, April, 2010
Published in print edition April, 2010

This book brings together contributions from experts in the fields to describe the current status of important topics in solid-state circuit technologies. It consists of 20 chapters which are grouped under the following categories: general information, circuits and devices, materials, and characterization techniques. These chapters have been written by renowned experts in the respective fields making this book valuable to the integrated circuits and materials science communities. It is intended for a diverse readership including electrical engineers and material scientists in the industry and academic institutions. Readers will be able to familiarize themselves with the latest technologies in the various fields.

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

Yan Han and Koubao Ding (2010). Advanced Simulation for ESD Protection Elements, Advances in Solid State Circuit Technologies, Paul K Chu (Ed.), ISBN: 978-953-307-086-5, InTech, Available from: http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/advanced-simulation-for-esd-protection-elements

INTECH
open science | open minds

InTech Europe
University Campus STeP Ri
Slavka Krautzeka 83/A
51000 Rijeka, Croatia
Phone: +385 (51) 770 447
Fax: +385 (51) 686 166
www.intechopen.com

InTech China
Unit 405, Office Block, Hotel Equatorial Shanghai
No.65, Yan An Road (West), Shanghai, 200040, China
中国上海市延安西路65号上海国际贵都大饭店办公楼405单元
Phone: +86-21-62489820
Fax: +86-21-62489821

IntechOpen