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Hafnium-based High-k Gate Dielectrics

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1. Introduction

Scaling of silicon dioxide dielectrics has once been viewed as an effective approach to enhance transistor performance in complementary metal-oxide semiconductor (C-MOS) technologies as predicted by Moore's law [1]. Thus, in the past few decades, reduction in the thickness of silicon dioxide gate dielectrics has enabled increased numbers of transistors per chip with enhanced circuit functionality and performance at low costs (Fig. 1). However, as devices approach the sub-45 nm scale, the effective oxide thickness (EOT) of the traditional silicon dioxide dielectrics are required to be smaller than 1 nm, which is approximately 3 monolayers and close to the physical limit (Fig. 2), thus resulting in high gate leakage currents due to the obvious quantum tunneling effect at this scale (Fig. 3). To continue the downward scaling, dielectrics with a higher dielectric constant (high-k) are being suggested as a solution to achieve the same transistor performance while maintaining a relatively thick physical thickness [2]. Many candidates of possible high-k gate dielectrics have been suggested to replace SiO_2 and they include nitrided SiO_2, Hf-based oxides, and Zr-based oxides. Hf-based oxides have been recently highlighted as the most suitable dielectric materials because of their comprehensive performance. One of the key issues concerning new gate dielectrics is the low crystallization temperature. Owing to this shortcoming, it is difficult to integrate them into traditional CMOS processes. To solve these problems, additional elements such as N, Si, Al, Ti, Ta and La have been incorporated into the high-k gate dielectrics, especially Hf-based oxides. In the following sections, the requirements of high-k oxides, brief history of high-k development, various candidates of high-k, and the latest hafnium-based high-k materials are discussed.

2. Requirements of high-k oxides

Among the various requirements of gate dielectric materials, the most important are good insulating properties and capacitance performance (Fig. 4). Because the gate dielectric materials constitute the interlayer in the gate stacks, they should also have the ability to prevent diffusion of dopants such as boron and phosphorus and have few electrical defects which often compromise the breakdown performance. Meanwhile, they must have good thermal stability, high recrystallization temperature, sound interface qualities, and so on.

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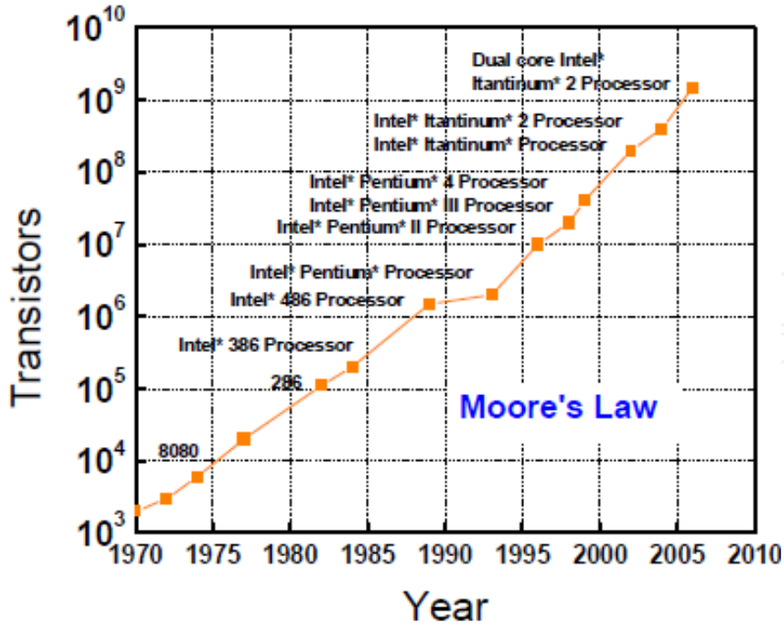

Fig. 1. Enhanced Performance Trend as Predicted by Moore's Law. Processing power has steadily risen as transistors become more complex [1].

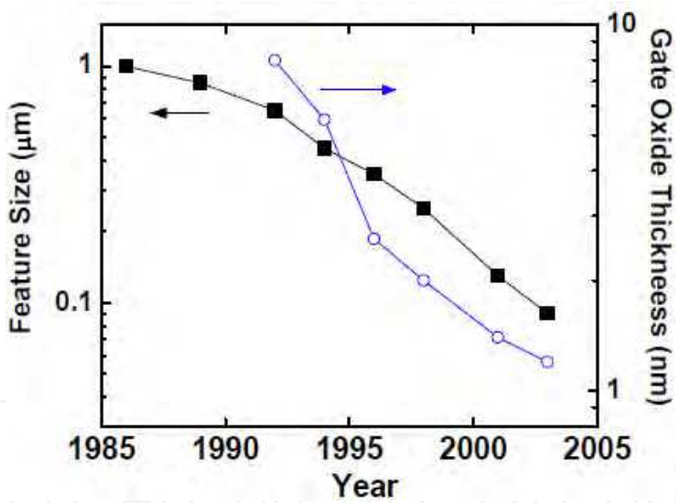

Fig. 2. Feature size of transistors downscales with time and the gate oxide thickness decreases accordingly [1].

2.1 K value, band gap and band offset

With regard to capacitance performance, the requirement is that the k value should be over 12, preferably 25–30. An appropriate k value means that the dielectrics will have a reasonable physical thickness which is enough to prevent gate leakage and not too thick to hamper physical scaling when achieving the target EOT. On the other hand, a very large k value is undesirable in CMOS design because they cause unfavorable large fringing fields at the source and drain regions [4]. Table 1 and Fig. 5 show that the k values of some oxides vary inversely with the band gap, so a relatively low k value is needed [5]. There are

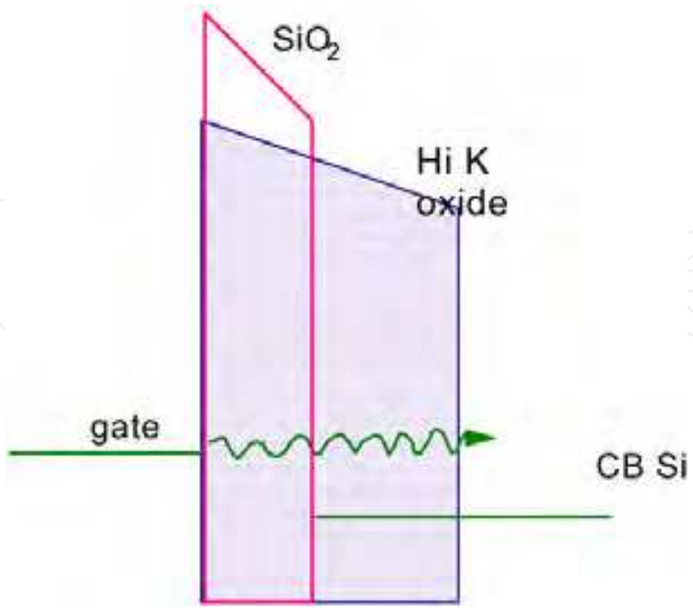

Fig. 3. Schematic of direct tunneling through SiO_2 [3].

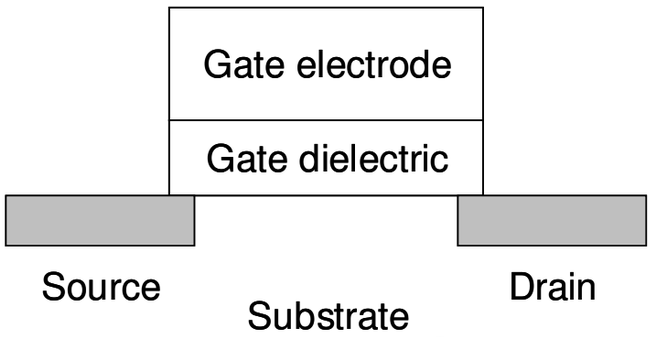

Fig. 4. Schematic drawing of a MOS stack.

numerous oxides with extremely large k values, such as $SrTiO_3$, which are candidates in DRAM capacitors [6], but their band gap is too small. According to the required insulating properties, the gate dielectrics must exhibit at least the band offset of 1 eV while in contact with the Si substrate in order to avoid serious gate leakage and breakdown. The band offset is required to be over 1 eV in order to inhibit conduction by the Schottky emission of electrons or holes into the oxide bands [5, 7], as schematically shown in Fig. 6. This means that the materials must have both the conduction band offset (CB) and valence band offset (VB) over 1 eV. In fact, the CB offset is less than the VB offset, which suggests oxides with band gaps wider than 5 eV may be excluded as gate dielectrics. For those oxides with narrow band gaps, either the CB offsets or the VB offsets may be smaller than 1 eV, also limiting the choice of these materials.

Dielectric	k	Band gap (eV)	CB offset (eV)
Si	-	1.1	-
SiO_2	3.9	9	3.2
Si_3N_4	7	5.3	2.4
Al_2O_3	9	8.8	2.8
Y_2O_3	15	6	2.3
Ta_2O_5	22	4.4	0.35
TiO_2	80	3.5	0
La_2O_3	30	6	2.3
a- $LaAlO_3$	30	5.6	1.8
$SrTiO_3$	2000	3.2	0
ZrO_2	25	5.8	1.5
HfO_2	25	5.8	1.4
$HfSiO_4$	11	6.5	1.8

Table I. Dielectric constant (k), band gap and CB offset on Si of the candidate gate dielectrics.

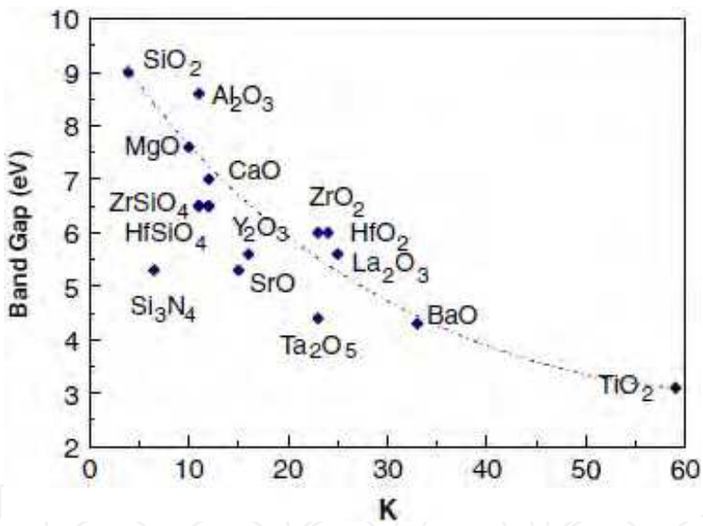

Fig. 5. Static dielectric constant versus band gap for candidate gate oxides [5].

2.2 Thermal stability

In present CMOS processes, the gate stacks must undergo rapid thermal annealing (RTA) of 1000 ^oC for 5s. This requires that the gate oxides must be thermally and chemically stable especially with the contacting materials. Thus, group II, III, IV oxides with a higher heat of formation than SiO_2 such as SrO, CaO, BaO, Al_2O_3, ZrO_2, HfO_2, Y_2O_3, La_2O_3 and lanthanides may be useful. Additionally, group II oxides which react with water are not favorable. Therefore, from the thermal stability point of view, only Al_2O_3, ZrO_2, HfO_2, Y_2O_3, La_2O_3, Sc_2O_3 and some lanthanides such as Pr_2O_3, Gd_2O_3 and Lu_2O_3 are left [3]. However, some materials with higher heat of formation than SiO_2 may also be slightly reactive with Si such as ZrO_2, forming the silicide, $ZrSi_2$ [8, 9]. Among these high k dielectrics, HfO_2 has both a high k value as well as chemical stability with water and Si.

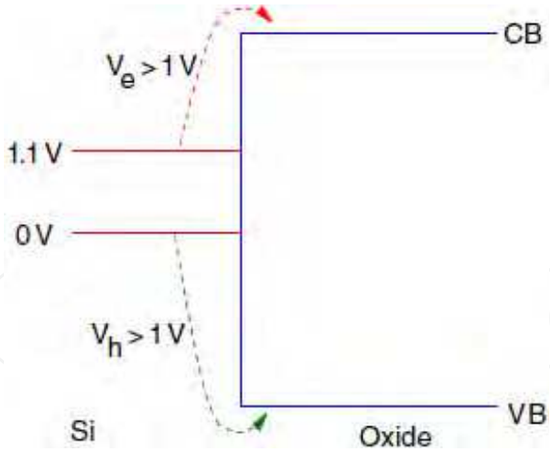

Fig. 6. Schematic of band offsets dependence of carrier injection in oxide band states.

2.3 Crystallization temperature

Owing to the absence of grains and good diffusion barrier properties, amorphous materials are preferred to crystalline ones. The grains which lie in the crystalline systems can often be the pathways for dopants diffusion and breakdown. Unlike SiO_2, high-k oxides usually have low crystalline temperature and can easily crystallize when subjected to RTA. In particular, HfO_2 and ZrO_2 crystallize at much lower temperatures at ~400 ^oC and ~300 ^oC, respectively (Fig. 7). According to the above factors, the approach to improve the crystallization temperature of HfO_2 and ZrO_2 should be considered. The crystallized HfO_2 has a much lower leakage current which has convinced many companies such as Intel and Freescale to adopt binary oxides because of their relative higher k values.

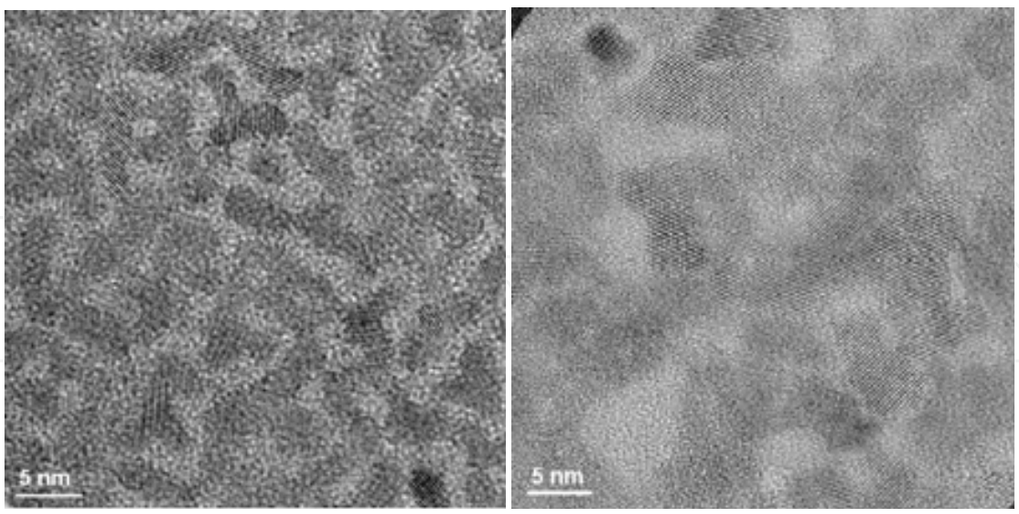

Fig. 7. TEM image of crystallization in HfO_2/SiO_2 dielectrics with (a) 40% HfO_2 and(b) 80% HfO_2 [10].

2.4 Interface quality

The interface between the high-k dielectrics and Si substrate must have the highest electrical quality and flatness, absence of interface defects, and low interface state density D_{it}. Bad

interface quality can cause high fixed charge density, inducing a large shift in the flat band voltage (V_{fb}) which severely reduces the performance and reliability of the transistor. Most of the high-k materials reported in this chapter have D_{it} ~10^{11}–10^{12} eV/cm^2 and also exhibit a substantial flatband voltage shift larger than 300 mV [11]. Therefore, it is crucial to improve the quality of the interface. There are two ways to ensure a high quality interface, either using a crystalline oxide grown epitaxially on the Si or an amorphous oxide. An amorphous oxide has many advantages over a poly-crystalline oxide. Firstly, it is more economically and more compatible with existing processes. Secondly, the amorphous oxide can minimize the number of interface defects. Thirdly, it is possible to gradually vary the composition of an amorphous oxide without creating a new phase, as in silicate alloys, or when adding nitrogen or other metal elements. Fourthly, an amorphous oxide and its dielectric constant are isotropic, so that fluctuations in polarization from differently oriented oxide grains will not cause scattering of carriers. Finally, amorphous phases have no grain boundaries. The advantages of epitaxial oxides may come in the future, where their more abrupt interfaces allows us to reach lower EOTs. Besides the above consideration, the configuration of interface bonding is also significant. As the SiO_2/Si interface has high quality, the ideal gate dielectric stack may well turn out to have an interface comprising several monolayers of Si–O (and possibly N) containing materials, which can be a pseudobinary layer at the channel interface. This layer can serve to preserve the critical, high-quality nature of the SiO_2 interface (D_{it} ~2x10^{10} eV/cm^2) while providing a higher-k value for that thin layer. The same pseudobinary materials can also extend beyond the interface, or a different high-k material can be used on top of the interfacial layer.

2.5 Defects

Similar to interface defects, bulk defects formed in high-k oxides during deposition also causes degraded transistor performance due to the rising number of defect-related fixed charges. In addition, charges trapped in defects will cause a shift in the gate threshold voltage of the transistor, which is the key characteristic of performance. Furthermore, the trapped charges change with time and so the threshold voltage also shifts with time, leading to problems associated with negative bias temperature instability (NBTI) and positive bias temperature instability (PBTI). Meanwhile, trapped charges scatter carriers in the channel causing reduced carrier mobility. Lastly, they are the starting points for electrical failure and oxide breakdown. Typically, these defects are sites of excessive or deficient oxygen or

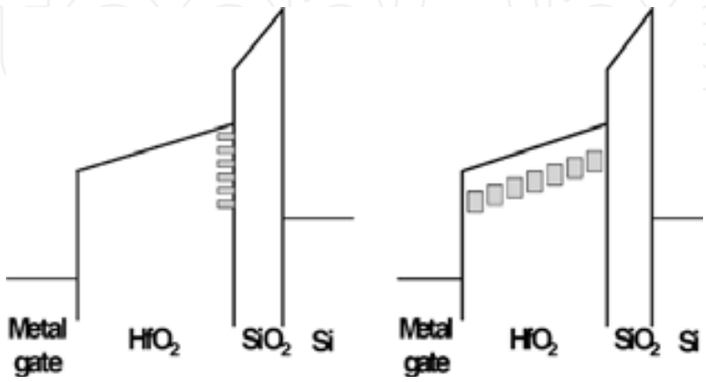

Fig. 8. Schematic diagram of two types of defects located (a) at the HfO_2/SiO_2 interface and (b) in the bulk of HfO_2 film.

impurities. Unfortunately, most of the high-k oxides inherently have more interface defects in contact with the Si substrate and bulk defects than SiO_2 because their bonding cannot relax as easily [12] (Fig. 8). Nowadays, many groups are endeavoring to reduce defect densities by either processing control or engineering of materials.

3. Brief history of high-k dielectric development

To overcome gate leakage problems and extend the usefulness of SiO_2-based dielectric, incorporation of nitrogen into SiO_2 has been adopted. There are several ways to introduce nitrogen into SiO_2, such as post deposition annealing in nitrogen ambient and forming a nitride/oxide stack structure. By incorporating nitrogen into SiO_2, it not only increases the dielectric constant but also acts as a better barrier against boron penetration. In addition, a nitride/oxide stack structure maintains the benefits of good interface quality between the oxide and substrate [13, 14], as schematically shown in Fig. 9.

Despite the immense development with SiO_2, these oxynitrides still have low k values and so a relatively thick layer is required to prevent direct tunneling current. Therefore, alternative materials with a higher k than SiO_2 (3.9) are needed to achieve the required capacitance without tunneling currents [15]. Oxides of group II, III, IV such as Al_2O_3, Y_2O_3, La_2O_3, Sc_2O_3 and some lanthanides such as Pr_2O_3, Gd_2O_3 and Lu_2O_3 have been proposed. Unfortunately, these dielectrics will only last a few generations due to limitations dictated by low power applications, scalability, or serious reactions with the Si substrate. Yet, these problems are much smaller for oxides and silicates of Hf and Zr. Thus, the choice of alternative gate dielectrics has been narrowed to HfO_2, ZrO_2 and their silicates due to their excellent electrical properties and high thermal stability in contact with Si [16]. However, another problem, namely low crystallization temperature, is associated with Hf-based and Zr-based oxides. They can easily crystallize during standard CMOS processes. These crystalline structures can increase the gate leakage by orders of magnitude and provide pathways for diffusion of dopants and dielectric breakdown. Up to date, many groups have focused on the improvement of the crystallization temperature of these oxides. Thus, elements such as N, Si, Al, Ta and La have been incorporated into these high-k oxides. Hf-based oxides are preferred over Zr-based oxides for its relative higher crystalline temperature.

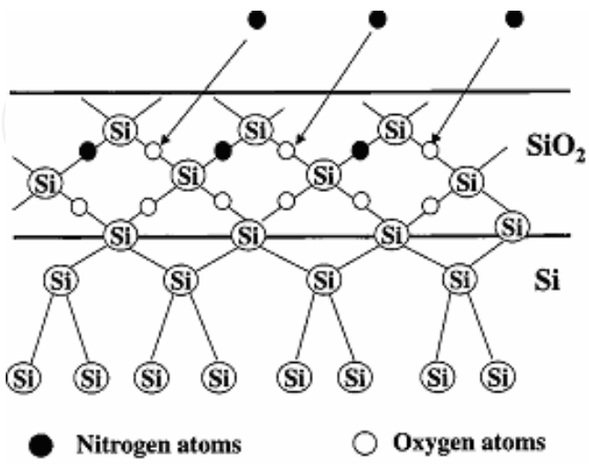

Fig. 9. Schematic showing incoming nitrogen radicals replace oxygen atoms to form Si–N bonds [17].

4. Latest development in Hf-based high-k oxides

4.1 Fabrication methods

Hf-based High-k dielectric oxides have replaced conventional SiO_2 as the gate dielectric in sub-0.1 μm complementary metal-oxide-semiconductor devices [18, 19]. The fabrication technology of Hf-based high-k ultrathin dielectrics has been developed very quickly. Overall, the techniques can be categorized into two major approaches based on the reaction mechanism during preparation, namely CVD (chemical vapor deposition) and PVD (Physical Vapor Deposition) processes. CVD-based approaches include metal-organic chemical vapor deposition (MOCVD) [20], plasma-enhanced chemical vapor deposition (PECVD) [21], atomic-layer chemical vapor deposition (ALCVD) [22], photo-assisted CVD synthesis [23] and so on. These growth methods provide more flexibility and have relatively low cost. Among them, ALCVD is considered particularly promising, since this is the only feasible method to control the thickness down to the nanometer range and layer-by-layer composition of the metal oxide ultrathin film [24].

4.2 Doping of Hf-based high-k oxides

Crystallization of pure HfO_2 occurs at only about 400–450 ^oC causing grain boundary leakage current and nonuniformity of the film thickness [25]. As a result, impurities such as O, B, and P can penetrate the grain boundaries during high temperature postprocessing. It causes equivalent oxide thickness (EOT) scaling and reliability concerns when Hf-based high-k ultrathin gate oxides are integrated into high temperature CMOS processes [26].

Recently, nitrogen incorporation has been extensively investigated in the field of high-k thin films [27, 28]. Nitrogen introduction into HfO_2 films has significantly improved the electric properties as well as crystallinity [29, 30]. On the contrary, nitrogen doping leads to decreased band gap. This is because it adds N 2p states which lie above the O 2p states in the free atoms and so the VB is raised and the CB is reduced due to the interaction between the nonbonding Hf 5d states and adjacent O and N states. The delocalized Hfd-Np bonding states contribute an indirect band gap E_g of 1.8 eV, which is smaller than the Op-Hfd band gap of larger than 5.8 eV [31, 32]. Despite the disadvantages, the introduced nitrogen can suppress the growth of microstructure and interfacial layer. When N is added to HfO_2, it is expected to distort the equilibrium of the lattice and produce disordered states. Choi et al. have demonstrated that adding nitrogen results in the reduction of the mobility of Hf and O atoms as well as increase in the nucleation temperature and consequently the crystalline temperature [33, 34]. All these indicate that nitrogen acts as a crystallization inhibitor and causes an increase in the crystallization temperature in Hf-based gate dielectrics (Fig. 10).

The interfacial layer between the high-k dielectrics and Si substrate is one of the key factors determining the performance and reliability of a MOS transistor. Hence, it is extremely crucial to fabricate a SiO_2/Si like interface. From this viewpoint, a SiO_2 interfacial layer is often grown between Hf-based oxide and Si by thermal oxidation. However, this HfO_2/SiO_2 gate dielectric stack usually introduces an additional EOT increase due to the low k SiO_x interfacial layer. In order to solve this problem, addition of Si into Hf-based oxide to form Hf silicate may be a plausible means. Besides improvement in the interface quality, incorporation of Si into Hf-based oxides can also foster the formation of amorphous or near-amorphous structures [36, 37]. A negative effect is the reduction in the k value. The k value decreases inversely with increasing Si concentration in Hf-based oxides. When the Si content approaches 100% (alternatively, Si-based oxide), the k value comes close to the lowest value of 3.9. Accordingly, the Si content must be selected to keep a balance between gains and defects.

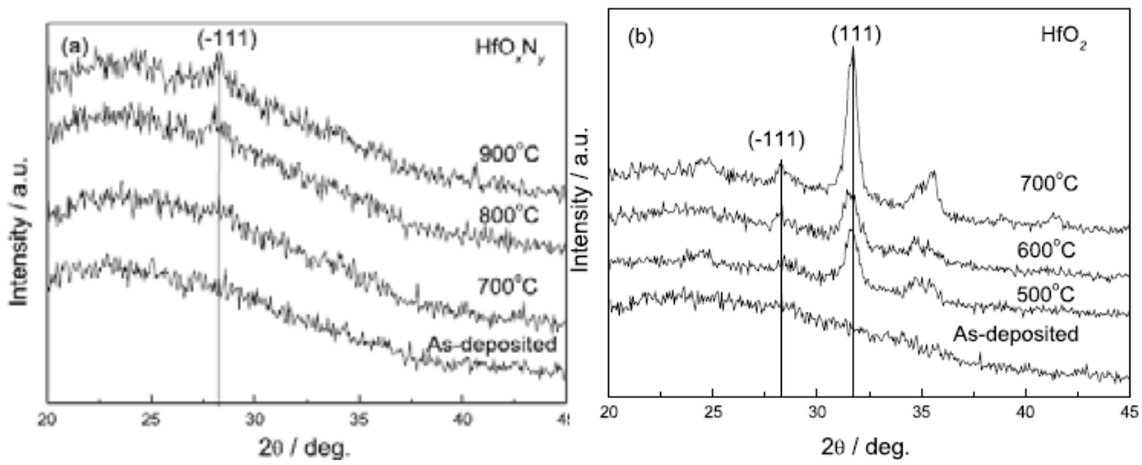

Fig. 10. XRD spectra for the HfO_2 and HfO_xN_y films: (a) as-deposited and HfO_xN_y films annealed at different temperatures and (b) as-deposited and HfO_2 films annealed at different temperatures [35].

HfSiON is thermally stable compared to HfO_2 due to the Si-N bonds that are created by the nitridation step, and thus HfSiON has the potential for implementation in a conventional gate-first process with high temperature activation annealing. By using nitrogen-incorporated HfSiO films, both the oxidation and reduction reactions can be suppressed in the annealing process at a proper partial pressure of N_2 gas. The N_2 gas suppresses only the reduction reaction, while nitrogen atoms incorporated in the dielectrics suppress both oxidation and reduction reactions, greatly improving the electrical characteristic of Hf-based high-k dielectrics [38]. Fig. 11 schematically shows the mechanism of the suppression of reaction and the results of suppression of interfacial layer growth can be seen in Fig. 12.
Many groups have reported that the crystallization temperature of HfO_2 (400–450 °C) can be increased by incorporation of Al_2O_3 forming an HfAlO alloy. Zhu et al. [39] have shown that Al inclusion in HfO_2 significantly increases the crystallization temperature. At an Al content of 31.7%, the crystallization temperature is about 400-500 °C higher than that without Al.

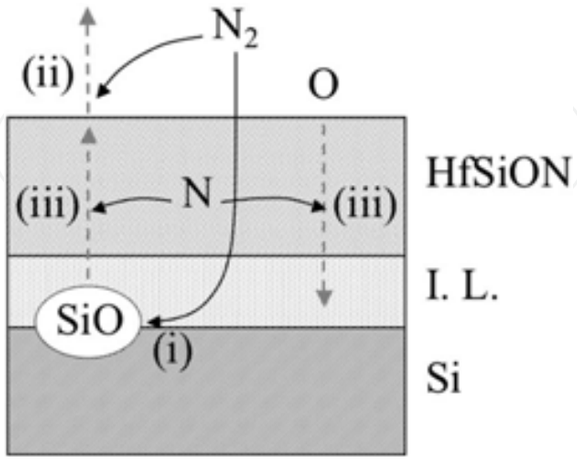

Fig. 11. Schematic of the mechanism for the suppression of reaction. N_2 ambient gas can suppress (i) SiO formation and (ii) SiO desorption. Nitrogen atoms in the dielectric film can suppress (iii) SiO and O diffusion [38].

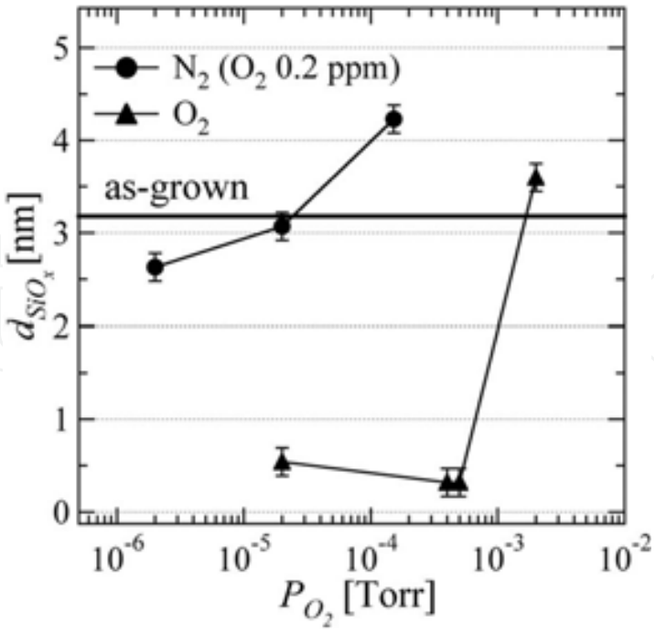

Fig. 12. SiO_2 equivalent thickness of dielectric films as a function of O_2 partial pressure (PO_2). These thicknesses were calculated from the peak-area ratio of the Si-oxide to the Si substrate, regarding the Si-oxide component as SiO_2 for simplicity. A straight line at around 3.2 nm denotes the thickness of the as-grown sample [38].

This additional Al increases the band gap of the dielectrics from 5.8 eV for HfO_2 without Al to 6.5 eV for HfAlO with 45.5% Al but reduced dielectric constant from 19.6 for HfO_2 without Al to 7.4 for Al_2O_3 without Hf. Considering the factors including the crystallization temperature, band gap, and dielectric constant, they conclude that the optimum Al concentration is about 30% for conventional CMOS gate processing technology. Moon et al. [40] have presented the similar trend in the change of the electrical and structural properties due to the Al incorporation. Their results suggest that the HfAlO film with 10% Al_2O_3 shows a great improvement in thermal stability and significant reduction of interfacial layer growth during subsequent thermal processes while maintaining a high k value (~19), leading to reduction in the leakage current by around 2 orders of magnitude compared to pure HfO_2. The HfAlO film also has good compatibility with the gate electrode in high temperature annealing process (Fig. 13). Bae et al. [41] have pointed out that while Al doping significantly increases the crystallization temperature in HfO_2 to up to 900 °C and improves its thermal stability, it also introduces negative fixed oxide charges due to Al accumulation at the HfAlO-Si interface, resulting in mobility degradation. The effects of Al concentration on the crystallization temperature, fixed oxide charge density, and mobility degradation in HfAlO have been characterized and correlated. In spite of these analyses, there are still a lot of issues to be settled in order to maximize the performance of the materials.

On account of the good thermal stability and electrical characteristics, HfTaO gate dielectrics have attracted attention. Incorporation of Ta into HfO_2 enhances the crystallization temperature dramatically while keeping a high k value of ~17 [42]. Compared to HfO_2 gate dielectrics, HfTaO also has the advantages of much lower charge trapping as well as BTI degradation and increased channel mobility [43]. Yu et al. [44] have confirmed that HfTaO

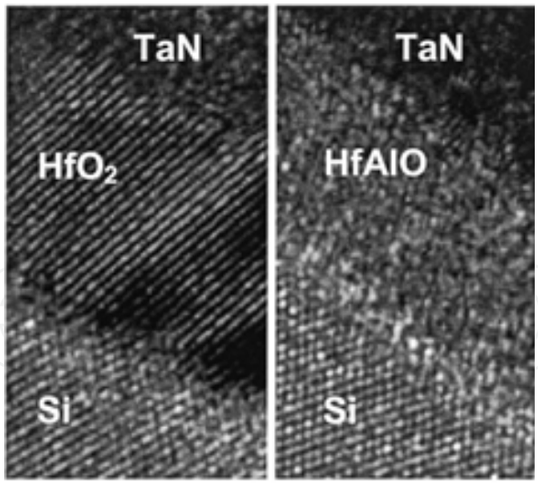

Fig. 13. XTEM images of HfO_2 and HfAlO after 700 °C in-situ PDA treatment. HfAlO layer remains amorphous while HfO_2 is crystallized. Both films were deposited at 400 °C without surface nitridation [40].

with 43% Ta remains amorphous even after annealing at 950 °C for 30 s, and the formation of low-k interfacial layer is reduced (Fig. 14). The results indicate good interface properties between the HfTaO and Si substrate and sufficiently suppressed boron penetration behavior in the HfTaO film. The negligible flat-band voltage shift in HfTaO with 43% Ta film is observed and attributed to its amorphous structure after device fabrication. It also contributes to the improvement in performance and reliability of the devices. Zhang et al. [45] have found that HfTaO with 40% Ta exhibits the highest crystallization temperature of 900 °C, while 35% and 52% HfTaO films show crystallization temperature of 800 °C (Fig. 15). The results demonstrate that HfTaO N-MOSFETs possess higher electron mobility than controlled HfO_2 devices. Among them, the transistors with 40% Ta doped HfTaO as the gate dielectrics have the highest electron mobility (Fig. 16).

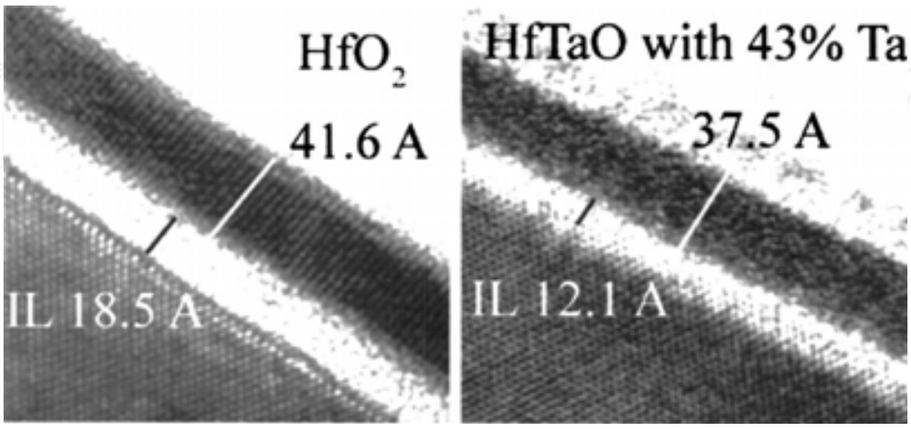

Fig. 14. TEM images of HfO_2 and HfTaO with 43% Ta after PDA at 700 °C for 40 s and activation annealing at 950 °C for 30 s. Pure HfO_2 film is fully crystallized whereas the HfTaO with 43% Ta film remains amorphous [44].

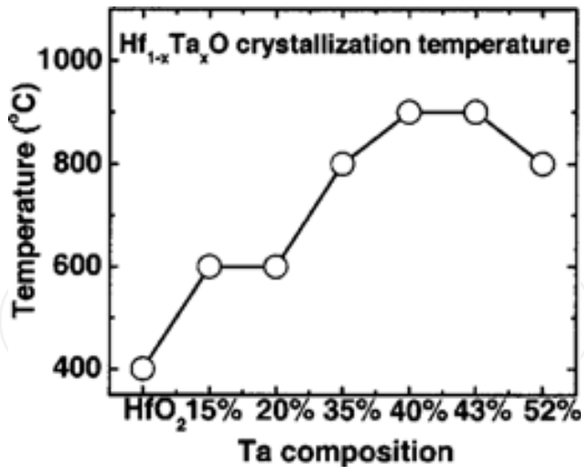

Fig. 15. Crystallization temperature of HfTaO with different Ta composition measured by XRD with incident angle of x ray: 3° [45].

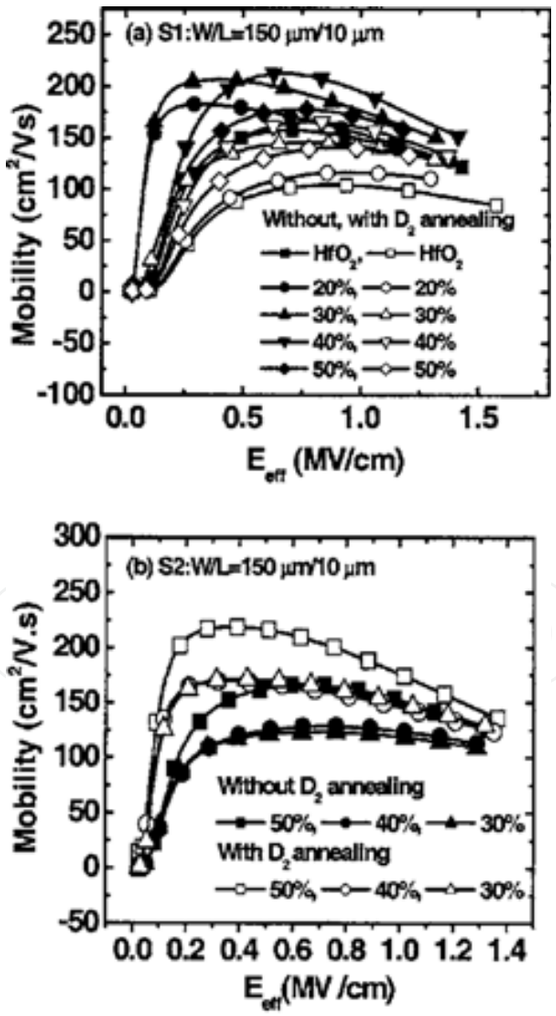

Fig. 16. Effective mobility of HfTaO N-MOSFETs (a) without and (b) with D_2 annealing [45].

In addition, some rare earth elements such as La can also improve the characteristics of Hf-based high-k dielectrics. Introduction of La_2O_3 into HfO_2 causes an increase in the crystallization temperature (Fig. 17). Furthermore, unlike other Hf-based amorphous materials such as $HfSiO_x$ or $HfAlO_x$, the permittivity of $HfLaO_x$ still yields a high k value (>20) [46] (Fig. 18). Besides, HfLaO also has the advantages of much lower charge trapping as well as BTI degradation and increased channel mobility. In addition, varying the La concentrations in the TaN/HfLaO or HfN/HfLaO gate stack can effectively tune the metal work function for N-MOSFETs [43]. In the capacitance-voltage curve of metal oxide semiconductor capacitor, Yamamoto et al. [46] have shown that the $HfLaO_x$ dielectric film exhibits very small degradation in both the interface and bulk properties, as shown in Fig. 19. A very low fixed charge density in $HfLaO_x$ films is demonstrated from a very small film thickness dependence on the flatband voltage in their study.

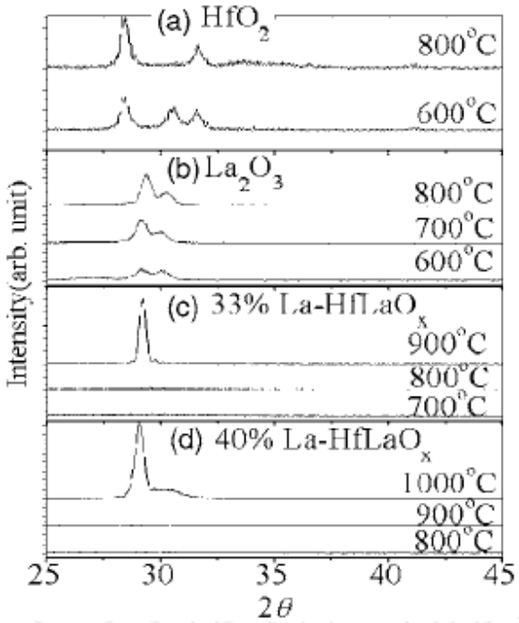

Fig. 17. XRD spectra of 30 nm films of (a) HfO_2, (b) La_2O_3, (c) 33% La–$HfLaO_x$, and (d) 40% La–HfLaOx annealed at various temperatures. HfO_2 and La_2O_3 films crystallize under 600 °C. On the other hand, 40% La–HfLaOx film remains amorphous after 900 °C annealing [46].

An et al. [47] have synthesized ultrathin HfO_2 and $HfLaO_x$ films with La/(Hf+La) ratios of 42%, 57%, and 64% by an atomic layer deposition process. By measuring the leakage current at different temperatures, they propose that the conduction mechanism of HfO_2 and $HfLaO_x$ films follow the Poole–Frenkel emission model under the gate injection condition. They have also demonstrated that the intrinsic trap energy levels are 1.42, 1.34, 1.03, and 0.98 eV in the $HfLaO_x$ samples with La/(Hf+La) ratios of 0%, 42%, 57%, and 64%, respectively, showing a decreasing behavior as the La content is increased (Fig. 20).

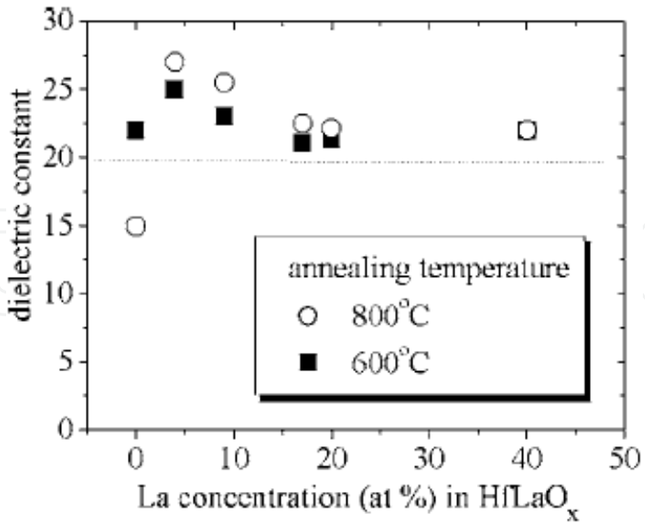

Fig. 18. Dielectric constants of $HfLaO_x$ film as a function of La concentrations. The dielectric constants are determined by MIM capacitors for the samples with La concentrations of 0%, 4%, 9%, and 17%. For 20% and 40%, CET vs physical thickness plots were used [46].

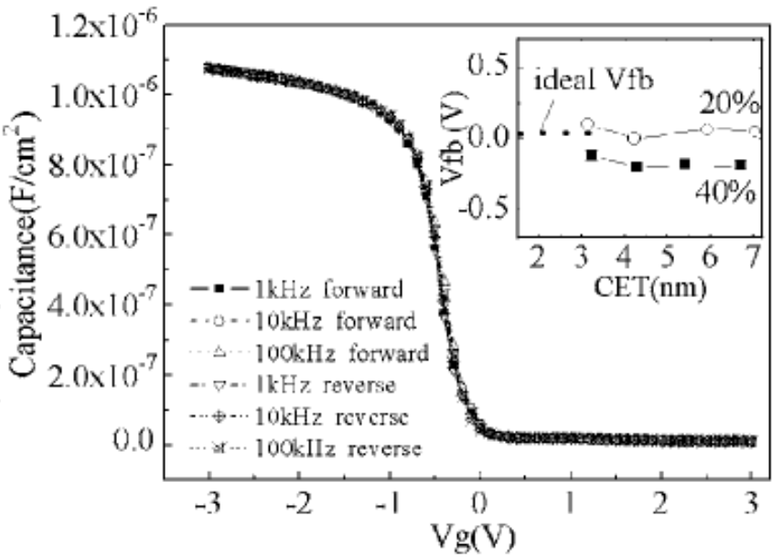

Fig. 19. C-V characteristics of Au/40% La–$HfLaO_x$/p-Si MOS capacitor annealed at 600 °C. The film thickness was 8.4 nm. It shows very small hysteresis and frequency dispersion. The inset in the upper right shows the flatband voltages of Au/20% La–HfLaO/p-Si or 40% La–HfLaO/p-Si MOS [46].

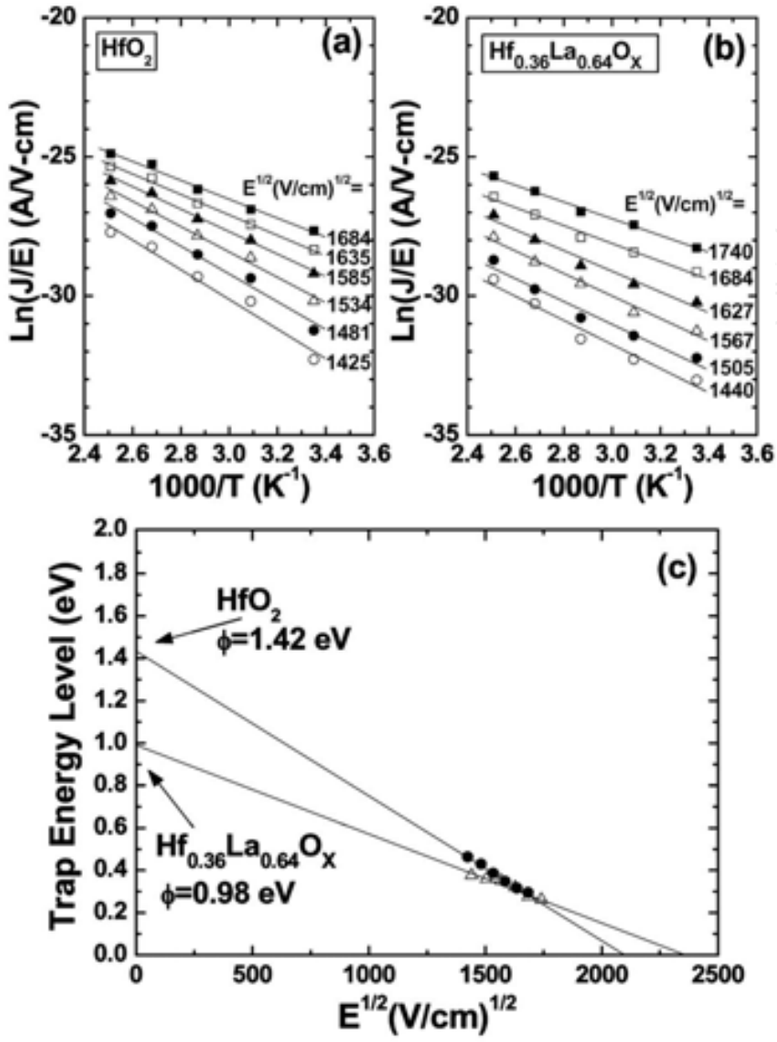

Fig. 20. ln(J/E) vs 1/T plots measured at various applied electric fields for (a) HfO_2 and (b) $Hf_{0.36}La_{0.64}O_x$ films, and (c) trap energy level as a function of $E^{1/2}$ for both samples [47].

From the above results, it can be easily inferred that $HfLaO_x$ is a potential dielectric material for amorphous high-k gate insulator in further advanced complementary metal oxide semiconductor (CMOS) devices.

5. Conclusion

This chapter succinctly reviews the motivation to replace traditional SiO_2 gate dielectrics, requirements of high-k dielectrics, brief history of high-k materials development, and latest development in Hf-based high-k dielectrics. In order to improve the performance of CMOS devices, Hf-based gate layers are being integrated into MOSFETs to achieve low leakage current. Excellent gate transistors with improved performance based on Hf-based gate dielectrics as the insulating layers are expected. Although much progress has been made in fabricating novel gate dielectrics, investigation of these Hf-based high-k gate dielectrics

continues to be exciting and the final target has not yet been reached. There is still room for development and many issues need better understanding.

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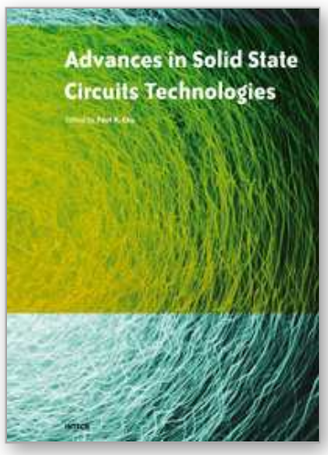

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