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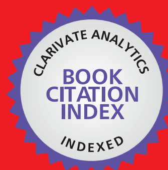

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A 7V-to-30V-Supply 190A/μs Regulated Gate Driver in a 5V CMOS-Compatible Process

David C. W. Ng[1], Victor So[1], H. K. Kwan[1], David Kwong[1] and N. Wong[2]
[1]*The Hong Kong Applied Science and Technology Research Institute (ASTRI)*
[2]*The University of Hong Kong*
Hong Kong, China

1. Introduction

The growing markets of electronic components in automotive electronics, LCD/LED drivers and TV sets lead to an extensive demand of high-voltage integrated circuits (HVICs), which are normally built by HV-MOSFETs. These HV-MOSFET devices generally occupy large die areas and operate at low speed due to large parasitic capacitance and small trans-conductance (g_m). There are two types of HV-MOSFET devices, namely, thick-gate and thin-gate oxide devices. Thick-gate oxide devices can sustain a high gate-to-source voltage, V_{GS}, but suffer from a reduced g_m, poor threshold voltage V_T control in production and higher cost due to the need of extra processing steps. Thin-gate devices have a larger g_m, smaller parasitic capacitance, less processing steps and a lower cost. These properties make the thin-gate HV-MOSFETs attractive, though they face severe limitation on V_{GS} swing. There are two main concerns when thin-gate HV-MOSFETs are used. The first is how to achieve high current driving capability to drive capacitive loads in high-voltage (HV) application, whereas the second is how to protect the thin-gate oxide from HV stress breakdown. For current-driving capability, Bales (Bales, 1997) proposed a class-AB amplifier using bipolar technology which consumes a high quiescent current and is expensive due to a large die area and complicated masking. Lu & Lee (Lu & Lee, 2002) proposed a CMOS class-AB amplifier which can only drive around 6mA and does not meet the driver requirements of large and fast current responses (Hu & Jovanovic, 2008). Mentze et al. (Mentze et al., 2006) proposed a HV driver using pure low-voltage (LV) devices but this architecture requires an expensive silicon-on-insulator (SOI) process to sustain substrate breakdown in HV application. Tzeng & Chen (Tzeng & Chen, 2009) proposed a driver that consumes a large die area with all transistors inside the circuit being HV transistors. On the other hand, transistor reliability becomes a serious issue in HV thin-gate oxide transistor circuits. Chebli et al. (Chebli et al., 2007) proposed the floating gate protection technique. The voltage range under protection will change according to the ratio of capacitors and the HV supply, V_{DDH}. This technique, however, cannot limit the voltage across the nodes of gate and source well when the variation of the supply voltage is large. Riccardo et al. (Riccardo et al., 2001) proposed a method which requires an extra Zener diode to protect the thin-gate oxide transistors, so a special process and higher cost are incurred. Declercq et al. (Declercq et al., 1993) suggested a HV-MOSFET op-amp driver with a clamping circuit to protect the thin-

Source: Advances in Solid State Circuits Technologies, Book edited by: Paul K. Chu,
ISBN 978-953-307-086-5, pp. 446, April 2010, INTECH, Croatia, downloaded from SCIYO.COM

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gate oxide, but it consumes a significant amount of die area as all devices are HV-MOSFETs. To overcome these drawbacks, the main aims of the proposed driver architecture are:

a. to minimize the number of HV devices so as to save die area in HV application.
b. to develop a HV driver with fast transient responses.
c. to develop reliable thin-gate protection circuitry in HV application, so as to enjoy cost saving from reduced processing steps and take advantages of better V_T process control and high current gain g_m comparing to the thick-gate HV-MOSFET counterparts.

As a result, a HV high-speed regulated driver is developed using mostly LV-MOSFETs with the minimum number of thin-gate HV-MOSFETs.

In this chapter, we present a high-speed CMOS driver that operates with a HV 7V-to-30V supply delivering an output drive up to 190A/μs at a regulated 4.8V output voltage. It is particularly suitable for HV applications such as LCD/LED/AC-DC drivers loaded with power (MOS)FETs. The circuit consists of only 5V LV devices and two thin-gate HV asymmetrical MOS transistors (HV-MOSFETs) fully compatible with standard CMOS technology. The design features a small-area cost-effective solution, measuring only 650μm×200μm in a 0.5μm standard 5V/40V (V_{GS}/V_{DS}) CMOS process. The approach of the regulated output driver can adjust itself to the desired V_{GS}, helping to fully utilize the effect of V_{GS} on minimizing the on-resistance, R_{DS-ON}, of the power FET. Novel thin-gate protection circuits, based on source-follower (SF) configurations, have been deployed to limit the V_{GS} swing to within 5V for the HV-MOSFETs. A dual-loop architecture provides an extremely fast slew rate and transient response under a low quiescent current of 90μA in its static state and 860μA during switching. A dead-time circuit is included to eliminate the power loss incurred by shoot-through current, saving 75mW under a 30V HV supply. Moreover, stability analysis and compensation techniques are described in details to ensure stable operation of the driver in both loaded and un-loaded conditions. Lab measurements are in good agreement with simulations. A comparison with existing works then demonstrates the efficacy and superiority of the proposed design.

In this chapter, Section 2 introduces the use of LV devices to build HV high-speed regulated driver, together with stability analyses for both cases when the power FET load is ON or OFF. Section 2 also discusses the power saving techniques in driving HV-MOSFETs. In Section 3, simulation and lab measurement results are shown which confirm the merits of the proposed design. Finally, the conclusion is drawn in Section 4.

2. Principles of operation

2.1 Circuit structure and basic operation

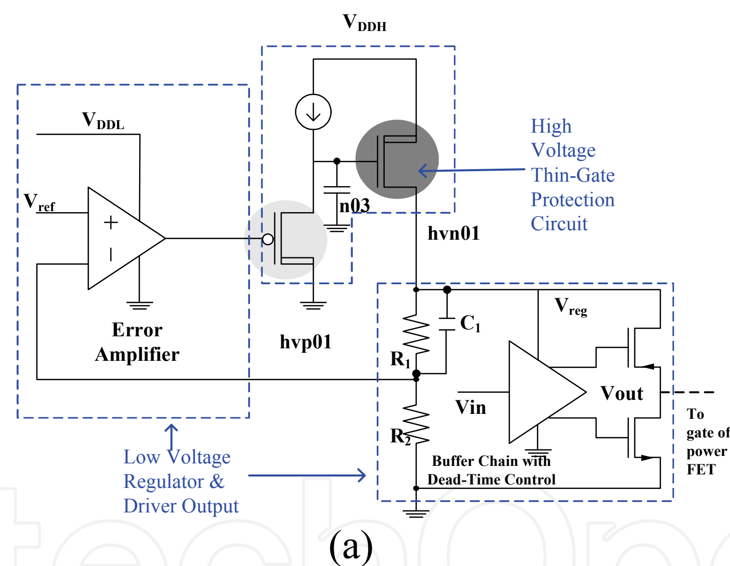
Fig. 1(a) shows the high-level block diagram of the proposed driver. It consists of a LV error amplifier, a HV thin-gate protection circuit, a feedback resistor network with pole-zero cancellation and a fast transient regulated driver with dead-time control. A HV nMOS, hvn01, is connected to the node V_{reg} in a SF configuration. The driver requires a LV supply, V_{DDL}, as well as a HV supply, V_{DDH}. We first develop an internal regulator, which gives a 4.8V DC voltage, V_{reg}, through hvn01. The drain of hvn01 is connected to V_{DDH}, which is 30V in our design. The V_{reg} acts as a supply voltage to a chain of inverter buffers, which in turn drive the output load at the node V_{out}. The switching activities are started from V_{in} all the way to V_{out}. The output load here is the gate of a 1A on-chip thin-gate power (MOS)FET. The equivalent gate capacitance is around 270pF. The driver provides a 4.8V output and therefore protects the thin gate of the loading power FET by limiting its V_{GS} right below 5V.

The node V_{out} can also be connected externally to drive external power FETs. The approach of the regulated output driver can always adjust itself to the desired V_{GS}, helping to fully utilize the effect of V_{GS} on the on-resistance, R_{DS-ON}, of the power FET. In this connection, and with reference to (1) and (2) (Gray et al., 1990), the on-resistance and die area of the on-chip power FET can be minimized:

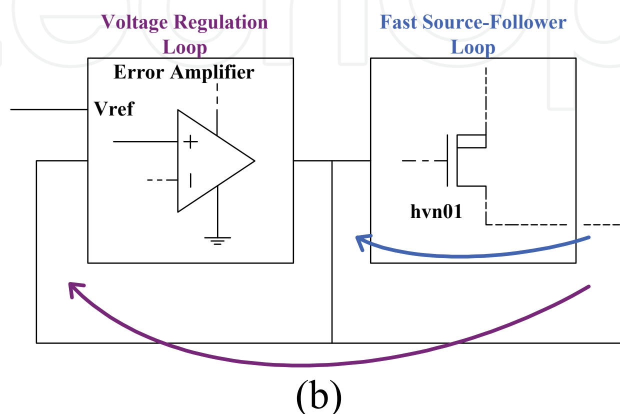
$$I_{DS} \approx \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2 , \quad (1)$$

$$R_{DS\text{-}ON} \approx \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)} . \quad (2)$$

Equation (1) describes the behavior of a (HV) nMOS in saturation region, while (2) approximates the turn-on resistance of a (HV) nMOS in the linear region. I_{DS} is the current flowing from the drain to source of a MOSFET. V_{GS} is the gate-to-source voltage. V_T is the threshold voltage to turn on the MOSFET. Also, μ_n is the mobility of electrons and C_{ox} is the gate-oxide capacitance per unit area, whereas W and L are the width and length of the transistor, respectively.



(a)



(b)

Fig. 1. (a) Architecture of the proposed driver; (b) Dual-loop structure in the driver

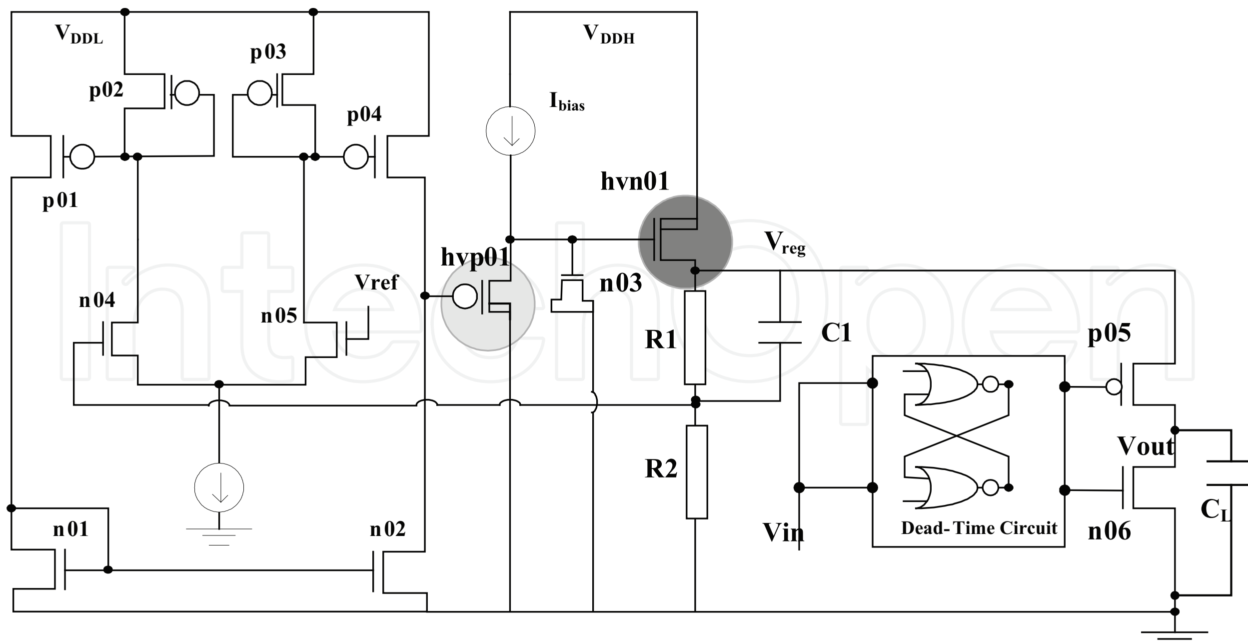


Fig. 2. Detail schematic of the proposed driver

	$C_L \approx$ 0pF (power FET OFF)	$C_L \approx$ 0pF (power FET OFF with Zero)	$C_L = C_{powerFET} \approx$ 270pF (power FET OFF)	$C_L = C_{powerFET} \approx$ 270pF (power FET ON with Zero)
Loop gain(dB)	45	45	45	45
Phase Margin (deg)	83.7	109	57.5	77.1
Unity-Gain Frequency (UGF) (kHz)	27.1	33.8	24.5	28.1
Gain Margin (dB)	35.7	31	18.2	21.9
Gain Margin Frequency (kHz)	623.6	918.3	94.6	184.6
Source Follower Unity-Gain Frequency (MHz)	>100 (Gray et al., 1990)	>100	>100	>100

Table I. Summary of frequency responses of the driver with output = high and output = low

2.2 Regulated driver with fast transient response

2.2.1 Fast dual-loop operation

As shown in Figs. 1 & 2, there are two loops in the driver, namely, the voltage-regulation (VR) loop and the source-follower (SF) loop to achieve fast transient responses. Firstly, for the VR loop, the error amplifier senses the V_{reg} through the resistor network and amplifies

the error signal between the scaled V_{reg} and the reference voltage V_{ref}. The error signal is then shifted up to a higher voltage through the thin-gate protection circuit and regulates hvn01 to correct the error, thereby generating a steady and accurate V_{reg}. Secondly, for the SF loop, the SF configuration of hvn01 itself is a fast feedback loop. Referring to (1) and Fig. 1, the feedback mechanism is obvious: When the node V_{reg} goes down due to load current change, the gate-to-source voltage of hvn01, $V_{GS-hvn01}$, increases and sources a larger output current to charge up the node V_{reg} again. The main function of the VR loop is to provide a regulated voltage of around 4.8V in the steady state, while the fast SF loop provides an immediate response when there is a sudden load change.

2.2.2 Loop gain analysis with the power FET being ON/OFF

We first analyze the SF loop and later the VR loop. For the SF loop, it is well known for its fast response with its unity-gain frequency (UGF) in the 100MHz to 1GHz range (Gray et al., 1990). Its pole effect is generally beyond the UGF of the VR loop and therefore negligible. For the VR loop, there are two scenarios in the stability analysis: the power FET ON and the power FET OFF. When it is ON, $C_L = C_{L-ON} = C_{powerFET} \approx 270$pF, and when it is OFF, $C_L = C_{L-OFF} \approx 0$pF. Here $C_{powerFET}$ is the equivalent gate capacitance of the power FET. The AC simulation with and without the power FET is shown in Table I and Fig. 3. The phase margin of the VR loop is larger when the power FET is OFF. This can be explained by the following loop gain analysis:

$$T(s) = A(s)\left(\frac{R_2}{R'}\right)\left(\frac{1+\frac{s}{z_{hvp01}}}{1+\frac{s}{p_{hvp01}}}\right)\left(\frac{1+\frac{s}{z_{hvn01}}}{1+\frac{s}{p_{hvn01}}}\right)\left(\frac{1+\frac{s}{z_f}}{1+\frac{s}{p_f}}\right), \tag{3}$$

where z_{hvp01}, z_{hvn01}, p_{hvp01} and p_{hvn01} are the zeros and poles from hvp01 and hvn01, respectively. A(s) is the transfer function of the error amplifier. $R' = R_1 + R_2$. The zeros and poles are defined as

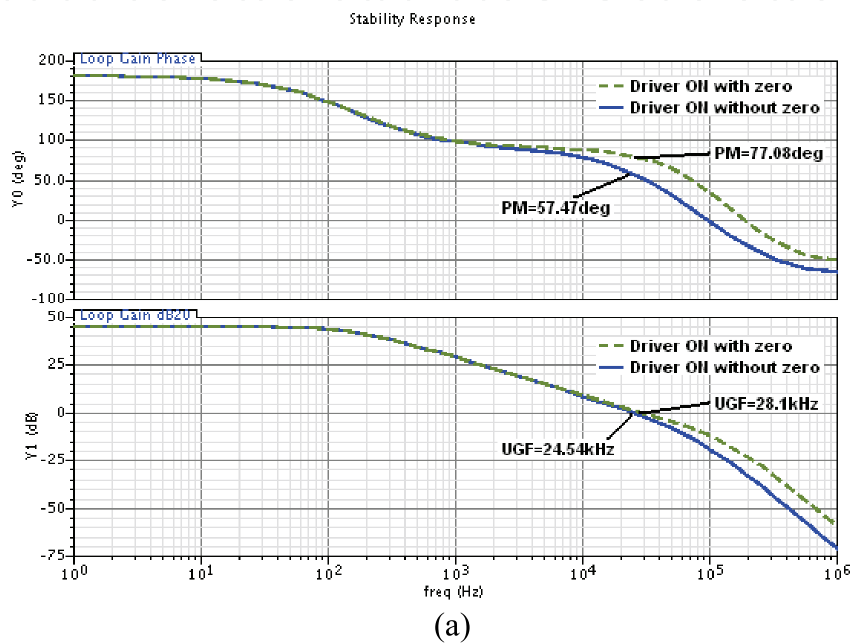
$$z_{hvp01} = \frac{g_{m,hvp01}}{C_{gs,hvp01}},\ z_f = \left(\frac{1}{R_1C_1}\right),\ p_{hvp01} = \frac{1+g_{m,hvp01}\, r_{o,Ibias}}{C_{gs,hvp01}\, r_{o,Ibias}},\ z_{hvn01} = \frac{g_{m,hvn01}}{C_{gs,hvn01}},$$
$$p_{hvn01} = \frac{1+g_{m,hvn01}R'}{(C_{gs,hvn01} + C_L)R'},\ p_f = \frac{R'}{C_1R_1R_2}, \tag{4}$$

where $g_{m,hvp01}$, $g_{m,hvn01}$, $C_{gs,hvp01}$, $C_{gs,hvn01}$ are the trans-conductances and gate capacitances of hvp01and hvn01, respectively, whereas $r_{o,Ibias}$ is the output impedance from the current source I_{bias}. We assume the gains of the SF configurations formed by hvp01 and hvn01 are unity. Also, p_{hvn01} is the pole contributed by hvn01 where $p_{hvn01} = p_{hvn01-ON}$ and $p_{hvn01} = p_{hvn01-OFF}$ when the power FET is ON and OFF, respectively. Typically, the zeros are located at higher frequencies than poles in the SF configuration except for p_{hvn01}. As $C_{L-ON} \approx 270$pF >> $C_{L-OFF} \approx 0$, the pole $p_{hvn01-ON} << p_{hvn01-OFF}$. A double-pole effect before the UGF happens and may lead to instability when $C_L = C_{L-ON} = C_{powerFET}$ when the power FET is ON.

To avoid instability, we designed a feedback-resistive network which creates a medium frequency zero for warranting the stability. Referring to R_1, R_2 and C_1 in Fig. 2,

$$\frac{v_{g,n04}}{v_{reg}} = \left(\frac{R_2}{R'}\right)\left(\frac{1+\frac{s}{z_f}}{1+\frac{s}{p_f}}\right), \tag{5}$$

where V_{reg} and $V_{g,n04}$ are the voltages at the nodes at V_{reg} and gate of n04, respectively. The frequency of the zero, z_f, is lower than the pole frequency, p_f, and this zero can be used to cancel the pole effect of $p_{hvn01-ON}$.



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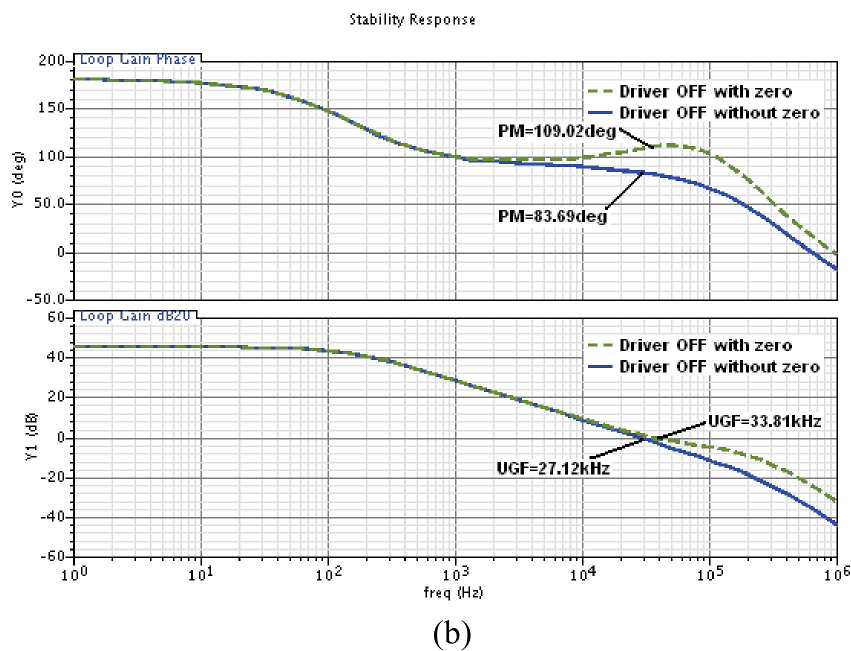


(b)

Fig. 3. (a) Simulated loop gain of the proposed driver with power FET ON; (b) Simulated loop gain of the proposed driver with power FET OFF

In order to have $z_f << p_f$, R_2 should be much smaller than R_1. From Fig. 3, the phase margin is very good even when the power FET is ON. However, if C_1 is not inserted, the double-pole effect will be significant. Results in Table I clearly show the pole-zero cancellation. When the power FET is OFF, the phase margins are around 109° and 83° with and without the zero z_f, respectively. When the power FET is ON, the phase margins are around 77° and 57° with and without the zero z_f, respectively. The differences in phase margin, with and without the zero z_f, are around 20° to 25° in both cases. With the pole-zero cancellation technique, the unity gain frequencies are also larger in both the power FET ON/OFF cases. These differences are significant in stability and transient analyses. The larger the phase margin, the less the ringing is. As the phase margin is larger, the settling time is faster also (Gray et al., 1990). The lab measurement results in Section 3 will demonstrate the steady and fast transient responses of the driver, thereby verifying the usefulness of the pole-zero cancellation technique in this type of regulated gate driver.

2.3 Power-saving: LV devices in HV application

HV devices differ from the normal LV ones in several ways. The size of a HV transistor is much larger than that of a LV transistor (Murari et al., 1995). There are several problems in using HV devices as inverter chains to drive power FETs, namely,

a. Large parasitic capacitance: The larger size HV transistors result in larger parasitic capacitance. The dynamic power, which is the product of the capacitance (C) and the square of the voltage (V), CV^2, is directly proportional to the parasitic capacitance. As a result, the total power consumption of a HV inverter is much higher than that of the LV one. The number of stages also trades off with the rise and fall times of the driver output and subsequently the delay of the driver output signal.
b. Severe V_{GS} limitation for thin-gate devices: Though LV devices are preferred, there is a gate-to-source V_{GS} swing limitation when LV devices are used in HV application. If the gate-to-source voltages of the pMOS and nMOS inside the inverters are above 5V, we must use thick-gate devices. The gate capacitance of the thick-gate devices are large and therefore will slow down the rise and fall times and the propagation delay. It also increases the cost as an extra processing step for thick-gate is needed.
c. Significant power loss in shoot-through current: During switching of the inverter chain, there is a shoot-through current flowing from the V_{reg} node to ground. Such dynamic current causes the V_{reg} voltage to drop (Heydari & Pedram, 2003). Since the operating voltage is 30V, the power of the shoot-through current still contributes much to the power loss.
d. Large die area: using HV-MOSFETs will occupy huge die areas and hence increase the wafer cost.

In the following, we propose solutions to solve the above problems by employing LV devices in HV driver application.

2.3.1 Power saving & thin-gate protection in the regulated driver

In the proposed design, we use all LV transistors (5V) in HV (30V) applications except two HV thin-gate transistors. This approach results in low dynamic power consumption and a small die area. We use LV devices to construct the inverter chain. The supply voltage of the inverters is given by the internal regulator at the V_{reg} node which maintains a 4.8V supply. This node is connected to the source of hvn01 whose drain is connected to V_{DDH}. This

connection ensures that the internal regulator can give sufficient current to the inverter chain to drive the load. The maximum current is limited by the size of hvn01, or the internal supply voltage V_{reg} will go down if the loading current is too large. This regulated driver approach helps protect the thin-gate oxide of the power FET from damage by HV stresses.

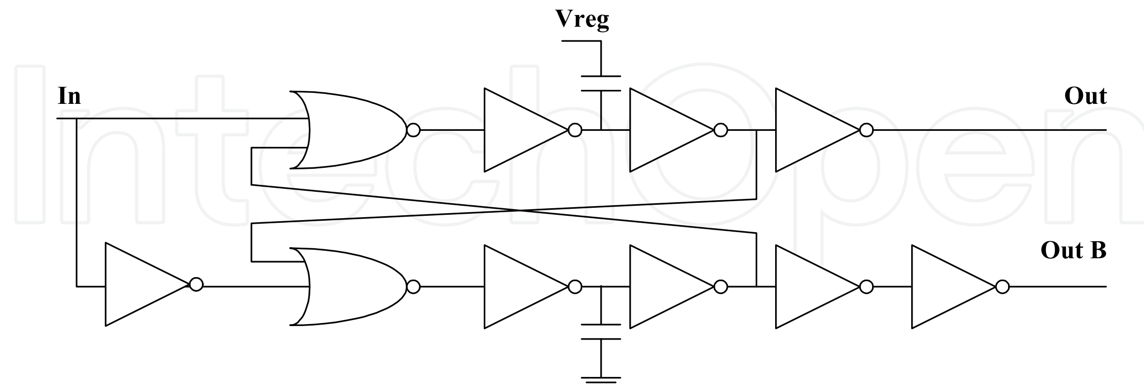


Fig. 4. Dead-time circuit

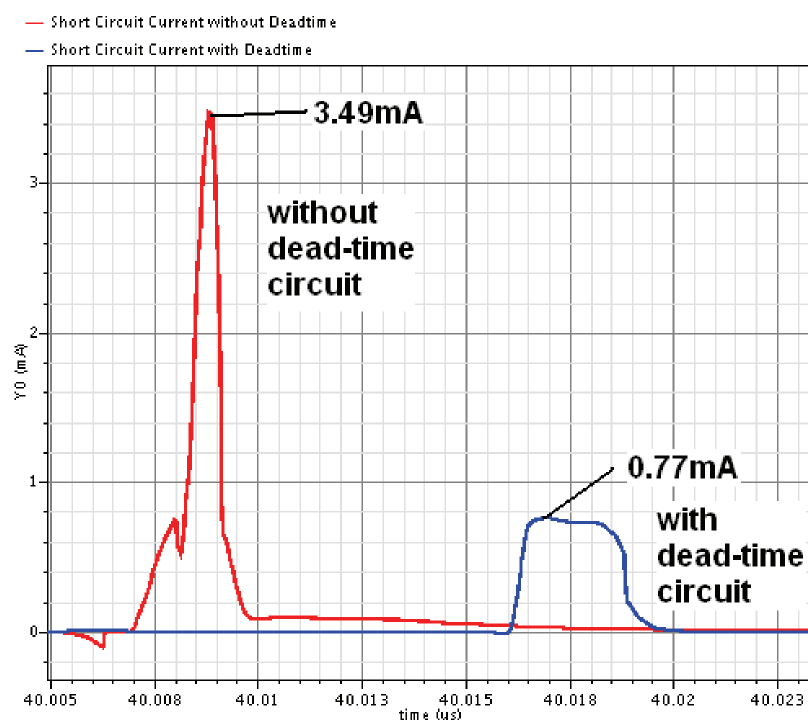


Fig. 5. Shoot-through current

2.3.2 Power saving via dead-time circuit

There are several ways to reduce the shoot-through current. In the proposed circuit, a dead-time control circuit is added for this purpose. This dead-time circuit prevents the flow of shoot-through current by a break-before-make logic. Fig. 4 shows the dead-time circuit and Fig. 5 shows the current going from the V_{reg} node to ground when the driver is charging up the load. Driver with the dead-time circuit only peaks up to 0.77mA, which is one-fifth of the driver without dead-time circuit. The 0.77mA current is mainly due to the switching

activity of the dead-time logic. Since the dead-time circuit eliminates the shoot-through current of the final-stage driver, the driver possesses a higher slew rate and higher efficiency to drive the output capacitive load. The original driver has a 97ns rise time and 39.41V/μs slew rate, while the one with the dead-time circuit is 73ns and 52.06V/μs, respectively. The slew rate is improved by 32% owing to a larger portion of current charging up the output load C_L instead of being shunted to ground as shoot-through current.

2.3.3 Thin-gate protection circuit

Using SF configuration as thin-gate protection circuitry for HV-MOSFET is one of the innovations in this design. Referring to Fig. 2, the gate voltage of hvn01, $V_{G-hvn01}$, is limited by the SF configuration, where the gate voltage of hvn01, $V_{G-hvn01} \approx (V_{DDL} - V_{DS-p04} + V_{GS-hvp01}) \approx (4.5 - 0.2 + 1.2) = 5.5$V. The gate-to-source voltage of hvn01, $V_{GS-hvn01} \approx V_{G-hvn01} - V_{reg} = 5.5 - 4.5 \approx 1$V. The gate-to-source voltage of hvp01 is limited by $V_{DS-n02} + V_{t-hvp} \approx 0.2 + 1.2 \approx 1.4$V. The gate-to-source voltages of both hvp01 and hvn01 are therefore well limited below 5V. In other words, we utilize the SF characteristic where the source voltage tracks the gate voltage and subsequently protects the thin-gate oxide.

3. Simulations and lab. measurements

3.1 High current drive

Fig. 6 shows V_{DDH} vs V_{reg} with V_{DDL} fixed at 5V. Measurement result shows that V_{reg} becomes regulated when V_{DDH} exceeds 7V. The line regulation of V_{reg} from V_{DDH} at 7V to 30V is 0.113mV/V. Fig. 7 shows the transient simulations of the driver. The corresponding lab measurements are shown in Figs. 8-11, and the die photo is shown in Fig. 12. Obviously, the measurement agrees with the simulation results. When the power FET turns ON, the transient output current rises from 0 to 100mA in 525ps, i.e., about 190A/μs. When the power FET turns OFF, the output sinking current is about 120mA. With the large current driving capability, the output can charge a 270pF load within 100ns. That is, the driver is able to operate up to 10MHz even under heavy loading.

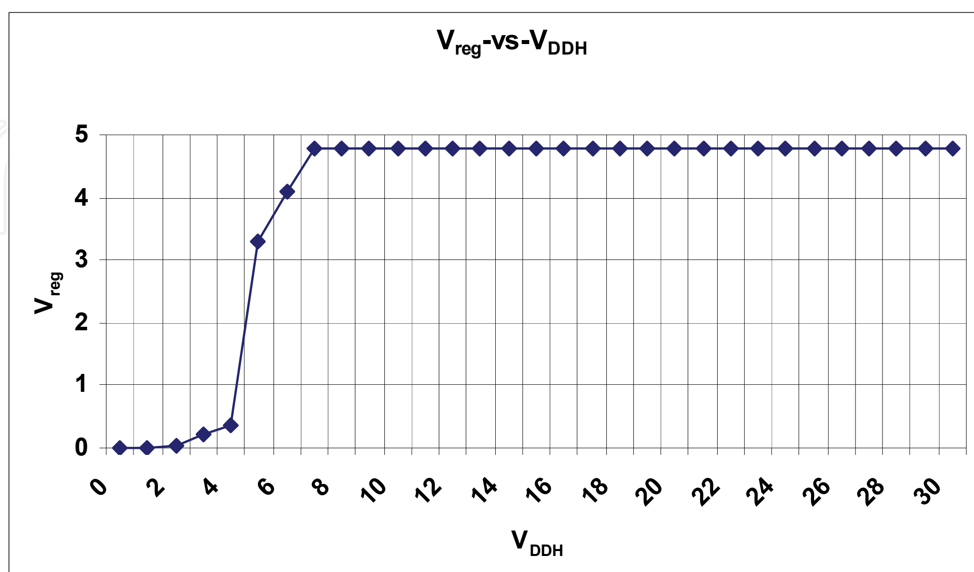
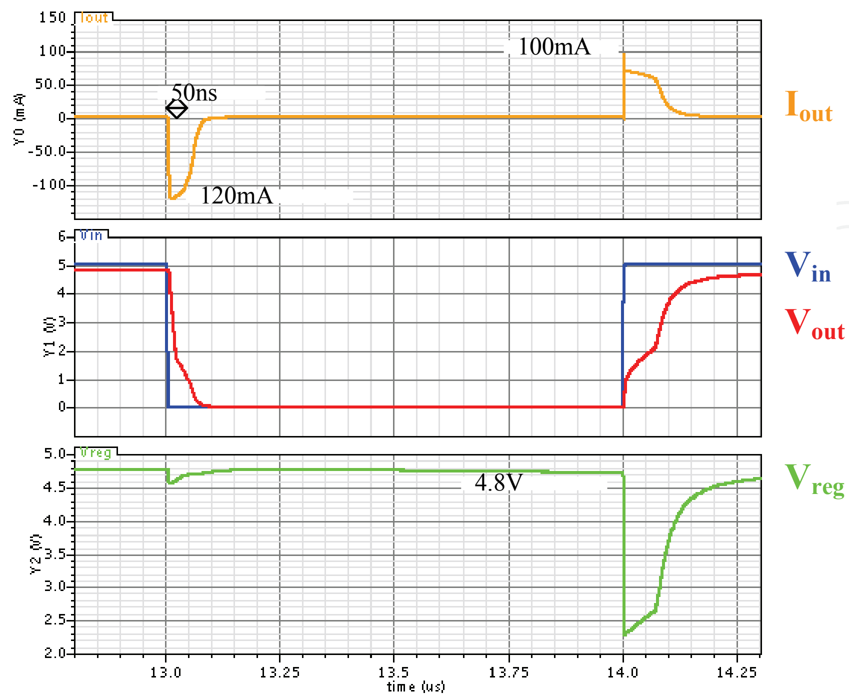
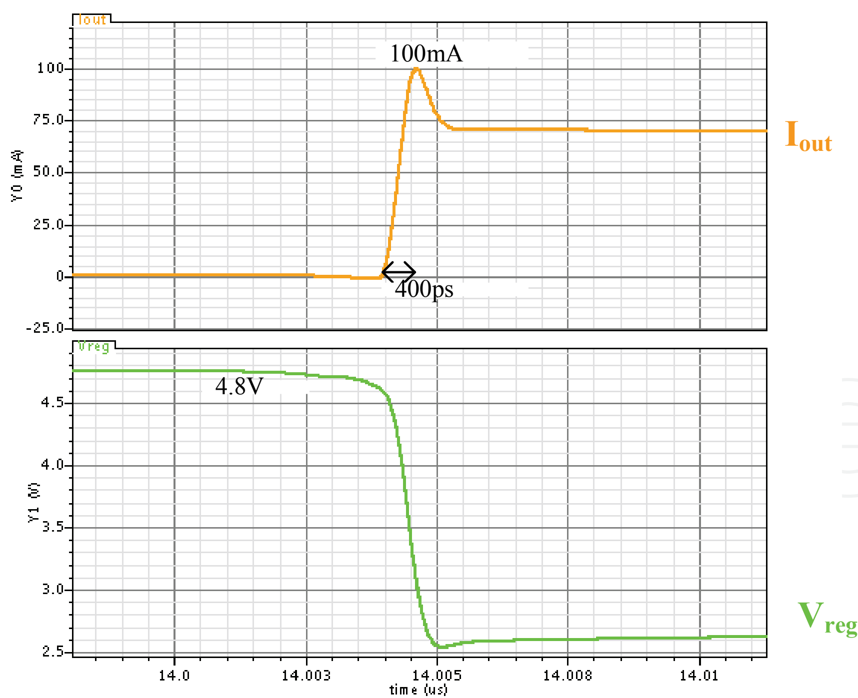


Fig. 6. V_{reg} vs V_{DDH} with V_{DDL}=5V



(a)



(b)

Fig. 7. Simulated transient responses with V_{DDH} = 30V: (a) overall waveforms (b) transient current I_{out} and V_{reg} when charging up output capacitor (gate capacitor of power FET)

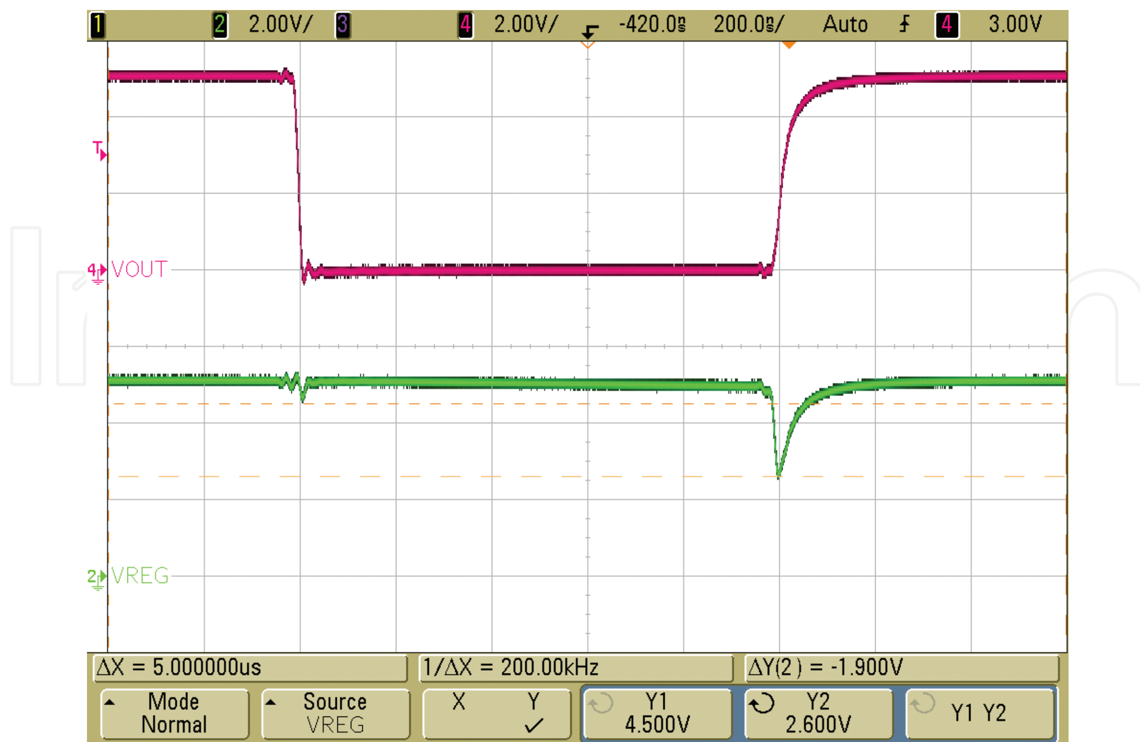


Fig. 8. V_{DDH}=30V; C_L=270pF; Red: V_{out}; Green: V_{reg}. Transient responses of V_{reg} when V_{out} is driving output capacitor (gate capacitor of power FET) (Zoomed in)

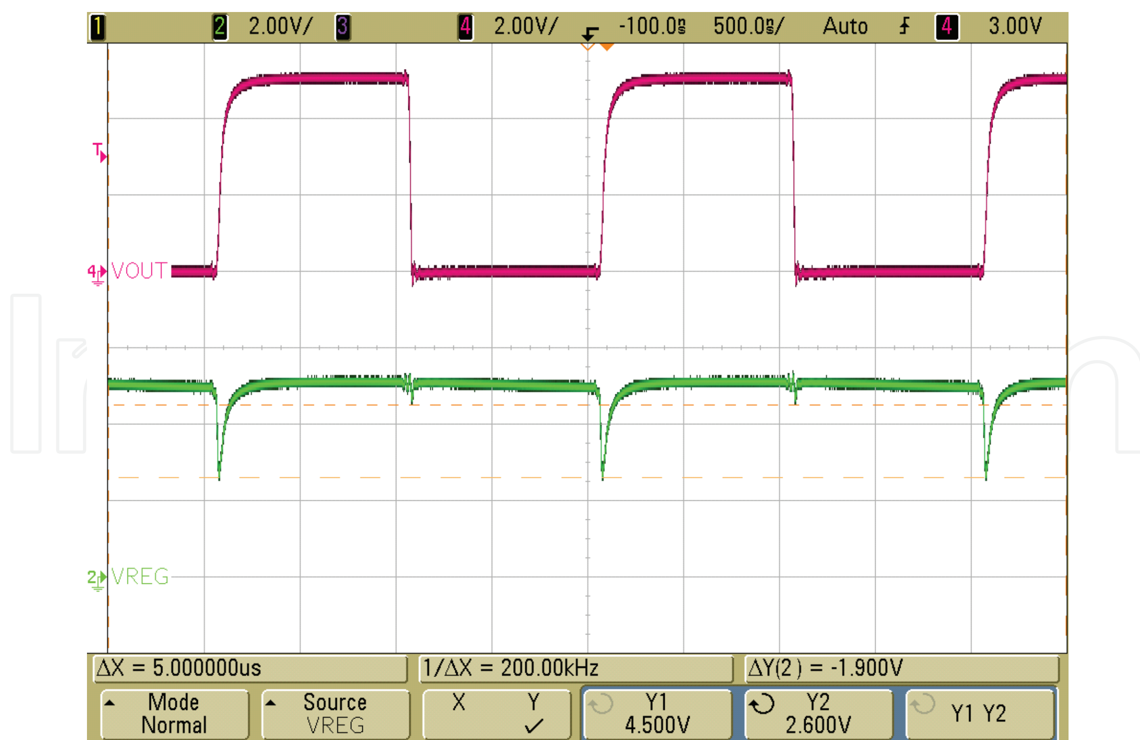


Fig. 9. V_{DDH}=30V; C_L=270pF; Red: V_{out}; Green: V_{reg}. Transient responses of V_{reg} when V_{out} is driving output capacitor (gate capacitor of power FET) (Zoomed out)

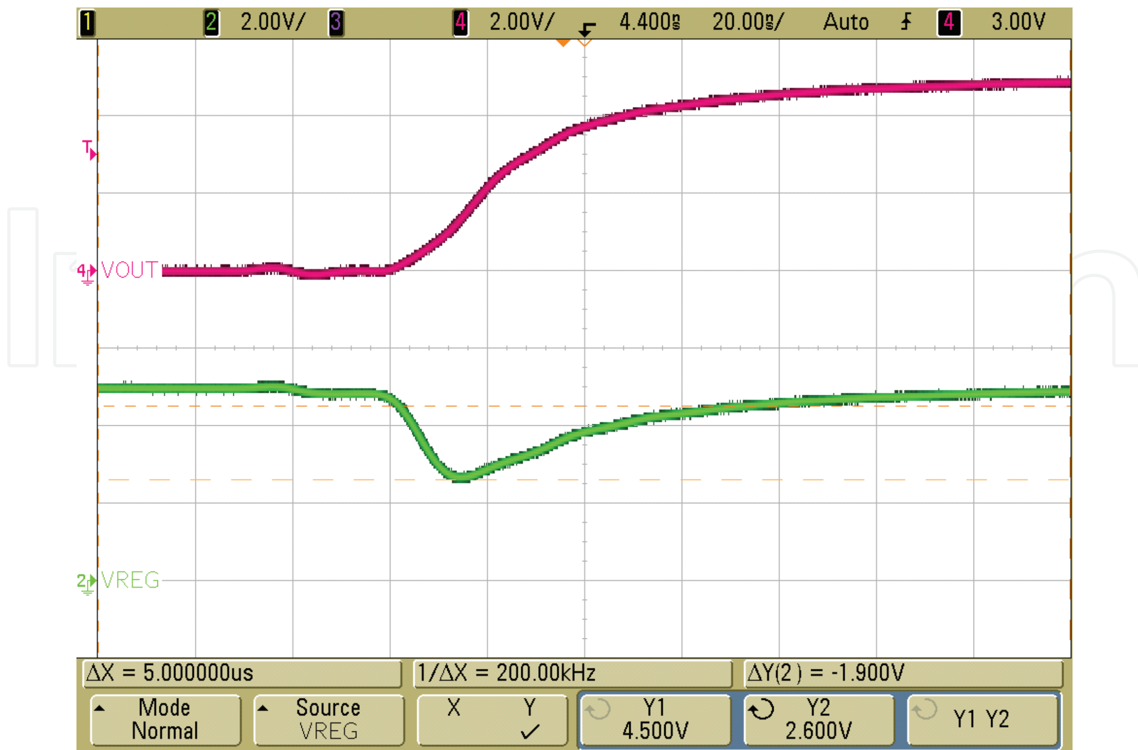


Fig. 10. Rise Time V_{DDH}=30V; C_L=270pF; Red: V_{out}; Green: V_{reg}

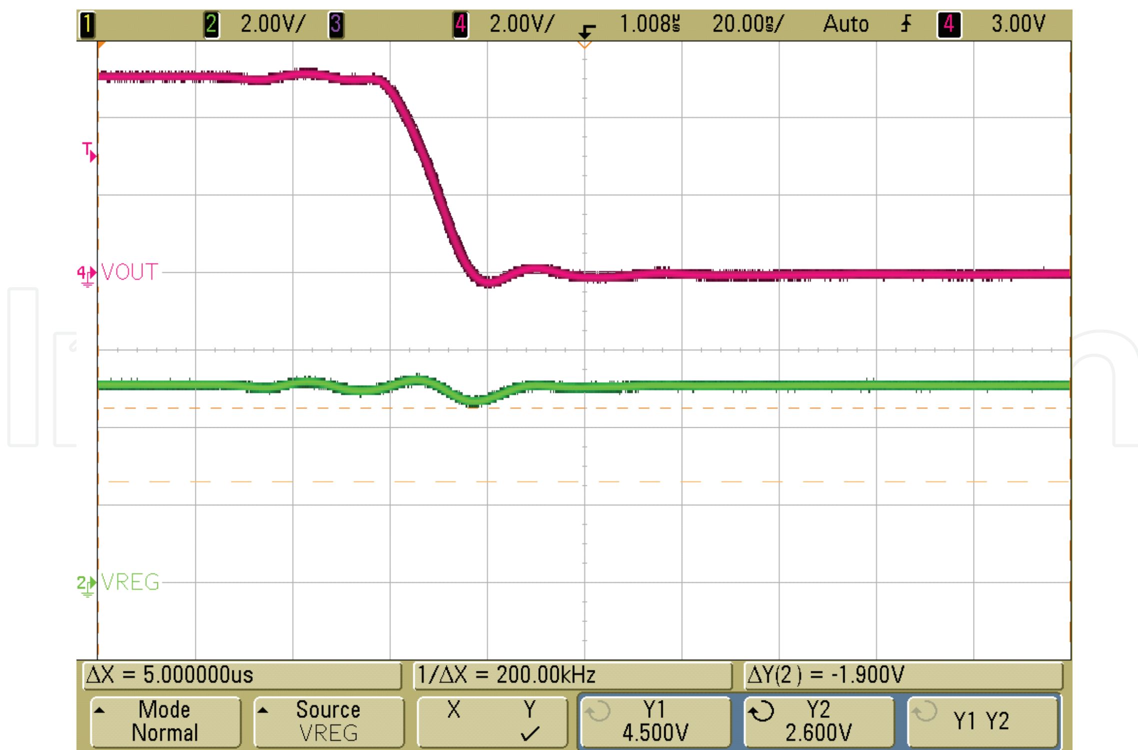


Fig. 11. Fall Time: V_{DDH}=30V; C_L=270pF; Red: V_{out}; Green: V_{reg}

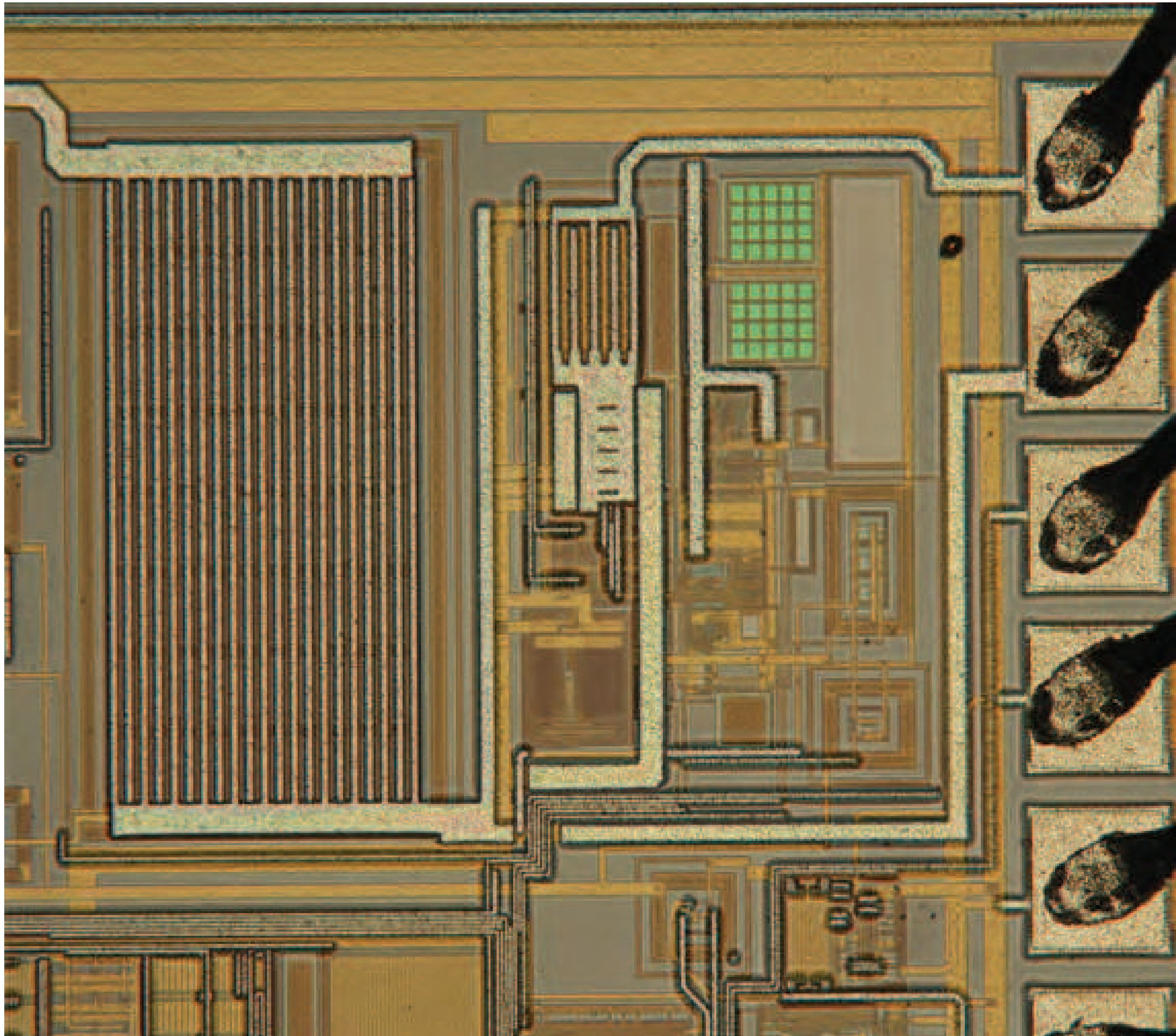


Fig. 12. Die photo of the proposed driver

3.2 Table of comparison

The left part of Table II shows the performance comparison between the proposed driver and other HV circuits with thin-gate protection. Our work features small die area (650μm × 200μm), high slew rate (52V/μs), fast transient current (190A/μs), fast rise (73.8ns) and fall time (17.5ns). The right part of Table II shows the comparison of our work and other drivers, including high-speed LV ones. Our work still features the smallest die area, highest slew rate, and fastest rise and fall times among all CMOS implementations. The bipolar implementation only shows fast rise and fall times under unloaded measurement, and its bipolar nature makes it unattractive for implementation due to high cost.

	This Work	Floating Gate Protection Technique (Chebli et al., 2007)	Low to High Voltage Digital Interface (Declercq et al., 1993)	High-Voltage CMOS OpAmp (Declercq et al., 1993)	Class AB Output Stage Op-Amp (Bales, 1997)	Class AB buffer amp with Slew Rate Enhancement (Lu & Lee, 2002)	Regulated Gate Driver (Tzeng & Chen, 2009)
Process	0.5μm	0.8μm	2.0μm	2.0μm	Bipolar	0.6μm	0.5μm
Die Area	0.13mm²	0.9mm²	N/A	N/A	0.8 mm²	N/A	0.72mm²
Dead-time circuit	√	×	×	×	×	×	×
Load	270pF	100pF	30pF	1000pF	N/A	680pF	2400pF
Slew Rate	52V/μs	N/A	—	15V/μs	N/A	2.41V/μs	N/A
Rise time	73.8ns	474ns	80ns	—	7ns	1.6μs	≈ 670ns
Fall time	17.5ns	445ns	80ns	—	7ns	1μs	N/A
Maximum output current	100mA @charge 120mA @discharge	N/A	N/A	20mA @charge	100mA @charge	N/A	N/A
HV supply, V_{DDH}	30V	60V	75V	75V	N/A	N/A	30V
LV supply, V_{DDL}	5V	5V	5V	N/A	5V	N/A	N/A
Thin-gate oxide Protected ?	Yes	Yes	Yes	Yes	N/A	N/A	N/A
Power	4mW	0.55mW	N/A	N/A	>7.5mW	1mW	546mW

Table II. Performance comparison between this work and similar works

4. Conclusion

A 7V-to-30V high-speed CMOS regulated driver for on-chip thin-gate power MOSFET has been developed. A small die area is achieved by minimizing the number of HV devices. The

HV devices are all thin-gate type and the corresponding V_{GS} and driver output voltages are constrained below 5V by the SF circuit technique. The driver is capable of delivering a fast transient current response of up to 190A/μs when charging up the output capacitor. The maximum charging and discharging currents are 100mA and 120mA, respectively, while keeping the quiescent current to below 90μA at static state for 7V to 30V application. A dead-time circuit is incorporated to reduce 75mW power loss due to shoot-through current. In short, we have developed a thin-gate-protected fast driver using standard HV CMOS process for HV applications with a small die area. This topology is applicable at 30V supply voltage or higher. The stability analysis for compensating this type of regulated driver is also presented to provide useful insights and guidelines for driver IC design.

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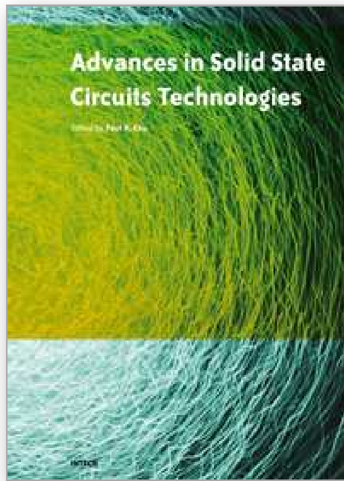

Advances in Solid State Circuit Technologies
Edited by Paul K Chu

ISBN 978-953-307-086-5
Hard cover, 446 pages
Publisher InTech
Published online 01, April, 2010
Published in print edition April, 2010

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How to reference
In order to correctly reference this scholarly work, feel free to copy and paste the following:

David C. W. Ng, Victor So, H. K. Kwan, David Kwong and N. Wong (2010). A 7V-to-30V-Supply 190A/µs Regulated Gate Driver in a 5V CMOS-Compatible Process, Advances in Solid State Circuit Technologies, Paul K Chu (Ed.), ISBN: 978-953-307-086-5, InTech, Available from: http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/a-7v-to-30v-supply-190a-s-regulated-gate-driver-in-a-5v-cmos-compatible-process

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University Campus STeP Ri
Slavka Krautzeka 83/A
51000 Rijeka, Croatia
Phone: +385 (51) 770 447
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InTech China
Unit 405, Office Block, Hotel Equatorial Shanghai
No.65, Yan An Road (West), Shanghai, 200040, China
中国上海市延安西路65号上海国际贵都大饭店办公楼405单元
Phone: +86-21-62489820
Fax: +86-21-62489821

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