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CMOS Integrated Switched-Mode Transmitters for Wireless Communication

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1. Introduction

Power amplifiers (PAs) determine much of the efficiency and linearity of transmitters in wireless communication systems, both on the base station side and in the handset device. With the move to third-generation (3G) communication systems as well as other systems such as Ultra-Wideband (UWB), a higher linearity is required due to envelope variations of the radio frequency (RF) signal. The traditional way of guaranteeing sufficient linearity is backing off the PA; however, this results in a significant drop in efficiency, and thus in reduced battery lifetime for the handheld device and increased cooling requirements for the base station. With the current energy costs, and increased density of base stations, this is fast becoming an important issue.

A second issue in current wireless communication systems is the requirement for a certain range of transmitter output power control, e.g. for 3G systems. Depending on the distance to the base station, a difference in handset output power in the range of tens of dB may occur. If the PA efficiency is peaking for maximum output power, and is reduced considerably for lower output power, the average efficiency of the transmitter calculated over its full output power range of operation will be low. Thus, efficiency improvement for lower output power is an important aspect in transmitter design.

Moreover, current wireless communication handsets require a multi-band/multi-standard approach, so that several communication standards are incorporated in one device. Ideally this would all be achieved by one PA, but current standard is that multiple PAs are used for multiple standards, in worst case each with its bulky, costly output filter.

In order to address efficiency and linearity issues, different transmitter architectures have been proposed and implemented throughout the years, such as for instance Envelope Elimination and Restoration (EER) or Envelope Tracking (ET), varieties of polar transmission where the envelope and phase of the signal are processed separately. Also, different PA architectures have been used, such as Doherty and switched mode amplifiers, often complemented with linearity-improving measures such as digital predistortion or feedback.

With the coming of age of handset production, cost effectiveness has driven wireless communication transceiver design to higher levels of integration. As many building blocks as possible are integrated on the same chip, and the use of external bulky filters is avoided if possible. CMOS technology has been the main choice for this development, due to the possible integration of digital, mixed-signal and analog circuits. However, CMOS was not

suitable for PA design due to frequency, output power, efficiency and linearity requirements. Thus, the stand-alone PA has long been manufactured in III-V technologies or specialized technologies such as LDMOS.

In recent years however, CMOS technology has evolved for radio frequencies in two ways: (1) Decreasing device dimensions have resulted in higher clocking frequencies, thus e.g. providing the opportunity for clocking speeds of several times the RF frequency; (2) The technology provides special RF properties such as thick top metal, allowing for e.g. integrated inductors or transformers with high quality factor. These two technology trends have enabled a higher level of transmitter integration. In combination with the use of switches, for which CMOS devices are extremely suitable, so-called digitally assisted RF transmitters have been designed, that is, transmitters where building blocks are switched on or off by means of digital control signals, or biasing settings are changed based on digital signals.

Recently transmitter design research has taken the next step: increasingly using digital techniques for the full transmitter. A fully integrated GSM radio has been presented with all-digital phase and amplitude signal paths, including an all-digital phase-locked loop. Other examples are a class-E switched mode PA with pulse-width and pulse-position modulation (PWPM) implemented with all-digital blocks, an array of power mixers, controlled by digital logic, and an array of digitally controlled cascode transconductance stages not unlike current-steering digital-to-analog converters, referred to as digital-to-RF conversion. However, efficiency over a wide power range is still a major concern, as will be shown.

In this chapter an overview of switched-mode power amplifiers will be presented. This will be followed by an overview of transmitter architectures suitable for switched-mode transmitters; direct modulation as well as polar and Cartesian modulation will be described by looking at traditional architectures and recent developments, with focus on switched-mode implementations, resulting in a future outlook for integrated transmitter design for wireless communication.

2. Power amplifier technology issues

Generally a switched-mode (SM) amplifier consists of one or more transistors that are behaving as a switch, that is, having an on- and an off-stage, ideally without on-resistance and near-zero raise- and fall time. These conditions can be approximated by heavily overdriving the transistor input, and by operating the device at significantly lower frequencies than the device's f_t. The SM transistor is thus used differently than normal amplifier transistors, which are generally used as either current, voltage or transconductance amplifying elements.

Overdriving the transistor input, however, has certain consequences: the device will act non-linearly, and small-signal models are not always valid. Moreover, for wireless communication applications the difference between operating frequency and device unity gain frequency f_t is rather small – this in contrast to e.g. audio applications, where switched-mode techniques have been used extensively. In this section we will first discuss power amplifier technology issues, and then address losses in switched-mode power amplifiers.

2.1 PA technology aspects

It is only fairly recent that CMOS technology has come up as an alternative for integrated circuit power amplifier design, as CMOS previously was not suitable for PA design due to

frequency, output power, efficiency and linearity requirements. Thus, stand-alone PAs have long been manufactured in III-V technologies such as GaAs or GaN, or specialized technologies such as LDMOS or SiGe bipolar junction transistors.

Largely driven by the drive for integrating more digital functionality on the same chip area, CMOS devices have continued to shrink in device dimensions, basically following Moore's law. Accordingly, transistor f_t and f_{max} are expected to rise to several hundreds of GHz, thus allowing for circuit operation in excess of 100GHz (Niknejad et al., 2007).

However, the trend of shrinking device dimension comes with certain distinct disadvantages for analog circuit design, and more specifically for PA design. Due to shrinking oxide thickness, the breakdown voltage of the devices is reduced, implying that supply voltages must be reduced for safe operation. This has implications for CMOS PAs, as the maximum output power, assuming load-line matching, is then given by

$$P_{out} = V_{DD}^2 / 2R_l \qquad (1)$$

such that in a 50Ω system, and a supply voltage of 1V, the output power is limited to 10mW or 10dBm. Thus, impedance transformation must be used so that the amplifier sees a lower impedance. This is practically limited to 1-5Ω; Having such a low impedance makes the PA efficiency very sensitive to parasitic series resistance in the output network, because of conduction losses: A 0.1mΩ parasitic resistance in series with a load resistance of 1Ω gives a loss of 10%.

Due to these increasing technology limitations, in modern CMOS deep-submicron technologies special transistors are provided having a thicker gate oxide and thus allowing for higher supply voltage.

2.2 Losses in switched-mode amplifiers

Looking at RF power amplifiers, we want to have an output signal at the frequency of interest – usually the fundamental frequency, sometimes a harmonic – but no disturbing output signals at other frequencies. In other words, some filtering must be performed in order to use a switch in a power amplifier.

The ideal waveforms for a switched-mode (SM) transistor in a PA, assuming a broadband load, are shown in Fig. 1. From this figure it can be seen that the voltage and current are ideally never non-zero simultaneously, thus no power is consumed, and ideally a 100% efficiency can be achieved. However, considerable power is generated at harmonic frequencies. Thus the maximum theoretical efficiency for this broadband SM PA is slightly larger than 80%, achieved at a 50% duty cycle.

In order to reduce the power present in harmonic frequencies, a tuned amplifier can be used. This can be implemented in several ways. One way is by introducing harmonic shorts in parallel to R_l in Fig. 1, so that harmonics other than the desired frequency are grounded. The maximum theoretical efficiency now reaches 100%, however, for relatively low duty cycles (and thus very short pulses and low output power) (Cripps, 1999, p. 153).

Another strategy is to have a resonance circuit in series with R_l, to make sure that only the desired frequency signal is passed on. This issue will be explored more in the section on class-F amplifiers.

Device and switching losses

Aside from the harmonic losses discussed in the previous section, some other losses can be identified in a SM amplifier/transistor (El-Hamamsy, 1994). First of all, the transistor will
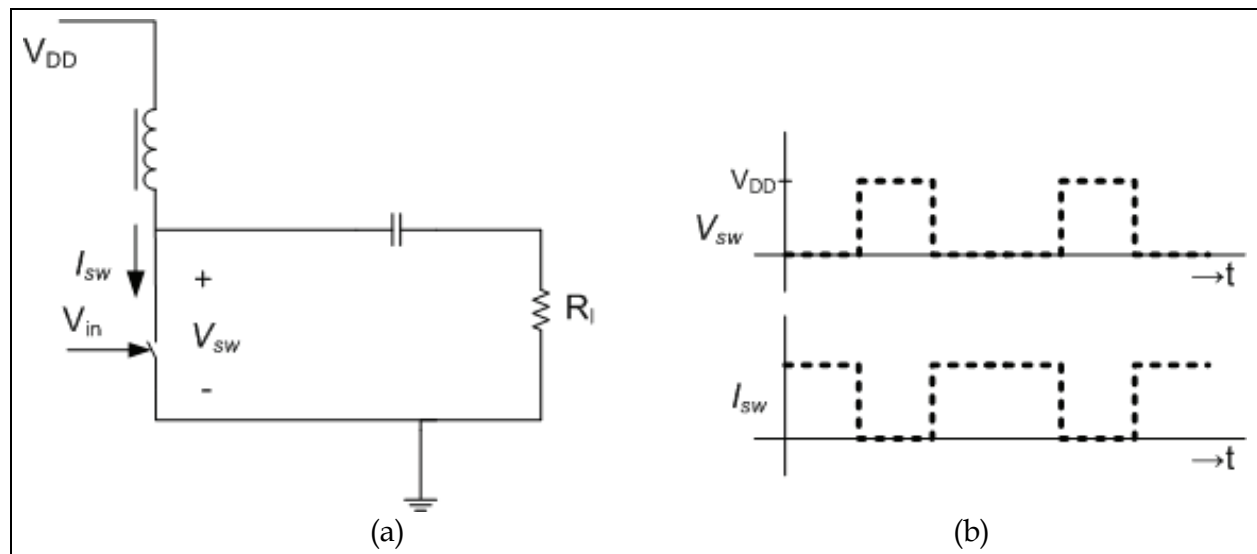
Fig. 1. An ideal switched-mode (SM) power amplifier, (a). Schematic, (b). Voltage and current waveforms.

suffer from non-idealities, of which one is a non-zero on resistance. This will cause a non-zero voltage drop and thus so-called conduction loss, resulting in reduced efficiency.

Secondly, the transistor will have non-zero rise- and fall times, potentially causing the current and voltage to be non-zero simultaneously. Also CMOS subthreshold current will contribute to this.

Thirdly, dynamic losses due to charging and discharging of parasitic capacitors must be taken into account – the switching losses. These are proportional to the switching frequency f, and will likely dominate for RF applications.

Other losses

External elements such as output networks may cause losses as well, for example a tuning or impedance transformation network consisting of on-chip or discrete passive elements. These inductors and capacitors will include parasitics such as capacitances or series resistances. These may cause power dissipation and thus reduce the amplifier efficiency.

A MOSFET is very suitable as a switch, toggling between the *off* mode for low gate-source voltage V_{GS}, and the triode region for high V_{GS}. The *on* resistance of the device is then given by

$$R_{on} = (L/W) \cdot (k'(V_{GS} - V_t - V_{DS}))^{-1} \tag{2}$$

where L is the transistor length, W the transistor width, k' the transistor gain factor, V_t the threshold voltage, and V_{GS} and V_{DS} the gate-to-source and drain-to-source voltage, respectively.

The *on* resistance can thus be minimized by choosing a large ratio W/L. Having a low resistance decreases the conduction losses caused by the switch. Other considerations of interest for PA design are the current density capacity and parasitic capacitances. The former is important if high output power is desired and the supply voltage is low. A larger width increases the current capacity. The parasitic capacitance may, however, cause increased dynamic losses, thus potentially decreasing the efficiency especially at high frequencies.

3. CMOS switched-mode power amplifiers

Now that general technology issues have been discussed, SM amplifiers for radio frequencies will be addressed in this section, and an overview will be given of specific CMOS implementations.

3.1 Switched-mode amplifier classes

In amplifier theory, several different switched-mode types are established: the classes D, E and F (Cripps, 1999; Raab, 2001). They will briefly be addressed below, before looking into CMOS implementations in the next section.

Class-D

Class-D amplifiers use a double-switch structure, with a series resonance circuit (see Fig. 2). The output current is alternatingly supplied by each switch, similar to a push-pull configuration. The simplest implementation for the two switches is an inverter. The maximum theoretical efficiency is 100%, with a square-wave voltage and a half-wave rectified sine wave current in each device. In that case the voltage contains only odd harmonics, and the current even harmonics.
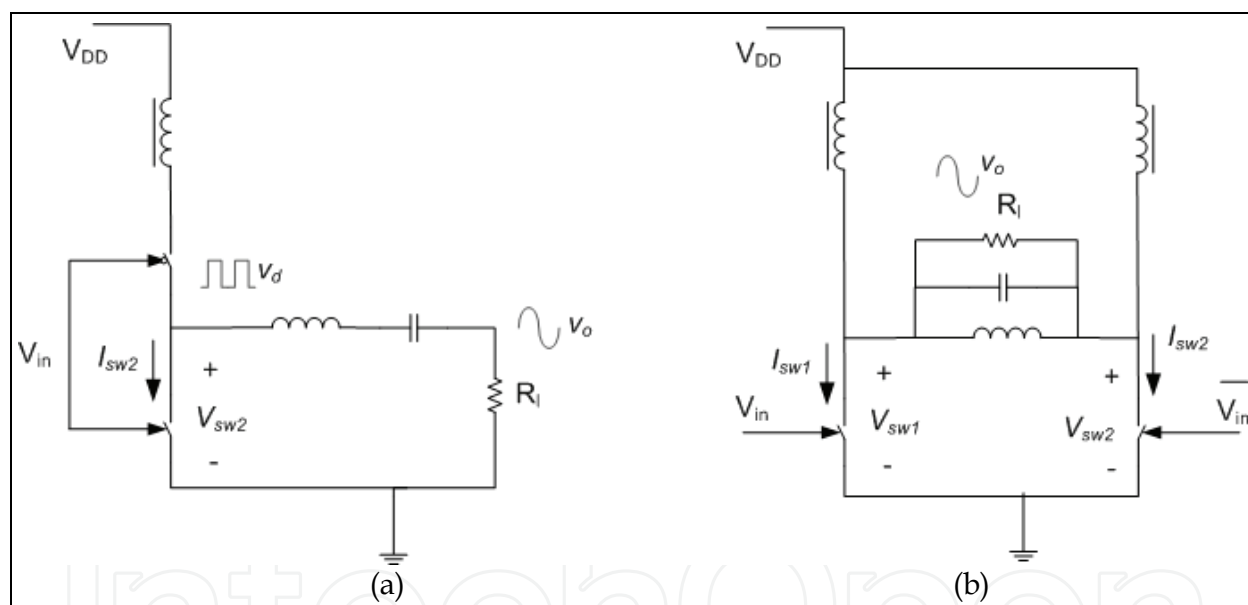

Fig. 2. Simplified schematic of a class-D amplifier, (a). A voltage-mode amplifier, (b). A current-mode amplifier.

This amplifier may also be implemented as current-mode (see Fig. 2b). Instead of having a series resonance circuit in series with the load, a parallel resonance circuit is then used at the output of the amplifier. In that case the current approximates a square-wave, containing odd harmonics, while the drain voltage for each device approximates a half-wave rectified sine wave. It has been shown that a high efficiency can be achieved, assuming the amplifier can be designed for Zero Voltage Switching (Long et al., 2002; Kobayashi et al., 2001).

Class-E

A class-E amplifier consists of a single switching device with a carefully tuned output network. The voltage derivative, close to the timing point when the device is switched off, is

designed to be very small (so-called Zero Voltage Switching, ZVS) so that potential static losses are kept very low. Also for this amplifier the theoretical maximum efficiency is 100%. One of the characteristics of class-E is that large voltage peaks occur; thus, care must be taken to avoid high voltages across the CMOS device, as the breakdown voltage of CMOS devices is relatively low.

Class-F

A class-F amplifier is basically an amplifier with a current that approaches a half-wave rectified sine wave, and a voltage that approaches a maximally flat shape. Tuning a limited number of odd-order harmonics of the fundamental signal is used to achieve this. Two different structures are in use for class-F design, depending on which harmonics are seen at the drain: Regular class-F for odd-order harmonics, that is, the voltage is approximately maximally flat, and inverse class-F for even harmonics, i.e. a half-wave rectified sine wave-shaped drain voltage and a maximally flat shaped drain current (Raab, 2001). It must be noted that the inherent pulse shaping makes this amplifier less suitable for e.g. Pulse Width Modulated (PWM) input signals (Sjöland et al., 2009).

All three amplifier classes depend to some extent on a frequency-selective output network. Thus, their operation cannot be considered broadband. Either they can only be used in a narrow, specific frequency range, or each amplifier's behavior may show significant differences depending on the frequency of operation.

Research is progressing into variable output networks, where digital control signals are used to e.g. change the frequency of operation, or reconfigurable PAs, as well as output networks allowing for concurrent multi-band operation (Colantonio et al., 2008). In such digitally assisted systems the use of CMOS technology, also for the PA, may lead to a higher level of integration. This will be addressed more extensively in the section on transmitter architectures.

3.2 CMOS PA implementations

By the mid-1990s, the first publications on integrated CMOS PAs for RF appeared. These works initially focused on more or less linear amplifier structures such as class A, AB, B or C, but research has since then focused more on the switched-mode class-D, E and F, as higher clocking or switching speeds became available with improvements in CMOS technology.

Su and McFarland (1997) presented a 0.8μm CMOS SM amplifier consisting of four stages with the final stage in switched-mode. A Power-Added Efficiency (PAE) of 42% was achieved at 850MHz with a 2.5V supply, and largely off-chip input and output matching networks were used. Yoo and Huang (2001) presented a 0.25μm CMOS class-E PA, using a finite DC feed inductor to reduce the peak voltage over the device, as well as Common Gate (CG) switching instead of the more usual Common Source (CS) structure. These strategies allow for a higher supply voltage to be used, thus reducing the necessity for a low load impedance.

Reynaert and Steyaert (2005) have presented a fully integrated 0.18μm CMOS class-E PA, consisting of three stages and including supply modulation to provide amplitude variation. A PAE of 34% was achieved for an output power of 23.8 dBm, using a supply voltage of 3.3 V and extra thick gate oxide for the final stage.

As limited supply voltage is one of the major challenges in CMOS PA design, other strategies have been used to effectively add the output voltages, such as using a transformer

to combine output power (Aoki et al., 2008; Haldi et al., 2008) or stacking devices, making sure that the voltage over each device stays below the maximum (Stauth & Sanders, 2008; Jeong et al., 2006). However, generally this slightly impairs the efficiency, counteracting the intended advantage of a higher supply voltage. Apart from voltage stacking, current combining has been implemented (Kavousian et al., 2008; Kousai & Hajimiri, 2009), as well as the switching in of several parallel stages (Walling et al., 2008). The latter two will be covered more in the section on transmitter architectures.

Reference	Class	Technology	Supply voltage	Output power	Efficiency (PAE)	Frequency
Su et al., 1997	D?	0.8μm CMOS	2.5 V	30 dBm	42%	850 MHz
Tsai et al., 1999	E	0.35μm CMOS	2.0 V	30 dBm	48%	1.9 GHz
Yoo et al., 2000	E	0.25μm CMOS	1.9 V	30 dBm	41 %	900 MHz
Kuo et al., 2001	F	0.2μm CMOS	3.0 V	32 dBm	43 %	900 MHz
Sowlati et al., 2003	?	0.18μm CMOS	2.4 V	24 dBm	42 %	2.4 GHz
Reynaert et al., 2005	E	0.18μm CMOS	3.3 V	24 dBm	34 %	1.75 GHz
Stauth et al., 2008	D	90nm CMOS	2.0 V	20 dBm	38.5%	2.4 GHz

Table 1. An overview of CMOS integrated switched-mode power amplifiers.

4. Transmitter architectures

As we have seen before, one of the basic requirements for power amplifiers in modern wireless communication systems is to accommodate envelope variations and to provide variable output power. Wireless communication standards have moved from constant-envelope, low- channel bandwidth to more complex signal shapes in order to increase data rates in limited bandwidth, resulting in variable envelope RF signals and larger channel bandwidths in the range of tens of MHz.

In SM amplifiers output power variation can be achieved by varying the supply voltage, by varying the duty cycle of the signal, by varying the load, or by a combination of these. In this section some transmitter architectures will be discussed that adopt such strategies; only the strategy of varying the load impedance will not be addressed here.

4.1 Supply variation

On the transmitter architecture level, one of the classical methods of varying the output power is based on polar modulation, where a baseband Cartesian signal $v_{RF}(t)$ is first converted into its polar form, separating envelope (amplitude) and phase information, which are then processed separately and combined before being transferred to the antenna:

$$\begin{aligned} v_{RF}(t) &= I(t) \cos(2\pi f_0 t) \cdot + Q(t) \sin(2\pi f_0 t) \quad \text{(Cartesian)} \\ &= A(t) \cos(2\pi f_0 t + \varphi(t)) \quad \text{(polar)} \end{aligned} \tag{3a}$$

where

$$\begin{aligned} A(t) &= \sqrt{(I(t)^2 + Q(t)^2)} \quad \text{(amplitude)} \\ \varphi(t) &= \tan^{-1}(I(t) / Q(t)) \quad \text{(phase)} \end{aligned} \tag{3b}$$

Polar modulation is recently gaining more and more interest due to its potential to maintain linearity while having a relatively high efficiency even for lower output power, thus improving the average efficiency over a wide output power range.

One of the most well-known polar schemes is Envelope Elimination and Restoration (EER), brought to attention by Khan (Khan, 1952; Wang et al., 2006; Su & McFarland, 1998). The envelope is used to control the PA supply level, while the phase signal is upconverted to RF and transformed to a constant envelope signal, driving the PA input. Thus, a non-linear PA can be used. Su and McFarland (1998) have demonstrated a CMOS implementation of an EER system, including a delta-modulated supply, a limiter, and envelope detectors, driving a switched-mode PA, resulting in significant linearity and efficiency improvements.
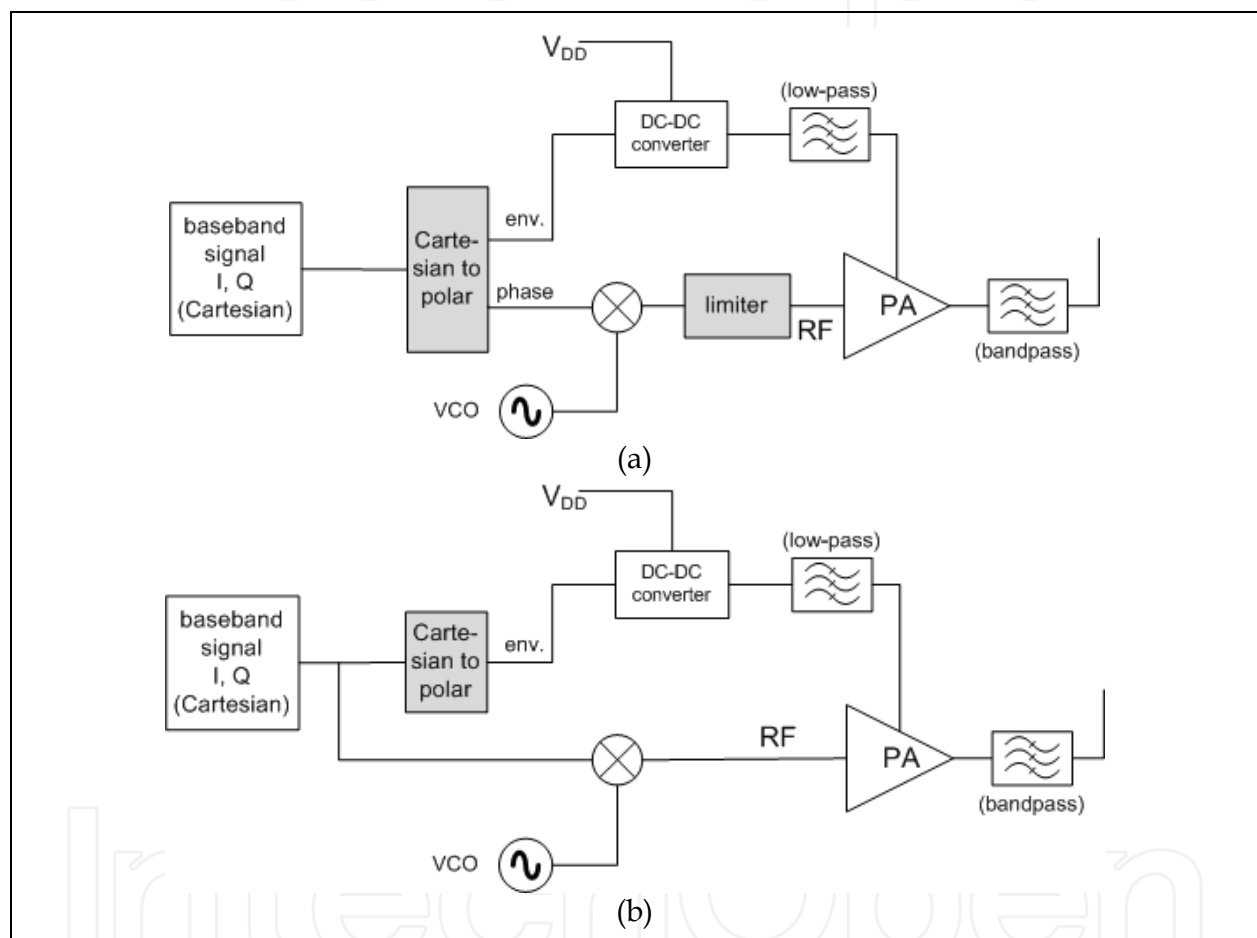
Fig. 3. Simplified representation of the Envelope Elimination and Restoration (EER) and Envelope Tracking (ET) transmitter architectures.

Envelope tracking (ET) describes a transmitter architecture where the Cartesian RF signal is amplified by means of a linear amplifier, with its supply controlled by the envelope of the signal (Hanington et al., 1999; Takahashi et al., 2008). One of the main advantages is that the bandwidth of the PA input signal is not expanded, but a linear amplifier generally has a lower efficiency than a SM amplifier. However, requirements on the envelope signal and timing are less stringent (Wang et al., 2006). So-called hybrid EER architectures have been demonstrated, where the ET linear amplifier is replaced by a SM amplifier, however, still driven by the full Cartesian RF signal (Wang et al., 2006).

Both the EER, ET and hybrid EER depend on utilizing an efficient power supply modulator, that must be able to handle the bandwidth of the envelope signal. For this, a boost dc-dc converter, a Buck dc-dc converter, or a switched-mode low-frequency amplifier can be used, controlled by a Pulse Width Modulator (PWM), a Sigma-Delta modulator ($\Sigma\Delta$M) or a Delta modulator (ΔM) (Kitchen et al., 2007). Generally, independent of supply modulator type, a bulky low-pass filter must be used to filter out undesired signals such as noise or harmonics.

4.2 Changing the duty cycle

If the duty cycle D of a square-wave signal is changed, the output power at the fundamental frequency will be changed according to

$$P_{out}(f_0) = (4V_{DD}^2/\pi^2 R_l)\ sin^2(\pi D) \tag{4}$$

assuming ideal frequency selection at the output. This can be used to accommodate the envelope and power variations in a polar transmitter, by changing the amplifier's threshold voltage. Implementations exist with discrete steps as well as continuous change (Yang et al., 1999; Cijvat et al., 2008; Smely et al., 1998). A major advantage of these strategies is that no DC-DC converter is necessary; A disadvantage is that linearity may be worse compared to an amplifier where the supply voltage is changed, possibly resulting in tougher requirements for digital predistortion. Moreover, the efficiency drops rapidly at small duty cycles (Cijvat et al., 2008).

Smely et al. (1998) combined discrete supply voltage steps with changing the drain current of the output stage of a class-F stage by means of varying the GaAs MESFET gate voltage, depending on the amplitude of the input signal. Yang et al. (1999) focused on improving the efficiency of a class-A amplifier, by using variable bias to change the current in the output stage as well as changing the supply voltage.

Variable gate bias was used (Cijvat et al., 2008) for CMOS class-D amplifiers, with the goal of creating a PWM signal at the output of the amplifier. The proposed architecture uses the envelope signal to control the gate bias, and the RF signal is assumed to be sinusoidal, containing only the phase information.

For this amplifier structure, loss mechanisms as discussed in section 2 cause a drop in drain efficiency for lower output powers. It is likely that switching and harmonic losses are significant; the amplifier switches as often as for full output power, thus having roughly the same switching loss, and the harmonic content of a PWM signal increases for duty cycles other than 0.5, thus increasing harmonic losses. As can be seen in Fig. 4.b, the amplifier aimed for higher output power, having larger output devices and thus larger parasitic capacitances, reaches a lower maximum drain efficiency as a result.

As was addressed by Sjöland et al. (2009), one of the challenges of polar modulation is the sharp notch in amplitude variation which causes fast amplitude variations that are difficult to track for a DC-DC converter with limited bandwidth. Thus, a combination of EER and Pulse Width Modulation is proposed. This is applied to the aforementioned 130 nm CMOS class-D inverters, and simulation results are presented in Fig. 5.

It can be seen from this figure that efficiency gains of EER and PWM combined are minimal in this case, compared to EER-only. Moreover, combining the two strategies will lead to greater transmitter complexity; the additional power that is required is not taken into account in the simulations. However, as was mentioned earlier, this solution may address the bandwidth limitations of EER.

(a)   (b)
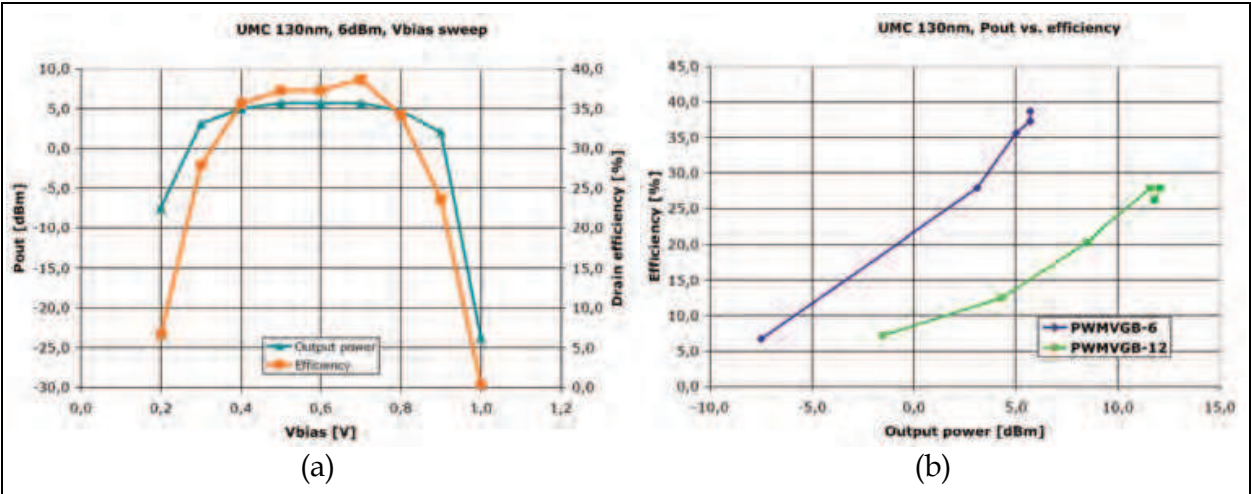
Fig. 4. (a). Measured output power and efficiency of a 6 dBm 130nm CMOS class-D inverter chain, using gate bias variation to create a pulse width modulated inverter output voltage (Cijvat et al., 2008). (b). Efficiency versus output power of two amplifiers, one with 6dBm and one with 12 dBm output power. The supply voltage was 1.2 V. The 6 dBm amplifier operated at 1.5 GHz, the 12 dBm amplifier at 1 GHz.
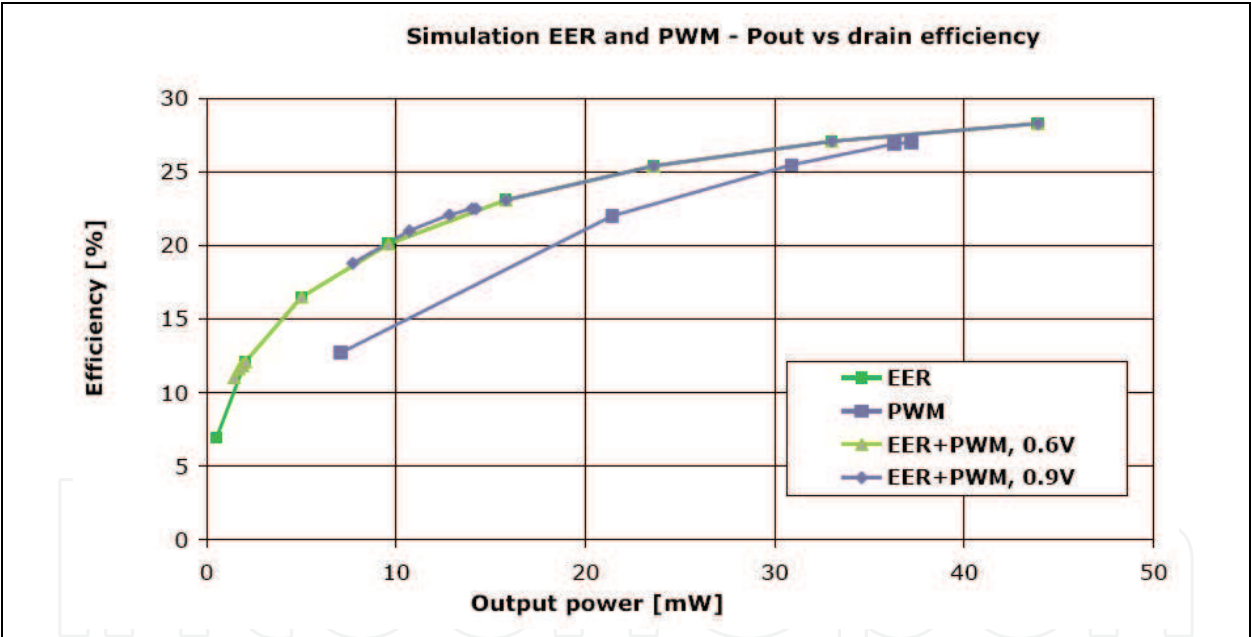

Fig. 5. Simulated PA drain efficiency versus output power, combining EER modulation for high amplitudes and PWM for lower amplitudes. The voltage where EER takes over is varied; one curve shows results for a border value of 0.6V and the second curve for a border value of 0.9V.

4.3 Burst-mode transmitters

A third method for varying the output power is so-called burst mode transmission. Effectively the RF signal is turned on and off by means of a bit stream. The envelope signal may be digitized e.g. by means of a ΣΔ or a Pulse Width Modulator (Jeon et al., 2005; Berland et al., 2006; Stauth & Sanders, 2008).

A burst-mode pulsed power oscillator to be used as a final stage in a transmitter was presented by Jeon et al. (2005). The oscillator is turned on and off by a PWM representation of the low-frequency envelope signal, thus resulting in the high-frequency RF signal multiplied by the PWM signal, appearing as bursts at the oscillator output. An isolator and bandpass filter are used to prevent reflected power to return into the oscillator and filter out undesired frequency components.

Berland et al. (2006) analyzed two varieties of using a one-bit signal to be multiplied with the slightly modified Cartesian signal. The one-bit signal was derived from the envelope signal by utilizing a Pulse Width Modulator and a Sigma-Delta Modulator, respectively. A high operating frequency of several GHz is, however, necessary to reach sufficient performance.

A polar modulator using a baseband ΣΔM and an RF Pulse Density Modulator (PDM) were used to drive a class-D amplifier with a 1-bit signal (Stauth & Sanders, 2008). This solution, basically all-digital, was implemented in 90nm CMOS and the cascade PA operated from a 2V supply. The PA performance can be seen in Table 1. The Bluetooth 2.1+EDR spectral mask was met for an output signal in the range of 10dBm, including a bandpass filter at the output.

4.4 Digitally controlled TX

In analogy to current-steering Digital-to-Analog converters (Zhou & Yuan, 2003), a fourth strategy to control output power has recently gained attention, which is switching in parallel stages. One example is the work by Kavousian et al. (2008), where the low-frequency envelope of the polar signal was transformed into a thermometer code used to switch on and off unit stages, while the constant-envelope RF phase signal drives the input of each stage. The authors refer to this as digital-to-RF conversion.

Shameli et al. (2008) used 6 control bits to both switch in a number of parallel output stages and at the same time change the supply voltage with a ΣΔ modulator. A 62 dB power control range was achieved, as well as a 27.8dBm maximum output power and an average WCDMA efficiency of 26.5%.

Current summing was also used by Kousai and Hajimiri (2009), utilizing 16 parallel power mixers and a transformer at the output. The phase information modulates the high-frequency digital LO signal. Linearization could be chosen to be analog, by sensing and feeding back the signal level for each mixer core, or digital, by using a thermometer code for the envelope signal, switching on and off mixer cores. Both the baseband and the LO signal where controlled digitally with a number of bits. A 16-QAM (Quadrature Amplitude Modulation) signal at 1.8 GHz and a symbol rate of 4 MSym/s was reproduced with an output power of 26 dBm, a PAE of 19% and an EVM (Error Vector Magnitude) of 4.9%.

Presti et al. (2009) used 7-bit thermometer + 3 bit binary weighted current summing combined with analog input power control for low-power levels. Relative broadband operation, 800-2000 MHz, and a 70dB power control range is achieved. With Digital Pre-Distortion (DPD) both WCDMA, EDGE and WiMAX specifications are met.

In these architectures no supply voltage modulator is used. Sufficient resolution to achieve a high linearity or amplitude accuracy is achieved by increasing the number of parallel stages. However, the efficiency of these current-summing amplifiers follows a class-B curve (Presti et al., 2009):

$$\eta \propto \sqrt{P_{out}} \qquad (5)$$

Walling et al. (2008) used control bits to generate a suitable Pulse Width/Pulse Position (PWPM) signal, which was then provided to four class-E quasi-differential stages. In a 65nm technology, a maximum output power of 28.6 dBm and PAE of 28.5% is achieved at 2.2 GHz with the output stage using a supply voltage of 2.5 V. For a 192kHz symbol rate, non-constant envelope π/4-DQPSK (Differential Quadrature Phase Shift Keying) modulated signal, an output power of 27 dBm is achieved with an EVM of 4.6%.

4.5 Direct RF modulation

A third strategy to process the signal is to directly modulate the RF signal into the SM amplifier. For instance, a Pulse Width/Pulse Position modulator (PWPM) or a Sigma-Delta (ΣΔ) modulator can be used (Nielsen & Larsen, 2008; Wagh & Midya, 1999). This is depicted in Fig. 6. A major disadvantage however is that generally a high sampling or operating frequency is necessary, typically at least $4f_{RF}$, in order to achieve the desired resolution. This implies a large power consumption in the modulator, as this is directly proportional to the frequency. Moreover, since the PA switches more often, more switching loss will occur, reducing the efficiency.
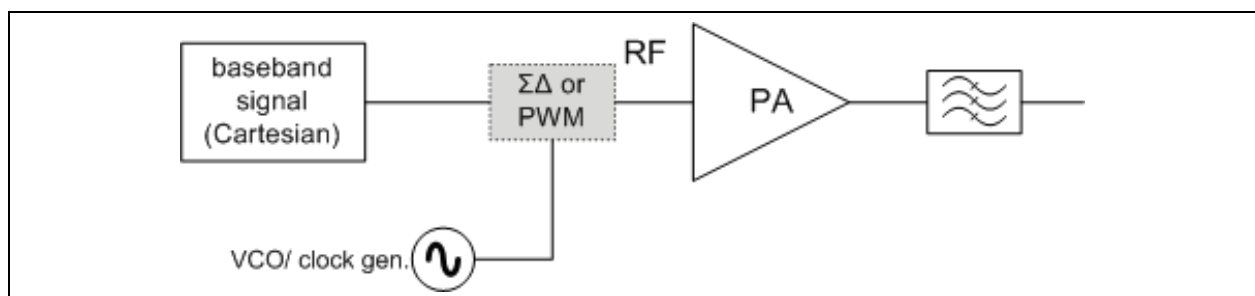

Fig. 6. Direct modulation of the RF signal by means of Sigma-Delta (ΣΔ) or Pulse Width Modulation (PWM).

Wagh and Midya (1999) presented the concept of Pulse Width Modulation for RF. Nielsen and Larsen (2008), utilizing GaAs technology, used a feedback circuit and a comparator to generate an RF PWM signal. The signal's adjacent channel power ratio stayed well below the UMTS spectrum mask, allowing for some non-linearity from a subsequent PA.
Direct modulation was also proposed by Jayaraman et al. (1998), utilizing a bandpass ΣΔ modulator, simulated with GaAs HBT technology. Discussions on efficiency were presented, and it was indicated that the linearity demands were moved from the PA to the ΣΔM.

4.6 Cartesian modulation

Even though polar modulation has some distinct efficiency advantages, as an alternative Cartesian modulation may be used, that is, the *I* and *Q* baseband signal that differ 90° in phase are each processed in the transmitter and then summed either directly before the PA, or alternatively, each signal is amplified and the two signals are combined after the amplifiers. An advantage is that the signal is not transformed into its amplitude- and phase component, a non-linear transformation putting tough requirements on the delay and recombination of the two signals.
Bassoo et al. (2009) have proposed a combination of Cartesian and polar modulation, where the SMPA input signal is a SD modulated Cartesian signal divided by the amplitude signal, which may be more or less bandlimited (see Fig. 7). Analysis showed that the envelope

signal can be limited to 75% of the channel bandwidth without impairing the efficiency, still keeping OFDM clipping limited and EVM very low. Thus, a combination of EER and PWPM can be used to have a high efficiency over a wide range of output power while avoiding the bandwidth expansion of polar modulation.
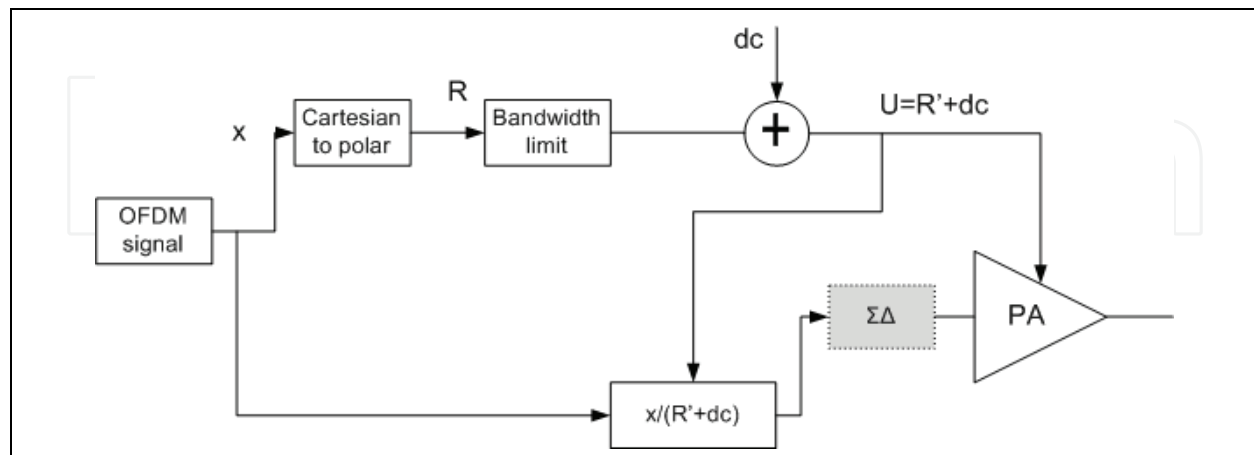

Fig. 7. Simplified architecture presented in Bassoo et al. (2009) for a combined polar and Cartesian modulator.

4.7 Efficiency comparison

Simulations have been performed on a 130nm CMOS class-D switched-mode amplifier, in order to compare the drain efficiency versus output power of the different architectures that have been discussed in the previous sections, such as Envelope Elimination and Restoration (EER), Envelope Tracking (ET), and Pulse Width Modulation by Variable Gate Bias (PWMVGB). Moreover, hypothetical curves for class-A and class-B operation have been drawn (see Fig. 8), with the peak efficiency as starting point. Class-A represents linear amplifier operation while class-B can be said to represent current-summing architectures.

Not unexpectedly the EER and ET architectures perform best, showing the highest efficiency for lower output power ranges. It may thus be concluded that the use of supply modulation is desirable for high average efficiencies. However, it can also be seen that efficiency remains a challenging aspect, especially taking into account numerous other requirements such as linearity, channel bandwidth, multi-mode/multi-standard operation and output power control range.

5. Summary

It is only fairly recent that CMOS technology has become a competitive alternative for integrated circuit power amplifier design for wireless communication handsets, as CMOS previously was not suitable for PA design due to frequency, output power, efficiency and linearity requirements. Thus, stand-alone PAs have long been manufactured in specialized technologies. Nowadays however CMOS has evolved to operating frequencies far into the GHz range, and many of the limitations, such as efficiency when used as linear amplification element, can be compensated by more digital control. Thus, a higher level of integration and more complex transmitter design result. However, the trend in CMOS technology development is to reduce device dimensions and as a consequence breakdown voltage. This complicates CMOS power amplifier design.
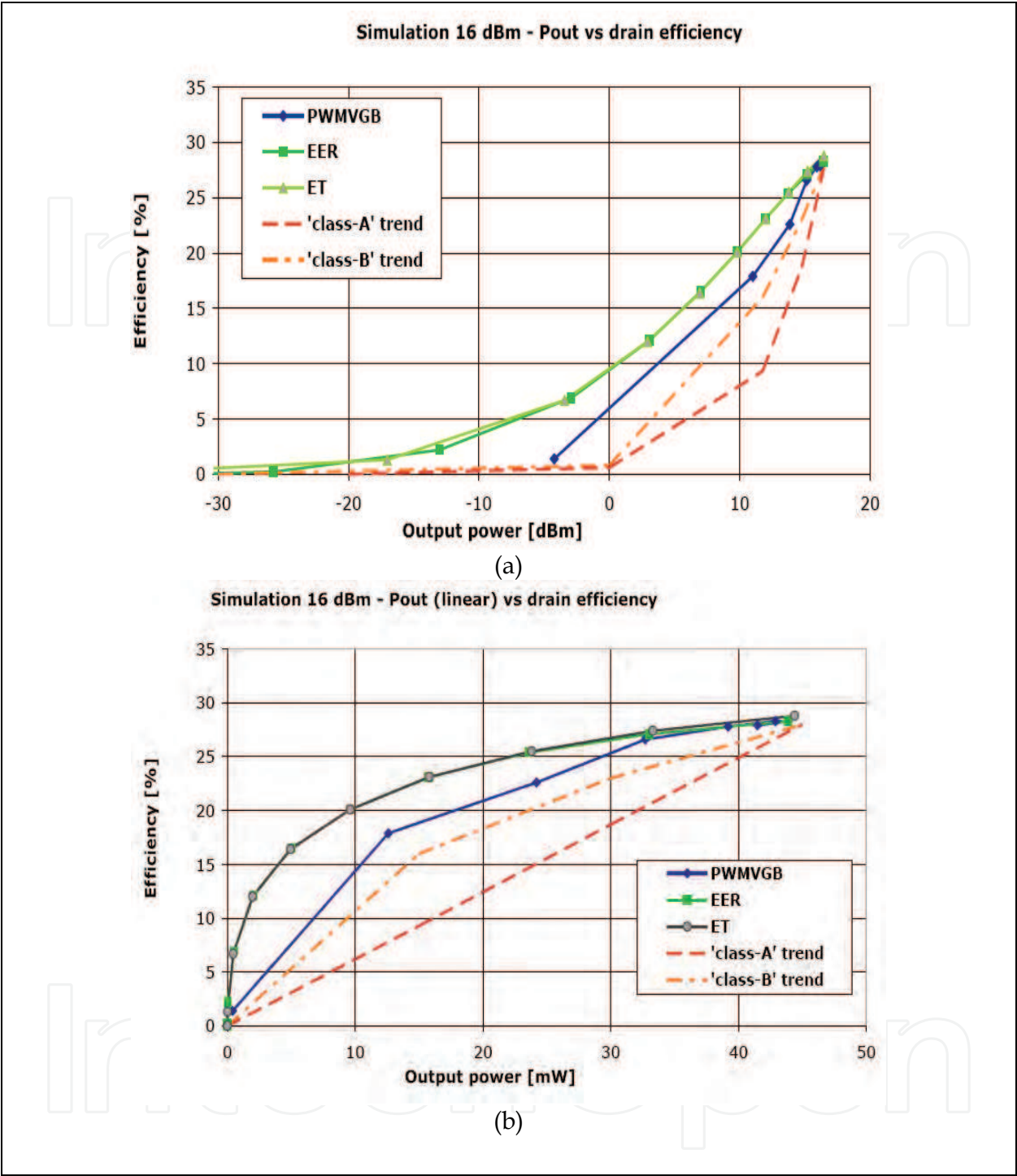
Fig. 8. Simulated drain efficiency for a CMOS class-D amplifier in different architectures, such as Envelope Elimination and Restoration (EER), Envelope Tracking (ET), and Pulse Width Modulation by Variable Gate Bias (PWMVGB). Class-A and class-B curves serve only as an illustration. The amplifier operated on a 1.2V supply and the input signal had a frequency of 2 GHz. (a). The output power (x-axis) represented in dBm, (b). The output power in mW.

Transmitter architectures using polar signals have gained in popularity, as splitting the Cartesian signal into a low-frequency envelope signal and a high-frequency phase signal

provides excellent opportunity for efficiency improvements because a non-linear power amplifier can be used. A number of different polar architecture implementations exist, both digital and analog. However, signal bandwidth and supply requirements are challenging aspects of such designs. Other strategies have thus been used to avoid supply voltage modulation, such as switched control of the supply voltage or variable gate bias. Moreover, direct RF modulation can be used, implemented as a sigma-delta or pulse width modulator at high operating frequency. Recently, design strategies such as current steering have gained interest for use in PA and transmitter design. Digital control bits are used to generate a scaled output current, providing a high output power without straining the devices.

However, efficiency over a wide range of output power is still a challenging aspect of transmitter design, especially if other requirements such as linearity, power control, multi-mode/multi-band operation and channel bandwidth must be fulfilled simultaneously.

5.1 Future outlook

As CMOS technologies continue to develop to dimensions well below 65nm, special devices suitable for high supply voltage will likely continue to be provided, for example using high-K metal gate material. Such devices can be used on the same chip as digital circuits with clocking speeds of several GHz. Moreover, other substrate types may be used more extensively, such as Silicon-on-Isolator substrates. As they are less lossy, this may provide efficiency improvements.

On the other hand, performance requirements will continue to rise with the development and maturing of wireless communication systems, especially because of the desire to cover more and more standards in one handset (multi-mode/multi-standard operation). Digital control may be used to accommodate greater flexibility, reconfigurability and on-chip calibration in transmitter design. Moreover, techniques may be used to increase the adaptivity of components such as antennas, duplexers, filters and matching networks.

CMOS will continue to expand into the millimeter-wave range, with operating frequencies beyond 60 GHz. However, other technology developments may play an important role in future integrated circuit design for wireless communication, such as integrated RF MEMS (microelectromechanical systems). Also devices such as carbon nanotubes may be used for wireless applications. But such technologies have some way to go until they reach the level of integration that current CMOS technology has.

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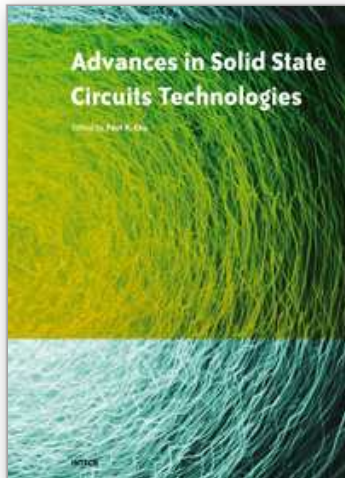
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This book brings together contributions from experts in the fields to describe the current status of important topics in solid-state circuit technologies. It consists of 20 chapters which are grouped under the following categories: general information, circuits and devices, materials, and characterization techniques. These chapters have been written by renowned experts in the respective fields making this book valuable to the integrated circuits and materials science communities. It is intended for a diverse readership including electrical engineers and material scientists in the industry and academic institutions. Readers will be able to familiarize themselves with the latest technologies in the various fields.

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