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Selective Oxidation on High-Indium-Content InAlAs/InGaAs Metamorphic High-Electron-Mobility Transistors

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1. Introduction

Up to now, many efforts have been continuously channeled toward the development of oxidation techniques on the III-V compounds for GaAs-based device application, which include thermal oxidation [1-7], chemical anodization [8-12], photochemical oxidation [13-16], plasma oxidation [17-20], Ga₂O₃ grown by molecular beam epitaxy (MBE) [21-23], Al₂O₃ grown by atomic layer deposition (ALD) [24], oxidized GaAs or InAlAs prepared by ultraviolet and ozone [25-27], and so on. Although the electrical quality of the GaAs-based MOS structures demonstrated to date is not as good as those obtained from the more mature SiO₂/Si system, some of them have yielded promising results for electronic and optoelectronic applications. However, the growth of oxides on the III-V surface is more complex than that on Si. Most of these methods require condensed gases, energy sources (such as excited plasma, electric potential, or optical illumination) or ultrahigh vacuum chamber, and so on, which complicate the oxidation process.

In the past years, a technique named liquid phase oxidation (LPO) [28] on GaAs-based materials operated at low temperature (30 °C to 70 °C) has been proposed and investigated. Much progress has been made to form a high-quality oxide on GaAs, for example, the mechanism and kinetics of oxidation [29], fabrication of GaAs MOSFET [30], pre-treatment and post-oxidation annealing of the oxide [31, 32], and GaAs-based devices [33, 34]. The oxidation takes place through the in-diffusion of oxygen at the semiconductor-oxide interface, where a fresh interface at the original semiconductor surface is achieved. This is an easy, economic, and low-temperature method to grow uniform and smooth native oxide films on GaAs-based materials. Utilizing the electroless technique, neither vacuum, gas condensation equipment, nor an assisting energy source is needed. Meanwhile, the technique has potential advantages for electronic and optical device applications due to its

substantial flexibility in device heterostructure designs and fabrications.

Another purpose of the work is to use the photoresist (PR) or metal as a mask for selective oxide growth on InAlAs with the low-cost, low-temperature LPO method. PR is widely utilized for photolithography processes and can be used as a mask for some device fabrication processes. However, the appearance of inherent problems such as flowing, outgassing, or blistering makes the PR unstable and useless at a high temperature [35]. The pH values of the aqueous oxidation solution for the LPO system range approximately from 5 to 3. Within the temperature and pH range, the PR is very stable. Utilizing the LPO method, the proposed application uses the PR as a stable mask for selective oxide growth on InAlAs.

InAlAs/InGaAs metamorphic high electron mobility transistors (MHEMTs) on GaAs substrates are characterized by high gains and low noise in millimeter-wave applications. They provide promising advantages over the structures grown on InP substrates, since they are less expensive, less fragile, and are available on a large scale. Meanwhile, efforts have been substantially devoted on the improvement of the instability and breakdown voltage. To solve the first problem, InP [36] or InGaP [37] has been used to achieve long-term reliability and to act as an etch-stop layer in a selective-etch recessed-gate process. However, if the InP is used as a Schottky layer, a special structure must be involved to enhance the Schottky barrier height on InP, which may still suffer from the high gate leakage issue. For the second problem, the composite channel [38] or the doped channel [39] has been used to overcome the small bandgap energy of the InGaAs channel. Aside from this, higher aluminum content in the InAlAs Schottky layer also induces a gate leakage issue, which causes the deterioration of device performance, especially when operating at higher bias conditions.

In conventional HEMT device, the undoped Schottky layer was used as the gate insulator, operating in a MIS transistor-like mode [40, 41]. Further improvement in leakage current and breakdown voltage for Schottky gate HEMT can be surmounted by using oxide film as an insulator between the two-dimensional electron gas (2DEG) channel and the gate electrode. The MOS-HEMT not only has the advantages of the MOS structure but also has the high-density, high-mobility, 2DEG channel. In addition, a very low interface trap density is needed in the oxide-semiconductor interface for MOSFET, however, which is different from the 2DEG channel positioned away from the oxide film with a barrier layer for MOS-HEMT in this study. When a negative voltage is applied to the gate, the electrons are depleted from a triangular quantum well. In this case, the vertical electric field points from the channel towards the gate electrode. As a result, some of the holes that are produced during impact ionization can get across the InAlAs barrier layer and are collected easily at the gate electrode without oxide film. Further discussion of impact ionization will follow later in context. When gate bias is made more positive, the bands straighten out and the vertical field drops. When the gate is more positively biased, the electrons are accumulated in a rectangular quantum well [34].

In order to achieve a better performance for InAlAs/InGaAs HEMTs, such as a smaller leakage current and higher breakdown voltage, one has to understand the mechanism of gate leakage and find the optimal device parameters. In this work, a thin InAlAs native oxide layer prepared by means of LPO as the gate dielectric for a 0.65 μm InAlAs/InGaAs MOS-MHEMT application is demonstrated.

2. Experimental

2.1 Liquid phase oxidation

For the LPO method, the most important and fundamental procedure is to prepare the growth solution. First, gallium-ion-containing nitric acid solution is obtained by the sufficient dissolution of high purity (6N) gallium metal in hot (60 °C) and concentrated nitric acid (70%) for more than 8 h and is then diluted with de-ionized (DI) water, ready for use. The second process is the pH adjustment of the solution, which is yet another critical process for the LPO method. The adjustment processes are performed by adding diluted ammonia water solution into the nitric acid solution. The pH value of the solution is usually adjusted within the range of 4.0 to 5.0, found to be the optimum initial pH value for oxidation. Finally, a clear solution is obtained by filtration with a pore size less than 0.1 μm. Figure 1 shows the simple growth system for LPO which consists of a temperature-controller heater and a pH meter. The GaAs-based wafers were first cleaned by organic solvents, followed by polishing and etching to remove the contaminants and residual oxides. These as-received wafers were prepared with minimized defect density before transferring into the LPO system. The oxidation procedure is performed by simply immersing the as-received wafers into the growth solution at a constant temperature. Moreover, in order to ensure the growth of uniform oxide layers, it is necessary to stir the growth solution and monitor the pH value during the oxidation. Without stirring the growth solution, the uniformity of the as-grown oxide will be relatively poor. Using the method described above, the wafers were oxidized at a constant temperature of 50 °C and finally rinsed by DI water and dried in nitrogen.

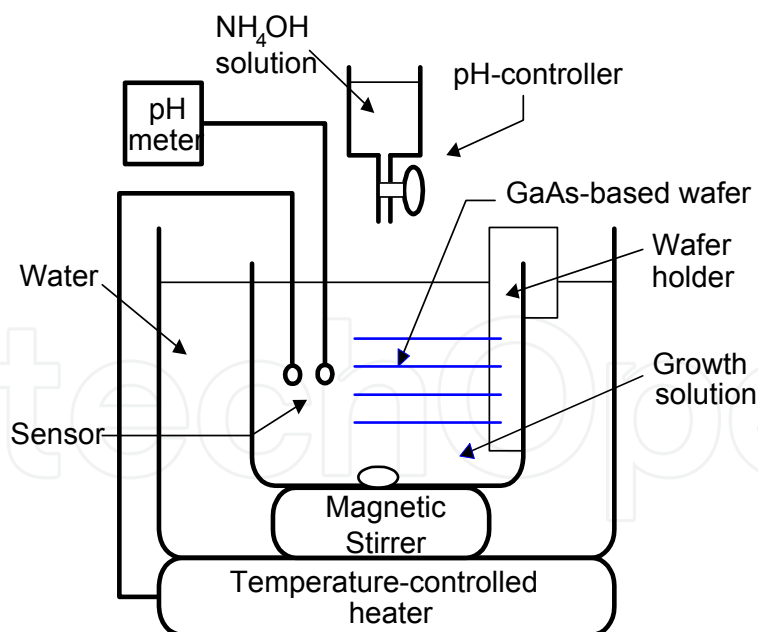


Fig. 1. The LPO system configuration.

2.2 Selective oxidation on InAlAs

The selective oxidation process is schematically illustrated in Fig. 2. After etching the InGaAs capping layer, the PR was coated on the InAlAs layer, and the pattern of which was

designed by the photolithographic processes. Then the sample was transferred into the growth solution for oxidation. An oxide layer can be grown only on a bare InAlAs surface that is not covered by PR. Since the oxidation occurs only at the oxide-semiconductor interface, the hetero deposition of films on PR can be avoided. After removing the PR, the final selectively oxidized structure can be obtained. As shown in Fig. 3, a high contrast between InAlAs and oxide layer on the top surface can be seen by the scanning electron microscopy (SEM) image. Similar results can also be observed by using metal masks (e.g., Au/Ge/Ni, Au, etc.) for selective oxidation.

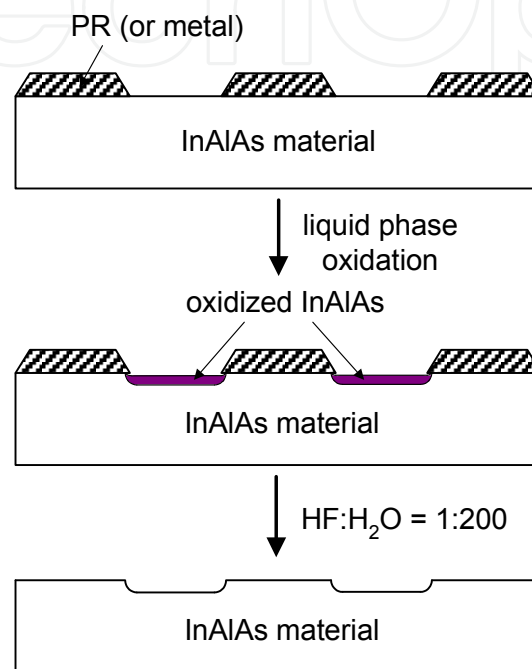


Fig. 2. Cross-sectional view of the proposed selective oxidation procedure on InAlAs material.

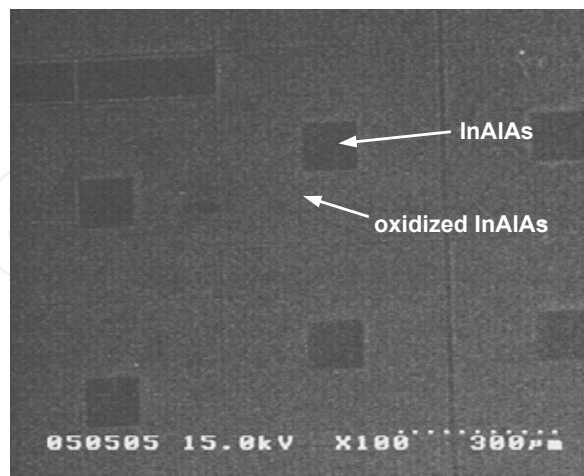


Fig. 3. Example of a top view of a SEM image. The high contrast of the InAlAs and oxide surface can be seen.

In this study, the MHEMT epitaxial structure was grown by metal-organic chemical vapor deposition (MOCVD) on a semi-insulating GaAs substrate as shown in Fig. 4. The measured

room- temperature Hall mobility and sheet carrier concentration were $7000 \text{ cm}^2/\text{Vs}$ and $2 \times 10^{12} \text{ cm}^{-2}$, respectively. The MOS-MHEMT fabrication started with mesa isolation by wet etching down to the buffer layer. The ohmic contacts of the Au/Ge/Ni metal were deposited by evaporation, and were then patterned by lift-off processes, followed by rapid thermal annealing. The gate recess was etched by the citric buffer etchant which was composed of the volume ratio of $\text{CA}:\text{H}_2\text{O}_2 = 1:1$ (CA was made by mixing the monohydrate citric acid and H_2O of 1:1 by weight) [42]. This step also leads a selective sidewall recessing to etch the exposed part of channel layer simultaneously, resulting in a reduction of gate leakage [43], as shown in Fig. 5. Then applying the LPO procedure, the wafer was immersed into the growth solution to generate a gate oxide at $50 \text{ }^\circ\text{C}$ for 15-30 min, yielding an oxidation rate of about 20 nm/h . After which, the oxide film selectively and simultaneously passivated the walls of the isolated surface. Utilizing the LPO, the proposed application uses the Au/Ge/Ni metal as a mask for selective oxide growth on InAlAs. Finally, the gate metal Au was deposited. The gate dimension and the drain-to-source spacing are $0.65 \times 200 \text{ }\mu\text{m}^2$ and $3 \text{ }\mu\text{m}$, respectively. The current-voltage (I - V) properties were characterized using HP4156B, and the microwave on-wafer measurements were conducted from 0.45-50 GHz in common-source configuration using an Agilent E8364A PNA network analyzer at 300 K.

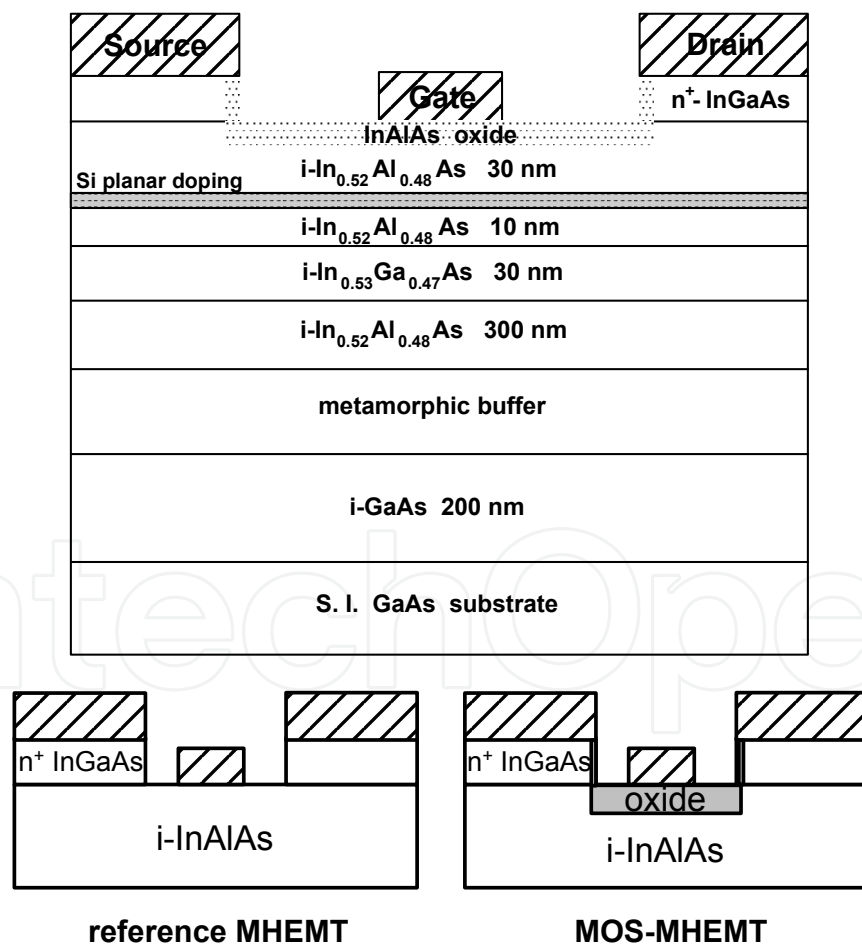


Fig. 4. Cross-sectional view of the studied InAlAs/InGaAs MOS-MHEMT structure.

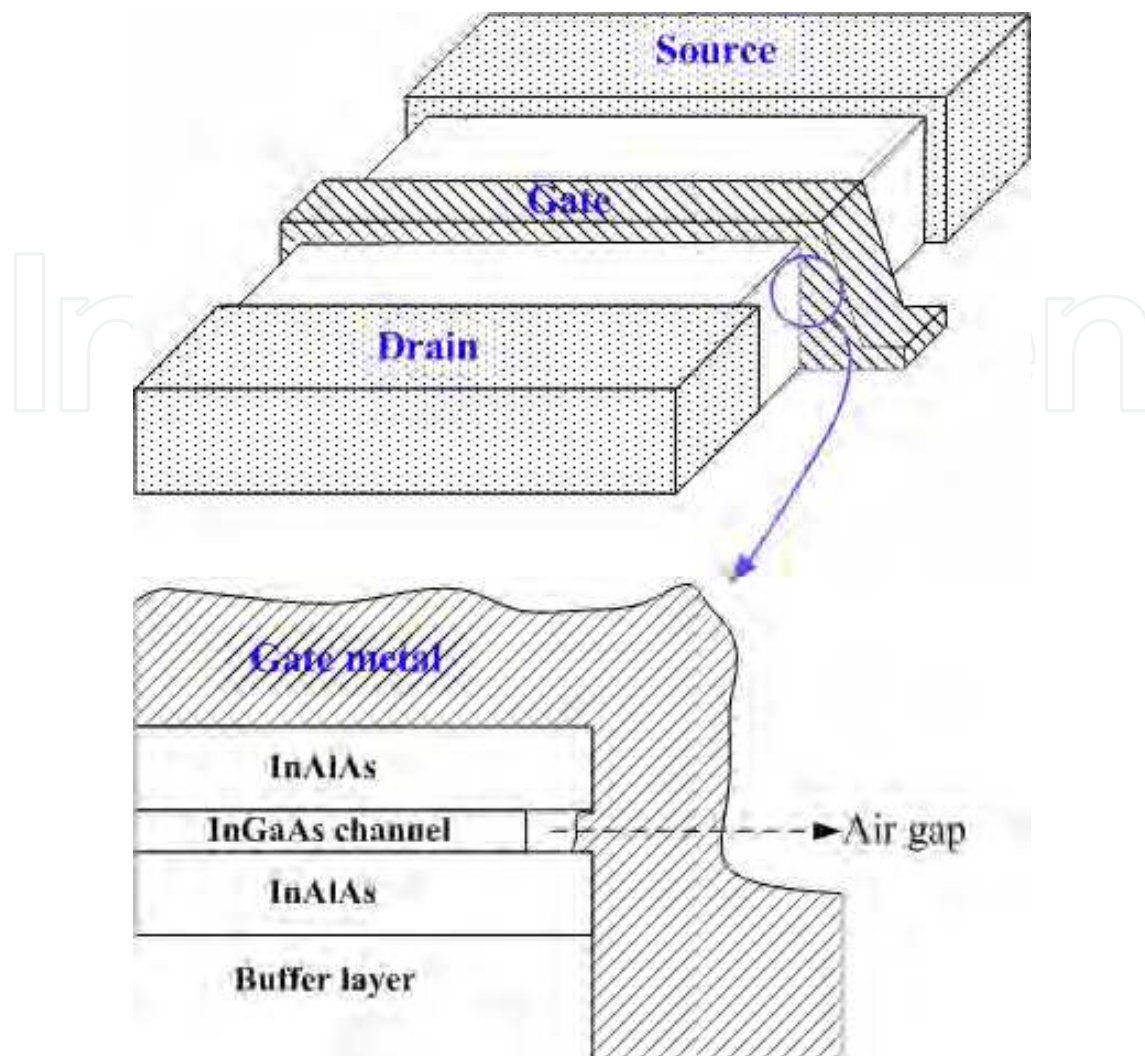
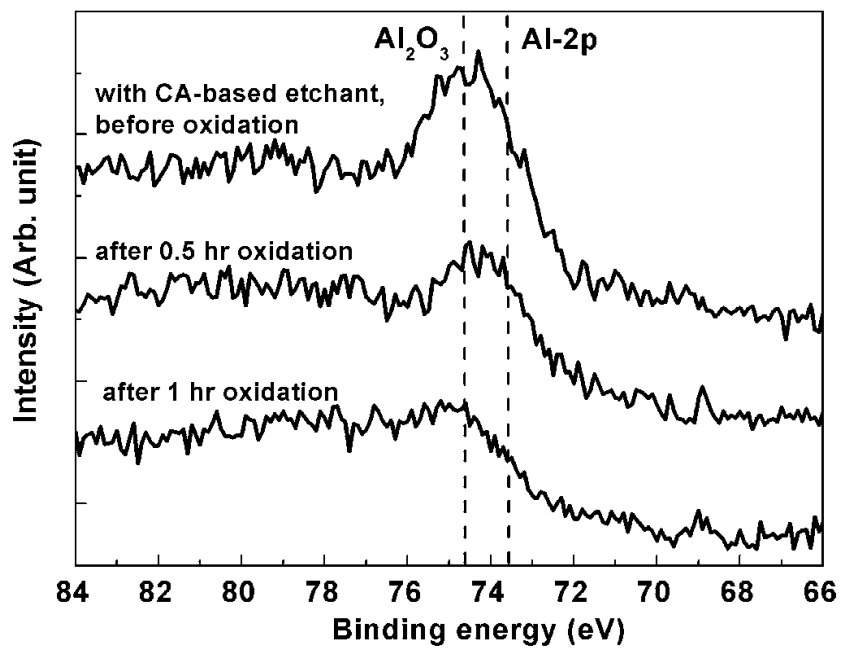


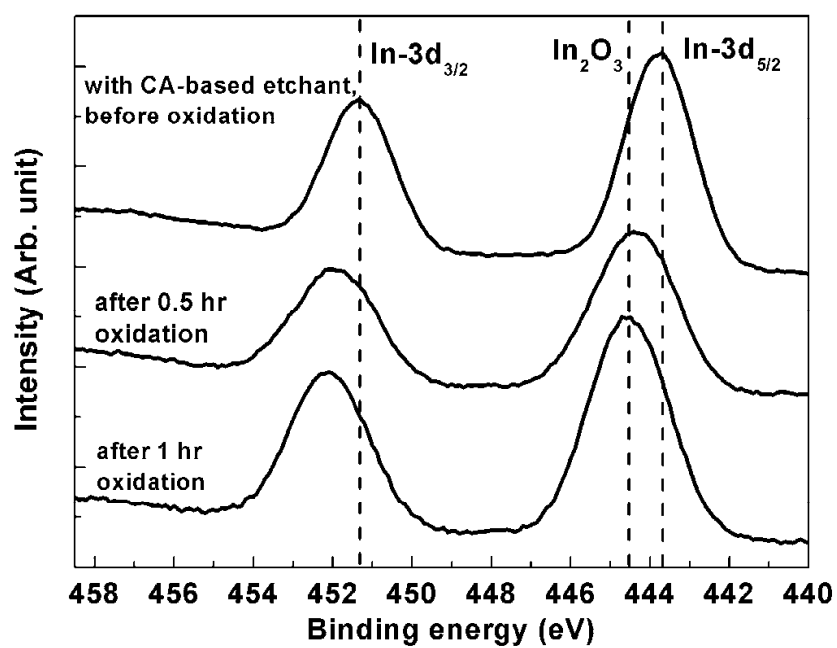
Fig. 5. The schematic cross-section view of the studied structure. (b) The diagram of separation of the gate metal from the channel.

3. Results and discussion

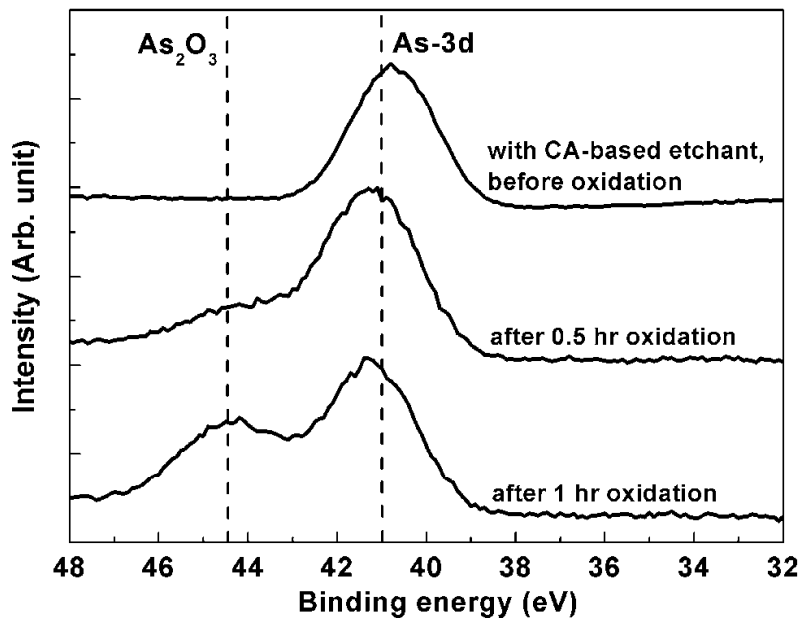
The oxide surface is mainly composed of Al_2O_3 , although arsenic oxide and indium oxide may still remain to some extent, as confirmed by the values of the peak energy and energy separations of X-ray photoelectron spectroscopy (XPS) between main core levels (i.e., Al-2p, In-3d and As-3d) in the oxide phases. Figure 6(a)-(c) show the XPS spectra of the surface of the etched samples by the citric buffer etchant before and after oxidation for Al-2p, In-3d, and As-3d core level, respectively. It is especially noteworthy that a stronger Al_2O_3 peak is detected on the Al-2p spectrum before oxidation, and the H_2O_2 plays a dominant role to achieve the selective etching. After oxidation, however, the signals of the Al-2p core level show that the Al oxides and AlAs on the surface are weak and even disappear after 2 h. This implies that the oxidizing materials of Al dissolve in this growth solution during the oxidation process, that is, Al oxide could be removed because etching in growth solution occurs through the repetition of formation and dissolution of oxide. Similar behaviors have also been investigated in AlGaAs material by LPO method [33].



(a)



(b)



(c)

Fig. 6. (a) Al-2p, (b) In-3d, and (c) As-3d XPS spectra of the surface of the etched samples by the citric buffer etchant before and after liquid phase oxidation.

Figure 7 shows the comparison of atomic force microscopy (AFM) 3D image for the InAlAs surface after gate recess by H_3PO_4 -based etchant ($\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1:1:30$) and CA-based etchant ($\text{CA}:\text{H}_2\text{O}_2 = 1:1$). Before gate metallization, the root mean square (rms) value of surface roughness is estimated to be 0.72 nm and 0.14 nm by the H_3PO_4 -based etchant and the CA-based etchant, respectively. These results are superior to those of previous studies using the same device structure [34]. That is, the device shows excellent etched uniformity by the citric buffer etchant. A good etched surface roughness is very important to achieve high device performance, which is very promising for power and microwave device applications.

On the other hand, the oxide film provides an improvement in the breakdown voltage in terms of the gate leakage current of the MOS-MHEMT, supported by the typical gate-to-drain I - V characteristics, as shown in Fig. 8. The reverse gate-to-drain breakdown voltage BV_{GD} (turn-on voltage V_{ON}) of the MOS-MHEMT is as high as -33.7 V (1.5 V), followed by -16.4 V (1.1 V) for the MHEMT with CA-based etchant, and -11.8 V (0.9 V) for the MHEMT with H_3PO_4 -based etchant. The BV_{GD} and the V_{ON} are defined as the voltage at which the gate current reaches 1 mA/mm. The higher V_{ON} allows a larger induced current in the InGaAs channel, enhancing the capability of the device power. The gate leakage current can be suppressed by at least more than 4-5 orders of magnitude with an oxide film at $V_{\text{GD}} = -15$ V. The smaller gate leakage current of MOS-MHEMT is owing to the MOS structure and the elimination of sidewall leakage paths that are directly passivated during the oxidation. In other words, the premium BV_{GD} and V_{ON} are attributed to the use of a thin InAlAs oxide film and the gate-recess processes.

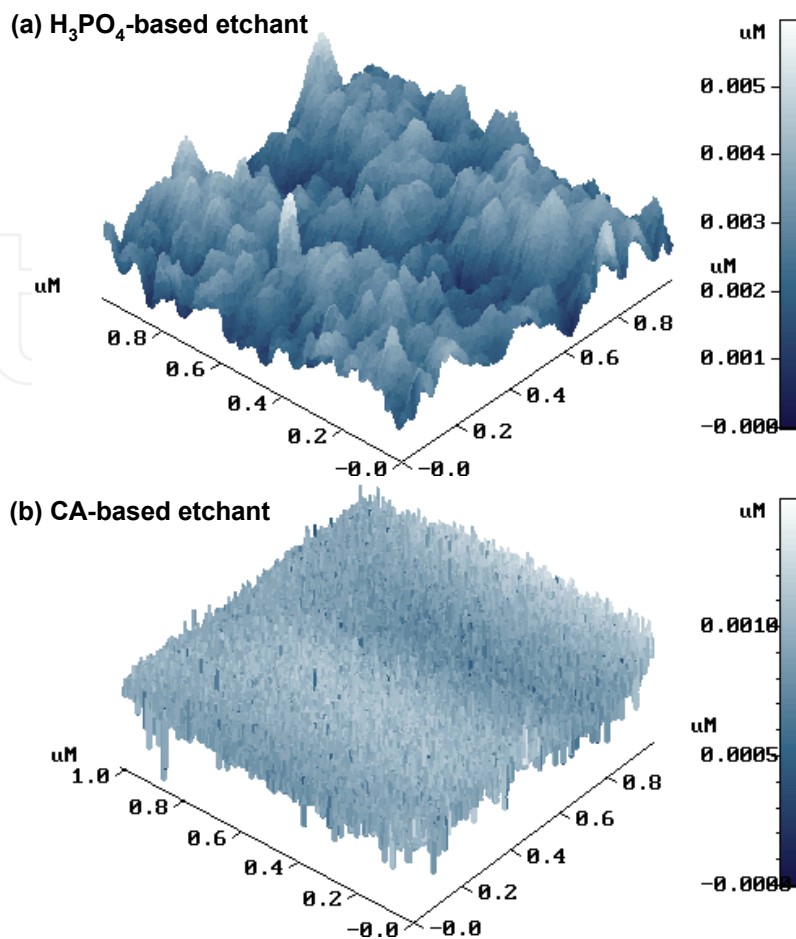


Fig. 7. AFM 3D image of the InAlAs surface after gate recess by (a) H_3PO_4 -based and (b) CA-based etchant.

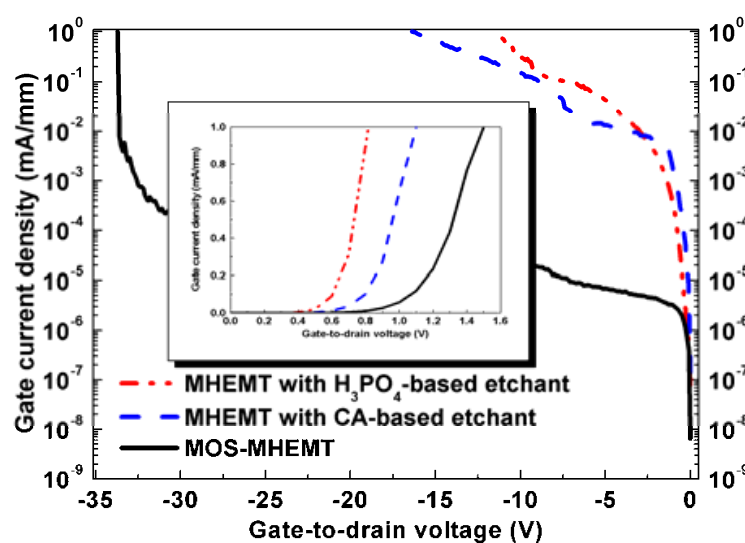
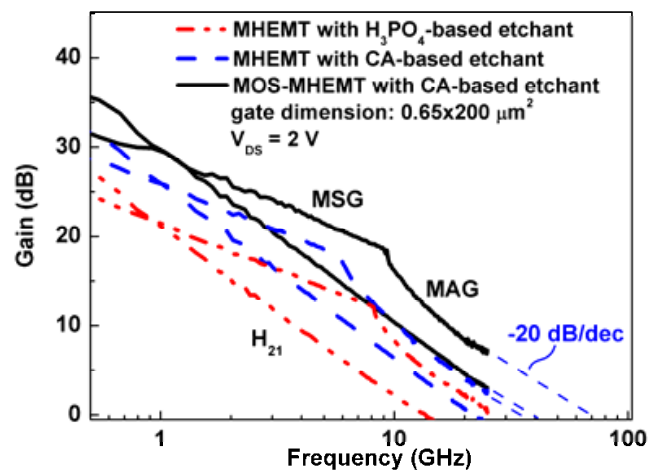
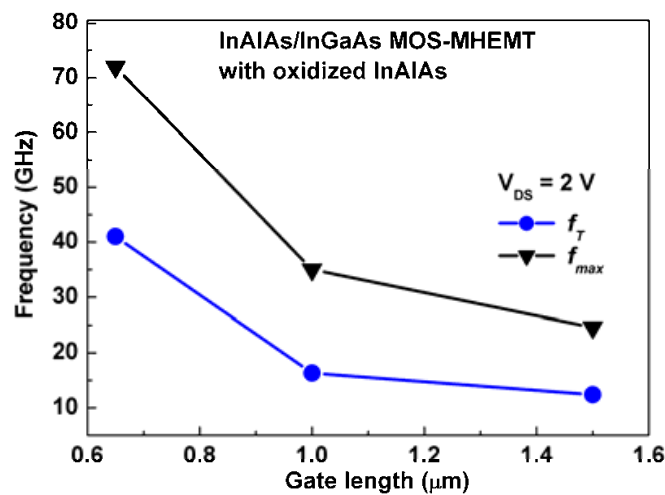


Fig. 8. Comparison of the reversed gate leakage current for MHEMTs with and without an oxide film. The inset shows the comparison of the forward gate-to-drain characteristics.

The measured unity-current-gain cutoff frequency f_T and the maximum oscillation frequency f_{max} are around 41 (22) GHz and 72 (39) GHz at maximum transconductance g_m for MOS-MHEMT (MHEMT with CA-based etchant), respectively, as shown in Fig. 9(a). These improved RF performances show the existence of a smooth and uniform etched surface after selective gate recessing by the CA-based etchant, which is superior to that of the H_3PO_4 -based etchant. Furthermore, the enhanced RF performances show the existence of a MOS structure on conventional MHEMT by LPO, which is superior to the reference MHEMT. Fig. 9(b) shows the microwave characteristics versus the gate length for InAlAs/InGaAs MOS-MHEMT with an oxidized InAlAs as gate insulator. The gate-source capacitance C_{gs} extracted from the S-parameters of the MOS-MHEMT is lower than that of the reference MHEMT at the V_{GS} with maximum g_m . Based on these results, we conjecture that the reason for the increase of cutoff frequency for MOS-MHEMT may be partly attributed to the C_{gs} .



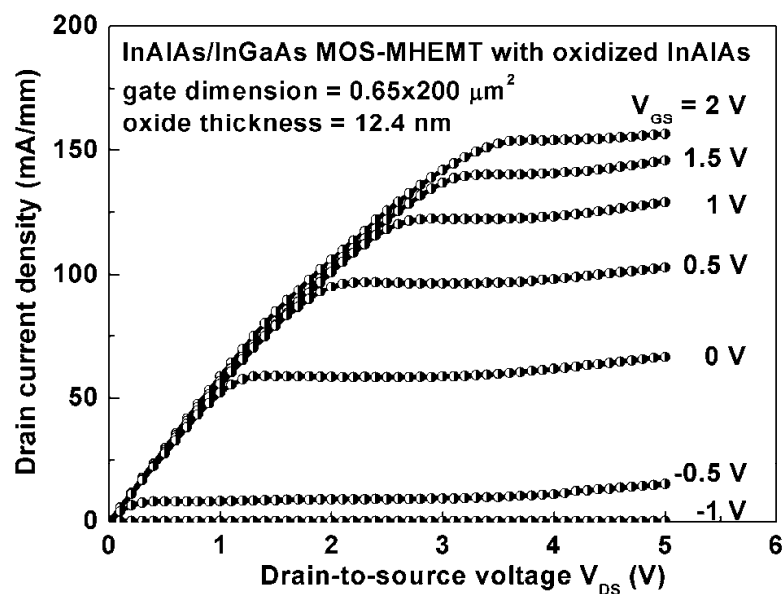
(a)



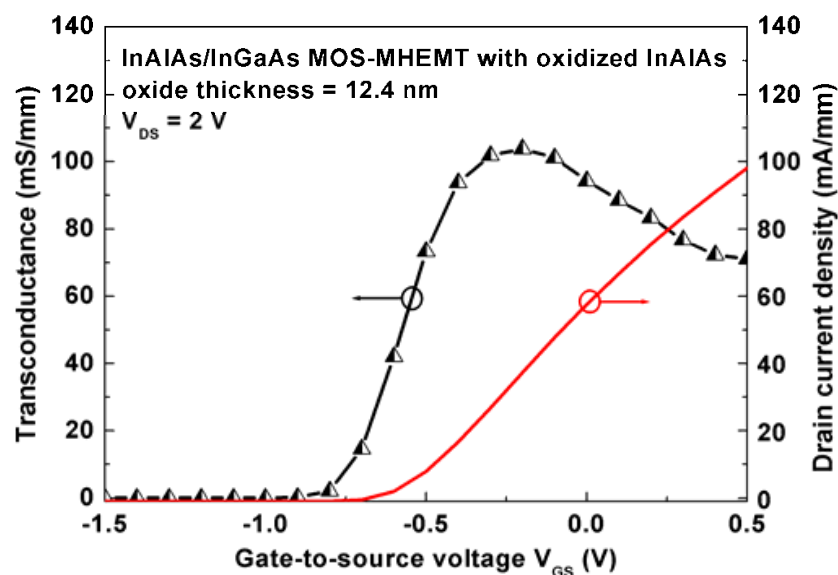
(b)

Fig. 9. (a) Comparison of the microwave characteristics at maximum g_m for the MOS-MHEMT and MHEMTs. (b) Microwave characteristics versus gate length for InAlAs/InGaAs MOS-MHEMT with an oxidized InAlAs as gate insulator.

The I - V characteristics of the studied MOS-MHEMT is shown in Fig. 10(a). Good pinch-off and saturation characteristics are achieved, though a significant resistance is obtained due to the nonoptimized source/drain contact formation and longer time oxidation. Fig. 10(b) shows the g_m and the drain current density as a function of the V_{GS} at $V_{DS} = 2$ V for the same device. The maximum g_m and the threshold voltage V_{th} are 104 mS/mm and -0.55 V, respectively. Much higher g_m and drain current density are expected with suitable device structure, such as inserting a Si-planar doping layer to enhance the carrier density.



(a)



(b)

Fig. 10. (a) I - V characteristics of the InAlAs/InGaAs MOS-MHEMT with 12.4-nm-thick oxide. (b) The g_m and the drain current density versus V_{GS} at $V_{DS} = 2$ V.

Conventional InAlAs/InGaAs MHEMTs drastically suffer from low breakdown voltages due to the enhanced impact ionization effects which occur in the narrow bandgap InGaAs channel. The impact ionization effect is dependent on channel electrical field and the amount of carriers (i.e., drain current). In MOS-MHEMT, however, the electrical field in the gate-to-drain region at a fixed V_{DS} and V_{GS} is smaller than that of the reference MHEMT due to the high barrier height between the gate metal and Schottky layer, resulting in the smaller channel electrical field (i.e., smaller impact ionization effect). In order to investigate the influence of the impact ionization effect, the gate current density as a function of V_{GS} at different V_{DS} is measured. The bell-shaped curve is the typical behavior of the impact ionization effect as shown in Fig. 11 [44, 45]. At pinch-off, i.e., $V_{GS} < V_{th}$, the gate current due to the tunneling effect is also observed. This gate current is very small due to the large diode breakdown voltage for MOS-MHEMT. However, for $V_{GS} > V_{th}$, the gate current is mainly attributed to the impact ionization current which is larger than the tunneling current. Clearly, a remarkable increase in the peak gate current takes place when devices are biased at a higher V_{DS} . Because of the existence of a high electric field in the gate-to-drain region, significant hot electron phenomena occur in the narrow bandgap InGaAs channel. Furthermore, electrons can obtain high energy to generate electron-hole pairs through enhanced impact ionizations, resulting in the easier injection of holes into the gate terminal [46]. However, the peak gate current density for MOS-MHEMT is significantly improved as compared to that of reference MHEMT. Therefore, the electrons and holes generated by the impact ionization are decreased to further reduce the drain and gate current due to the native oxide layer.

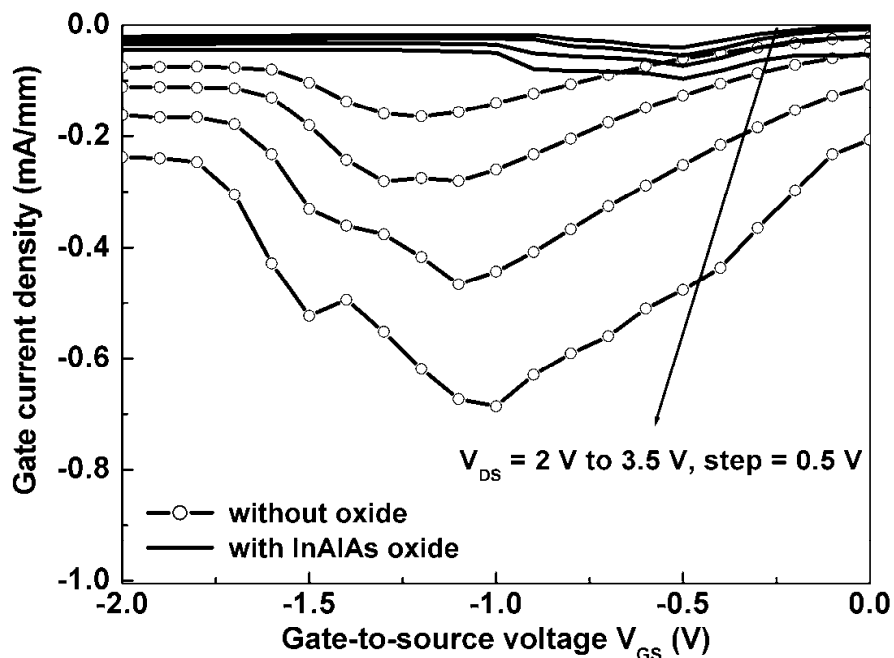
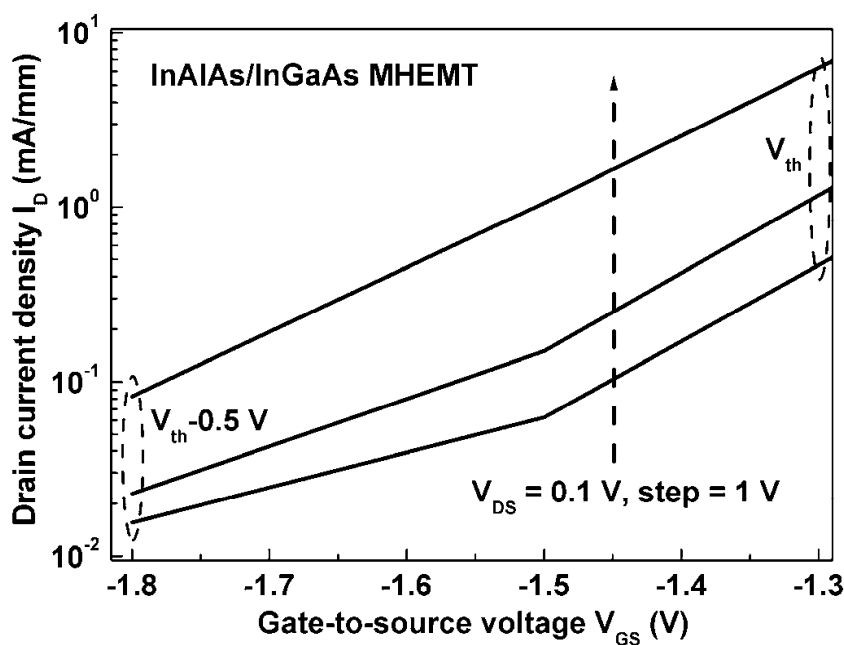
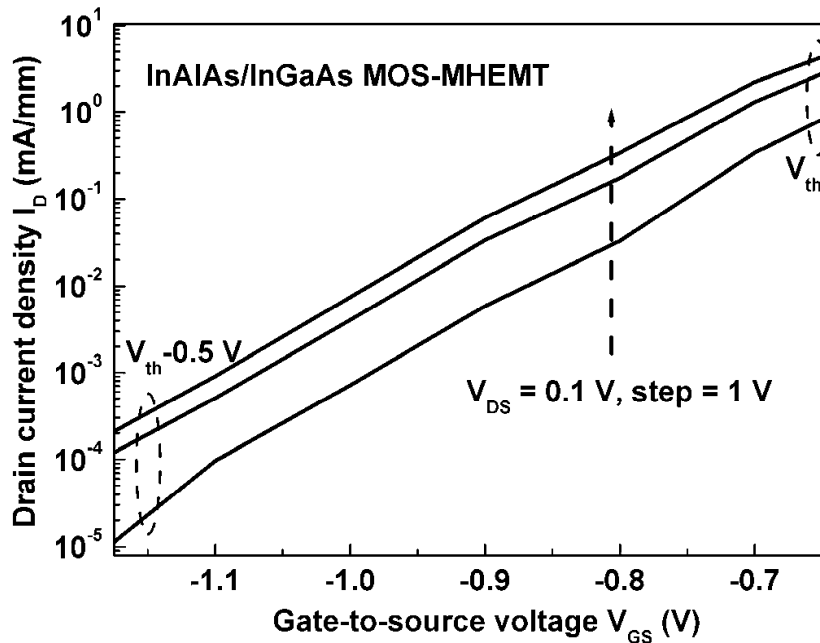


Fig. 11. Comparison of the gate current density versus V_{GS} at various V_{DS} for the MOS-MHEMT and the reference MHEMT.

So far, there have been many reports on InAlAs/InGaAs HEMT device performance, such as dc transfer characteristics, cutoff frequency, noise figure, output power density, and so on. The gate bias is operated above the threshold voltage, i.e., the device is in ON state. C. Jiang *et al.* have investigated the subthreshold current in short-channel GaAs/AlGaAs HEMT with and without a higher potential barrier in the buffer [47]. However, there are very few reports that discuss leakage current in the subthreshold region for InAlAs/InGaAs HEMT. When the gate bias is as low as the pinch-off voltage, some carriers pass through the InGaAs channel. The subthreshold current depends on the device structures, fabrication processes, and epitaxial technology. It determines the ideal OFF state, and impacts the power dissipation and circuit applications, e.g., transmitter/receiver modules. Figure 12 shows the comparison of the subthreshold current density versus the gate bias at $V_{DS} = 0.1, 1.1, \text{ and } 2.1$ V for reference MHEMT and MOS-MHEMT. At $V_{GS} = V_{th}$, both devices have a similar value of drain current. However, in the region of V_{GS} around $V_{th}-0.5$ V, drain current density of the MOS-MHEMT is about 1000 times smaller than that of the conventional MHEMT. The MOS-MHEMT has a smaller subthreshold swing, ~ 100 mV/dec, defined as the change in gate voltage needed to reduce the drain current by one decade, than the reference one (250-500 mV/dec) for the same V_{DS} . Here, there is no distinction between the InGaAs channel and buffer layer for both devices. These results clearly suggest that the studied MOS-MHEMT suppresses the subthreshold current due to the reduction of the surface recombination current of the native oxide around the ohmic contact regime, i.e., suppression of the undesirable carriers' injection from the source under OFF state.



(a)



(b)

Fig. 12. (a) Subthreshold current density versus gate bias at $V_{DS} = 0.1, 1.1,$ and 2.1 V for a conventional MHEMT. (b) Subthreshold current density versus gate bias at $V_{DS} = 0.1, 1.1,$ and 2.1 V for the MOS-MHEMT.

Group	K.W. Lee, <i>et al</i> [48]	K.W. Lee, <i>et al</i> [34]	N.C. Paul, <i>et al</i> [27]	Y. Sun, <i>et al</i> [49]
HEMT Structure	In _{0.53} Ga _{0.47} As/ In _{0.52} Al _{0.48} As/ In _{0.53} Ga _{0.47} As	In _{0.53} Ga _{0.47} As/ In _{0.52} Al _{0.48} As/ In _{0.53} Ga _{0.47} As	In _{0.53} Ga _{0.47} As/ In _{0.52} Al _{0.48} As/ InP/ In _{0.52} Al _{0.48} As/ InGaAs	In _{0.53} Ga _{0.47} As/ In _{0.52} Al _{0.48} As/ In _{0.7} Ga _{0.3} As
Gate oxide	Oxidized InGaAs	Oxidized InAlAs	Oxidized InAlAs	Al ₂ O ₃
Oxidation method	LPO	LPO	UV-ozone	ALD
Temperature (°C)	50	50	100	300
Gate length (μm)	0.65	0.65	1.5	0.26
Maximum V_{GS} (V)	2	1	3	2
Maximum I_{DS} (mA/mm)	390	257	163	115
Maximum g_m (mS/mm)	207	226	200	157
Subthreshold Swing (mV/dec)	-	100	-	200

Table 1. A summary of the DC characteristics of the InAlAs/InGaAs MOS-HEMTs for this study and the previous reported data.

Also, the oxidation of InGaAs and its application to the same device without gate recess were studied [48]. Without gate recessing, the gate oxide is obtained directly by oxidizing

the InGaAs capping layer in the LPO system (see Fig. 4). Besides, this process can simplify one mask and grow reliable oxide films as well as sidewall passivation layers simultaneously. Table I summarizes the DC characteristics among the LPO, UV-ozone, and ALD technology on the high-indium-content InAlAs/InGaAs MOS-HEMTs for other groups [27, 49].

4. Conclusion

The oxidized InAlAs as the gate dielectric of InAlAs/InGaAs MOS-MHEMT, which was prepared by LPO at a low temperature before gate metallization, was demonstrated. The selective oxidation between oxide film and PR (or metal) has been studied, and the oxide surface composition for a long oxidation time has been evaluated. The XPS signals of the Al-2p core level indicate that Al and Al-oxides on the oxide surface are weak for a long oxidation time due to the strongly pH-dependent solubility of Al₂O₃. Moreover, as compared to the conventional InAlAs/InGaAs MHEMT, a larger gate bias operation, higher drain-to-source breakdown voltage, lower subthreshold current, lower gate leakage current with the suppressed impact ionization effect, and improved RF performances for the MOS-MHEMT make the proposed economic and low-temperature LPO suitable for device applications. The enhanced high-frequency performances due to the lower C_{gs} of MOS-MHEMT are expected, exhibiting its promising applications to millimeter-wave integrated circuit designs. Thus, the LPO provides new opportunities to explore many alternative dielectrics to produce gate oxides as well as effective passivation layers on III-V compound semiconductor devices.

5. Acknowledgements

The authors wish to thank Hsien-Chang Lin, Kai-Lin Lee, Chia-Hong Hsieh, Chao-Hsien Tu, and Chih-Chun Hu whose research made this work possible. This work was supported in part by the National Science Council of Taiwan under contract number NSC95-2221-E-006-428-MY3, NSC97-2221-E-214-063, and the MOE Program for Promoting Academic Excellence of Universities.

6. References

- [1] H. T. Minden, "Thermal oxidation of GaAs," *J. Electrochem. Soc.*, vol. 109, pp. 733-736, 1962.
- [2] D. N. Butcher and B. J. Sealy, "Electrical properties of thermal oxides on GaAs," *Electron. Lett.*, vol. 13, pp. 558-559, 1977.
- [3] H. Takagi, G. Kano, and I. Teramoto, "Thermal oxidation of GaAs in arsenic trioxide vapor," *J. Electrochem. Soc.*, vol. 125, pp. 579-581, 1978.
- [4] K. Maezawa, T. Mizutani, K. Arai, and F. Yanagawa, "Large transconductance n⁺-Ge gate AlGaAs/GaAs MISFET with thin gate insulator," *IEEE Electron Device Lett.*, vol. EDL-7, pp. 454-456, 1986.
- [5] N. Basu and K. N. Bhat, "High-pressure thermal oxidation of n-GaAs in an atmosphere of oxygen and water vapor," *J. Appl. Phys.*, vol. 63, pp. 5500-5506, 1988.

- [6] T. H. Oh, D. L. Huffaker, L. A. Graham, H. Deng, and D. G. Deppe, "Steam oxidation of GaAs," *Electron. Lett.*, vol. 32, pp. 2024-2026, 1996.
- [7] K. D. Choquette, K. M. Geib, C. I. H. Ashby, R. D. Twesten, O. Blum, H. Q. Hou, D. M. Follstaedt, B. E. Hammons, D. Mathes, and R. Hull, "Advances in selective wet oxidation of AlGaAs alloys," *IEEE J. Selected Topic in Quantum Electron.*, vol. 3, pp. 916-926, 1997.
- [8] H. Hasegawa, K. E. Forward, and H. L. Hartnagel, "New anodic native oxide of GaAs with improved dielectric and interface properties," *Appl. Phys. Lett.*, vol. 26, pp. 567-569, 1975.
- [9] D. J. Coleman, D. W. Shaw, and R. D. Dobrott, "On the mechanism of GaAs anodization," *J. Electrochem. Soc.*, vol. 124, pp. 239-241, 1977.
- [10] G. P. Schwartz, J. E. Griffiths, and B. Schwartz, "Interfacial reactions on anodized GaAs," *J. Vac. Sci. Technol.*, vol. 16, pp. 1383-1386, 1979.
- [11] M. J. Jeng and J. G. Hwu, "Thin-gate oxides prepared by pure water anodization followed by rapid thermal densification," *IEEE Electron Device Lett.*, vol. 17, pp. 575-577, 1996.
- [12] P. Schmuki, G. I. Sproule, J. A. Bardwell, Z. H. Lu, and M. J. Graham, "Thin anodic oxides formed on GaAs in aqueous solutions," *J. Appl. Phys.*, vol. 79, pp. 7303-7311, 1996.
- [13] P. A. Bertrand, "The photochemical oxidation of GaAs," *J. Electrochem. Soc.*, vol. 132, pp. 973-976, 1985.
- [14] S. D. Offsey, J. M. Woodall, A. C. Warren, D. Kirchner, T. I. Chappell, and G. D. Pettit, "Unpinned (100) GaAs surfaces in air using photochemistry," *Appl. Phys. Lett.*, vol. 48, pp. 475-477, 1986.
- [15] T. Sawada, H. Hasegawa, and H. Ohno, "Electronic properties of a photochemical oxide-GaAs interface," *Jpn. J. Appl. Phys.*, vol. 26, pp. L1871-L1873, 1987.
- [16] E. Etedgui, K. T. Park, J. Cao, Y. Gao, and M. W. Ruckman, "Growth of a Cr oxide layer on GaAs(100) by oxidation with condensed water," *J. Appl. Phys.*, vol. 73, pp. 1781-1787, 1993.
- [17] T. Sugano, "Oxidation of GaAs_{1-x}P_x surface by oxygen plasma and properties of oxide film," *J. Electrochem. Soc.*, vol. 121, pp. 113-118, 1974.
- [18] C. R. Liu and L. Liu, "Measurement and analysis of the infrared absorption band for plasma anodized film on GaAs(100)," *J. Phys. D: Appl. Phys.*, vol. 21, pp. 799-803, 1988.
- [19] W. A. Loong and H. L. Chang, "Oxidation of GaAs surface by oxygen plasma and its application as an antireflection layer," *Jpn. J. Appl. Phys.*, vol. 30, pp. L1319-L1320, 1991.
- [20] R. Nakamura and H. Ikoma, "Magnetically excited plasma oxidation of GaAs," *Jpn. J. Appl. Phys.*, vol. 35, pp. L8-L11, 1996.
- [21] M. Passlack, M. Hong, E. F. Schubert, J. R. Kwo, J. P. Mannaerts, S. N. G. Chu, N. Moriya, and F. A. Thiel, "In situ fabricated Ga₂O₃-GaAs structures with low interface recombination velocity," *Appl. Phys. Lett.*, vol. 66, pp. 625-627, 1995.
- [22] F. Ren, J. M. Kuo, M. Hong, W. S. Hobson, J. R. Lothian, J. Lin, H. S. Tsai, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, "Ga₂O₃(Gd₂O₃)/InGaAs enhancement-mode n-channel MOSFET's," *IEEE Electron Device Lett.*, vol. 19, pp. 309-311, 1998.

- [23] M. Passlack, J. K. Abrokwhah, R. Droopad, Z. Yu, C. Overgaard, S. I. Yi, M. Hale, J. Sexton, and A. C. Kummel, "Self-aligned GaAs p-channel enhancement mode MOS heterostructure field-effect transistor," *IEEE Electron Device Lett.*, vol. 23, pp. 508-510, 2002.
- [24] P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H.-J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, M. Hong, K. K. Ng, and J. Bude, "GaAs MOSFET with oxide gate dielectric grown by atomic layer deposition," *IEEE Electron Device Lett.*, vol. 24, pp. 209-211, 2003.
- [25] R. Driad, Z. H. Lu, S. Laframboise, D. Scansen, W. R. Mckinnon, and S. P. Mcalister, "Reduction of surface recombination in InGaAs/InP heterostructures using UV-irradiation and ozone," *Jpn. J. Appl. Phys.*, vol. 38, pp. 1124-1127, 1999.
- [26] K. Iiyama, Y. Kita, Y. Ohta, M. Nasuno, S. Takamiya, K. Higashimine, and N. Ohtsuka, "Fabrication of GaAs MISFET with nm-thin oxidized layer formed by UV and ozone process," *IEEE Trans. Electron Devices*, vol. 49, pp. 1856-1862, 2002.
- [27] N. C. Paul, K. Nakamura, H. Seto, K. Iiyama, and S. Takamiya, "Oxidation of InAlAs and its application to gate insulator of InAlAs/InGaAs metal oxide semiconductor high electron mobility transistor," *Jpn. J. Appl. Phys.*, vol. 44, pp. 1174-1180, 2005.
- [28] H. H. Wang, C. J. Huang, Y. H. Wang, and M. P. Houng, "Liquid phase chemical-enhanced oxidation for GaAs operated near room temperature," *Jpn. J. Appl. Phys.*, vol. 37, pp. L67-L70, 1998.
- [29] H. H. Wang, J. Y. Wu, Y. H. Wang, and M. P. Houng, "Effects of pH values on the kinetics of liquid phase chemical enhanced oxidation of GaAs," *J. Electrochem. Soc.*, vol. 146, pp. 2328-2332, 1999.
- [30] J. Y. Wu, H. H. Wang, Y. H. Wang, and M. P. Houng, "A GaAs MOSFET with a liquid phase oxidized gate," *IEEE Electron Device Lett.*, vol. 20, pp. 18-20, 1999.
- [31] D. W. Chou, R. F. Lou, H. H. Wang, Y. H. Wang, and M. P. Houng, "Properties of the GaAs oxide layer grown by the liquid-phase chemical-enhanced technique on the S-passivated GaAs surface," *J. Electronic Materials*, vol. 31, pp. 71-75, 2002.
- [32] D. W. Chou, L. T. Wang, H. H. Wang, Y. H. Wang, and M. P. Houng, "Influence of annealing ambient on GaAs oxide prepared by the liquid phase method," *Solid-State Electron.*, vol. 48, pp. 2175-2179, 2004.
- [33] K. W. Lee, Y. H. Wang and M. P. Houng, "Liquid phase chemical enhanced oxidation on AlGaAs and its application," *Jpn. J. Appl. Phys.*, vol. 43, pp. 4087-4091, 2004.
- [34] K. W. Lee, K. L. Lee, X. Z. Lin, C. H. Tu, and Y. H. Wang, "Improvement of impact ionization effect and subthreshold current in InAlAs/InGaAs metal-oxide-semiconductor metamorphic HEMT with a liquid phase oxidized InAlAs as gate insulator," *IEEE Trans. Electron Devices*, vol. 54, no. 3, pp. 418-424, 2007.
- [35] H. H. Wang, Y. H. Wang, and M. P. Houng, "Near-room-temperature selective oxidation on GaAs using photoresist as a mask," *Jpn. J. Appl. Phys.*, vol. 37, pp. L988-L990, 1998.
- [36] D. R. Greenberg, J. A. del Alamo, and R. Bhat, "A recessed-gate InAlAs/n⁺-InP HFET with an InP etch-stop layer," *IEEE Electron Devices Lett.*, vol. 13, p. 137, 1992.
- [37] S. Fujita, T. Noda, C. Nozaki, and Y. Ashizawa, "InGaP/InAlAs HEMT with a strained InGaP Schottky contact layer," *IEEE Electron Devices Lett.*, vol. 14, p. 259, 1993.

- [38] T. Enoki, K. Arai, A. Kohzen, and Y. Ishii, "Design and characteristics of InGaAs/InP composite-channel HFET's," *IEEE Trans. Electron Devices*, vol. 42, p. 1413, 1995.
- [39] J. A. del Alamo and T. Mizutani, "An $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{n}^+\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MISFET with a modulation-doped channel," *IEEE Electron Device Lett.*, vol. 10, p. 394, 1989.
- [40] H. Kinoshita, Y. Sano, T. Ishida, S. Nishi, M. Akiyama and K. Kaminishi, "A new insulated-gate inverted-structure modulation-doped AlGaAs/GaAs/N-AlGaAs field-effect transistor," *Jpn. J. Appl. Phys.*, vol. 43, p. L836, 1984.
- [41] S. Fujita, M. Hirano, and T. Mizutani, "Small-signal characteristics of $\text{n}^+\text{-Ge}$ gate AlGaAs/GaAs MISFET's," *IEEE Electron Device Lett.*, vol. 9, p. 518, 1988.
- [42] M. Tong, K. Nummila, A. Ketterson, I. Adesida, C. Caneau, and R. Bhat, "InAlAs/InGaAs/InP MODFET's with uniform threshold voltage obtained by selective wet gate recess," *IEEE Electron Device Lett.*, vol. 13, p. 525, 1992.
- [43] S. R. Bahl and J. A. del Alamo, "Elimination of mesa-sidewall gate leakage in InAlAs/InGaAs heterostructures by selective sidewall recessing," *IEEE Electron Device Letters*, vol.13, pp. 195-197, 1992.
- [44] G. Meneghesso, T. Grave, M. Manfredi, M. Pavesi, C. Canali, and E. Zanoni, "Analysis of hot carrier transport in AlGaAs/InGaAs pseudomorphic HEMT's by means of electroluminescence," *IEEE Trans. Electron Devices*, vol. 47, p. 2, 2000.
- [45] M. Boudrissa, E. Delos, C. Gaquiere, M. Rousseau, Y. Cordier, D. Theron, and J. C. De Jaeger, "Enhancement-mode $\text{Al}_{0.66}\text{In}_{0.34}\text{As}/\text{Ga}_{0.67}\text{In}_{0.33}\text{As}$ metamorphic HEMT: modeling and measurements," *IEEE Trans. Electron Devices*, vol. 48, p. 1037, 2001.
- [46] T. Suemitsu, T. Enoki, N. Sano, M. Tomizawa, and Y. Ishii, "An analysis of the kink phenomena in InAlAs/InGaAs HEMT's using two-dimensional device simulation," *IEEE Trans. Electron Devices*, vol. 45, p. 2390, 1998.
- [47] C. Jiang, D. C. Tsui, B. J. F. Lin, H. Lee, A. Lepore, and M. Levy, "Subthreshold current in MODFET's of tenth-micrometer gate," *IEEE Electron Device Lett.*, vol. 11, p. 63, 1990.
- [48] K. W. Lee, H. C. Lin, K. L. Lee, C. H. Tu, and Y. H. Wang, "Selectively liquid-phase oxidation of InGaAs and application to metal-oxide-semiconductor InAlAs/InGaAs metamorphic HEMT without gate recess," *J. Electrochem. Soc.*, vol. 155, pp. H932-H936, 2008.
- [49] Y. Sun, E. W. Kiewra, S. J. Koester, N. Ruiz, A. Callegari, K. E. Fogel, D. K. Sadana, J. Fompeyrine, D. J. Webb, J.-P. Locquet, M. Sousa, R. Germann, K. T. Shiu, and S. R. Forrest, "Enhancement-mode buried-channel $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ MOSFETs with high- κ gate dielectrics," *IEEE Electron Device Lett.*, vol. 28, pp. 473-475, 2007.



Semiconductor Technologies

Edited by Jan Grym

ISBN 978-953-307-080-3

Hard cover, 462 pages

Publisher InTech

Published online 01, April, 2010

Published in print edition April, 2010

Semiconductor technologies continue to evolve and amaze us. New materials, new structures, new manufacturing tools, and new advancements in modelling and simulation form a breeding ground for novel high performance electronic and photonic devices. This book covers all aspects of semiconductor technology concerning materials, technological processes, and devices, including their modelling, design, integration, and manufacturing.

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

Yeong-Her Wang and Kuan-Wei Lee (2010). Selective Oxidation on High-Indium-Content InAlAs/InGaAs Metamorphic High-Electron-Mobility Transistors, *Semiconductor Technologies*, Jan Grym (Ed.), ISBN: 978-953-307-080-3, InTech, Available from: <http://www.intechopen.com/books/semiconductor-technologies/selective-oxidation-on-high-indium-content-inalas-ingaas-metamorphic-high-electron-mobility-transist>

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