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High Performance Organic Thin-Film Transistors and Nonvolatile Memory Devices Using High-κ Dielectric Layers

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1. Introduction

Pentacene-based organic thin-film transistors ($OTFT_S$) are attractive because of their inherit merits of low cost, small weight and visible-light transparency, for potential use in applications such as organic displays, flexible displays and low-cost integrated circuit (IC) (Klauk et al, 1999; Zhou et al, 2005). The low thermal budget and rapid processing have strong advantages of energy saving and environment friendly (Chang et al, 2008), which are in sharp contrast to the prolonged 600°C annealing in conventional solid-phase crystallized (SPC) poly-crystalline silicon (poly-Si) TFTs (Hung et al, 2005). Although low thermal budget poly-Si TFTs can also be formed on plastic substrate using excimer laser annealing (Lemmi et al, 2004), the uniformity of threshold voltage (V_t) and mobility are the major concerns for TFTs on different poly-Si grains. Alternatively, although even single crystal sub-μm MOSFETs can be realized on plastic substrate (Kao et al, 2005) by fabrication first, thinning down the substrate, transferring and bonding, this method still requires high thermal budget for device fabrication.

However, conventional OTFTs require a high operating voltage and show a poor sub-threshold swing, which are opposite to the low power technology trend and detract from their suitability in IC operation. Besides, the relative low transistor current is difficult to drive the need high operation current of organic light-emitting diode (OLED). To address these issues, high dielectric constant (κ) material is required for OTFTs to improve the device performance. Using high-κ HfLaO as the gate dielectric, the pentacene OTFTs fabricated on SiO_2 showed even comparable device performance with SPC poly-Si TFTs, with extra merit of much better sub-threshold swing for low voltage and low power application (Chang et al, 2008). Similar good device performance was also achieved using high-κ HfLaO on pentacene OTFTs, fabricated on low-cost flexible polyimide substrates and useful for portable low power electronics (Chang et al, 2009).

Besides the logic TFTs, non-volatile memory function is also necessary for system-on-panel (SOP) application (Yin et al, 2008). Previously, OTFT memory devices have been reported using polymer insulators as the charge trapping layer (Baeg et al, 2006). Nevertheless, the OTFT memory devices require low program/erase (P/E) voltages, low reading voltages and

long data retention. Using the high-κ dielectrics for pentacene non-volatile memory fabricated on flexible polyimide substrate, low P/E voltage and reasonable long data retention were reached (Chang et al, 2008). The low P/E voltage results from the high gate capacitance using high-κ layers, while the small band-gap high-κ HfON trapping layer with deep trapping energy yields acceptable data retention. Further performance improvement of OTFT-based non-volatile memory is expected using advanced device design such as charge-trapping-engineered flash (CTEF) (Lin et al, 2008). The good device performance of logic OTFT and OTFT-based non-volatile memory should be useful to realize the flexible displays and low-cost IC in the near future.

2. High-κ Dielectric OTFT

2.1 Device Requirements

The technology goals for OTFT ICs are to achieve high speeds, large drive current and low power consumption. The high speed is necessary for SOP without using external Si logic ICs, while the low power is required for portable electronics. The high circuit speed arises from the high drive current of the OTFT, since the circuit delay (τ) is determined by

$$\tau = C_{load} V_{max} / I_{drive} \quad (1)$$

Here the C_{load}, V_{max} and I_{drive} are the load capacitance, maximum voltage and drive current respectively. The current of OTFT is expressed as the following equation of a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

$$I_d = \mu C_{ox}(W/L)[(V_g - V_t)V_d - V_d^2/2] \quad (2)$$

The μ and C_{ox} are the mobility and gate capacitance density, respectively. The L, W, V_g and V_d are the transistor's gate length, gate width, gate voltage and drain voltage, respectively. The source voltage is connected to ground (0 V). The maximum transistor drive current for the OTFT operated at saturation region (V_g-V_t<V_d) is simplified as

$$I_d = \mu C_{ox}(W/L)(V_g - V_t)^2/2 \quad (3)$$

A low V_t is beneficial for high drive current and low voltage operation, which is limited to a minimum 0.11 V of $4kT/q$ based on the thermal noise considerations. The increasing V_g can give the required high drive current but unfortunately increases the power consumption. Although the desired high drive current is reachable by decreasing L, the minimum L is limited to μm range from the practical consideration of low cost lithography. The increasing W can also increase the drive current, but this is opposite to the needed high resolution of display pixel. This is a fundamental challenge to use OTFT to drive high current OLED (Nomura et al, 2004), because of the low drive current from relatively low mobility.
One useful method to improve the drive current is to increase C_{ox}:

$$C_{ox} = \varepsilon_0 \kappa / t_{ox} \quad (4)$$

Although higher C_{ox} can be reached by decreasing the dielectric thickness (t_{ox}), this is restricted by the exponentially increasing leakage current. Therefore, the most effective method is to use high-κ material as the gate dielectric.
Currently, the high-κ gate dielectric has been used for Intel's 45 nm node MOSFET, with a small equivalent oxide thickness (EOT) of 1 nm. Here the EOT is defined as

$$EOT = t_{ox}(\kappa_{sio2}/\kappa) = t_{ox}(3.9/\kappa) \quad (5)$$

The κ_{sio2} is the dielectric constant for SiO_2, which has a value of 3.9.
It is important to notice that the combination of inorganic high C_{ox} and good mobility organic channel is the few practical method to realize the integrated OTFT with OLED, because of the needed high operation current for OLED. The high-κ dielectric OTFT can be implemented to the existing process line of Si TFT for low cost and light weight displays shown in following sections.

2.2 OTFT Device Design

One important advantage of OTFT is the significantly lower thermal budget and fast device process than SPC poly-Si TFT. However, the low hole mobility and poor sub-threshold swing are the drawbacks that give unwanted low drive current and slow turn on when operated at low voltage.
To overcome these problems, we used high-κ HfLaO as the gate dielectric for OTFTs. To mimic poly-Si TFTs fabricated on glass panel, we first fabricated the metal-gate and high-κ OTFTs on a thick SiO_2 layer grown on Si wafers. This is because of the different substrate size and processing equipments used for commercial glass panel and high-κ dielectric process for Si MOSFET. Figure 1 shows the schematic device diagram of the high-κ dielectric and organic channel OTFT, where a bottom gate electrode is used.

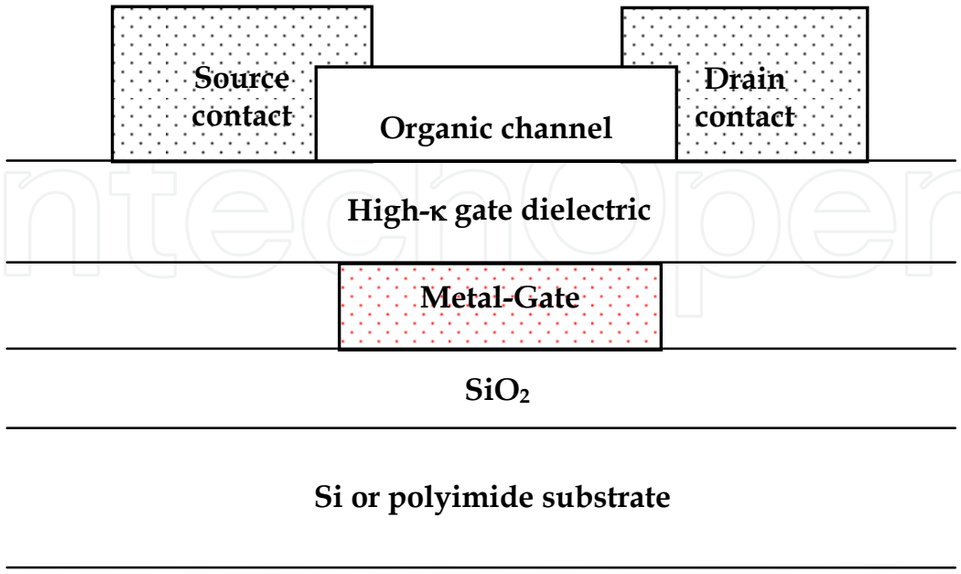

Fig. 1. Schematic device diagram of the OTFT using high-κ gate dielectric and metal gate.

Currently, the pentacene is the commonly used organic material for OTFT. The first question is what kind of gate electrode should be used. The metal gate offers a simple and low temperature process compared with doped poly-Si gate used in sub-μm MOSFET. However, the choice of proper metal-gate with adequate work-function is important to reach low leakage current of pentacene/high-κ/metal-gate OTFT.
Figure 2 shows the schematic diagram of energy-levels of molecular pentacene. For comparison, those of the single crystalline Si are also plotted. The energy levels for small-molecular materials like pentacene are defined as the lowest unoccupied molecular orbital (LUMO) and the highest occupied molecular orbital (HOMO), which are different from the electronic bands in crystalline lattice such as Si. The appreciable energy bands in polymer material may be obtained for highly crystalline defect-free material but this is difficult to reach. The important current conduction for OTFT is mainly along the direction of the polymer chain. For pentacene, the majority carriers for conduction are the holes that are occupied at HOMO energy level with work-function very close to the valence band of Si crystal with only 0.1 eV difference.

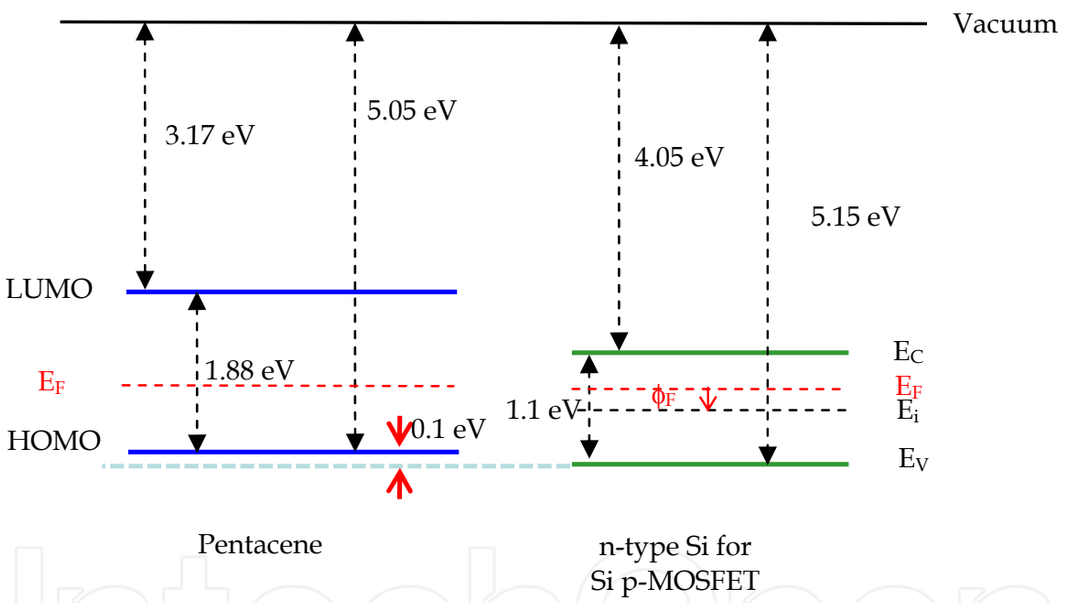

Fig. 2. Schematic energy-level diagrams of molecular pentacene and single crystal Si. An n-type doping in Si body is needed to form the p-MOSFET, but pentacene is difficult to dope into n-type.

For low V_t pentacene OTFT, the gate electrode should have work-function close to HOMO energy similar to a hole conductive p-type Si MOSFET (p-MOSFET). The V_t of the Si p-MOSFET is expressed as

$$V_t = \phi_{MS} - Q_{ox}/C_{ox} - 2\phi_F - Q_{dpl}/C_{ox} \quad (6)$$

Here ϕ_{MS} (ϕ_M-ϕ_S), Q_{ox}, Q_{dpl} and $2\phi_F$ are the work-function difference of metal-gate and pentacene, oxide charge, depletion region charge and surface bending voltage to turn on

OTFT, respectively. The ϕ_F is energy difference of Fermi level (E_F) to intrinsic level (E_i), which is related to doping concentration (N_D) and intrinsic carrier density (n_i) in Si by

$$\phi_F = (kT/q)\ln(N_D/n_i) \quad (7)$$

Note that the Si body of p-MOSFET is doped with opposite n-type doping. This lowers the leakage current in a p-MOSFET at off-state, when transistor is biased at V_g=0 V and V_{ds}<0 V. The n-type doping moves E_F toward E_C and forms energy barriers of p^+-n junctions in source and drain that lowers the off-state leakage current.
The V_t equation can also give important guideline to design the pentacene OTFT, although some of the important parameters are unknown in pentacene. Nevertheless, the pentacene is generally p-type and difficult to dope into n-type. Therefore, no leakage current blocking p^+-n junctions can be easily formed. One alternative method to lower the off-state leakage current is to form the partially depleted OTFT structure shown in Fig. 3(a), which has an opposite surface bend bending to accumulation mode shown in Fig. 3(b). This can be reached using relative low work-function metal-gate compared with the high work-function one used for low V_t Si p-MOSFET. However, the needed low leakage current is traded off the slightly high V_t, since higher V_g is required to form the strong hole accumulation mode and turn on the OTFT shown in Fig. 3(c). Such partially or even fully depleted channel has previously led to the invention of low leakage current Ge-on-Insulator (GOI) MOSFET (Huang et al, 2003), where the very high leakage current from small energy bandgap Ge (0.66 eV) is the major concern of the Ge MOSFET (Chin et al, 2005).

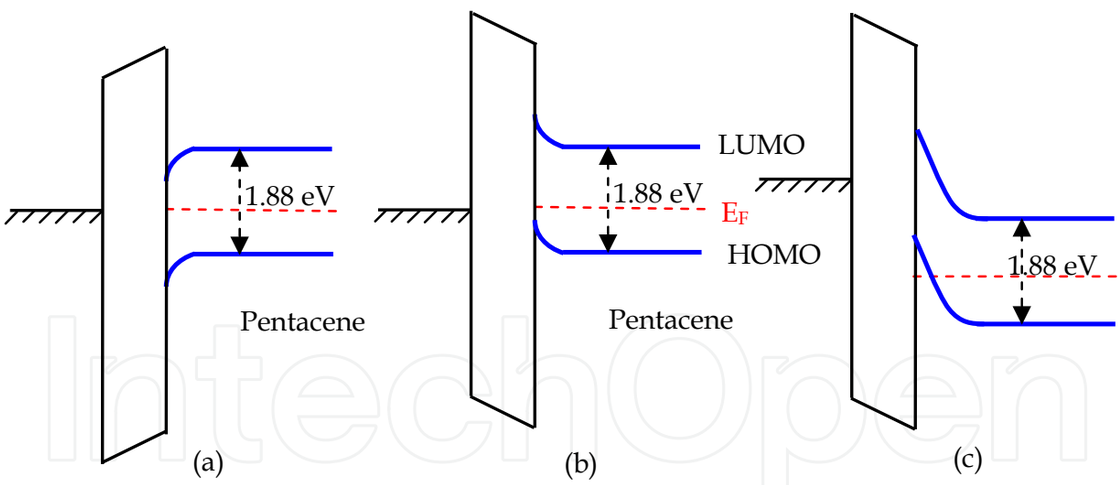

Fig. 3. Schematic energy-level diagrams of pentacene/oxide/metal-gate OTFT with (a) low and (b) high work-function metal-gate under equilibrium and V_g=0; (c) under a negative V_g bias to reach strong hole accumulation.

Although many elements in the periodic table have low work-function to meet the requirement of low off-state leakage, we choose the TaN as the gate electrode. This TaN electrode has been developed previously for metal-insulator-metal (MIM) capacitors used for Analog/RF and Dynamic Random Access Memory (DRAM) applications (Chiang et al, 2006), where similar bottom electrode device structure and process sequence were used. The

reason to choose TaN is because it has larger bond enthalpy than pure metals, which also has one of the strongest bond enthalpies among various metal-nitrides in the periodic table (Yu et al, 2005). Such robust metal-gate is required to lower the oxidation rate of gate electrode during subsequent high-κ gate dielectric deposition and post-deposition anneal (PDA), under an O_2 ambient. The oxidized metal-surface will degrade the EOT and leakage current by trap-assisted tunneling.

The second question is the choice of source-drain contact metals. Figure 4 shows the work-function of atoms in the periodic table. There are only 3 stable elements of Ir, Pt and Au that have work-function larger than the HOMO energy. The higher work-function than HOMO allows direct hole conduction via Schottky contact, without using p^+ doping in pentacene. Such direct source-drain metal contact provides unique advantages for low temperature and fast process compared with the high thermal budget of n^+-doped SPC poly-Si TFT (Hung et al, 2005), which is the enable technology on low temperature flexible substrate. Note that the Ni metal may be a low cost choice since it has reported 5.0~5.1 eV work-function (Chiang et al, 2007) close to that of HOMO. However, the vital OTFT drive current may decrease exponentially with increasing energy barrier of metal-pentacene energy difference, if the metal work function is slighter lower than HOMO level. Here the Au is the most widely used source-drain contact metal for pentacene, due to the significantly lower melting temperature than Pt and Ir for easy deposition using a simple thermal evaporation.

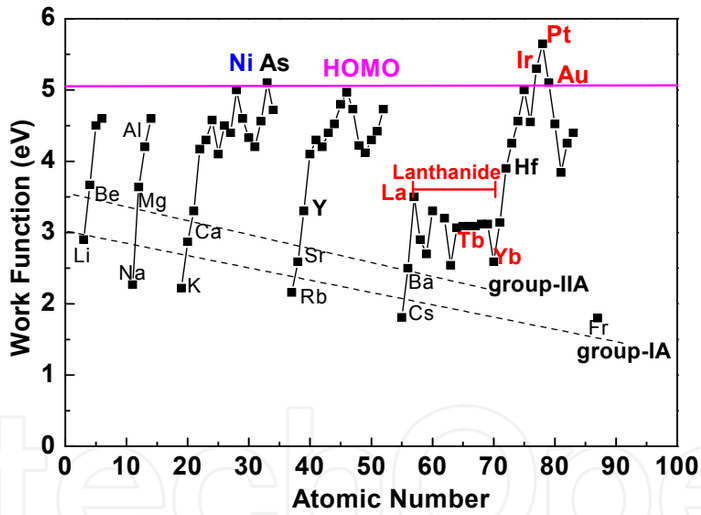

Fig. 4. Metal work-function as a function of atomic number in the periodic table.

The next question is the choice of proper high-κ gate dielectric for OTFT. Figure 5 shows the potential binary gate oxides for pentacene OTFT. Generally, the energy bandgap of high-κ dielectric and valence or conduction band offset (ΔE_V or ΔE_C) to pentacene decrease monotonically with increasing κ value. The higher κ value provides the wanted higher drive for OTFT. Nevertheless, a large enough ΔE_V or ΔE_C energy barrier of ~1 eV is required to reach the low gate leakage current for practical application. Fortunately, the ΔE_V is larger than ΔE_C for most high-κ dielectrics that is useful to reach low gate leakage current in p-type OTFT. Therefore, the HfO_2, ZrO_2, La_2O_3 (Chin et al, 2000) and TiO_2 (Cheng et al, 2008) are the few good candidates for pentacene OTFT. However, the κ value of TiO_2 or $SrTiO_3$

depends strongly on the growth temperature and the degree of dielectric crystallization. The high process temperature of 450~550°C for higher κ $SrTiO_3$ (Chiang et al, 2006) is not suitable to integrate the OTFT onto organic substrate. Here the HfO_2 is the most used high-κ gate dielectric for Intel's 45 nm node MOSFET using gate-last technology. The La_2O_3 capping (Wu et al, 2000) on HfSiON has been widely used for low V_t 32 nm node gate-first high-κ n-MOSFET, such as IBM, Toshiba, IMEC, SEMATECH etc.

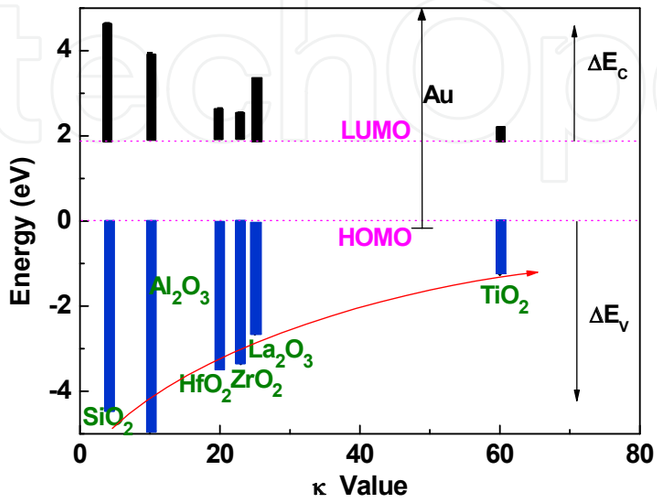

Fig. 5. Energy bandgap of oxides and band alignment to pentacene. Generally, both the bandgap and band offset become smaller with increasing κ value.

2.3 High Performance OTFT on SiO_2

The OTFT on SiO_2 has potential to replace the amorphous Si TFT on glass panel. The process of pentacene/high-κ/metal-gate OTFT starts with a 50 nm thick TaN gate electrode that was formed by sputtering deposition on the SiO_2/Si substrate through a shadow metal mask. An NH_3 plasma was further applied to the TaN surface (Chiang et al, 2005). Such NH_3 plasma treatment is the key factor to achieve low leakage current and small EOT in previous DRAM capacitors (Chiang et al, 2005; Cheng et al, 2008; Lin et al, 2009). Then the HfLaO gate dielectric with 20 nm thickness was deposited by electron beam evaporation at room temperature and followed by a 350°C O_2 PDA for 10 min. The adding La_2O_3 into HfO_2 is especially important to decrease the leakage current at low process temperature (Chang et al, 2008). After that the pentacene active layer with 70 nm thickness was deposited by electron beam evaporation through a shadow mask. The OTFT was finished by depositing 50 nm thick Au onto the pentacene and forming the source/drain contact electrodes.

Figure 6 shows the output characteristics of the fabricated pentacene/high-κ/metal-gate OTFT. Well-behaved I_d-V_d characteristics were measured under dark and air ambient, even at a low operation voltage of 2 V. This is the lowest reported operation voltage of OTFT for low power ($I_d \times V_d$) circuit application. Figure 7 shows the transfer characteristics of the pentacene/HfLaO/TaN OTFT. Here the V_t and mobility can be extracted from the linear $I_d^{1/2}$-V_g plot using *eq.* (3). This pentacene/high-κ/metal-gate OTFT shows excellent device integrity of a low V_t of -1.3 V, a record small sub-threshold swing of 78 mV/decade, good μ_{FE} of 0.7 cm^2/Vs and a large on- and off-state current ratio (I_{on}/I_{off}) of 1.0×10^5 (Chang et al,

2008). The low V_t and small sub-threshold swing ensure the OTFT to operate at low voltage. Such small sub-threshold swing is the best reported data among Si TFT (Hung et al, 2005) and OTFT (Klauk et al, 1999; Zhou et al, 2005; Kawasaki et al, 2006) to date, to the best knowledge. This small sub-threshold swing is close to the theoretical ideal value of 60 mV/decade for MOSFET at room temperature and even comparable with that of a 0.18-μm single crystalline Si MOSFET fabricated from an IC foundry (Kao et al, 2006).
To further understand the record low sub-threshold swing $[d(\log_{10}I_d)/dV_g]^{-1}$ of OTFT, we have examined the relation

$$\text{Sub-threshold swing} = (kT/q)ln10[1+(C_{dpl}+ C_{it})/C_{ox}] \quad (8)$$

Here C_{dpl} is the gate depletion capacitance density of pentacene. The C_{it} is the capacitance density from the pentacene/high-κ interface trapped charges that equals to interface trap density D_{it} by C_{it}/q. To measure the gate capacitance density C_{ox}, an Au/HfLaO/TaN capacitor was fabricated side-by-side along with the pentacene/HfLaO/TaN OTFT. A C_{ox} of 950 nF/cm² and a high-κ value of 24 were measured that gave a small EOT of 3.6 nm.

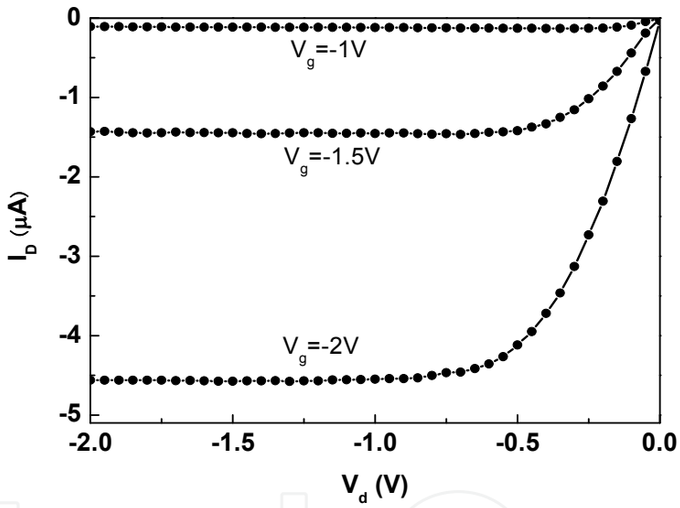

Fig. 6. Output characteristics of the pentacene/HfLaO/TaN OTFT. The device channel length and width are 80 μm and 2000 μm, respectively.

The C_{dpl} is smaller than high-κ C_{ox} and negligible, which leads to a D_{it} of 2×10^{12} eV^{-1}/cm^2 even processed at low temperature. This value is typical for high-κ gate dielectric MOSFET on single crystalline Si (Cheng et al, 2007). This good electrical interface property is the merit of using HfLaO as the gate dielectric for OTFT.

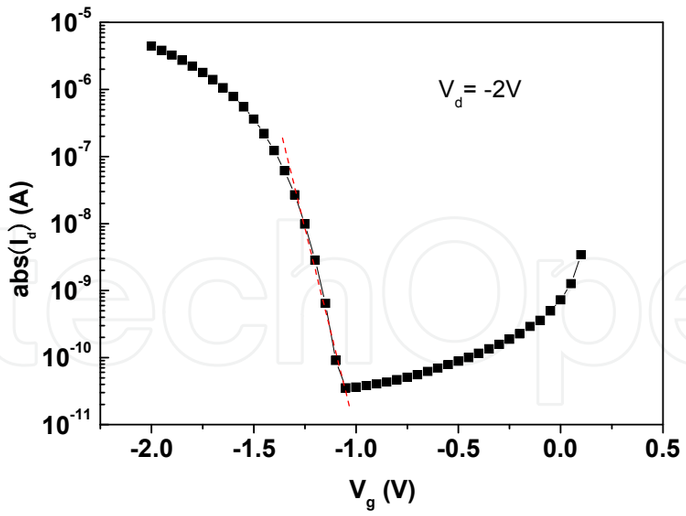

Fig. 7. Transfer characteristics of the pentacene/HfLaO/TaN OTFT with channel length and width of 80 μm and 2000 μm respectively. The sub-threshold swing is defined as the slope of I_d-V_g curve in voltage per current increase for 10X (a decade).

Table 1 summarizes the important device data of this p-channel OTFT and conventional n-channel poly-Si TFTs (Choi et al, 1999; Lin et al, 1999; Chang et al, 2003). The pentacene/high-κ/metal-gate OTFT has better device performance in terms of lower V_t and much smaller sub-threshold swing. This OTFT device also has comparable normalized drive current (μC_{ox}) with the poly-Si TFTs. Here the μC_{ox} is normalized to the channel length L, width W and over-drive V_G-V_T:

$$\mu C_{ox} = 2I_d\,(L/W)\,/(V_G\text{-}V_T)^2 \tag{9}$$

Thus, the high C_{ox} is as important as the high mobility for high drive current. Besides, higher mobility above 5 cm²/Vs is reachable by optimizing the chemistry (Lee et al, 2006). The excellent device characteristics ensues the good potential for OTFT used for display.

Active channel	Gate dielectric	V_t, V	Sub-threshold swing, V/decade	μ, cm²/Vs	μC_{ox}, nF/cm²	I_{on}/I_{off}
Pentacene (This work)	HfLaO	-1.3	0.078	0.7	674	1.0×10^5
poly-Si (Choi et al, 1999)	LPCVD SiO_2	5.6	1.4	20	863	3.5×10^5
poly-Si (Lin et al, 1999)	PECVD TEOS SiO_2	8.1	1.97	12	716	3.0×10^5
poly-Si (Chang et al, 2003)	PECVD TEOS SiO_2	-	2.67	3	259	-

Table 1. Device data of p-channel pentacene/HfLaO/TaN OTFTs and compared with n-channel poly-Si TFTs.

2.4 OTFT on Flexible Substrate

The important advantages of OTFT are its flexibility and low process temperature that can be used for flexible displays and low-cost flexible electronics. Based on the excellent device performance of pentacene/high-κ/metal-gate OTFTs on SiO_2 shown in previous section, the process temperature was further decreased to 200°C to fabricate the OTFTs on low-cost flexible polyimide substrates (Kapton HPP-ST, Dupont). This substrate is much more economical than other polyimide (Kapton E-type, DuPont) and polyethylene naphthalate (PEN) (Teonex Q65 PEN, Dupont) substrates, although the cost is traded off the degraded performance of poor surface roughness and impurity out-diffusion.

To improve the impurity diffusion, the polyimide substrates (Kapton HPP-ST, DuPont) with 125 μm thickness were annealed at 200°C in a vacuum environment. To lower the internal stress, a thin 100 nm SiO_2 was deposited on the polyimide substrate at room temperature by electron beam evaporation. Then the pentacene/HfLaO/TaN OTFTs were fabricated on SiO_2/polyimide by following the similar process steps in previous section on SiO_2/Si, with lower 200°C PDA temperature and thicker 30 nm HfLaO gate dielectric (Chang et al, 2009). The thicker HfLaO is to compensate the degraded gate leakage current when processed at lower temperature. The schematic diagram of fabricated devices is shown in Fig. 1, where the OTFTs were measured in the dark and air ambient.

Figure 8 shows the output characteristics of the fabricated OTFT on SiO_2/polyimide. Well-behaved I_d-V_d characteristics were obtained, under a low voltage operation of 2.5 V for low power electronics application. Figure 9 shows the I_d-V_g characteristics of the pentacene/high-κ/metal-gate OTFT on SiO_2/polyimide. The V_t and mobility were extracted from the linear $I_d^{1/2}$-V_g plot.

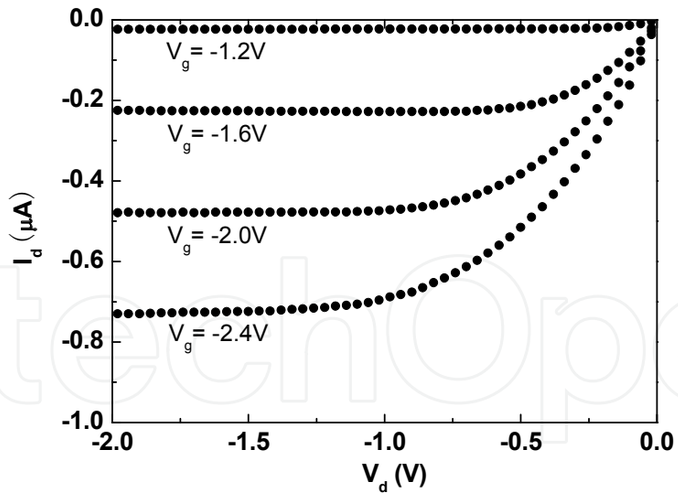

Fig. 8. Output characteristics of the pentacene/HfLaO/TaN OTFT on SiO_2/polyimide. The device channel length and width are 100 μm and 2000 μm, respectively.

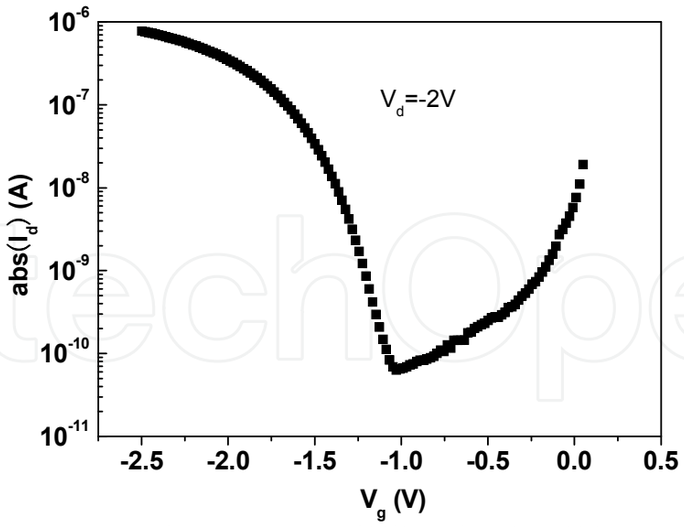

Fig. 9. Transfer characteristics of the pentacene/HfLaO/TaN OTFT on SiO_2/polyimide, with device channel length and width of 100 μm and 2000 μm respectively. The increasing current at V_g>-1 V suggests the electron conduction, but the small current is due to the high barrier source-drain electrodes.

The pentacene/HfLaO/TaN OTFT on SiO_2/polyimide shows good device performance of a low V_t of -1.25 V, a small sub-threshold swing of 130 mV/decade, a μ_{FE} of 0.13 cm²/Vs and a I_{on}/I_{off} of 1.2×10⁴ (Chang et al, 2009). The low operation voltage of -2.4 V is due to the low V_t and small sub-threshold swing. Such small sub-threshold swing is better than other reported values for flexible OTFTs (Choi et al, 2005, Kang et al, 2005; Klauk et al, 2005; Mizukami et al, 2006; Na et al, 2007), which is due to the using high-κ HfLaO dielectric with a high capacitance density of 450 nF/cm² and a small EOT of 7.7 nm. The smaller mobility and I_{on}/I_{off} than similar OTFT fabricated on SiO_2/Si were due to the rougher HfLaO surface of 4.2 nm measured by Atomic Force Microscopy (AFM), which was originated from the poor 9.0 nm surface roughness of low cost polyimide substrate (Kapton HPP-ST, Dupont). The drain current at V_g>-1 V may be attributed to the ambipolar behavior of electron conduction (Schön & Kloc 2001), although the current is limited by inadequate high work-function source-drain electrodes. However, this ambipolar conduction may be useful for pentacene-based non-volatile memory discussed in next session.

Table 2 compares the important device data of our work with other flexible pentacene OTFTs using various gate dielectrics and fabricated on high quality polyimide (Kapton E-type) and PEN (Teonex Q65 PEN, DuPont) substrates. The pentacene/HfLaO/TaN flexible OTFT shows comparable device performance of normalized drive current and I_{on}/I_{off} with other OTFTs fabricated on high cost substrates, with the added merit of the best sub-threshold swing for fast turn on and low voltage operation. The good device performance of low voltage operated OTFT, on low cost polyimide substrate, should lead to future more economic low-power flexible electronics.

Flexible substrate	Gate dielectric	V_t, V	Sub-threshold swing, V/decade	μ, cm^2/Vs	μC_{ox}, nF/cm^2	I_{on}/I_{off}
Polyimide Kapton HPP-ST (This work)	HfLaO	-1.25	0.13	0.13	58	1.2×10^4
Polyimide Kapton E-type (Choi et al, 2005)	BZN	0.1	0.3	0.5	110	3.5×10^5
Polyimide Kapton E-type (Kang et al, 2005)	Mn-doped $BaSrTiO_3$	-1	-	0.32	35	$<1\times10^3$
PEN (Klauk et al, 2005)	PVP	-	0.6	0.1	6	1×10^4
PEN (Mizukami et al, 2006)	Ta_2O_5	0.8	-	0.25	35	-
PEN (Na et al, 2007)	$TiSiO_2$	-0.88	0.315	0.67	95	1×10^4

Table 2. Device data of pentacene active channel OTFTs using various gate dielectrics and fabricated on different flexible substrates.

3. Organic Non-volatile Memory Devices Using High-κ Dielectric

3.1 Device requirements

Based on the good device performance of flexible OTFT, we can further apply to the non-volatile memory. Such non-volatile memory function is indispensible for SOP (Baeg et al, 2006). The first task for OTFT-based non-volatile memory is to choice the proper device structure that can meet the device requirement of low write power, long retention, good endurance and fast write speed.

Among various new types non-volatile memory devices such as Phase Change Random Access Memory (PRAM) and resistive RAM (RRAM), the SiO_2/poly-Si/SiO_2 floating gate flash memory device still has irreplaceable advantage of the lowest write current and being one-transistor (1T) in size compared with other one-transistor-one-resistor (1T1R) designs. Such low current is mandatory for page writing NAND logic and low power portable electronics. This floating gate flash memory shown in Fig. 10 (a) employs the well-known device physics and manufacturing experience of the Si industry. Digital data can be programmed into the device by injecting charges over tunnel oxide, or erased by removing the stored charges or injecting different polarity charges into the trapping layer. The program or erase function can be obtained by applying a large gate electric field across the tunnel oxide. This charge transfer is readable by measuring the V_t of the transistor.

The fundamental challenge of a conventional floating-gate flash device is that all the storage charges can leak out via a single oxide defect by trap-assisted tunneling shown in Fig. 10(a). This is due to the drawback of electrically conductive poly-Si charge storage layer. Unfortunately, such oxide defect is inevitable that can be generated by continuous device

operation and measurable from the stress-induced leakge current (SILC). One method to address this issue is to use the [metal-gate]-oxide-nitride-oxide-semiconductor (MONOS) device structure. As shown in Fig. 10(b), the programmed charges are stored in discrete and electrically-isolated zero-dimensional quantum traps within the Si_3N_4, while only the trapped charges, close to oxide defects generated by write cycles, can leak out. Besides, the physically separated traps allow the storage of 2 bits/cell in both source and drain sides to increase the memory density.

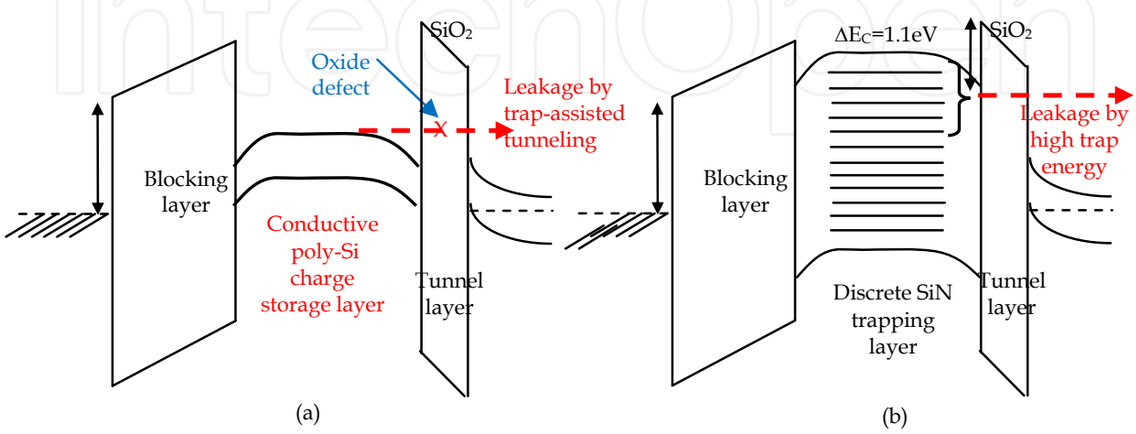

Fig. 10. Schematic energy band diagram of the electron trapping (a) poly-Si floating gate and (b) MONOS non-volatile memory devices.

In addition to the low write current and good endurance of multiple write cycles, the non-volatile memory devices also need good data retention and fast write speed. However, the charge-storage energy in Si_3N_4 traps is much higher than conventional poly-Si floating gate flash as shown in Fig. 10 that causes the stored charges to leak out. One method to maintain the good data retention, without scarifying the write speed, is to engineer the trap energy level. Here the deeper trapping energy level, the better data retention.

This can be reached by replacing the conventional Si_3N_4 with a high-κ metal-nitride dielectric shown in Fig. 11, where the later should have deeper ΔE_C or ΔE_V to barrier oxide layers for better charge retention. However, there are few metal-nitrides in the periodic table that can meet this requirement. Most metal-nitrides are metallic and similar to conductive poly-Si floating gate, which failed for discrete trapping MONOS application. The few candidates left are BN, AlN, GaN, InN etc, but the BN is difficult to process because of the strong bonding energy. Note that the AlGaN and GaInN have been widely used for blue-light LED. The using deep trapping energy AlN and AlGaN were initiated by Chin's group (Lai et al, 2005; Chin et al, 2005). Further lowering the P/E voltage with good retention can be reached by using higher κ synthesized HfON trapping layer (Lai et al, 2006). The significantly better retention using deep ΔE_C AlGaN trapping layer was also affirmed by Samsung's work (Joo et al, 2006). The alternative high-κ metal-nitride trapping layer was also listed in the *International Technology Roadmap for Semiconductors* (*ITRS*, 2007) for future generation charge-trapping flash (CTF) non-volatile memory.

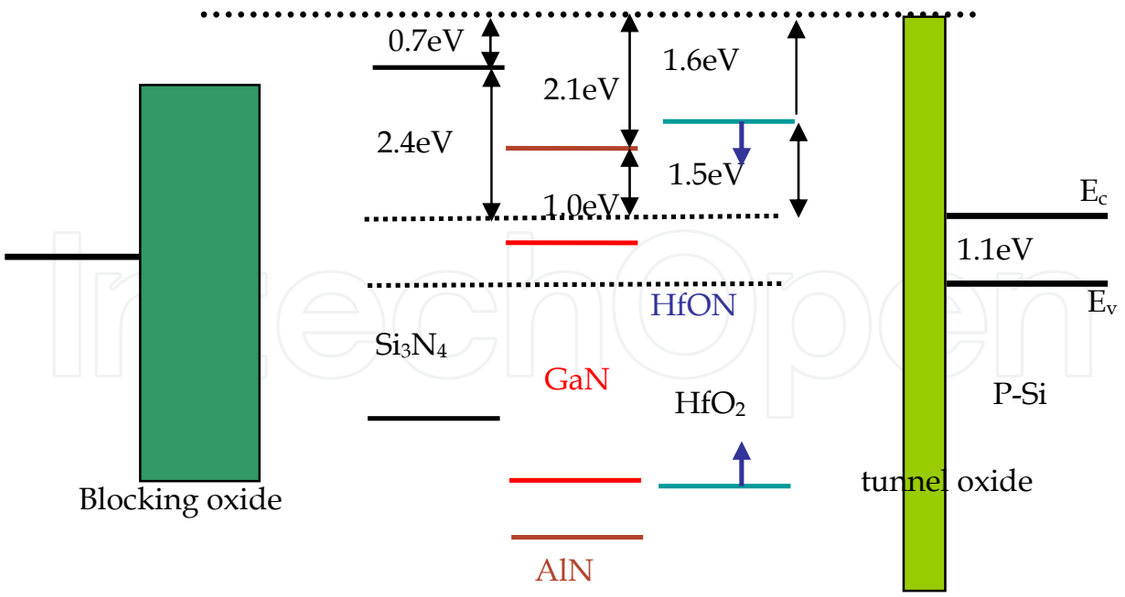

Fig. 11. Schematic energy band alignments for different trapping layers of Si_3N_4, AlN, GaN and HfON within the MONOS structure.

3.2 OTFT MONOS Non-volatile Memory on Flexible Polyimide

Similar to the OTFT on flexible polyimide, the bottom gate TaN-HfLaO-HfON-HfO_2-Pentacene (MONOP) memory was fabricated on a low-cost flexible polyimide substrate (Kapton HPP-ST). The device fabrication starts the substrates annealing at 200°C. Then 100 nm SiO_2 was deposited and 50 nm TaN gate electrode was formed. After applying the NH_3^+ plasma to TaN surface, the 20 nm HfLaO blocking oxide, 20 nm HfON trapping layer and 6 nm HfO_2 tunnel layer were deposited. Then a 200°C O_2 PDA was applied to improve the dielectric quality. After that 70 nm pentacene active layer was deposited at 70°C. The device was finished by making Au source-drain electrodes and forming ohmic-like contact for the hole injection. Here a thicker HfLaO blocking layer is important to reduce gate leakage current during erase.

The transfer hysteresis curves of OTFT MONOP memory device under P/E are shown in Fig. 12. From the initial transfer characteristics at a saturation V_d of -3 V, the V_t, sub-threshold swing, mobility, and I_{on}/I_{off} were -1.4 V, 160 mV/decade, 0.1 cm^2/Vs and 1×10^4, respectively. These data are very close to the pentracene/HfLaO/TaN OTFT on the same flexible polyimide substrate shown in previous section. When a program V_g of -12 V and 1 ms was applied, the holes accumulated at HfO_2/pentacene interface can tunnel through the HfO_2 by the large gate electric field and trapped in the HfON layer. This increases the $|V_t|$ and shifts the I_d-V_g curve in negative direction. When an erase V_g of 12 V for 100 ms was applied, the trapped holes in the HfON may tunnel out over the HfO_2 by the electric field and lowered the $|V_t|$. Alternatively, the minority carriers of electrons may also be generated in the depletion region of pentacene, tunnel into the HfON and annihilate the trapped holes (Chin et al, 2006). Therefore, the V_t value can be shifted, reversibly, by applying an appropriate program or erase V_g. Nevertheless, the erase is much more difficult than program since the density of minority carriers is less in large bandgap pentacene.

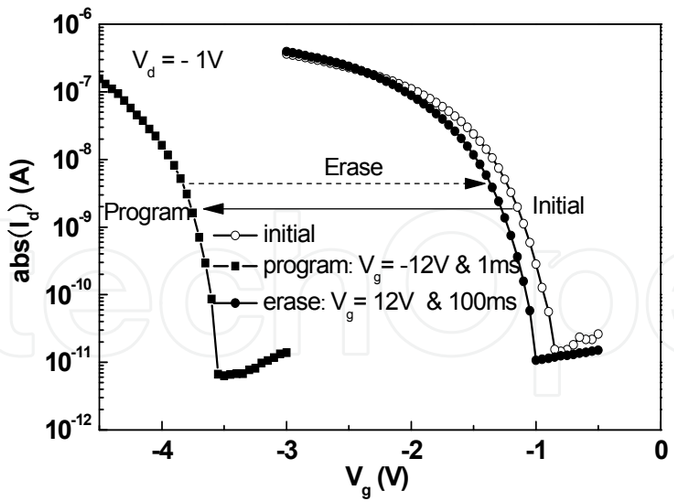

Fig. 12. Transfer hysteresis curves for a pentacene OTFT memory device under V_g = -12 V, 1 ms program and V_g = 12 V, 100 ms erase at V_d = -1 V. The channel length and width were 150 and 1500 μm, respectively.

Good retention characteristics are necessary for non-volatile memory. Figure 13 shows the retention data under a program and erase condition of -12 V for 1 ms and 12 V for 100 ms. Here the V_t was extracted from the linear I_d-V_g characteristics. The initial memory window of 2.4 V was obtained that decreased to 0.78 V after 48 hrs retention. The fast charge loss for the first 10^3 s is possibly due to the defects in the low temperature formed HfO_2 and the rough tunnel oxide surface by low cost polyimide substrate. The charge loss becomes stable at time longer than 10^3 s. If no other charge loss mechanism, an extrapolated 10-year retention window of 0.55 V may be reachable that is large enough for sense amplifier.

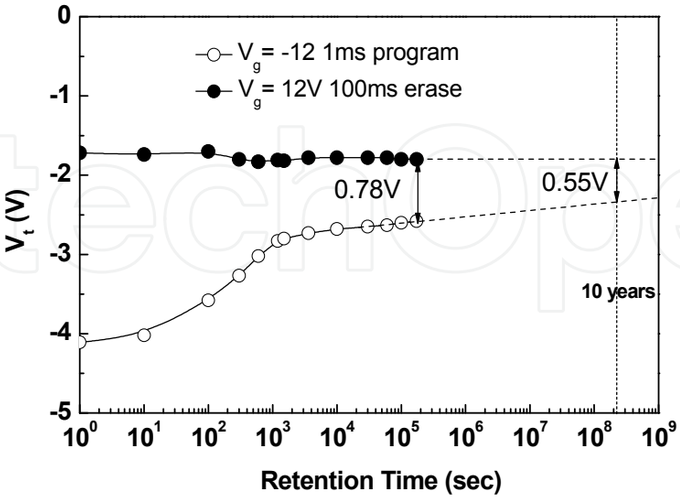

Fig. 13. Retention characteristics for pentacene MONOP OTFT device.

4. Conclusions and Future Directions

The high transistor current of OTFT is the key factor to drive the high operation current OLED and high resolution display. This can be achieved by increasing the mobility of pentacene and gate dielectric C_{ox} using high-κ dielectric. Although the highest reported mobility for pentacene is better than amorphous Si, it is still inferior to poly-Si or high mobility InGaZnO (Nomura, et al, 2004). This limit makes the using high-κ gate dielectric more important and inevitable. The using metal-gate is also necessary to decrease the OTFT leakage current and improve the I_{on}/I_{off} by forming the partially depleted OTFT. Good device integrity of pentacene/HfLaO/TaN OTFT on SiO_2 is reached with a low V_t of -1.3 V, the record best sub-threshold swing of 78 mV/decade, a good μ_{FE} of 0.7 cm^2/Vs and a large I_{on}/I_{off} of 1.0×10^5. The pentacene/HfLaO/TaN OTFT on low-cost flexible polyimide shows still reasonable good device performance of a low V_t of -1.25 V, a small sub-threshold swing of 130 mV/decade, a μ_{FE} of 0.13 cm^2/Vs and a I_{on}/I_{off} of 1.2×10^4. Based on the good OTFT device performance, the MONOP non-volatile memory shows an initial memory window of 2.4 V and a 48 hrs retention window of 0.78 V, under a low P/E condition of -12 V for 1 ms and 12 V for 100 ms. Further improving the retention may be achievable using advanced CTEF non-volatile memory structure and using smoother flexible substrate.
One of the reasons to give pentacene the higher mobility than amorphous Si is due to the short range ordering. Further improving mobility might be achievable by forming other ordering in organic martial such as Si Cage Clusters (Hiura, Miyazaki, & Kanayama, 2001).

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This book provides a timely overview of a current state of knowledge of the use of polymer thin film for important technological applications. Polymer thin film book covers the scientific principles and technologies that are necessary to implement the use of polymer electronic device. A wide-ranging and definitive coverage of this emerging field is provided for both academic and practicing scientists. The book is intended to enable readers with a specific background, e.g. polymer nanotechnology, to become acquainted with other specialist aspects of this multidisciplinary field. Part A of the book covers the fundamental of the key aspect related to the development and improvement of polymer thin film technology and part B covers more advanced aspects of the technology are dealt with nano-polymer layer which provide an up-to-date survey of current research directions in the area of polymer thin film and its application skills.

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