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A Novel De Bruijn Based Mesh Topology for Networks-on-Chip

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1. Introduction

The mesh topology is the most dominant topology for today's regular tile-based NoCs. It is well known that mesh topology is very simple. It has low cost and consumes low power. During the past few years, much effort has been made toward understanding the relationship between power consumption and performance for mesh based topologies (Srivasan et al., 2004). Despite the advantages of meshes for on-chip communication, some packets may suffer from long latencies due to lack of short paths between remotely located nodes. A number of previous works try to tackle this shortcoming by adding some application-specific links between distant nodes in the mesh (Ogras & Marculescu, 2005) and bypassing some intermediate nodes by inserting express channels (Dally, 1991), or using some other topologies with lower diameter (sabbaghi et al., 2008).

The fact that the de Bruijn network has a logarithmic diameter and a cost equal to the linear array topology motivated us to evaluate it as an underlying topology for on-chip networks. De Bruijn topology is a well-known network structure which was initially proposed by de Bruijn (de Bruijn, 1946) as an efficient topology for parallel processing. Samathan (Samathan & Pradhan, 1989) showed that de Bruijn networks are suitable for VLSI implementation, and several other researchers have studied topological properties, routing algorithms, efficient VLSI layout and other important aspects of the de Bruijn networks (Park & Agrawal, 1995; Ganesan & Pradhan, 2003).

In this chapter, we propose a two-dimensional de Bruijn based mesh topology (2D DBM for short) for NoCs. We will compare equivalent mesh and 2D DBM architectures using the two most important factors, network latency and power consumption. A routing scheme for the 2D DBM network has been developed and the performance and power consumption of the two networks under similar working conditions have been evaluated using simulation experiments. Simulation results show that the proposed network can outperform its equivalent popular mesh topology in terms of network performance and energy dissipation.

2. The 2D DBM Topology

2.1 The Structure

The basic idea about our work is based on digraphs, and in this section, we present the information compiled from studies conducted on the de Bruijn digraph (Liu & Lee, 1993 ; Mao & Yang , 2000).

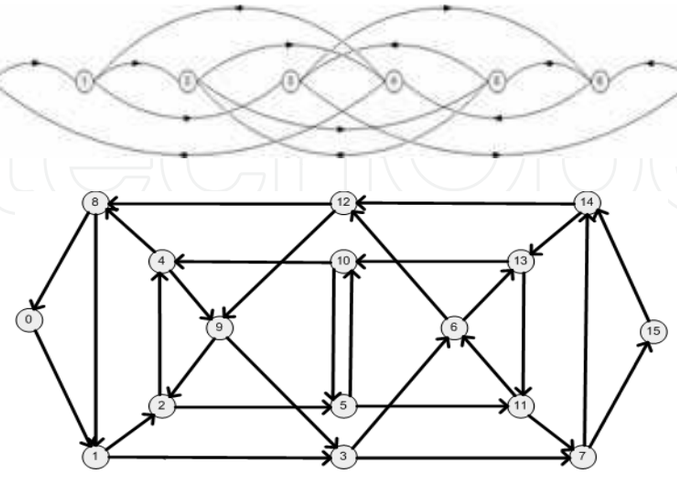
The de Bruijn topology has many applications in communication networks and parallel processing (Samanathan & Pradhan, 1989). A de Bruijn graph has k^n nodes. Each node $u=(u_{n-1},...,u_0)$ has an edge to node $v=(v_{n-1},...,v_0)$ if and only if $v_i = u_{i-1}$ $1 \le i \le n-1$. Node v has a unidirectional direct link to node u if and only if

$$u = v \times k + r (\mathrm{mod}\, k^n), \quad 0 \le r \le k-1 \tag{1}$$

The in-degree and out-degree of a node is equal to k. Therefore, the degree of each node is equal to $2k$. The diameter of a de Bruijin graph is equal to n which is optimal. The de Bruijn also has a simple routing algorithm. Case k=2 is the most popular de Brujin network which is also used in this study. Due to the logarithmic (optimal) diameter and a simple routing algorithm, it can be expected that the traffic on channels in the network will be less than other networks, resulting in a better performance (Ganesan & Pradhan, 2003).

Examples of de Bruijn networks are illustrated in Fig. 1. Several researchers have studied the topological properties (Liu & Lee, 1993 ; Mao & Yang , 2000) and efficient VLSI layout (Samanathan & Pradhan, 1989; Chen et al., 1993) of the de Bruijn networks. Moreover, the scalability problem of de Bruijn networks is addressed in (Liu & Lee, 1993). In de Brujin network data is circulated from node to node until it reaches its destination. Each node has two outgoing (incoming) connections to (from) other nodes via shuffle (rotate left by one bit) and shuffle-exchange (rotate left by one bit and complement LSB) operations to neighboring nodes (Louri & Sung, 1995). Owing to the fact that these connections are unidirectional, the degree of the network is the same as the one-dimensional mesh networks (or linear array network). The diameter of a de Bruijn network with size N, that is, the distance between nodes 0 and N-1, is equal to log (N).

(a)



(b)

Fig. 1. The de Bruijn network with (a) 8 nodes and (b) 16 nodes

2.2 The 2D DBM Topology

In a 2D DBM network, the nodes in each row and each column form a de Bruijn network. Each node has two outgoing edges along which data packets can be sent to other nodes, and two incoming links receiving data packets from other nodes in each dimension. Thus, node (u, v), $u = (u_{n-1},...,u_0)$, $v = (v_{n-1},...,v_0)$, has edges to node (u', v) if and only if $u'_i = u_{i-1}$ for $1 \le i \le n-1$, and node (u, v'), if and only if $v'_i = v_{i-1}$ for $1 \le i \le n-1$. Node (u', v') has a direct link to node (u, v') if and only if

$$u = 2u' + r_{\bmod 2^n}, \quad r = 0,1 \tag{2}$$

and to node (u', v) if and only if

$$v = 2v' + r_{\bmod 2^n}, \quad r = 0,1 \tag{3}$$

The 8×8 2D DBM is shown in Fig. 2.

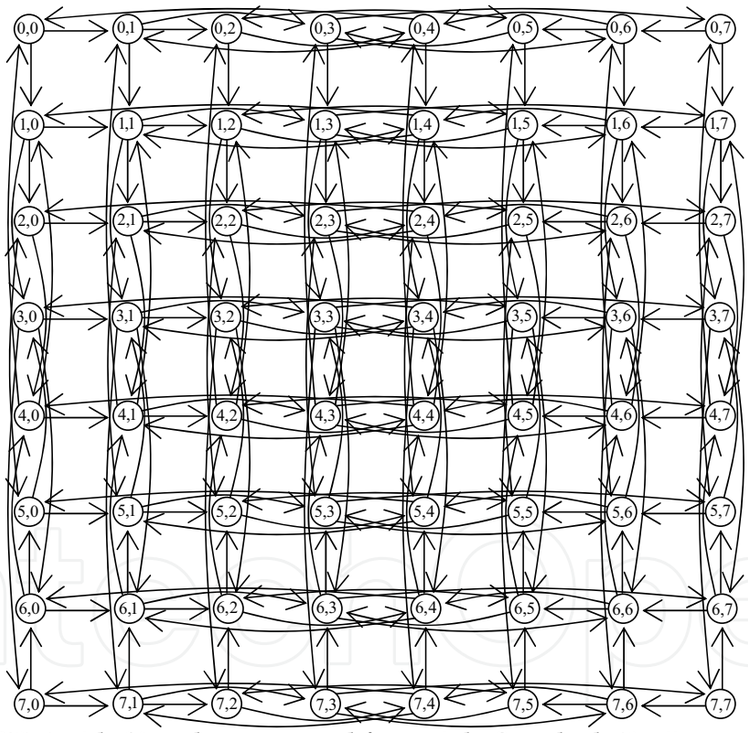


Fig. 2. A 2D DBM with 64 nodes composed from eight 8-node de Bruijn networks (as shown in Fig.1. a) along each dimension

The 2D DBM networks have some interesting topological properties that motivate us to consider them as a suitable candidate for on-chip network architectures. The most important property of 2D DBM networks is that while the number of links in a 2D DBM and an equal-sized mesh are exactly the same, the network diameter of this network is less than that of the

mesh. More precisely, the diameter of a 2D DBM and a mesh are $2\log N^{0.5}$ and $2(N^{0.5}-1)$, respectively, where N represents the network size.
Although, establishing the new links removes the link between some adjacent nodes (for example 1 to 0, 2 to 1 and 3 to 4 connections in Fig. 1) and increases their distance by one hop. In this network, however, the distance between many nodes is decreased by one or multiple hops, compared to a mesh, and this can lead to a considerable reduction in the average inter-node distance in the network.
The 2D DBM links are unidirectional and at most 8 unidirectional links are used per node. This is equal to the number of links connected to a node in a mesh (which is 4 bidirectional links). Since the node degree of a topology has an important contribution in (and usually acts as the dominant factor of) the network cost, the proposed topology can achieve lower average distance than a 2D mesh while it has almost the same cost. However, we will discuss the area overhead due to longer links in 2D DBM in next sections.

2.3 Routing Algorithm

During past years, a number of routing algorithms have been developed for the original de Bruijn network. Ganesan (Ganesan & Pradhan, 2003) proposed a routing algorithm which routes the packets toward the destination by changing one bit at a time, starting from the most significant bit of an n-bit address in a network of size 2^n. At the i^{th} step of this algorithm, the n-i^{th} bit of the destination address is compared to the MSB of the current address. If they are equal, the message is routed over the shuffle channel, to keep the bit unchanged and rotate the address. Otherwise, the message is routed over the shuffle-exchange channel to make the two bits identical and then rotate the address (self-loops are avoided). This algorithm involves a maximum of n steps. In order to be deadlock-free, this algorithm requires n virtual channels and the message uses the i^{th} channel at the n-i^{th} step. Since in this virtual channel selection scenario routing is performed in a descending order regarding channel numbers, the dependency graph of virtual channels is acyclic and the routing is deadlock-free (Dally & Seitz, 1987).
Ganesan (Ganesan & Pradhan, 2003) splits the networks into two trees: T1 and T2. A message is routed between T1 to T2, and then in T2, and then the message is routed between T2 to T1 and then in T1. Therefore, this routing algorithm has four different steps, which may also decrease, depending on the source and destination nodes. The algorithm has two phases and initiates with phase 0 (using virtual channel 0). When the message goes through T2 to T1, the phase number increases (virtual channel 1 is used). Ganesan (Ganesan & Pradhan, 2003) proved that this method is deadlock-free. The two trees, T1 and T2, are depicted in Fig. 3 for N=8.

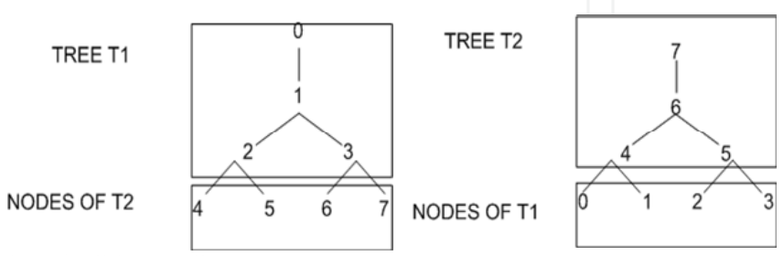


Fig. 3. Trees T1 and T2 for N=8

Park (Park & Agrawal, 1995) has deformed the de Bruijn as two graphs, increasing and decreasing. In the i^{th} stages, the MSB of the current node is compared with the n-i^{th} bit of the destination node, and if they are the same, shuffle cycle is used; otherwise, shuffle-exchange is used. If the path switches from increasing graph to the decreasing graph, the virtual channel number increments by 1. It is proved that the mentioned algorithm for the de Brujin network is deadlock-free (Park & Agrawal, 1995). Park (Park & Agrawal, 1995) has shown that for a de Brujin network with N nodes (N=2^n) this kind of routing requires

$$\text{Number of V.C.} = n - \left\lfloor \frac{n-1}{2} \right\rfloor \tag{4}$$

virtual channels to ensure deadlock freedom.
So, for N=8, it requires 2 virtual channels. For N=16 nodes, (n=4), based on equation (4), the number of virtual channels needed for a deadlock-free routing is equal to 3. Virtual channel 0 is more crowded than the other virtual channels. The routing algorithm uses virtual channels unevenly and very few packets use all the virtual channels.
We revised the routing algorithm to balance the use of virtual channels. In our proposed solution, at each node, the header flit has a degree of flexibility in selecting virtual channels, as used in (Kiasari et al., 2005). For example, for N=16, some of the source nodes may use only 1 virtual channel. Some nodes use 2 virtual channels and a few source nodes use 3 virtual channels. For the last group (those use 3 virtual channels), virtual channel 0 is selected in the source node. For the second group, we start with virtual channel 1 and for the first group we start from virtual channel 2. If virtual channel 2 is occupied, then we can use virtual channel 1 and finally virtual channel 0 is chosen. Using this method, virtual channels are used uniformly.
In this chapter, for routing in the 2D DBM, we use the revised method of Park (Park & Agrawal, 1995) in each dimension and we choose the paths and nodes in a way that the routing is minimal. Like XY routing in mesh networks, the deterministic routing first applies the routing mechanism in rows in order to deliver the packet to the column at which the destination is located. Afterwards, the message is routed to the destination by applying the same routing algorithm in the columns. Obviously, adding the second dimension in this routing scheme does not generate a cycle and the whole routing in the 2D network is deadlock-free provided that the routing in each dimension is deadlock-free (Duato et al., 2005).

3. Simulation Results

3.1 Simulator

To simulate the proposed NoC topology, we have used an interconnection network simulator that is developed based on POPNET simulator (Popnet, 2007) with Orion power library embedded in it. Orion is a library which models the power consumption of the interconnection networks (Wang et al., 2002). Providing detailed power characteristics of the network elements, Orion enables the designers to make rapid power performance tradeoffs at the architecture level (Wang et al., 2002). As mentioned in (Wang et al., 2002), the total energy each flit consumes at a specified node and its outgoing link is given by

$$E_{flit} = E_{wrt} + E_{arb} + E_{read} + E_{xb} + E_{link} \quad (5)$$

It consists of five components: 1) the power that is consumed for writing into buffers, 2) the power of arbiter, 3) the power that is consumed in reading from buffers, 4) the power of the internal crossbar, and 5) the power that is consumed in the links.

The POPNET simulator is only introduced for a two-dimensional mesh topology (Popnet, 2007). We have customized the simulator to support other topologies and other routing algorithms such as shuffle-exchange (Sabbaghi et al., 2008), and de Bruijn topologies. The power is obtained and reported for each layer and each component of the network.

We set the networks link width to 32 bits. Each link has the same bandwidth and one flit transmission is allowed on a link. The power is calculated based on a NoC with 90 nm technology whose routers operate at 250 MHz. Based on the core size information presented in (Mullins et al., 2006), we set the width of the IP cores to 2 mm, and the length of each wire is set based on the number of cores it passes. The simulation results are obtained for 8×8 and 16×16 mesh NoCs with XY routing algorithm, and 8×8 and 16×16 de Bruijn NoCs using the routing algorithms described in the previous section. The message length is assumed to be 32 and 64 flits and 2 and 3 virtual channels per physical channel are used. Messages are generated according to a Poisson distribution with rate λ. The traffic pattern can be *Uniform, Matrix-transpose*, and *Hotspot* (Duato et al., 2005).

3.2 Comparison Results

In this section, we evaluate the 2D DBM and compare it with the mesh, the most common topology for NoCs. Based on the necklace properties in de Bruijn layout (Chen et al., 1993), we have considered a more efficient layout for each row and column of the 2D DBM as shown in Fig. 4. With this new layout the total wire length used in the network is decreased. For example, for an 8×8 2D DBM about 25% reduction in total wire length is obtained and this can be increased to a 50% reduction for a 16×16 2D DBM.

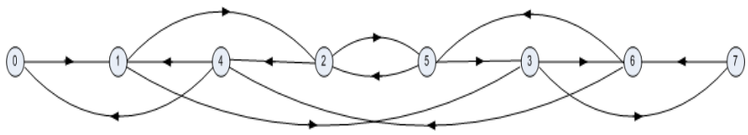


Fig. 4. A better node placement of de Bruijn network of 8 nodes

As mentioned before, we have also revised the routing algorithm in (Park & Agrawal, 1995) to have balanced use of virtual channels. Fig. 5 compares the performance of original routing algorithm and the new routing algorithm in the 8×8 2D DBM using 2 virtual channels with messages of 32 flits. As can be seen in the figure, the new algorithm exhibits better performance in terms of average message latency.

Figures 6-9 compare power consumption and the performance of simple 2D mesh and 2D DBM NoCs under various traffic patterns, network sizes and message lengths. In Fig. 6 and Fig. 7, the average message latency is displayed as a function of message generation rate at each node for the 8×8 and 16×16 networks under deterministic routing. As can be seen in the figures, the 2D DBM NoC achieves a reduction in message latency with respect to the popular 2D mesh network for the full range of network load under various traffic patterns (especially in uniform traffic). Note that for matrix-transpose traffic load, it is assumed that 30% of messages generated at a node are of matrix-transpose type (i.e. node (x,y) sends the message to

node (y,x)) and the rest of 70% messages are sent to other nodes uniformly. For hotspot traffic load a hotspot rate of 16% is assumed (i.e. each node sends 16% of its messages to the hotspot node (node (4,4) in 8×8 network and node (8,8) for 16×16 network) and the rest of 84% of messages are sent to other nodes uniformly). Note that increasing the network size causes earlier saturation in a simple 2D mesh.

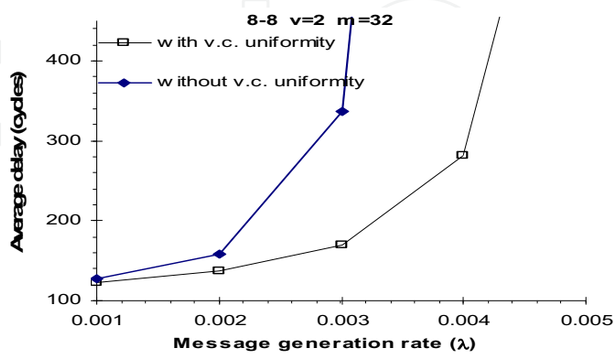
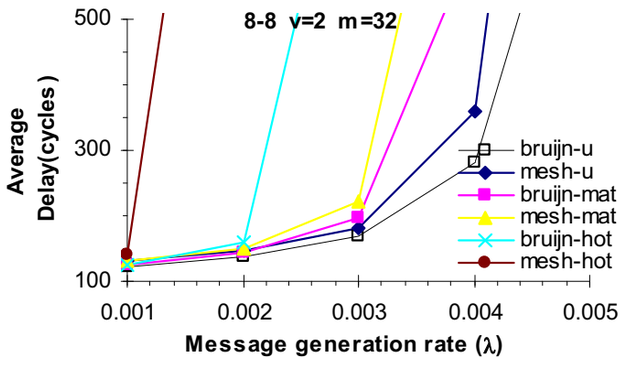
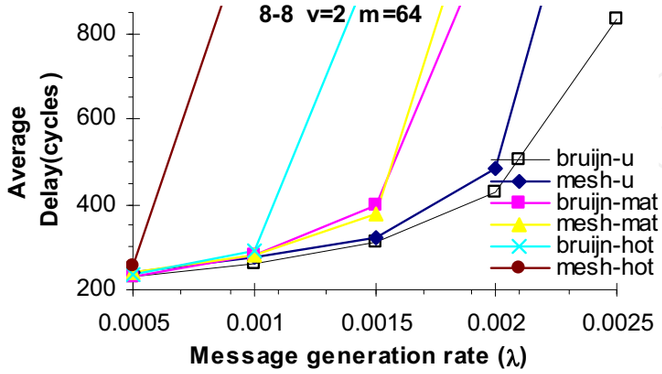


Fig. 5. The effect of balanced use of virtual channels

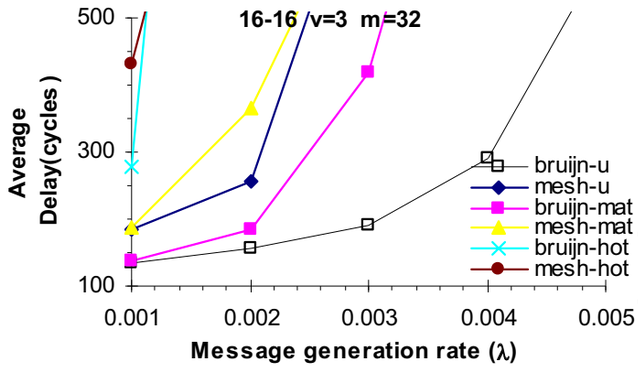


a)



b)

Fig. 6. The average message latency in the 8×8 simple 2D mesh and 2D DBM for different traffics patterns with message size of (a) 32 flits and (b) 64 flits



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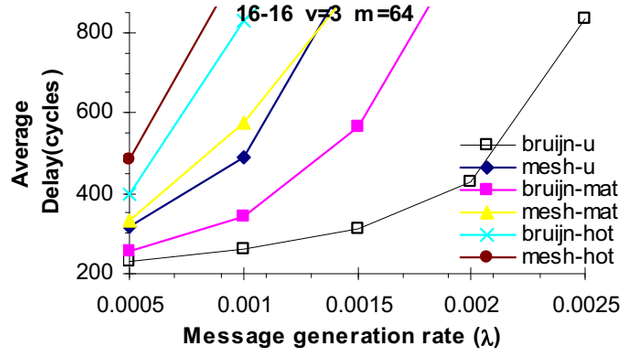
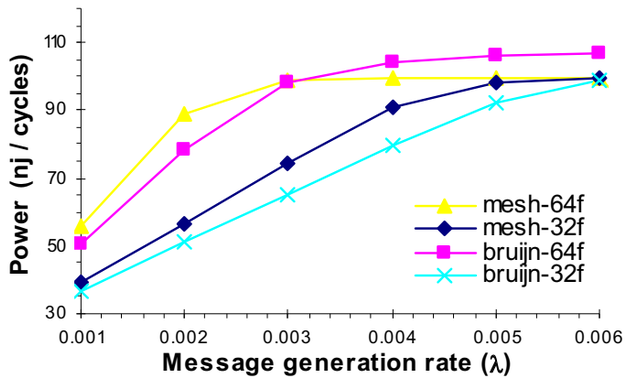


b)

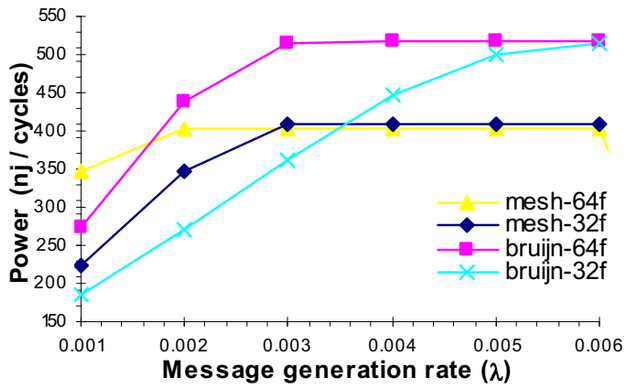
Fig. 7. The average message latency in the 16×16 simple 2D mesh and 16×16 network of 2D DBM for different traffics patterns with message size of (a) 32 flits and (b) 64 flits

According to the simulation results reported above, the 2D DBM has a better performance compared to the equivalent simple 2D mesh NoC. The reason is that the average distance a message travels in the network in a 2D DBM network is lower than that of a simple 2D mesh. The node degree of the 2D DBM and simple 2D mesh networks (hence the structure and area of the routers) are the same. However, unlike the simple 2D mesh topology, the 2D DBM links do not always connect the adjacent nodes and therefore, some links may be longer than the links in an equivalent mesh. This can lead to an increase in the network area and also create problems in link placement. The latter can be alleviated by using efficient VLSI layouts (Samanathan & Pradhan, 1989; Chen et al., 1993) proposed for de Bruijn networks, as we used.

Fig. 8 demonstrates power consumption of the simple 2D mesh and 2D DBM under deterministic routing scheme with uniform traffic. It is again the 2D DBM that shows a better behavior before reaching to the saturation point. Fig. 9 reports similar results for hotspot and matrix-transpose traffic patterns in the two networks.

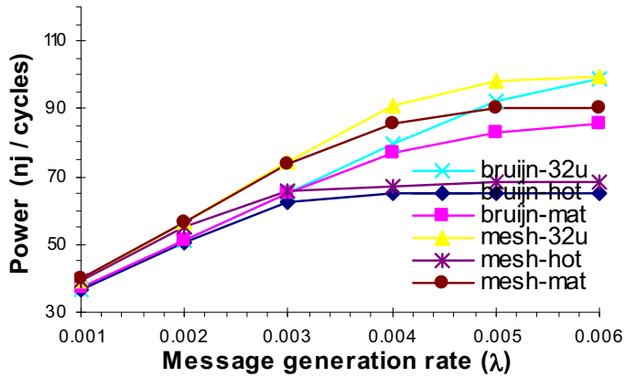


a)

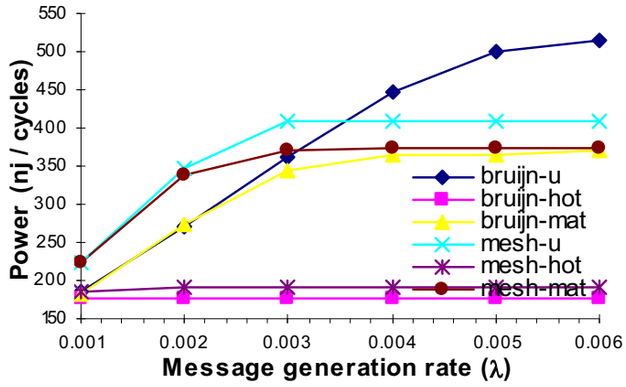


b)

Fig. 8. Power consumption of the simple 2D mesh and 2D DBM with uniform traffic pattern and message size of 32 and 64 flits for (a) 8×8 network and (b) 16×16 network



a)



b)

Fig. 9. Power consumption of simple 2D mesh and 2D DBM for different traffic patterns and message size 32 flits for (a) 8×8 and (b) 16×16 networks

The results indicate that the power of 2D DBM network is less for light to medium traffic loads. The main source of this reduction is the long wires which bypass some nodes and hence, save the power which is consumed in intermediate routers in an equivalent mesh topology.

Although for low traffic loads the 2D DBM network provides a better power consumption compared to the simple 2D mesh network, it begins to behave differently near heavy traffic regions.

It is notable that a usual advice on using any networked system is *not to take the network working near saturation region* (Duato et al., 2005). Having considered this and also the fact that most of the networks rarely enter such traffic regions, we can conclude that the 2D DBM network can outperform its equivalent mesh network when power consumption is considered.

The area estimation is done based on the hybrid synthesis-analytical area models presented in (Mullins et al. , 2006; Kim et al., 2006; Kim et al. 2008). In these papers, the area of the router building blocks is calculated in 90nm standard cell ASIC technology and then analytically combined to estimate the router total area. Table 1 outlines the parameters. The analytical area models for NoC and its components are displayed in Table 2. The area of a router is estimated based on the area of the input buffers, network interface queues, and crossbar switch, since the router area is dominated by these components.

The area overhead due to the additional inter-router wires is analyzed by calculating the number of channels in a mesh-based NoC. An $n \times n$ mesh has $2 \times n \times (n-1)$ channels. The 2D DBM has the same number of channels as mesh but with longer wires. In the analysis, the lengths of packetization and depacketization queues are considered as large as 64 flits.

In Table 3, the area overhead of 2D DBM NoC is calculated for 8×8 and 16×16 network sizes in a 32-bit wide system. The results show that, in an 8×8 mesh, the total area of the 2mm links and the routers are 0.0633 mm^2 and 0.1089 mm^2, respectively. Based on these area estimations, the area of the network part of the 2D DBM network shows a 44% increase compared to a simple 2D mesh with equal size. Considering 2mm×2mm processing elements, the increase in the entire chip area is less than 3.5%. Obviously, by increasing the

buffer sizes, the network node/configuration switch area increases, leading to much reduction in the area overhead of the proposed architecture.

Parameter	**Symbol**
Flit Size	F
Buffer Depth	B
No. of Virtual channels	V
Buffer area (0.00002 *mm²/bit* (Kim et al., 2008))	B_{area}
Wire pitch (0.00024 *mm* (ITRS, 2007)	W_{pitch}
No. of Ports	P
Network Size	N (= n×n)
Packetization queue capacity	PQ
Depacketization queue capacity	DQ
Channel Area (0.00099 mm²/bit/mm (Mullins et al. , 2006)	W_{area}
Channel Length (2mm)	L
No. Of Channels	$N_{channel}$

Table 1. Parameters

	Symbol	**Model**
Crossbar	RCX_{area}	$W^2_{pitch}\times P\times P\times F^2$
Buffer (per port)	RBF_{area}	$B_{area}\times F\times V\times B$
Router	R_{area}	$RCX_{area}+P\times RBF_{area}$
Network Adaptor	NA_{area}	$PQ\times B_{area} + DQ \times B_{area}$
Channel	CH_{area}	$F\times W_{area}\times L\times N_{channel}$
NoC Area	NoC_{area}	$n^2\times (R_{area}+ NA_{area})+ CH_{area}$

Table 2. Area analytical model

Network	Link Area	Router Area	Increase percent to mesh	increase percent in the entire chip
8×8 mesh	.06338	.1089	0	0
8×8 2D DBM	.1086	.1089	44.38	3.46
16×16 mesh	.06338	.1217	0	0
16×16 2D DBM	.1626	.1217	103.58	9.57

Table 3. 2D DBM area overhead

4. Conclusion

The simple 2D mesh topology has been widely used in a variety of applications especially for NoC design due to its simplicity and efficiency. However, the de Bruijn network has not been studied yet as the underlying topology for 2D tiled NoCs. In this chapter, we introduced the two-dimensional de Bruijn Mesh (2D DBM) network which has the same cost as the popular mesh, but has a logarithmic diameter. We then conducted a comparative simulation study to assess the network latency and power consumption of the two

networks. Results showed that the 2D DBM topology improves on the network latency especially for heavy traffic loads. The power consumption in the 2D DBM network was also less than that of the equivalent simple 2D mesh NoC.
Finding a VLSI layout for the 2D and 3D DBM networks based on the design considerations in deep sub-micron technology, especially in three dimensional design, can be a challenging future research in this line.

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The process of Integrated Circuits (IC) started its era of VLSI (Very Large Scale Integration) in 1970's when thousands of transistors were integrated into one single chip. Nowadays we are able to integrate more than a billion transistors on a single chip. However, the term "VLSI" is still being used, though there was some effort to coin a new term ULSI (Ultra-Large Scale Integration) for fine distinctions many years ago. VLSI technology has brought tremendous benefits to our everyday life since its occurrence. VLSI circuits are used everywhere, real applications include microprocessors in a personal computer or workstation, chips in a graphic card, digital camera or camcorder, chips in a cell phone or a portable computing device, and embedded processors in an automobile, et al. VLSI covers many phases of design and fabrication of integrated circuits. For a commercial chip design, it involves system definition, VLSI architecture design and optimization, RTL (register transfer language) coding, (pre- and post-synthesis) simulation and verification, synthesis, place and route, timing analyses and timing closure, and multi-step semiconductor device fabrication including wafer processing, die preparation, IC packaging and testing, et al. As the process technology scales down, hundreds or even thousands of millions of transistors are integrated into one single chip. Hence, more and more complicated systems can be integrated into a single chip, the so-called System-on-chip (SoC), which brings to VLSI engineers ever increasingly challenges to master techniques in various phases of VLSI design. For modern SoC design, practical applications are usually speed hungry. For instance, Ethernet standard has evolved from 10Mbps to 10Gbps. Now the specification for 100Mbps Ethernet is on the way. On the other hand, with the popularity of wireless and portable computing devices, low power consumption has become extremely critical. To meet these contradicting requirements, VLSI designers have to perform optimizations at all levels of design. This book is intended to cover a wide range of VLSI design topics. The book can be roughly partitioned into four parts. Part I is mainly focused on algorithmic level and architectural level VLSI design and optimization for image and video signal processing systems. Part II addresses VLSI design optimizations for cryptography and error correction coding. Part III discusses general SoC design techniques as well as other application-specific VLSI design optimizations. The last part will cover generic nano-scale circuit-level design techniques.

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