28

Pseudo Floating-Gate and Reverse Signal Flow

Omid Mirmotahari and Yngvar Berg
Dept. of Informatics, University of Oslo
Norway

This chapter presents a pseudo floating-gate (PFG) inverter. The PFG inverter is made bi-directional by simply controlling the reference voltages of the inverter. Moreover, the bi-directionality of the gate is further evolved to be able to control the signal flow direction. Different circuits implementing the bi-directionality of the PFG gates are presented and finally a reversible converter is demonstrated.

1. Floating-Gate

Floating-gate technology had its beginning in the late sixties, and is now becoming a mature technology. Kahng and Sze first proposed the concept of a floating-gate device in 1967 [1]. The first commercially available floating-gate based memory, the floating-gate avalanche-injection MOS device (FAMOS) was developed in 1970 [2]. Since then floating-gate transistors have been used extensively as non-volatile memory elements [3]. The number and variety of nonvolatile memory circuits, such as EPROMs, EEPROMs and Flash have been steadily growing. As well as being memory elements, floating-gate transistors can also be used as computational elements [4]. Although the majority of the research reported in the field of floating-gate pertains to the non-volatile types, it is not necessarily given that a volatile floating-gate is not useful.

1.1 Non-volatile Floating-Gate

A floating-gate transistor is simply a normal MOS transistor, except that the gate terminal is electrically isolated and has no DC path to a fix potential: hence, the name floating. The gate is completely surrounded by SiO2, a high quality insulator, which provides and creates a potential barrier that prevents charge stored on the floating-gate from leaking. Furthermore, when extracting the design, the usual parasitic capacitances of traditional MOSFET arise. The parasitic capacitances would affect the gate in terms of response time, i.e. delay and transconductance, and gain.

1.2 Volatile Floating-Gate

Non-volatile floating-gate transistors inherently have good charge retention capabilities. However, in most cases, using a standard CMOS process, a small leakage often exists [5]. For modern processes, like nanoscale, this leakage is crucial and for a 0.35 μm m process

with an oxide thickness less than 70Å, reprogramming may be necessary [6]. As their programming and initializing makes slight use of some complex techniques, involving high voltages or additional postprocessing, there can be structures involving direct coupling to the floating-gate. Thus, the actual gate would no longer be truly floating, and gives rise to the name volatile floating-gate. Some may argue that these structures should not even be called floating-gate. The discussion seems to have given birth to several alternative namings, e.g. semi-floating-gate (SFG) [7,8], pseudo-floating-gate (PFG) [9,10], quasi-floating-gate (QFG) [11,12]. My opinion on the usage of such names is that, in the case of semi-floating-gate, the floating-gates are being recharged and then left floating: much of the same behaviour as non-volatile floating-gates can be expected during evaluation. On the other hand, pseudo-floating-gate and quasi-floating-gate are constantly being recharged, either by a forced leakage, or by a constant feedback.
The frequent recharging can be done in different ways and the joint function is to set the floating-gate to a known value. One established design is the switch-capacitor (switch-cap or SC) design. In switch-cap designs, the input gate of an operational amplifier is capacitively coupled. Switch-cap designs usually recharge their floating-gates to Gnd [13]. Given the similarity of capac-itively coupled inputs and the recharging, we would classify switch-cap design as semi- floating-gates. Frequent recharging may require additional elements, thus adding some unwanted side effects, such as leakage. Nevertheless, it has been shown that the recharging mechanism can be used cleverly and actually includes properties and functionality [7,8,14-17].

1.3 Multiple-Valued Logic

The essence is to exploit the floating-gates' computational property to implement multiple-values of logic or functions. The multiple-valued logic is based on signal processing that is carried out using multiples of logic levels and thresholds, in contrast to binary logic with its two states, i.e. "0" and "1" [18]. Consequently, multiple-valued logic circuits are a promising approach to reduce signal lines on the chip [19,20], effectively due to the increase of information per line. The theoretical study of multiple-valued logic has a long history. Moreover, the annual International Symposium on Multiple-Valued Logic (ISMVL) meets for the 39th time this year. The hardware realization of multiple-valued logic circuits for practical use is making progress. Most of the designs have been current-mode circuits, due to the difficulties inherent in adding up signals in the voltage-mode and the need for additional fabrication steps/masks. However, current-mode multiple-valued logic circuits consume a significant amount of power due to static currents for each logic level, which in turn would not make them good candidates to reduce heat. A step towards a solution to both the wiring and heat radiation problems may be taken by establishing the voltage-mode multiple-valued logic circuits in a conventional CMOS VLSI chip. The challenges that voltage-mode CMOS circuits within multiple-valued logic have encountered have been to construct and realize a device that can distinguish the logical levels. Furthermore, the use of the conventional production process is required to keep fabrication costs to a minimum and to enable hybridization with present binary logic systems. In fact, some voltage-mode multiple-valued logic modules have been constructed, which have the benefit that they can easily be fabricated by conventional CMOS processes. Generally, it may be difficult to compare multiple-valued design with binary, but some have claimed multiple-valued designs that consume less area and are faster [21-28].

1.3.1 Multiple-Valued Floating-Gate Inverter

A voltage-mode multiple-valued floating-gate inverter was presented in [7]. The capacitive divider function of the floating-gate is used to weight the input signals and the floating-gate potential would determine the output. For this case of multiple-valued signal processing, the inverter is made analogue. Figure 1. shows an analogue floating-gate inverter with multiple-inputs. The feedback capacitor, $\mathbf{C_f}$, can be scaled to obtain a certain gain for the inverter. Preferably, the gain should be |1| and this can be achieved by adjusting the $\mathbf{C_f/C_i}$ ratio. To toggle different logical levels, hence multiple-valued, with the use of capacitive division, the output satisfying $V_{out} = V_{dd} - \mathbf{V_{in}}$ is preferred. The multiple-valued floating-gate inverter has been measured in a 0.6 μm process, with input capacitance of 10 fF and a feedback capacitor of approximately 9 fF showed by Figure 2 and its respective gain appears in Figure 3. The linear behaviour is quite evident and, moreover, the non-linear properties of the output signal near the rails are due to the linear range of the transistors.

This design resembles a switched capacitor design: the difference is the use of an inverter instead of an operational amplifier. To our knowledge, there have been very few switched capacitor circuit designs proposed for multiple-valued logic, e.g. in [29,30]. The main reason can be related to the requirement of the extensive use of switches. Therefore, it is also reasonable to believe that the multiple-valued floating-gate inverter would be more suitable because of its simpler design topology.

1.4 Semi Floating-Gate

The multiple-valued floating-gate inverter, Figure 1., has evolved to become a recharged structure [7]. The recharging mechanism is obtained by short-

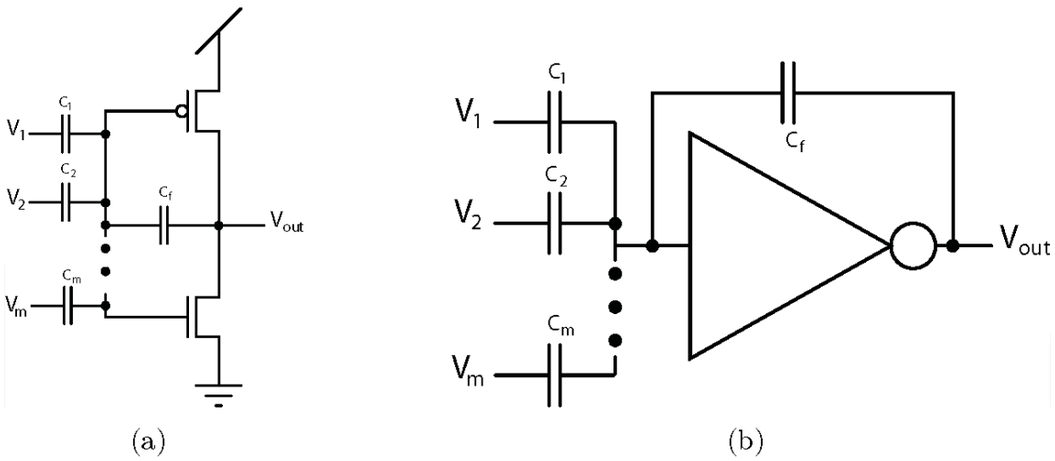

Fig. 1. A multiple-input analogue floating-gate inverter. In (a) the gate level and in (b) the symbolic level. In order to use this as a multiple-valued block the gain of the inverter must be jtj, i.e. C_f should be approximately equal to the sum of the input capacitances, C_i.

circuiting the output to the floating-gate [7,31]. Figure 2. illustrates the final result of the recharged multiple-valued semi floating-gate. Contrary to switch capacitor designs, this semi-floating-gate is recharged to $V_{dd}/2$, instead of either of the rails. The recharge level of $V_{dd}/2$ is obtained due to the equilibrium state of the inverter. During recharge the output

would stabilize at a level between the references, V_{dd} and Gnd, as a function of the matching of nMOS and pMOS. In a matched transistor pair, the equilibrium state, i.e. recharge state, would output

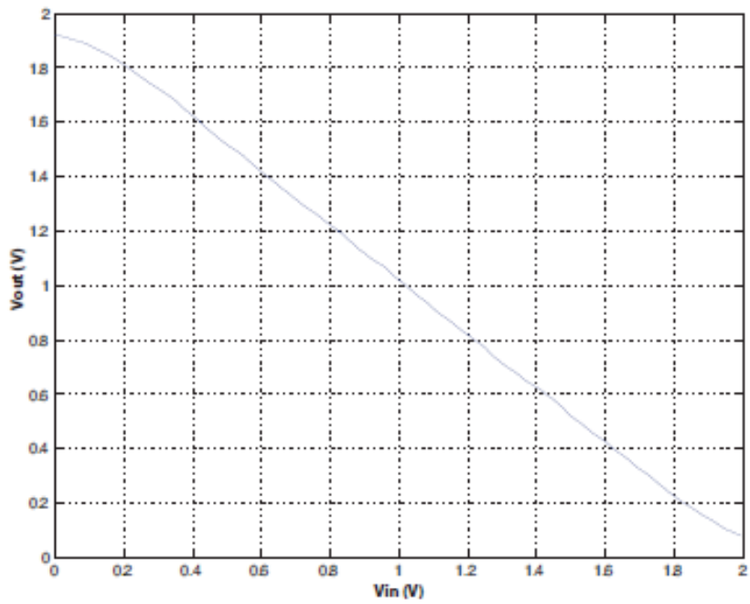

Fig. 2. Measurement of a single-input multiple-valued inverter. The capacitor values are C_i = 10 fF and ¨C$_f$ ≈ 9 fF, while the transistor sizes are 1.0/1.2 μm for nMOS and 2.5/1.2 for pMOS.

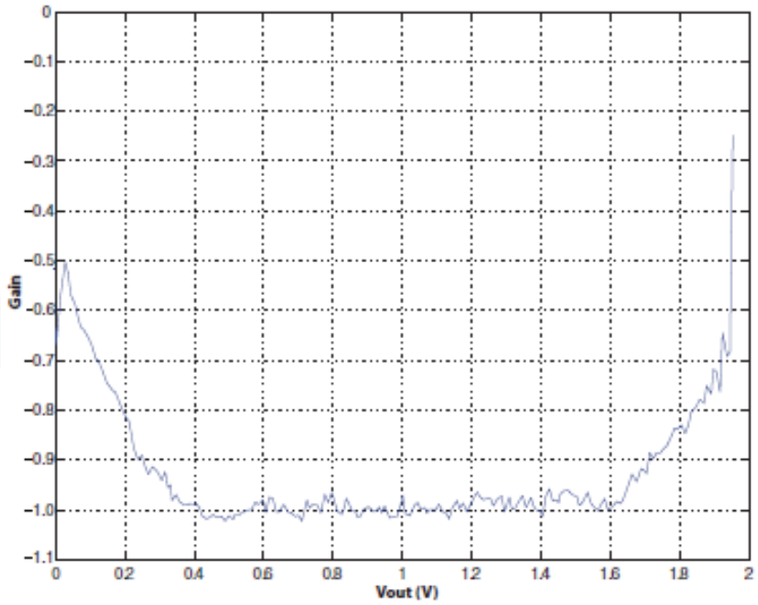

Fig. 3. The gain of a single-input multiple-valued inverter is presented. The supply voltage is 2.0V. The plot clearly shows the non-linear characteristic near the rails. Furthermore, this is a single measurement and, hence, there is some random noise obvious in this measurement.

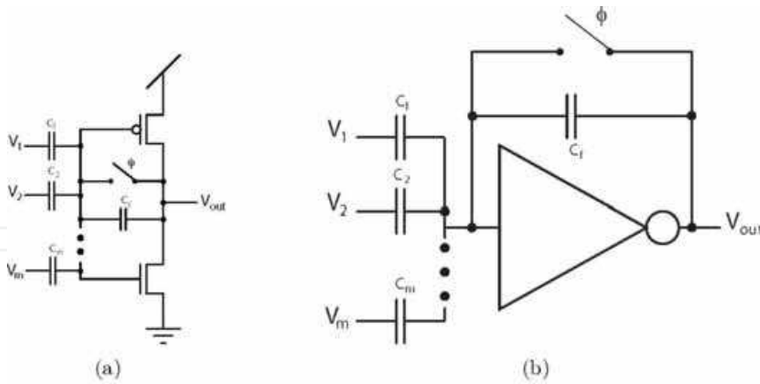

Fig. 4. A programming scheme for the floating-gate of the multiple-valued inverter. The initializing scheme is carried out by adding a switch between the output and the floating-gate. In (a) the schematic is shown and in (b) the symbol. During programming/recharging the output is short-circuited to the semi floating-gate and obtains the equilibrium state, $\mathbf{V}_{dd}/2$.

close to $V_{dd}/2$. The level of $\boldsymbol{V}_{dd}/2$ is also motivated by previous work with UV-programming [32]. In a cascaded design, all the outputs would become $V_{dd}/2$ and hence all the following inputs would be $V_{dd}/2$. One of the benefits of working with an equilibrium state for the recharge is that the voltage switching span would at worst be $V_{dd}/2$. The recharge switch can be implemented in various ways, e.g. by a single transistor or a transmission gate. The single transistor must be strong enough to short-circuit the semi-floating-gate to the output. The advantages the single transistor has over the transmission gate include a smaller area, while the transmission gate has better mobility; in addition, the layout can be designed more symmetrically than the single transistor solution. Furthermore, a transmission gate would require a two-phase clocking strategy and hence increase the power consumption. Although these structures may suffer from charge-injections in the same manner as sample and hold circuits [33,34] and switched capacitor circuits [35], different strategies can be selected. More effort can be put into asserting dummy switches and timing properties of the recharge signal in order to obtain a balanced charge distribution [36]. A measurement in a 0.6 μm process for a multiple-valued inverter, more precisely a radix-8 semi floating-gate inverter, is shown in Figure 5.

2. Pseudo Floating-Gate

Changing the way of recharging the floating-gate results in another solution for the recharging mechanism. A proposed structure is found in [37]. Although this pseudo-floating-gate, Figure 6., was first introduced for a frequency detecting application that suppresses low frequencies, the design is of interest due to the power of liberating the semi-floating-gates from the recharge clocking overhead. The pseudo floating-gate resembles greatly to the previous semi floating-gates and thus many of the same applications as for semi floating-gates apply to this new gate. Nevertheless, some of the electrical behaviours have changed. The main difference is the use of a feedback "buffer" instead of a recharge switch and thus eliminating the recharge clocks and periods. The feedback "buffer" can be

implemented, among others, as a voltage follower. Although this may not be the ideal feedback in terms of linearity, it adds simplicity and symmetry as far as synthesis and layout are concerned. One of the first noticeable characteristics (after some test simulations) was the increased operating frequency in contrast to the semi floating-gates. The frequency characteristic resembles a band pass filter, as demonstrated in Figure 7.. Moreover, it was found that the high cut-off frequency is determined by the inverter's response limit, while the low cut-off frequency is dependent on the response for the feedback "buffer" [37], as shown in Figure 9. The gain of the band pass filter can be made higher by increasing the input capacitances, thus transferring more of the input signal. Our hand calculations indicated a band pass of a maximum of three decades. Given enough time and assuming ideal conditions, the pseudo floating-gate would settle at an equilibrium state $V_{dd}/2$ (DC-point). Moreover, the design has been treated such that it operates at low-voltages, in fact as low

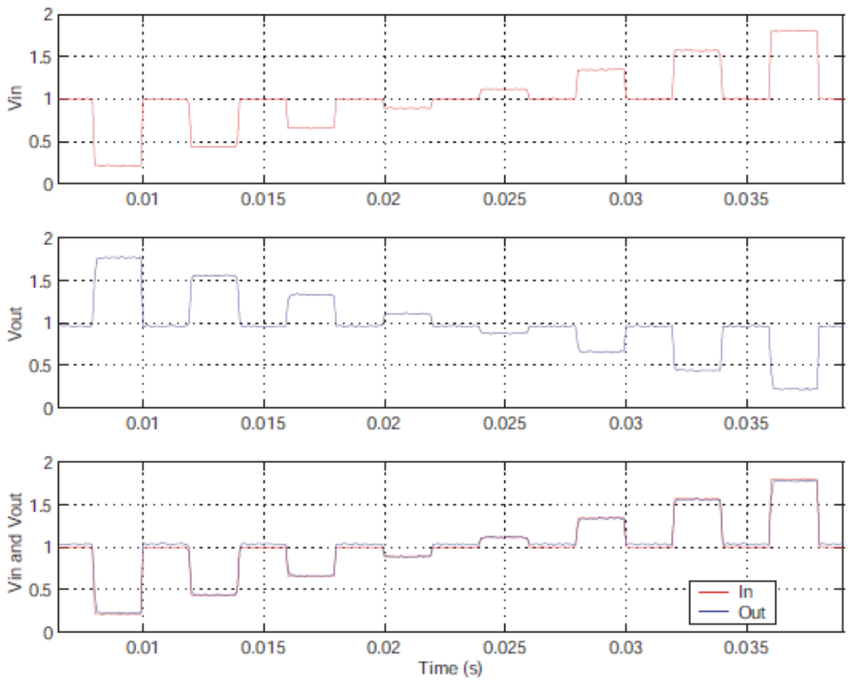

Fig. 5. The multiple-valued recharge inverter is measured with a radix-8 input-signal at a 2.0V supply voltage. In the lowest plot the output is inverted and plotted with the input. The capacitance values are C_i = 10 fF and $C_f \approx$ 9 fF, while the recharge transistor sizes are 0.8/0.6 μm for nMOS and 0.8/0.6 μm for pMOS.

as $2V_{th}$. The pseudo floating-gate used to implement multiple-valued logic was first demonstrated in [38]. The main goals were to release the traditional semi floating-gate designs from the recharge mode and thus emphasize the design's ability to operate in continuous mode. Nevertheless, the pseudo floating-gates can compute multiple-valued signals and they have actually been demonstrated to obtain higher frequencies than their prior semi floating-gates [38]. In Sim-Res 1.2.4, the multiple-valued voltage level transitions are shown. These results demonstrate the speed and functionality of the pseudo floating-gate and, moreover, their ability to operate on either binary, analogue or multiple-valued

logic and also their operational mode of either recharge or continuous mode. Although the pseudo floating-gate has been shown to relieve the clocking overhead, a clever functionality by reintroducing some of the aspects of clocking is presented in the following [38]. Mainly, it is related to the idea of reversing the reference voltages while programming UV- floating-gates. Moreover, we will also present a method of operating the pseudo floating-gate which results in bi-directional property (reversibility).

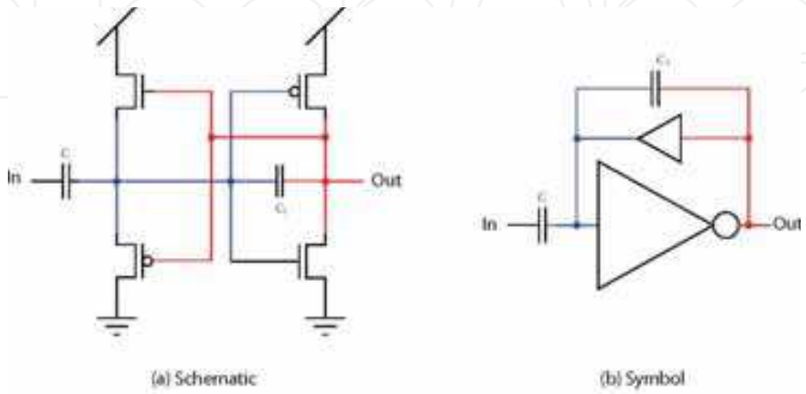

Fig. 6. The single input analog or multiple-valued pseudo floating-gate inverter are shown. Both the schematic (a) and the symbol (b) is shown. By removing the feedback capacitor, C_f, a binary pseudo floating-gate inverter is obtained. The transistors are matched and are kept equal for both the inverter and the weak feedback "buffer".

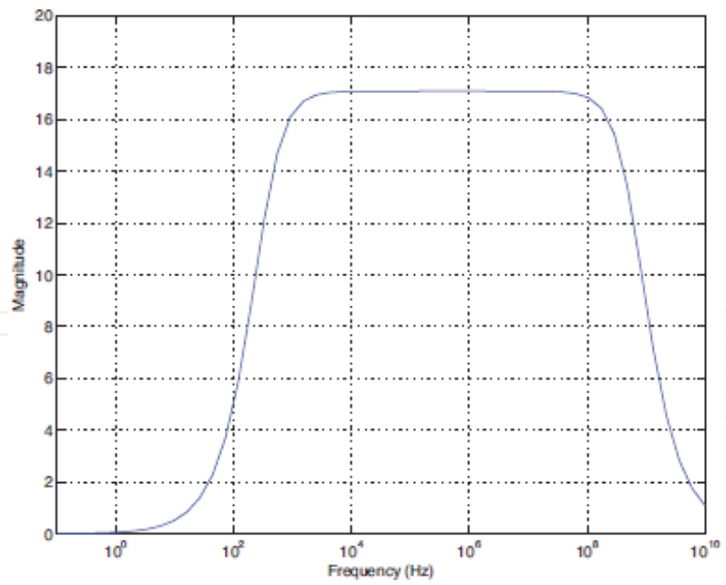

Fig. 7. The plot shows the operating frequency for the pseudo floating-gate inverter. It shows a high cut-off frequency at approximately 100 MHz for a V_{dd} = 2V. The adjustment parameters for the magnitude is the input capacitance, C_i. The low cut-off frequency is a direct result of the weak feedback "buffer", while the high cut-off is the frequency response for the inverter given its dimensions.

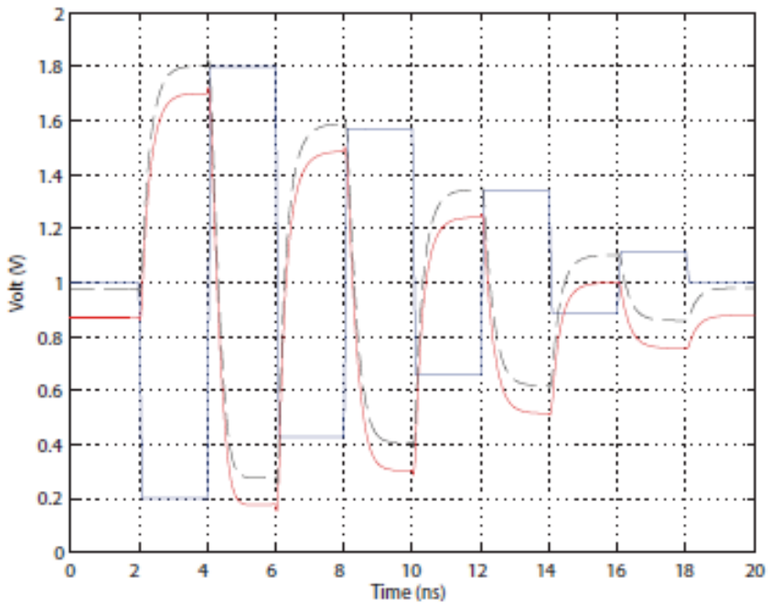

Fig. 8. Simulation result for a single-input pseudo floating-gate with the worst case level transitions in continuous mode. The blue line represents the input, the red line the actual output, while the black dotted line represents the output with adjusted equilibrium level (DC). The simulation shows a frequency of 500 MHz and there is still room to increase the frequency.

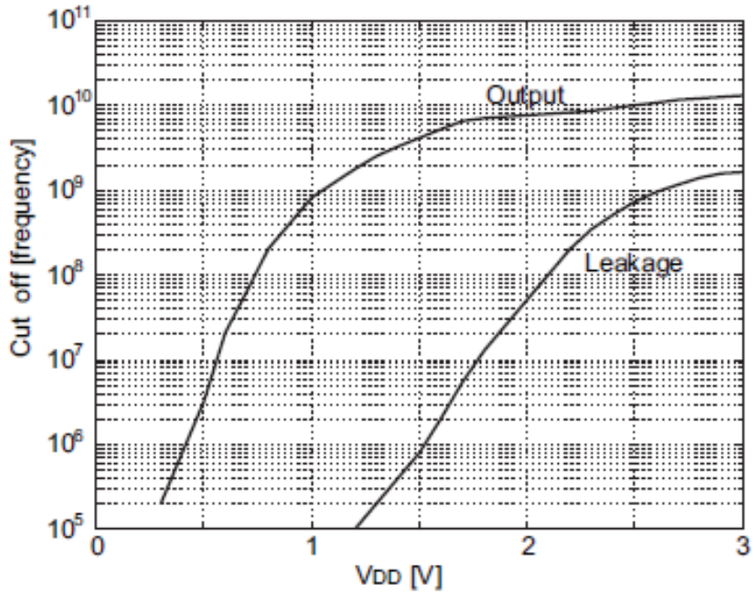

Fig. 9. The plot show the operating frequency for the pseudo floating-gate inverter. The curve labeled Output is the inverters cut-off frequency, while the curve labeled Leakage is the weak feedback "buffers" cut-off frequency. It shows cut-off frequency for different supply-voltages

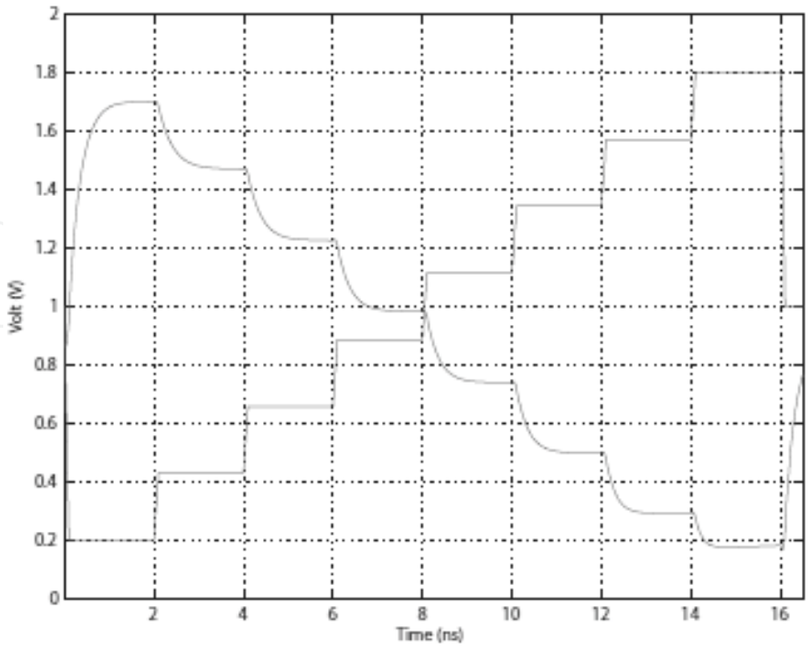

Fig. 10. The simulation result for a single input pseudo floating-gate inverter in the context ofmultiple-valued logic. The output steps are a little smaller compared with the input, but are justifiable within the noise margin.

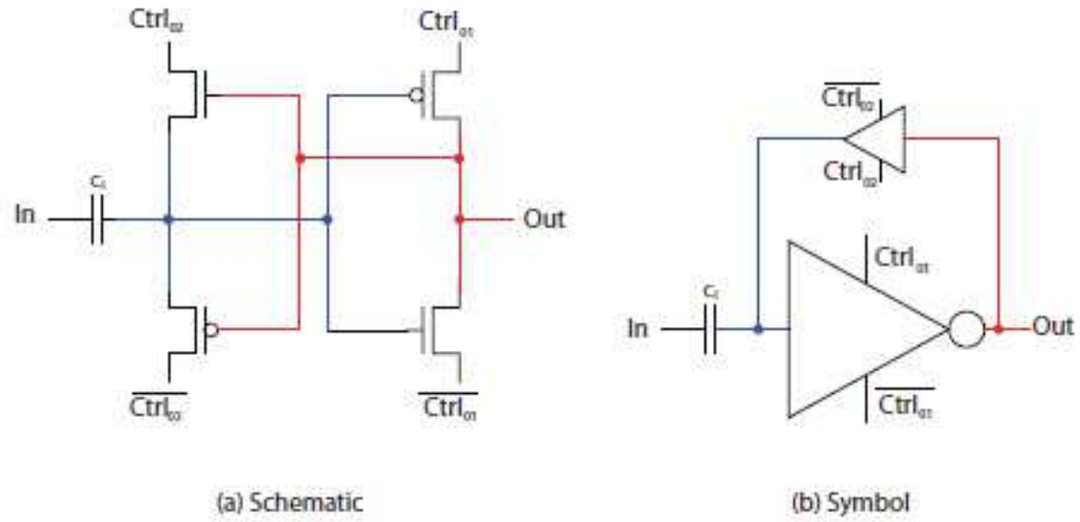

Fig. 11. The single-input binary pseudo floating-gate inverter is shown: the schematic (a) and the symbol (b). The inverter operat es on control signal $Ctrl_{01}$ with the signal processing capabilities from left to right. When $Ctrl_{01}$ is high, the feedback operates on $Ctrl_{02}$ and hence the weak feedback "buffer". The transistors are matched and are kept equal for both the inverter and the "buffer".

Most of the proposed bi-directional designs are current mode and, to my knowledge, there are only a few voltage mode designs. In order to obtain a bidirectional property, the design must obviously be symmetrical in order to obtain the same condition for both directions. The pseudo floating-gate consists of an inverter and a weak feedback "buffer". One of the first solutions to the symmetrical approach is to use a voltage follower as the weak feedback "buffer". This would fulfil the symmetrical property owing to the fact that the voltage follower can be constructed by an inverter. The only difference is to invert the references, i.e. swap the V_{dd} and Gnd. With the pseudo floating-gate, we can obtain a bi-directional gate by introducing a control signal. The key idea is to have the gates reference provided by control signals. As Figure 11 illustrates, we have included two sets of control signals**,** $\mathbf{Ctrl_{01}}$ and $\mathbf{Ctrl_{02}}$. Figure 11 shows a pure binary gate and does not contain the feedback capacitor. With the ability to control the reference signals separately, we can alter the signal direction through the gate. Figure 12 serves as an illustration and truth table for the four possible combinations when applying the two control signals. The table clearly demonstrates that, by changing the reference voltage, we can choose which of the two inverters in the pseudo floating-gate becomes an inverter or a feedback "buffer". Furthermore, we see that, by including control signals in the pseudo floating-gate, we obtain more than just bi-directionality. The pseudo floating-gate is now able to process four different functions or states: (1) *stop/shunt,* (2) *signal direction (right-to-left),* (3) *signal direction (left-to-right)* and (4) *memory.* If the main goal is to have only bi-directional gates, one control signal strategy is sufficient. The pseudo floating-gate would, therefore, only have one external signal to control the signal direction. In order to describe the switching of the signal direction and to be able to test only one pseudo floating-gate, a proposed test-bench is shown in Figure 13. The control signal $\mathbf{Ctrl_{01}}$ controls both the reference voltage of the pseudo floating-gate and the pass transistor. The signal direction from left to right uses *In Left* and *Out Right* and, therefore, the pass transistors 2 and 4 are closed. When altering the signal direction with the other control signal, $\mathbf{Ctrl_{02}}$**,** the pass-transistors 2 and 4 open, while 1 and 3 close, hence the signal direction becomes right to left (In *Right* and *Out Left).* Figure 14 serves as verification that the bi-directional pseudo floating-gate works for a single control signal design. Note that the capacitor at the *In Right* is actually the input capacitor of the following gate. Simulating and verifying the bi-directionality of a single pseudo floating-gate includes some extra overheads due to the pass-transistors. When verifying larger designs, all the internal gates and signals would alter their signal direction without any overhead. The overhead of including pass-transistors becomes of interest at the high-level input

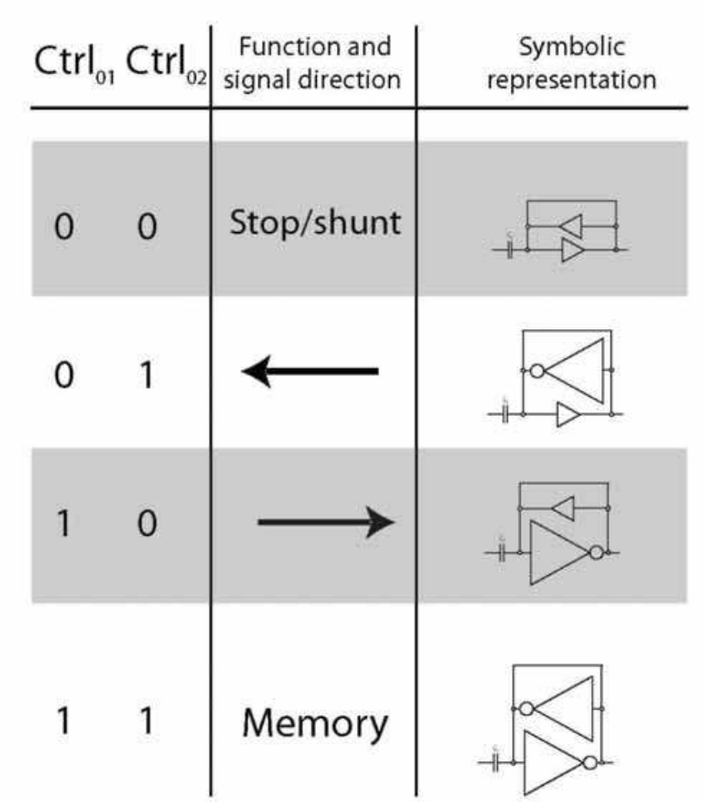

Fig. 12. The four possible combinations for the control signals for the pseudo floating-gates signal processing are listed. In the first combination, that is when both control signals are high, the pseudo floating-gate acts as a "memory element", and so on. If only bi-directional gates are wanted, only one clock can easily be used, i.e. $\mathrm{Ctrl}_{02} = \overline{Ctrl_{01}}$.

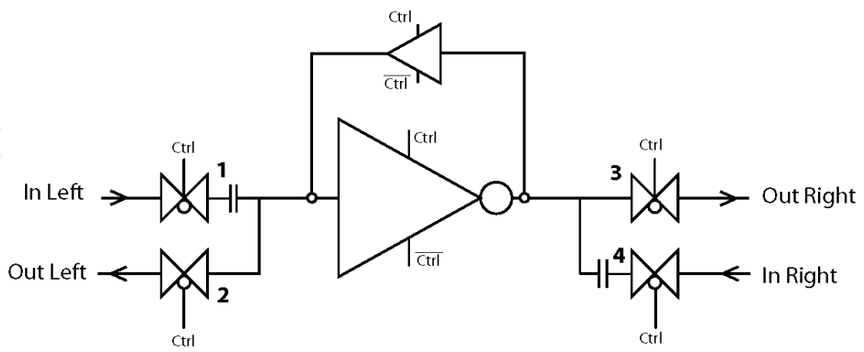

Fig. 13. The test-bench to verify a single binary pseudo floating-gate. The pass transistors on either side are only added to be able to reconstruct inputs and outputs of other gates. The pass-transistors are kept at minimum and matched. The pass transistor 1 and 3 are open, while 2 and 4 are closed, and vice versa. The signal direction from left-to-right is through pass transistor 1 and 3, while for right-to-left it is through 2 and 4. *and output pins, e.g. IC pins.*

3. The Multiplexor

The pseudo floating-gate circuits can, as refereed by Figure 12, behave in four different ways. In order to give a thorough analysis of the different states and examples of their use in applications, we first consider the state to stop/shunt a signal. A first approach to a pseudo floating-gate proposal for a 2-input binary multiplexor is presented in Figure 16 [39]. In order to make it easier to understand, we will in the following refer to the weak feedback "buffer" as "feedback". The multiplexor consists of three pseudo floating-gates and they all share the same reference signal with the inverters. The first two gates have a separate control signal at the reference of the feedback. Using only one control signal, **Ctrl,** would make the feedback either stop/shunt the signal or allow a signal to propagate from left-to-right. The concept for this particular multiplexor is to have the opposite control signal for the first two gates. The obtained functionality with this construction of a multiplexor element is that the **Ctrl** actually controls which input, either **A** or **B,** to output. In more detail, the **Ctrl** logical value given by input **A** is "0" and input **B** is "1". The last pseudo floating-gate, due to its capacitive inputs, sums the voltage change, ΔV, at the outputs of the two previous pseudo floating-gates. Note that both inputs are weighted equally. Since all the gates are binary, the output value of the multiplexor would be " 1" for $\Delta V_{tot} < V_{dd}/2$, while for $\Delta V_{tot} > V_{dd}/2$ the output is "0". A simulation environment with the following conditions is presented in Figure 16: input **A** is a binary signal with a frequency of 250 MHz: secondly, input **B** has a binary signal with a frequency of 166 MHz: and, finally, the **Ctrl** chooses input **A** whenever logically "1". The simulation results obtained in a 0.35 μm process are presented in Figure 16 and clearly illustrate that the output of the

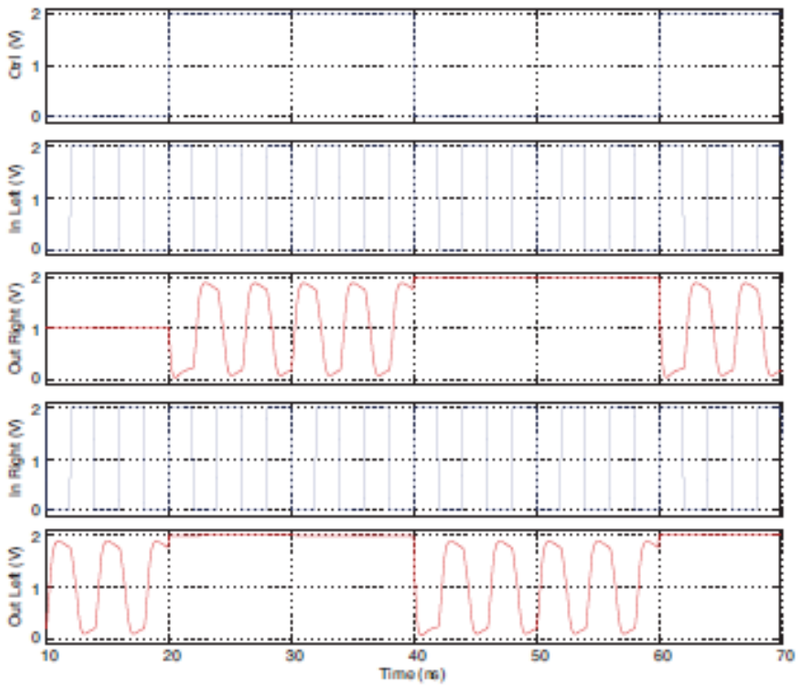

Fig. 14. The simulation results for a bi-directional pseudo floating-gate are shown. The design only uses one control signal, and hence the reference signal alternates the signal

direction of the pseudo floating-gate. The simulation results verify the bi-directional operation of the pseudo floating-gate.
multiplexor is the same frequency as the chosen input at any given time. We would like to stress that the only combination of modes the pseudo floating-gates, in this example, can have are either (1) *stop/shunt* or (3) *signal direction (left-to-right),* referring to Figure 12.
Taking the idea of using the bi-directionality of the pseudo floating-gates further and connecting it to reversible logic in the case of the multiplexor, it is possible to obtain a reverse element which is a multiplexor and reverse a signal path selector, e.g. encoder/decoder element. Regarding the previously described multiplexor, the whole element can be made bi-directional and not just the internal gates. The third and last pseudo floating-gate's feedback can also be controlled with a control signal, **$Ctrl_{02}$.** The second control signal would actually control the bi-directionality of the whole element and thus make the element reversible. The behaviour of the bi-directional 2-input binary multiplexor can therefore be regarded as:

(left-to-right): 2-input multiplexor, outputs the one input selected by the control signal **$Ctrl_{01}$**.

(right-to-left): Signal path selector, outputs the input signal on the selected output by control signal **$Ctrl_{02}$.**

In Figure 17, a proposal for a 2-input binary bi-directional pseudo floating-gate multiplexor design is illustrated [39]. Note that the capacitor on the right-hand side is actually the following gate's input capacitor, and thus is only to be considered when using a right-to-left signal direction. The pseudo floating-gate bi-directional multiplexor needs two control signals: one to alter the overall signal direction and one to choose which path/signal to output. Verification of the bi-directional multiplexor is presented in Figure 19 Even though it cannot fully be called a reversible element, it can still perform a reverse function. In the case of this multiplexor, it can be regarded as an encoder/decoder element. In the following sections, this concept of bi-directionality to implement reversible functions is developed further. Furthermore, multiple-valued logic is included to construct an element which is a converter (AD/DA).

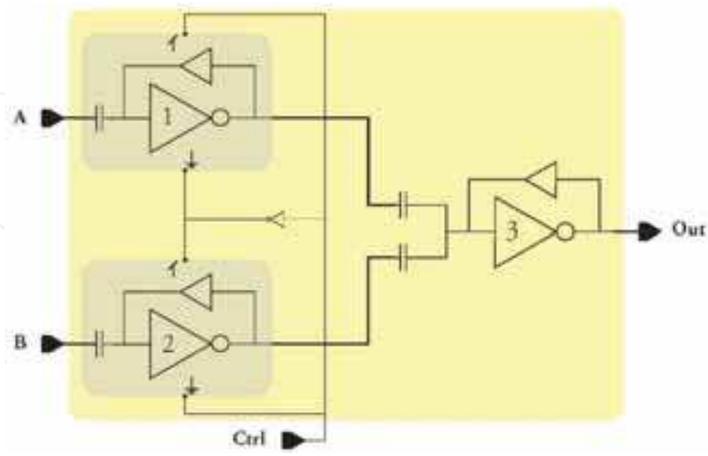

Fig. 15. A 2-input binary pseudo floating-gate multiplexor. The main proof of concept demonstrates an application where the pseudo floating-gate's bidirectional advantage make designs simpler. In this design there is no clock signal deciding the signal direction, but rather a control signal, ***Ctrl.*** The ***Ctrl*** chooses which input, ***A*** or **B**, to allow at the output, ***Out.*** The transistor sizes are the same as in previous figures.

4. Bidirectional - AD/DA

In order to have the bi-directional property, it is obvious that the design must be symmetrical in order to provide the same conditions for both directions. The pseudo floating-gate consists of an inverter and a weak feedback buffer. One of the first solutions to achieve symmetry is to use a voltage follower as the weak feedback buffer. This fulfils the symmetrical property owing to the fact that the voltage follower can be constructed as an inverter. The pseudo floating-gate ciruits are able to handle both binary as well as multiple-valued signals. In the following, a multiple-valued to binary converter will be presented that has the ability to be reversible by changing the signal's direction, i.e. an "undo" step, without losing any information [40]. First, the multiple-valued to binary converter (hereby referred to as AD) is shown in Figure 18. This converter operates on a radix of 4, i.e. the signals can have up to 4 levels, representing {0,1,2,3} . The simulation results, shown in Figure 20, prove the correct operation of the design. Using the possibility of reversing the signal direction, as described earlier, a reversible AD can be obtained, which is a DA (binary to multiple-valued) converter. This reversible function and what the "reversed" design of the one in Figure 18 would look like are shown in Figure 21. The simulation results are detailed in Figure 22. Some may point out that, the AD and the DA are not perfectly symmetrical, and that some elements have been added. The explanation is that by reversing the signal direction the output becomes the input and vice versa. Owing to the design of the pseudo floating-gate, all inputs must come from floating-gates: therefore, in the case of the DA, a capacitor was added to the input (see Figure 21, grey area). In a larger design, the capacitor would actually be represented by the next gate's input capacitor (which is included).

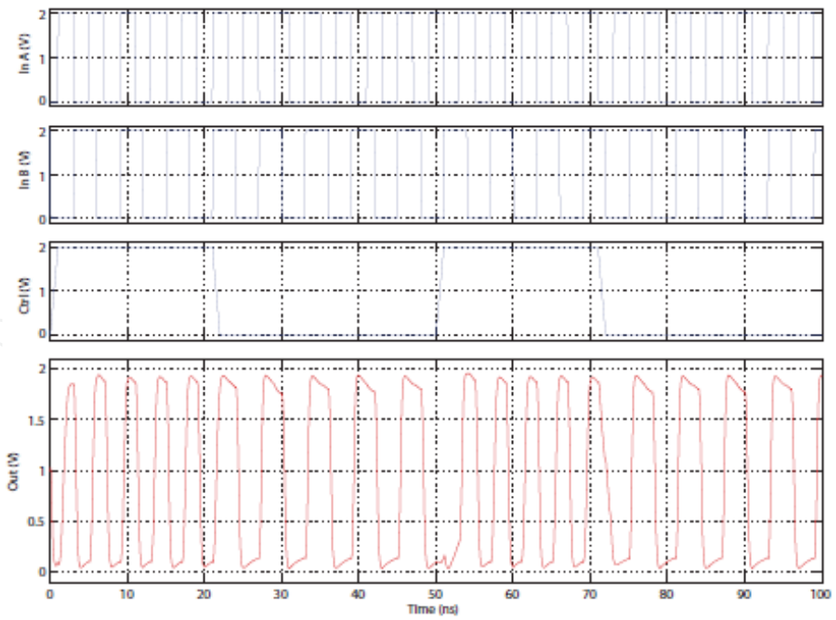

Fig. 16. The simulation results verifying the 2-input binary pseudo floating-gate multiplexor. The simulation has been conducted with different input frequencies at ***A*** and **B**. As is evident from the results that the output frequency is the same as the one at the chosen input. While ***Ctrl*** is high the input ***A*** is chosen.

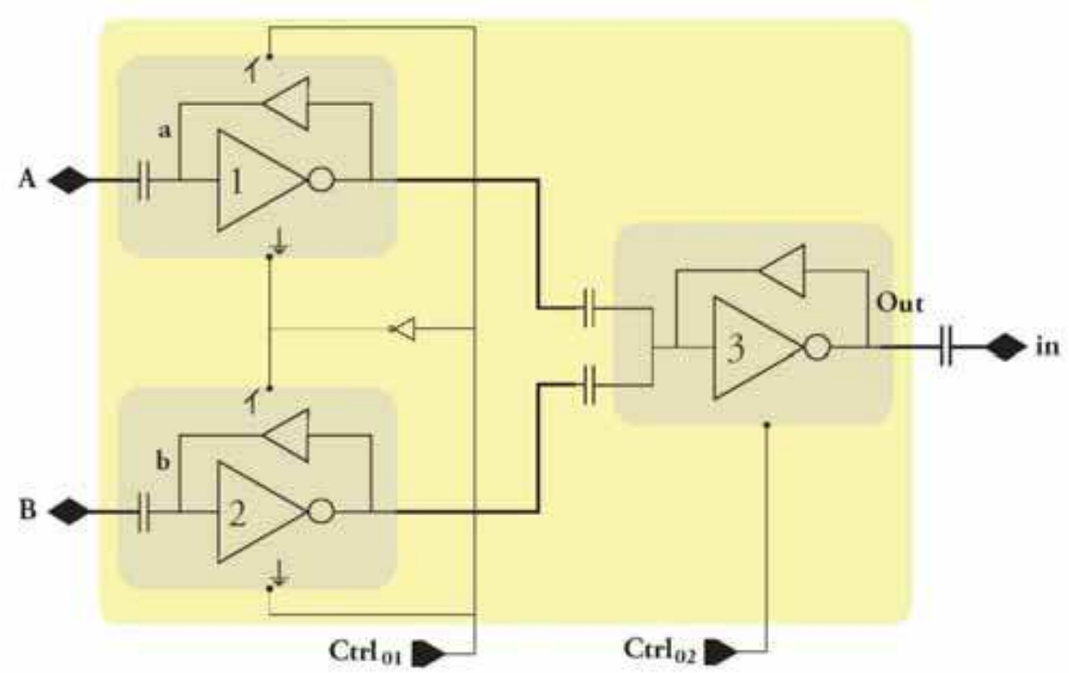

Fig. 17. The 2-input binary bi-directional pseudo floating-gate multiplexor is illustrated. In this design there are two control signals, ***Ctrl***$_{01}$ and ***Ctrl***$_{02}$, one to control the bi-directionality and one to choose the signal path, respectively. The transistor sizes are the same as in previous figures.

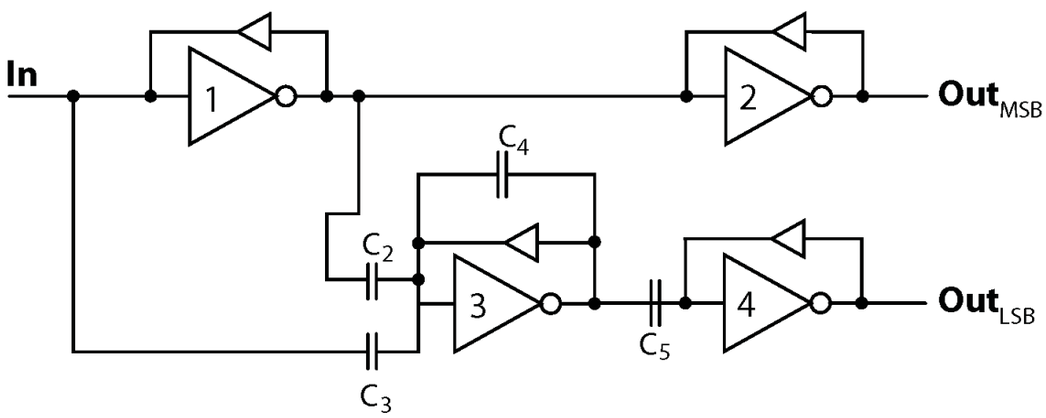

Fig. 18. A radix-4 to binary (AD) converter implemented with pseudo floating-gates. The transistor sizes are kept at a minimum and matched, while the capacitors are C_2 = 5fF, C_3 = 7fF, C_4 = 6fF and C_5 = 10fF. The control signal, ***Ctrl,*** has intentionally not been depicted for the sake of clarity. All the pseudo floating-gates have the ***Ctrl*** signal included.

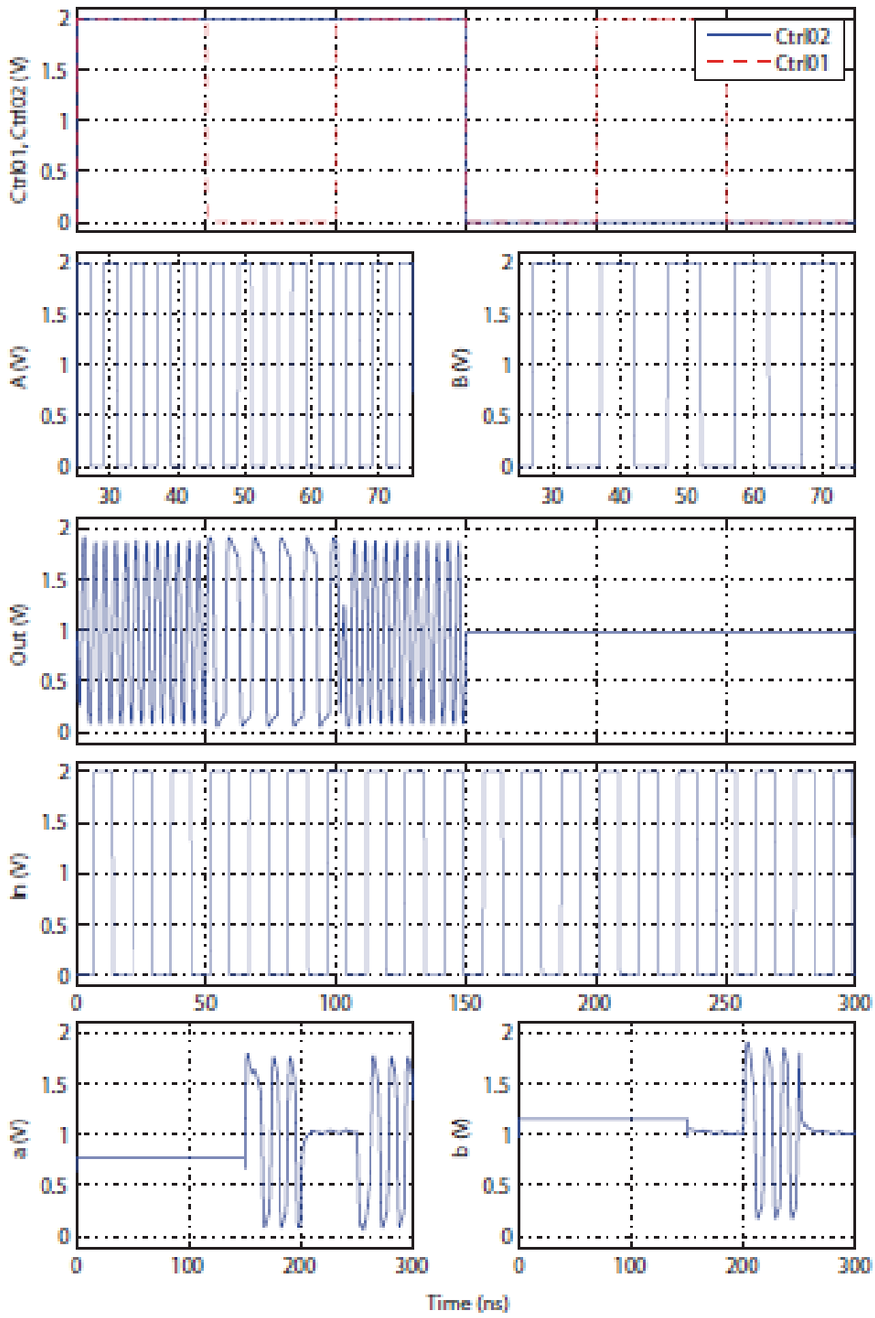

Fig. 19. Simulation results for the bi-directional 2-input binary pseudo floating-gate multiplexor. At the top the control signals are shown, where $\boldsymbol{Ctrl_{01}}$ represents the selector and $\boldsymbol{Ctrl_{02}}$ represents the bi-directionality. In the second row (for the sake ofclarity only a window ofthe signals is displayed) the input signals $\boldsymbol{A}$ and $\boldsymbol{B}$ are shown. The output of the multiplexor is shown afterwards, while at the bottom of this chart the path selector outputs are shown.

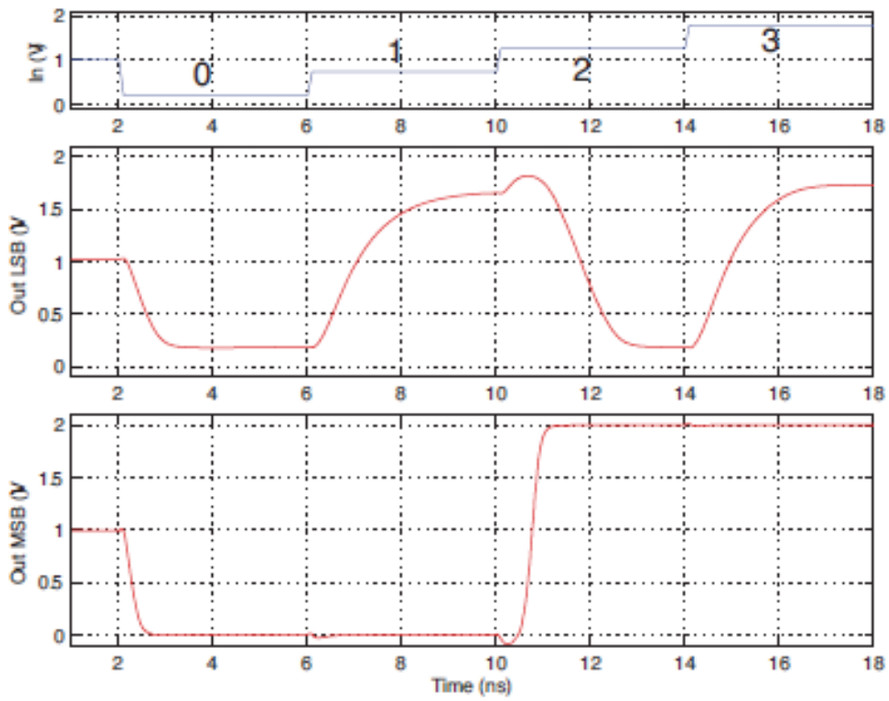

Fig. 20. The simulation results for the radix-4 to binary converter shown in Figure 18. The AD's logical behavior is evident from these results. The only transition which has some latency is the logical level 2. The solution is to increase the width of the transistor in inverter no. 2 to gain in higher frequency response.

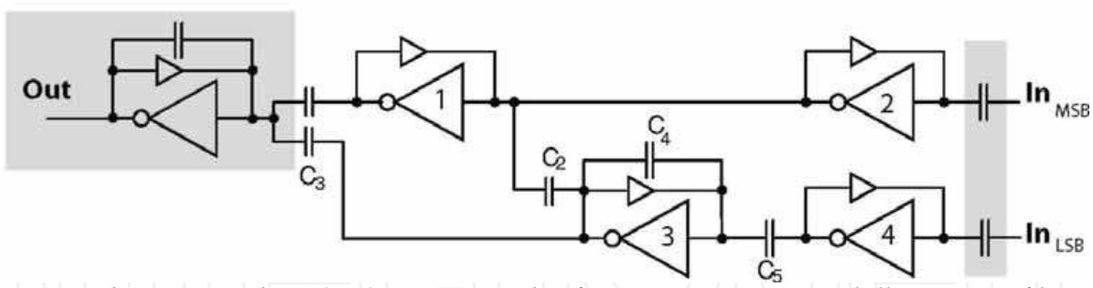

Fig. 21. A binary to radix-4 (DA) converter. This figure serves as a visual illustration of how the signal propagation through the circuit in Figure 18 appears, when the circuit is reversed. The same capacitors and pseudo floating-gates are used. In order to reverse the signal direction some elements from the previous and the next circuits are included (illustrated by a grey area).

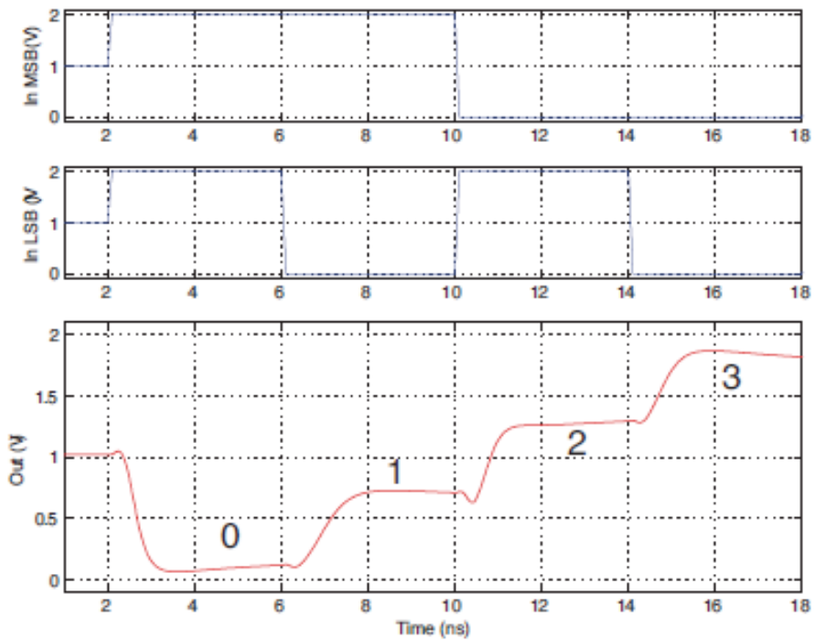

Fig. 22. The simulation results for the binary to radix-4 (DA) converter shown in Figure 21. All levels are within the noise margins. Focusing on a small detail it can be noticed that the output signal actually is inverted as one would expect. This is due to the last inverter (i.e. inverter no. 0). The actually correct output would be the floating-gate of inverter no. 0.

5. References

D. Kahng and S. M. Sze. (1999). A floating-gate and its application to memory devices. The Bell System Technical Journal, 46(4):1288-1295, 1967. IEEE standard definitions and characterization of using floating-gate semiconductor arrays, February 1999.

S. Lai. (1998). Flash memories: where we were and where we are going. In International Electron Devices Meeting, pages 971-974. IEEE, 1998.

T. Shibata and T. Ohmi. (1991). An intelligent MOS transistor featuring gate-level weighted sum and threshold operation. In International Electron Devices Meeting, Technical Digest, pages 919-922. IEEE, 1991.

W.P. Millard, Z.K. Kalayjian, and A.G. Andreou. (2000). Calibration and matching of floating gate devices. In International Symposium on Circuits and Systems (ISCAS), volume 4, pages 389-392. IEEE, May 2000.

K. Rahimi, C. Diorio, C. Hernandez, and M.D. Brockhausen. (2002). A simulation model for floating-gate MOS synapse transistor. In International Symposium on Circuits and Systems (ISCAS), volume 2, pages 532-535. IEEE, May 2002.

Y. Berg, S. Aunet, O. Mirmotahari, and M. Høvin. (2003). Novel recharged semi-floating-gate CMOS logic for multiple-valued systems. In International Symposium on Circuits and Systems (ISCAS), volume 5, pages 193-196. IEEE, May 2003.

O. Mirmotahari and Y. Berg. (2003). A novel multiple-input multiple-valued semifloating-gate latch. In International Symposium on Multiple- Valued Logic (ISMVL), pages 227-231. IEEE, May 2003.

O. Roux dit Buisson, G. Moring, F. Paillardet, and E. Mazaleyrat. (1998). A new characterization method for accurate capacitor matching measurements using pseudo-floating gate test structures in submicron CMOS and BiCMOS technologies. In International Conference on Microelectronic Test Structures (ICMTS), pages 223-227, 1998.

O. Roux dit Buisson, G. Moring, F. Paillardet, and E. Mazaleyrat. (1999). A new characterization method for accurate capacitor matching measurements using pseudo-floating gate test structures in submicron CMOS and BiCMOS technologies. IEICE Transactions on Electronics, 82(4):624-629, 1999.

J. Ramirez-Angulo, C. A. Urquidi, R. Gonzalez-Carvajal, A. Torralba, and A. Lopez-Martin. (2003). A new family of very low-voltage analog circuits based on quasi-floating-gate transistors. IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 50(3):214-220, 2003.

J. Ramirez-Angulo, A. Lopez-Martin, R. Gonzalez-Carvajal, and F. M. Chavero. (2004). Very low-voltage analog signal processing based on quasi-floating-gate transistors. IEEE Journal of Solid-State Circuits, 39(3):434-442, 2004.

D.A. Johns and K. Martin. (1997). Analog Integrated Circuit Design. John Wiley & Sons, first edition, 1997.

O. Mirmotahari, Y. Berg, Ø. Naess, and J. Bush. (2002). A novel proposal for a multiple-valued floating-gate C²MOS latch. In NORCHIP Conference, volume 1. IEEE, November 2002.

Y. Berg, S. Aunet, Ø. Naess, and O. Mirmotahari. (2004). Basic multiple-valued functions using recharge CMOS logic. In International Symposium on Multiple-Valued Logic (ISMVL), pages 346-351. IEEE, May 2004.

H. Gundersen and Y. Berg. (2004). Max and min functions using multiple-valued recharged semi-floating-gate circuits. In International Symposium on Circuits and Systems (ISCAS), volume 2, pages 857-860. IEEE, May 2004.

O. Mirmotahari and Y. Berg. (2004). A novel D-latch in multiple-valued semifloating-gate recharged logic. In International Symposium on Multiple-Valued Logic (ISMVL), pages 210-213. IEEE, May 2004.

K.C. Smith. (1988). Multiple-valued logic: a tutorial and appreciation. IEEE Computer, 21:17-27, April 1988.

W.J. Dally. (1987). A VLSI Architecture for Concurrent Data Structures. Kluwer Academic Publishers, 1987.

R.W. Keyes. (1982). The wire-limited logic chip. IEEE Journal of Solid-State Circuits, 17(6):1232-1233, December 1982.

Takahiro Hanyu, Kaname Teranihi, and Michitaka Kameyama. (1998). Multiple-valued floating-gate-MOS pass logic and its application to logic-in-memory VLSI. In International Symposium on Multiple-Valued Logic (ISMVL), pages 270-275. IEEE, May 1998.

R. Jensen and Y. Berg. (2007). Dual data-rate cyclic d/a converter using semi floating-gate devices, 2007.

I.M.Thoidis, D.Soudris, J.M. Fernandez, and A.Thanailakis. (2001). The circuit design of multiple-valued logic voltage-mode adders. In International Symposium on Circuits and Systems (ISCAS), volume 4, pages 162-165. IEEE, May 2001.

M. Inaba. (2007). Experiment result of down literal circuit and analog inverter on cmos double-polysilicon process, 2007.

R.C.G. da Silva, H. Boudinov, and L. Carro. (2006). A novel voltage-mode CMOS quaternary logic design. IEEE Transactions on Electron Devices, pages 1480-1483, June 2006.

K. Tanno M. Inaba and O. Ishizuka. (2002). Multi-valued flip-flop with neuron-CMOS NMIN circuits. In International Symposium on Multiple-Valued Logic (ISMVL), pages 282-288. IEEE, 2002.

I. Thoidis, D. Soudris, I. Karafyllidis, S. Christoforidis, and A. Thanailakis. (1998). Quaternary voltage-mode CMOS circuits for multiple-valued logic. IEEE Circuits, Devices and Systems, 145(2):71—77, April 1998.

I. Thoidis, D. Soudris, J.M. Fernandez, and A. Thanailakis. (2001). The circuit design of multiple-valued logic voltage-mode adders. In International Symposium on Circuits and Systems (ISCAS), volume 4, pages 162-165. IEEE, May 2001.

L. Liusheng, S. Bingxue, and L. Zhijian. (1996). A switched-capacitor fuzzy processor. In International Conference on Neural Information Processing, volume 2, pages 1028-1032, 1996.

T. Inoue, F. Ueno, and S. Sonobe. (1988). Switched-capacitor building blocks for fuzzy logic and neural networks. Transactions ofthe Institute ofElectronics, Information and Communication Engineering, 71(12):1259-1260, 1988.

C.C. Enz, E.A. Vittoz, and F. Krummenacher. (1987). A CMOS chopper amplifier. IEEE Journal of Solid-State Circuits, 22(3):335-342, June 1987.

Y. Berg, T. S. Lande, and Ø. Næss. (2001). Programming floating-gate circuits with UV-activated condictances. IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 48(1):12-19, January 2001.

D. Liang and R. Harjani. (1998). CMOS switched-OpAmp based sample-and-hold circuit. In International Symposium on Circuits and Systems (ISCAS), volume 1, pages 476-479. IEEE, June 1998.

C. Eichenberger and W. Guggenbuhl. (1991). Charge injection of analogue CMOS switches. IEE Proceedings G Circuits, Devices and Systems, 138(2):155-159, April 1991.

P.K. Chan and H.L. Zhan. (2001). A switched-capacitor interface circuit for integrated sensor applications. In International Symposium on Circuits and Systems (ISCAS), volume 1, pages 372-375. IEEE, May 2001.

C. Eichenberger and W. Guggenbuhl. (1990). On charge-injection in analog MOS switches and dummy switch compensation techniques. IEEE Transactions on Circuits and Systems, 37(2), February 1990.

Y. Berg, O. Mirmotahari, and S. Aunet. (2006). Pseudo floating-gate inverter with feedback control. In International Conference on Very Large Scale Integration (VLSI-SOC), volume 1, pages 272-276, October 2006.

O. Mirmotahari, J. Lomsdalen, and Y. Berg. (2007). A continuous mode MVL gate using pseudo floating-gate. In International Conference on Mixed Design ofIntegrated Circuits and Systems (MIXDES), pages 185-189, June 2007.

O. Mirmotahari and Y. Berg. (2008). Proposal for a bidirectional gate using pseudo-floating-gate. In International Symposium on Electronic Design, Test and Application (DELTA), pages 196-200. IEEE, January 2008.

O. Mirmotahari and Y. Berg. (2009). Digital ultra low voltage high speed logic. In Accepted at International MultiConference of Engineers and Computer scientists (IMECS), pages 1-1, Mars 2009.

Recent Advances in Technologies

Edited by Maurizio A Strangio

ISBN 978-953-307-017-9

Hard cover, 636 pages

Publisher InTech

Published online 01, November, 2009

Published in print edition November, 2009

The techniques of computer modelling and simulation are increasingly important in many fields of science since they allow quantitative examination and evaluation of the most complex hypothesis. Furthermore, by taking advantage of the enormous amount of computational resources available on modern computers scientists are able to suggest scenarios and results that are more significant than ever. This book brings together recent work describing novel and advanced modelling and analysis techniques applied to many different research areas.

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

Omid Mirmotahari and Yngvar Berg (2009). Pseudo Floating-Gate and Reverse Signal Flow, Recent Advances in Technologies, Maurizio A Strangio (Ed.), ISBN: 978-953-307-017-9, InTech, Available from: http://www.intechopen.com/books/recent-advances-in-technologies/pseudo-floating-gate-and-reverse-signal-flow

INTECH
open science | open minds

InTech Europe
University Campus STeP Ri
Slavka Krautzeka 83/A
51000 Rijeka, Croatia
Phone: +385 (51) 770 447
Fax: +385 (51) 686 166
www.intechopen.com

InTech China
Unit 405, Office Block, Hotel Equatorial Shanghai
No.65, Yan An Road (West), Shanghai, 200040, China
中国上海市延安西路65号上海国际贵都大饭店办公楼405单元
Phone: +86-21-62489820
Fax: +86-21-62489821

IntechOpen